19-0046; Rev. 1; 3/94

MAXIM

Dual, Serial-Input, Voltage-Output, 12-Bit MDAC

General Description

The MAX532 is a complete, dual, serial-input, 12-bit multiplying digital-to-analog converter (MDAC) with output amplifiers. No external user trims are required to achieve full specified performance. The MAX532's 3-wire serial interface minimizes the number of package pins, so it uses less board space than parallel-interface parts. The interface is SPI™, QSPI™ and Microwire™ compatible. A serial output, DOUT, allows cascading of two or more MAX532s and read-back of the data written to the device.

The device's serial interface minimizes digital-noise feedthrough from its logic pins to its analog outputs. Serial interfacing also simplifies opto-coupler-isolated or transformer-isolated applications.

The MAX532 is specified with ±12V to ±15V power supplies. All logic inputs are TTL and CMOS compatible. It comes in space-saving 16-pin DIP and wide SO packages.

Applications

Automatic Test Equipment

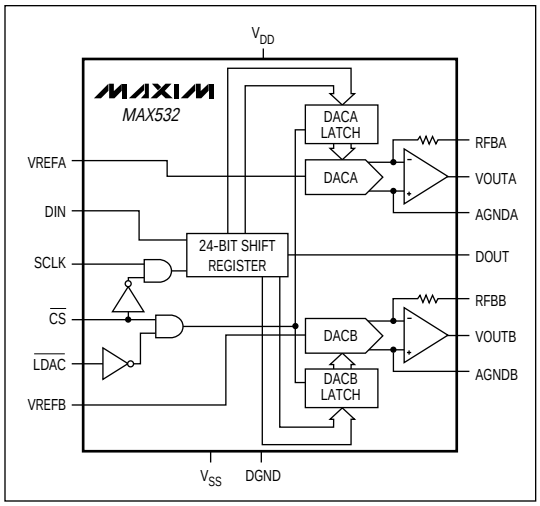
Arbitrary Waveform Generators

Programmable-Gain Amplifiers

Motion Control Systems

Servo Controls

Functional Diagram



Features

- ♦ **Two 12-Bit MDACs with Output Amplifiers**
- ♦ **Fast, 6MHz 3-Wire Interface**
- ♦ **SPI, QSPI, and Microwire Compatible**
- ♦ **±12V Output Swing**
- ♦ **±10mA Output Current**
- ♦ **2.5µs Settling Time to ±1/2LSB**
- ♦ **Guaranteed Monotonic Over Temperature**
- ♦ **Low Integral Nonlinearity: ±1/2LSB Max**
- ♦ **Low Gain Tempco: 2ppm/°C**
- ♦ **Operates from ±12V to ±15V Supplies**
- ♦ **Power-On Reset**
- ♦ **Available in 16-Pin DIP and Wide SO Packages**

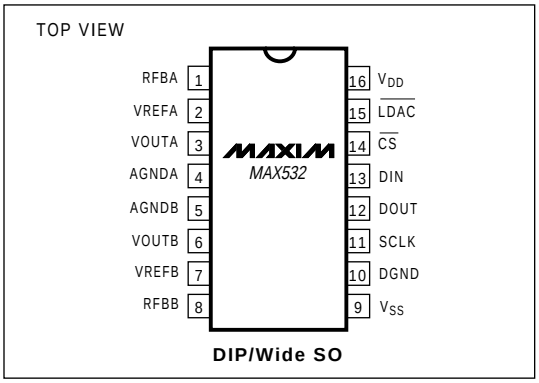
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	ERROR (LSBs)
MAX532ACPE	0°C to +70°C	16 Plastic DIP	±1/2
MAX532BCPE	0°C to +70°C	16 Plastic DIP	±1
MAX532ACWE	0°C to +70°C	16 Wide SO	±1/2
MAX532BCWE	0°C to +70°C	16 Wide SO	±1
MAX532BC/D	0°C to +70°C	Dice*	±1

Ordering Information continued on last page.

** Contact factory for dice specifications.*

Pin Configuration



DIP/Wide SO

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Dual, Serial-Input, Voltage-Output, 12-Bit MDAC

ABSOLUTE MAXIMUM RATINGS

Pin Voltages
- V_{DD} to DGND, AGNDA, AGNDB .....-0.3V to +17V
- V_{SS} to DGND, AGNDA, AGNDB (Note 1) .....+0.3V to -17V
- VREFA, VREFB .....(V_{SS} - 0.3V) to (V_{DD} + 0.3V)
- AGNDA, AGNDB .....(DGND - 0.3V) to (V_{DD} + 0.3V)
- VOUTA, VOUTB .....(V_{SS} - 0.3V) to (V_{DD} + 0.3V)
- RFBA, RFBB .....(V_{SS} - 0.3V) to (V_{DD} + 0.3V)
- SCLK, DIN, DOUT, $\overline{LDAC}$, $\overline{CS}$ ..(DGND - 0.3V) to (V_{DD} + 0.3V)

DOUT Sink Current 20mA

Continuous Power Dissipation (T_A = +70°C)
- Plastic DIP (derate 10.53mW/°C above +70°C) 842mW
- Wide SO (derate 9.52mW/°C above +70°C).....762mW
- CERDIP (derate 10.00mW/°C above +70°C).....800mW

Operating Temperature Ranges:
- MAX532_C__ .....0°C to +70°C
- MAX532_E__.....-40°C to +85°C
- MAX532_MJE .....-55°C to +125°C

Junction Temperatures:
- MAX532_C__, E__.....+150°C
- MAX532_MJE.....+175°C

Storage Temperature Range ..... -65°C to +160°C

Lead Temperature (soldering, 10sec) ..... +300°C

Note 1: If V_{SS} is open-circuited with V_{DD} and either AGND applied, the V_{SS} pin will float positive, exceeding the Absolute Maximum Ratings. A Schottky diode connected between V_{SS} and GND ensures the maximum ratings will not be exceeded.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = 11.4V to 16.5V, V_{SS} = -11.4V to -16.5V, AGNDA = AGNDB = DGND = 0V, VREFA and VREFB = +10V, R_L = 2kΩ, C_L = 100pF, VOUT_ connected to RFB_, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
STATIC PERFORMANCE (Note 1)							
Resolution				12			Bits
Relative Accuracy	INL		MAX532A			±1/2	LSB
			MAX532B			±1	
Differential Nonlinearity		Guaranteed monotonic				±1	LSB
Zero-Code Offset Error		DAC latch loaded with all 0s	T_A = +25°C, MAX532_			±2	mV
			T_A = T_{MIN} to T_{MAX}, MAX532A			±3	
			T_A = T_{MIN} to T_{MAX}, MAX532B			±4	
Zero-Code Offset Temperature Coefficient		DAC latch loaded with all 0s			±5		µV/°C
Gain Error		T_A = +25°C, DAC latch loaded with all 1s	MAX532A			±2	LSB
			MAX532B			±5	
		T_A = T_{MIN} to T_{MAX}, DAC latch loaded with all 1s	MAX532A			±4	
			MAX532B			±7	
Gain-Error Temperature Coefficient					±2		ppm/°C of FSR
REFERENCE INPUTS (VREFA, VREFB)							
VREFA, VREFB Input Resistance				8	10	13	kΩ
VREFA, VREFB Input Resistance Matching					±0.5	±3.0	%

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 11.4V to 16.5V, V_{SS} = -11.4V to -16.5V, AGNDA = AGNDB = DGND = 0V, VREFA and VREFB = +10V, R_L = 2kΩ, C_L = 100pF, VOUT_ connected to RFB_, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DIGITAL INPUTS (SCLK, DIN, $\overline{LDAC}$, $\overline{CS}$)							
Input High Voltage	V_{INH}			2.4			V
Input Low Voltage	V_{INL}					0.8	V
Input Current		Digital inputs at 0V or V_{DD}				±1	µA
Input Capacitance (Note 2)						8	pF
DIGITAL OUTPUT (DOUT) (Note 3)							
Output Voltage Low	V_{OL}	I_{SINK} = 5mA			0.08	0.4	V
		I_{SINK} = 16mA			0.2		
Output High Leakage	I_{LKG}	V_{DOUT} = 0V to V_{DD}				±10	µA
Output High Capacitance (Note 2)	C_{OUT}					15	pF
ANALOG OUTPUTS (VOUTA, VOUTB)							
DC Output Impedance					0.2		Ω
Short-Circuit Current		VOUTA, VOUTB connected to AGNDA, AGNDB			20		mA
Output Voltage Swing				(V_{DD} - 2.5) to (V_{SS} + 2.5)			V
POWER REQUIREMENTS							
Positive Supply Voltage	V_{DD}			11.4		16.5	V
Negative Supply Voltage	V_{SS}			-11.4		-16.5	V
Power-Supply Rejection	PSR	ΔFull scale/ΔV_{DD}, V_{DD} = 11.4V to 16.5V, VREF = -8.9V, DAC latches loaded with all 1s				±0.035	LSB/%
		ΔFull scale/ΔV_{SS}, V_{SS} = -11.4V to -16.5V, VREF = 8.9V, DAC latches loaded with all 1s				±0.035	
Positive Supply Current	I_{DD}	Output unloaded			5	10	mA
Negative Supply Current	I_{SS}	Output unloaded			4	6	mA
AC CHARACTERISTICS							
Voltage-Output Settling Time		Settling time to within 1/2 LSB of final DAC value; DAC latch alternately loaded with all 0s and all 1s			2.5		µs
Slew Rate					8		V/µs
Digital-to-Analog Glitch Impulse		DAC latch alternately loaded with 011...11 and 100...00			60		nV-s
Channel-to-Channel Isolation		VREFA to VOUTB	VREFA = 20V_{p-p} 10kHz sine wave; DAC latches loaded with all 0s		-100		dB
		VREFB to VOUTA	VREFB = 20V_{p-p} 10kHz sine wave; DAC latches loaded with all 0s		-100		

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 11.4V to 16.5V, V_{SS} = -11.4V to -16.5V, AGNDA = AGNDB = DGND = 0V, VREFA and VREFB = +10V, R_L = 2kΩ, C_L = 100pF, VOUT_ connected to RFB_, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Multiplying Feedthrough Error		VREF = $20V_{p-p}$ 10kHz sine wave; DAC latch loaded with all 0s		-77		dB
Unity-Gain Small-Signal Bandwidth		VREF = $100mV_{p-p}$ sine wave; DAC latch loaded with all 1s		1.0		MHz
Full-Power Bandwidth		VREF = $20V_{p-p}$ sine wave; DAC latch loaded with all 1s		125		kHz
Total Harmonic Distortion	THD	VREF = $6V_{RMS}$, 1kHz sine wave; DAC latch loaded with all 1s		-90		dB
Digital Feedthrough		$\overline{CS}$ = 1; transitions on SCLK, $\overline{LDAC}$, DIN		1.1		nV-s
Digital Crosstalk		DACA code all 1s, DACB code transition from all 0s to all 1s		10		nV-s
Output Noise Voltage		0.1Hz to 10Hz		2		μV_{RMS}

Note 1: Static performance tested at V_{DD} = +15V, V_{SS} = -15V. Performance over supplies guaranteed by PSR test.
Note 2: Guaranteed by design. Not subject to production testing.
Note 3: Open-drain output.

TIMING CHARACTERISTICS

(V_{DD} = 11.4V to 16.5V, V_{SS} = -11.4V to -16.5V, AGNDA = AGNDB = DGND = 0V) (Notes 4, 5)

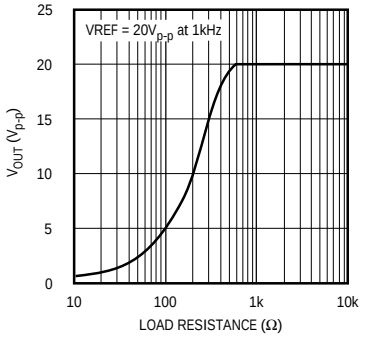
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCLK Clock Frequency	f_{CLK}				6.25	MHz
SCLK Pulse Width High	t_{CH}		80			ns
SCLK Pulse Width Low	t_{CL}		80			ns
DIN to SCLK Rise Setup Time	t_{DS}		50			ns
DIN to SCLK Rise Hold Time	t_{DH}		0			ns
$\overline{CS}$ Fall to SCLK Rise Setup Time	t_{CSS0}		50			ns
$\overline{CS}$ Rise to SCLK Rise Setup Time	t_{CSS1}		50			ns
SCLK Fall to $\overline{CS}$ Fall Hold Time	t_{CSH0}		5			ns
SCLK Rise to $\overline{CS}$ Rise Hold Time	t_{CSH1}		80			ns
$\overline{CS}$ Pulse Width High	t_{CSW}		120			ns
SCLK Fall to DOUT Valid (Note 6)	t_{DO}	C_L = 20pF, $R_{PULL-UP}$ = 1kΩ to 5V	0		200	ns
$\overline{CS}$ Fall to DOUT Enable (Note 7)	t_{DV}	C_L = 20pF, $R_{PULL-UP}$ = 1kΩ to 5V			100	ns
$\overline{CS}$ Rise to DOUT Disable (Note 7)	t_{TR}	C_L = 20pF, $R_{PULL-UP}$ = 1kΩ to 5V			60	ns
$\overline{LDAC}$ Pulse Width Low	t_{LDAC}		60			ns
$\overline{CS}$ Rise to $\overline{LDAC}$ Fall Setup Time	t_{LDACS}		100			ns

Note 4: All input signals are specified with t_R = t_F ≤ 5ns. Logic input swing is 0V to 5V.
Note 5: See Figure 1.
Note 6: Timing is for SCLK fall to DOUT fall to 0.8V, or for SCLK fall to DOUT rise to 2.4V. Additional time must be added for any larger passive RC pull-up delay.
Note 7: DOUT enable: DOUT falls to 4.5V from 5.0V. DOUT disable: DOUT rises to 0.5V from 0V.

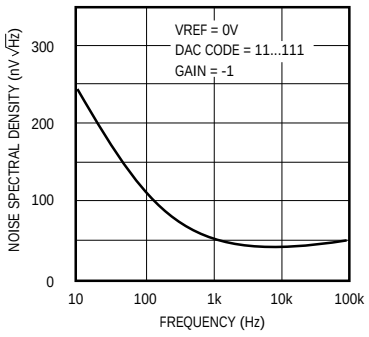
Typical Operating Characteristics

(V_{DD} = 15V, V_{SS} = -15V, R_L = 2kΩ, C_L = 100pF, unless otherwise noted.)

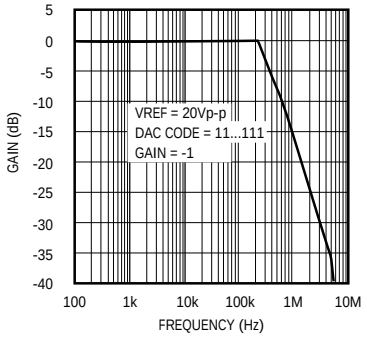
OUTPUT VOLTAGE SWING vs. RESISTIVE LOAD



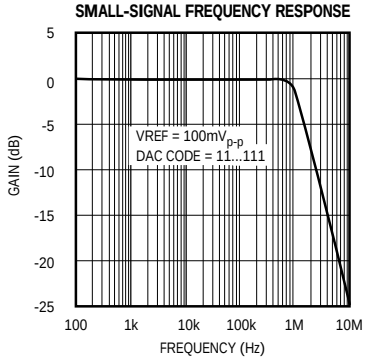
NOISE SPECTRAL DENSITY



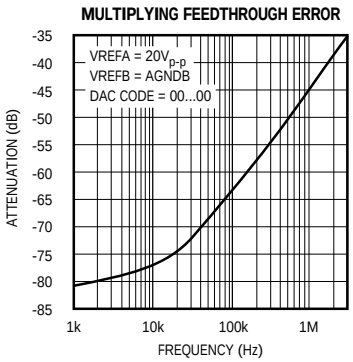
LARGE-SIGNAL FREQUENCY RESPONSE



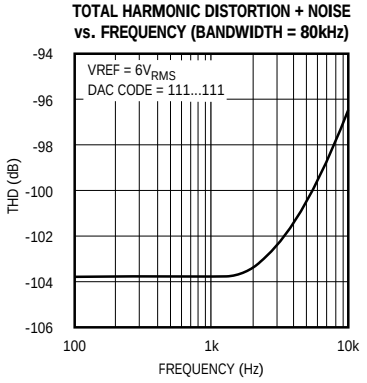
SMALL-SIGNAL FREQUENCY RESPONSE



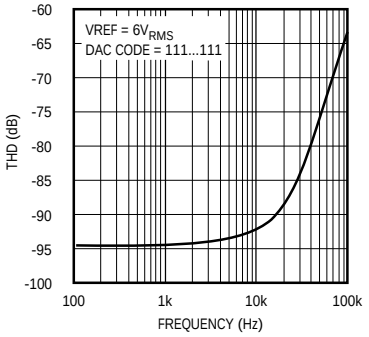
MULTIPLYING FEEDTHROUGH ERROR



TOTAL HARMONIC DISTORTION + NOISE vs. FREQUENCY (BANDWIDTH = 80kHz)



TOTAL HARMONIC DISTORTION + NOISE vs. FREQUENCY (BANDWIDTH > 500kHz)

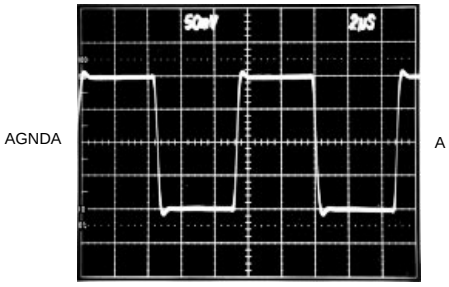


Dual, Serial-Input, Voltage-Output, 12-Bit MDAC

Typical Operating Characteristics (continued)

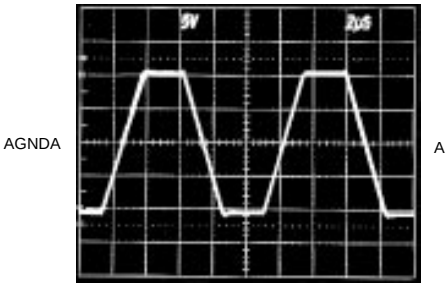
(V_{DD} = 15V, V_{SS} = -15V, R_L = 2kΩ, C_L = 100pF, unless otherwise noted.)

SMALL-SIGNAL PULSE RESPONSE



A = V_{OUTA}, 50mV/div
TIMEBASE = 2µs/div
V_{REFA} = ±100mV SQUARE WAVE

LARGE-SIGNAL PULSE RESPONSE



A = VOUTA, 5V/div
TIMEBASE = 2µs/div
VREFA = ±10V SQUARE WAVE

Pin Description

PIN	NAME	FUNCTION
1	RFBA	Feedback Resistor for DACA
2	VREFA	Reference Input for DACA
3	VOUTA	Voltage Output for DACA
4	AGNDA	Analog Ground for DACA
5	AGNDB	Analog Ground for DACB
6	VOUTB	Voltage Output for DACB
7	VREFB	Reference Input for DACB
8	RFBB	Feedback Resistor for DACB
9	V_{SS}	Negative Supply Voltage
10	DGND	Digital Ground
11	SCLK	Serial Clock Input
12	DOUT	Serial Data Output. Open-drain N-channel MOSFET output: requires external pull-up resistor. Data on DOUT changes on the falling edge of SCLK. Serial output data is delayed 24 clock cycles from DIN.
13	DIN	Serial Data Input. CMOS- and TTL-compatible input. Data is clocked into DIN on the rising edge of SCLK. $\overline{CS}$ must be low for data to be clocked in.
14	$\overline{CS}$	Chip-Select Input, active low. Data is shifted in and out when $\overline{CS}$ is low. DAC latches are updated when $\overline{CS}$ is high and $\overline{LDAC}$ is low.
15	$\overline{LDAC}$	Asynchronous Load DAC Input, active low. DAC latches are updated when $\overline{CS}$ is high and $\overline{LDAC}$ is low.
16	V_{DD}	Positive Supply Voltage

Timing Diagrams

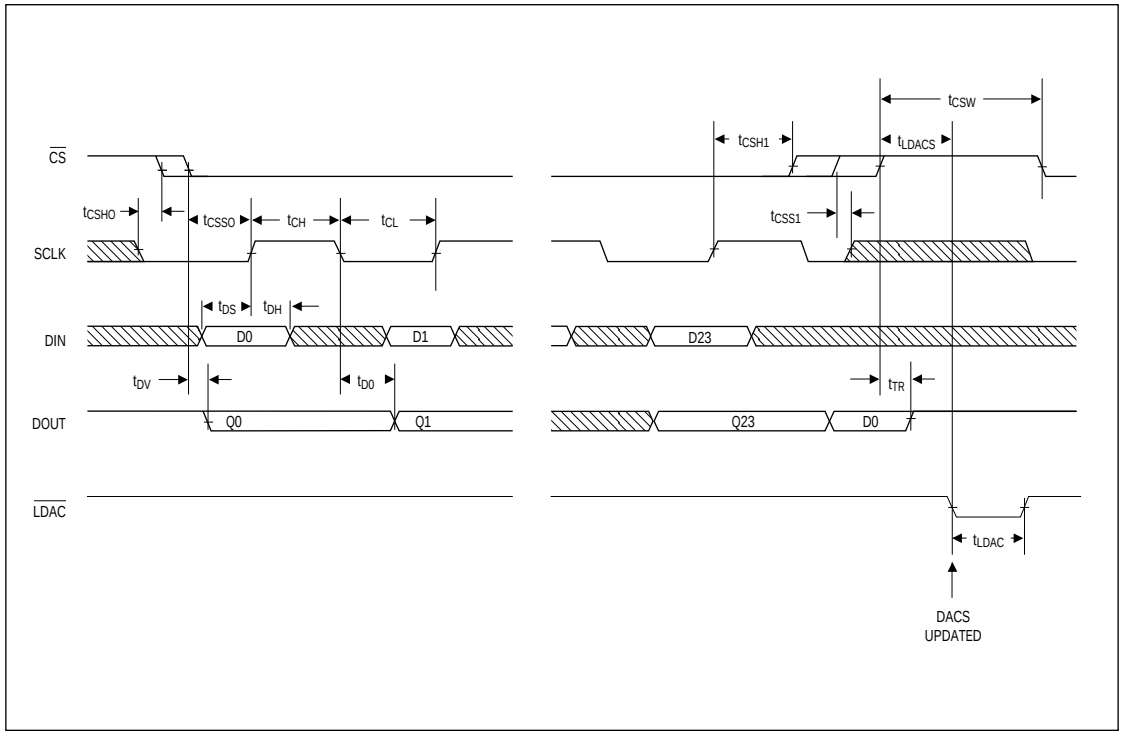


Figure 1. Timing Diagram

Timing Diagrams (continued)

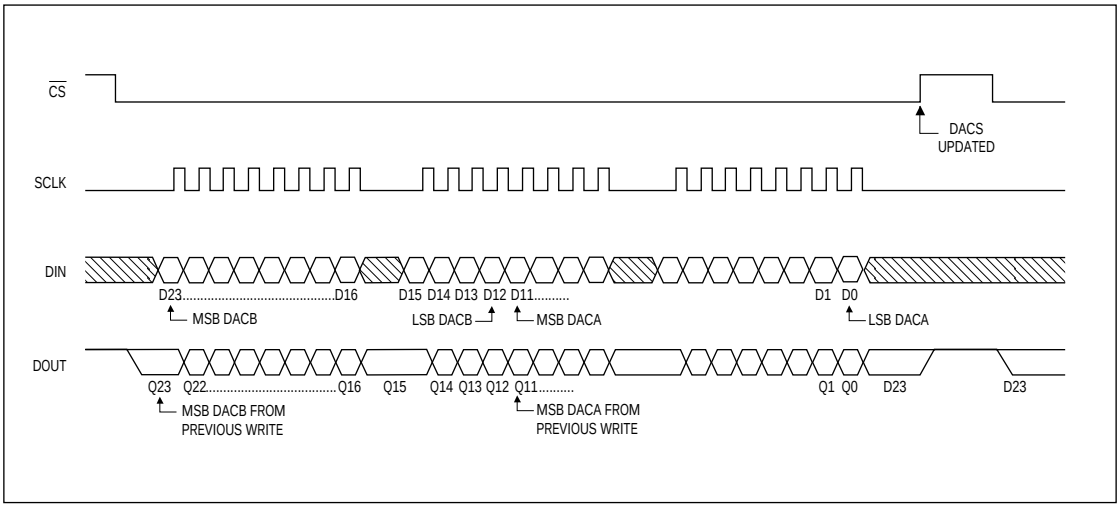


Figure 2. 3-Wire Interface Timing Diagram ($\overline{LDAC}$ = DGND)

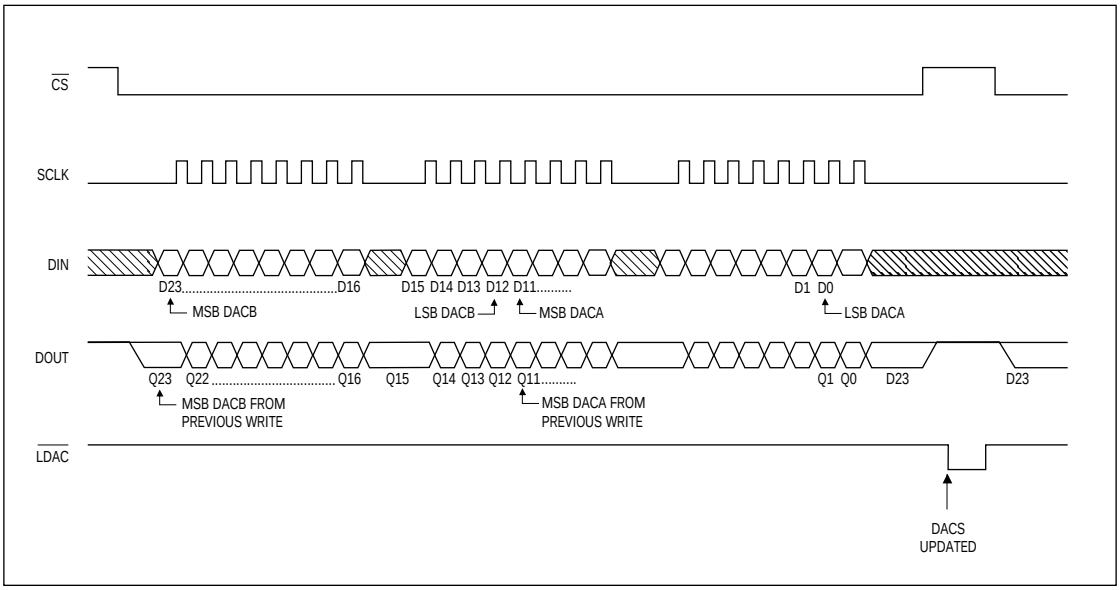


Figure 3. 4-Wire Inferface Timing Diagam

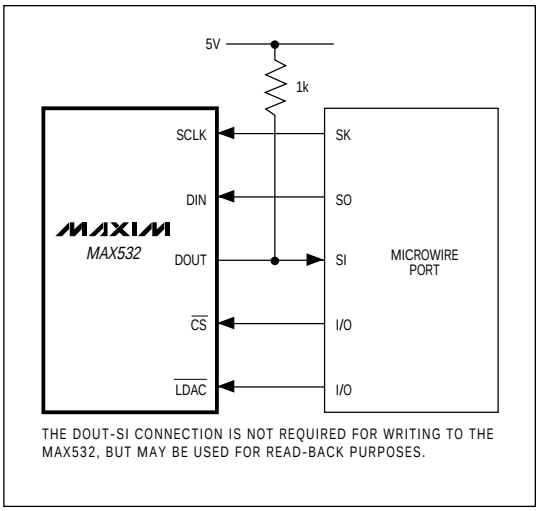


Figure 4. Connections for Microwire

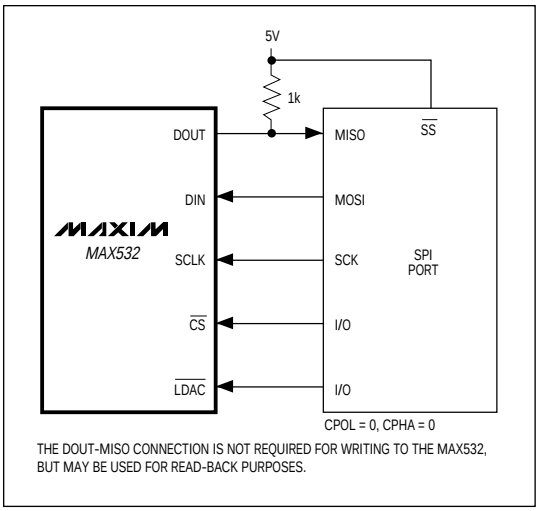


Figure 5. Connections for SPI

Detailed Description

Digital Interface

The MAX532 is Microwire and SPI compatible (Figures 4 and 5). Both DACs are programmed by writing three 8-bit words (see Figures 2 and 3, and the *Functional Diagram*). Serial data is clocked into the data registers MSB first, with DACB information preceding DACA information. Data is clocked in on the rising edge of SCLK while $\overline{CS}$ is low. With $\overline{CS}$ high, data can not be clocked into DIN, and DOUT is high impedance. SCLK can be driven at rates up to 6.25MHz.

The MAX532 uses either a 3-wire or a 4-wire serial interface. Three wires may be used ($\overline{CS}$, DIN, SCLK) by tying $\overline{LDAC}$ low. With $\overline{LDAC}$ low, the DACs are updated simultaneously when $\overline{CS}$ goes high (see Figure 2 and the *Functional Diagram*). The 3-wire interface may be used if the MAX532 is used alone, or if two or more MAX532s are cascaded (DOUT of one device tied to DIN of the other) (Figure 6).

The 4-wire interface ($\overline{LDAC}$, $\overline{CS}$, DIN, SCLK) is required if several serial devices are tied to the same data line, and it is desirable to update them simultaneously (Figure 7). With the 4-wire interface, the DACs are updated when $\overline{LDAC}$ goes low (see Figure 3 and the *Functional Diagram*).

A serial output, DOUT, allows cascading of two or more MAX532s and allows read-back of the data written to the device's 24-bit shift register. The data at DOUT is delayed 24 clock cycles from the data at DIN (see Figures 2 and 3, and the *Functional Diagram*). DOUT is an open-drain N-channel MOSFET that requires an external pull-up resistor (typically 1kΩ if pulled up to +5V, and 3kΩ if pulled up to +12V or +15V). Logic levels are guaranteed with sink currents up to 5mA (see *Electrical Characteristics*). Output data changes on the falling edge of SCLK when $\overline{CS}$ is low. If $\overline{CS}$ is high, DOUT is three-state (high-impedance).

Daisy-Chaining Devices

Any number of MAX532s can be daisy-chained by connecting the DOUT pin of one device (with a pull-up resistor) to the DIN pin of the following device in the chain (Figure 6).

When daisy-chaining devices, t_{CSS0} ($\overline{CS}$ low to SCLK high), must be the greater of $t_{DV} + t_{DS}$ or $t_{DS} + (t_{RC} + t_{TR} - t_{CS})$, where t_{CSW} is the $\overline{CS}$ pulse width used in the system and the term $(t_{RC} + t_{TR} - t_{CSW})$ accounts for the time spent charging the DOUT capacitance with the external pull-up resistor. So, for $t_{RC} < 250ns$, t_{CSS0} is simply $t_{DV} + t_{DS}$. Calculate t_{RC} using the following equation:

$$t_{RC} = R_P \times C \times \ln (V_{PULL\text{-}UP}/(V_{PULL\text{-}UP} - 2.4V))$$

where $V_{PULL\text{-}UP}$ is the voltage that the pull-up resistor is connected to, R_P is the value of the pull-up resistor, and C is the capacitance at DOUT. Values of t_{RC} are given in Table 1.

Dual, Serial-Input, Voltage-Output, 12-Bit MDAC

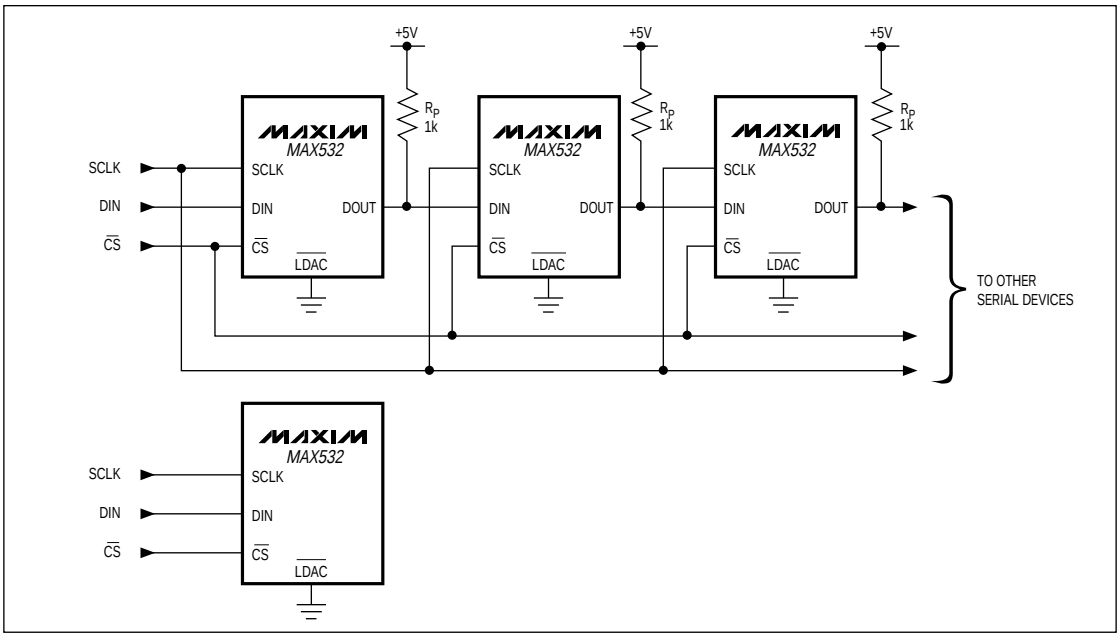


Figure 6. Daisy-chained or individual MAX532s are simultaneously updated by bringing $\overline{CS}$ high when using the 3-wire interface ($\overline{LDAC}$ = DGND).

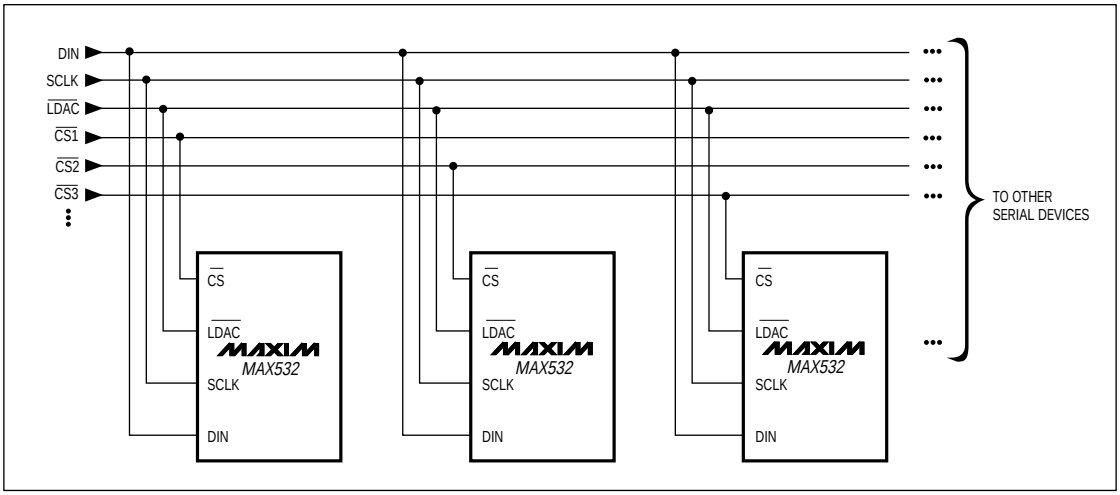


Figure 7. Multiple devices sharing a common DIN line may be simultaneously updated by bringing $\overline{LDAC}$ low. CS1, CS2, CS3, . . ., are driven separately, thus controlling which data are written to devices 1, 2, 3, ...

Table 1. t_{RC} Delay Times

$V_{PULL-UP}$ (V)	C (pF)	R_P (kΩ)	t_{RC} (ns)
4.5	20	1	15
4.5	35	1	27
4.5	50	1	38
4.5	100	1	76
4.5	150	1	114
11.4	20	3	14
11.4	35	3	25
11.4	50	3	35
11.4	100	3	71
11.4	150	3	106
13.5	20	3	12
13.5	35	3	21
13.5	50	3	29
13.5	100	3	59
13.5	150	3	88

With the values of t_{RC} given in Table 1, t_{CSS0} is always given by t_{DV} + t_{DS}. For different values of R or C, t_{RC} must be calculated to determine t_{CSS0}.

Additionally, the maximum clock frequency is limited to

$$f_{CLK}\,(max) = \frac{1}{2 \times (t_{DO} + t_{RC} - 15ns + t_{DS})}.$$

For example, with t_{RC} = 15ns (5V ±10% supply with 1kΩ pull-up), the maximum clock frequency is 2MHz.

Digital-to-Analog Section

Figure 8 shows a simplified circuit diagram for one of the DACs and the output amplifier.

A segmented scheme is used to improve linearity, whereby the two MSBs of the 12-bit data word are decoded to drive the three switches, SA, SB, and SC. The remaining ten bits drive the switches S0 through S9 in a standard R-2R ladder configuration.

Each of the switches, SA, SB, and SC, steers 1/4 of the total reference current with the remaining 1/4 passing through the R-2R section.

The output amplifier and feedback resistor perform the current-to-voltage conversion, giving the following:

VOUT_ = -D x VREF_,

where _ denotes A or B, and D is the fractional representation of the digital word. (D can be set from 0 to 4095/4096.)

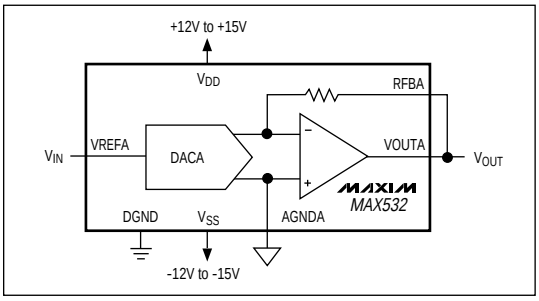


Figure 9. Unipolar Binary Operation

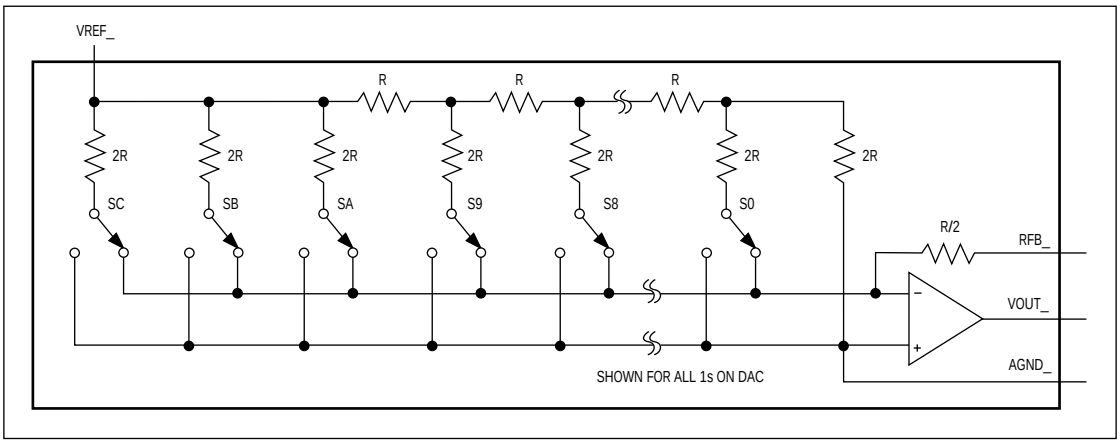


Figure 8. Simplified D/A Circuit Diagram

Dual, Serial-Input, Voltage-Output, 12-Bit MDAC

Output Amplifiers

The output amplifiers are stable with any combination of resistive loads ≥ 2kΩ and capacitive loads ≤ 100pF. They are internally compensated, and settle to ±0.01% FSR (1/2LSB) in 2.5µs.

Unipolar Configuration

Figure 9 shows DACA connected for unipolar binary operation. Similar connections apply for DACB. When V_{IN} is an AC signal, the circuit performs two-quadrant multiplication. Table 2 shows the codes for this circuit.

Bipolar Operation

Figure 10 shows the MAX532 connected for bipolar operation. The coding is offset binary, as shown in Table 3. When V_{IN} is an AC signal, the circuit performs four-quadrant multiplication. To maintain gain error specifications, resistors R1, R2, and R3 should be ratio-matched to 0.01%.

Applications Information

Layout, Grounding, and Bypassing

For best system performance, use printed circuit boards with separate analog and digital ground planes. Wire-wrap boards are not recommended. The two ground planes should be tied together at the low-impedance power-supply source, as shown in Figure 11.

The board layout should ensure that digital and analog signal lines are kept separate from each other as much as possible. Do not run analog and digital lines parallel to one another.

The output amplifiers are sensitive to high-frequency noise in the V_{DD} and V_{SS} power supplies. Bypass these supplies to the analog ground plane with 0.1µF and 10µF bypass capacitors. Minimize capacitor lead lengths for best noise rejection.

Table 2. Unipolar Code Table

DAC Latch Contents MSB LSB	Analog Output, V_{OUT}
1111 1111 1111	$-V_{IN}$ x (4095/4096)
1000 0000 0000	$-V_{IN}$ x (2048/4096) = $-1/2V_{IN}$
0000 0000 0001	$-V_{IN}$ x (1/4096)
0000 0000 0000	0V

1LSB = V_{IN}/4096

Table 3. Bipolar Code Table

DAC Latch Contents MSB LSB	Analog Output, V_{OUT}
1111 1111 1111	$+V_{IN}$ x (2047/2048)
1000 0000 0001	$+V_{IN}$ x (1/2048)
1000 0000 0000	0V
0111 1111 1111	$-V_{IN}$ x (1/2048)
0000 0000 0000	$-V_{IN}$ + (2048/2048) = $-V_{IN}$

1LSB = V_{IN}/2048

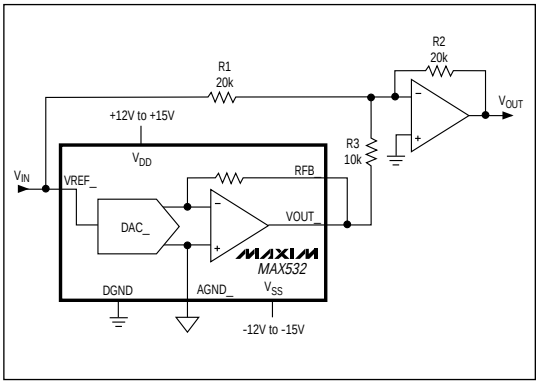


Figure 10. Bipolar Operation

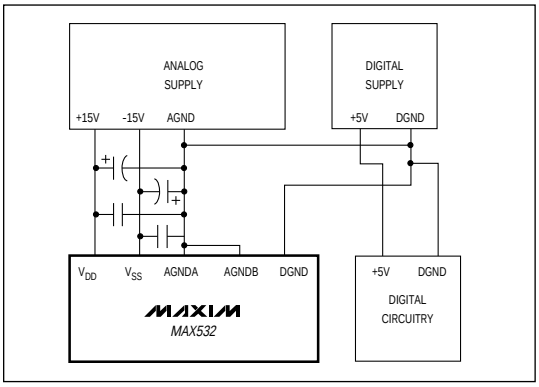


Figure 11. Power-Supply Grounding

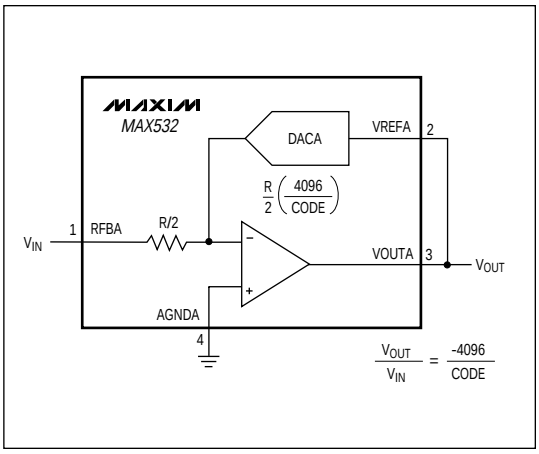


Figure 12. Programmable-Gain Amplifer

Programmable-Gain Amplifier (PGA)

The DAC/amplifier combination, along with access to the feedback resistors, makes the MAX532 ideal as a programmable-gain amplifier. In this application, the DAC functions as a programmable resistor in the feedback loop. This type of configuration is shown in Figure 12, and is suitable for AC gain control. The DAC code controls the gain for the PGA. As the code decreases, the effective DAC resistance increases, and so the gain also increases. The transfer function is given by:

$$V_{OUT}/V_{IN} = -REQA/RFBA,$$

where RFBA is the value of the feedback resistor (R/2), and REQA is the effective DAC resistance controlled by the digital input code:

$$REQA = \frac{R}{2}\left(\frac{4096}{CODE}\right),$$

where CODE is the DAC code in decimal.

The transfer function is thus:

$$\frac{V_{OUT}}{V_{IN}} = \frac{-4096}{CODE}$$

The code may be programmed between 1 and (2^{12} -1). The zero code is not allowed, as it results in an open-loop amplifier response.

Power-On Reset

On power-up, the internal DAC latches are set to 00 . . . . .00.

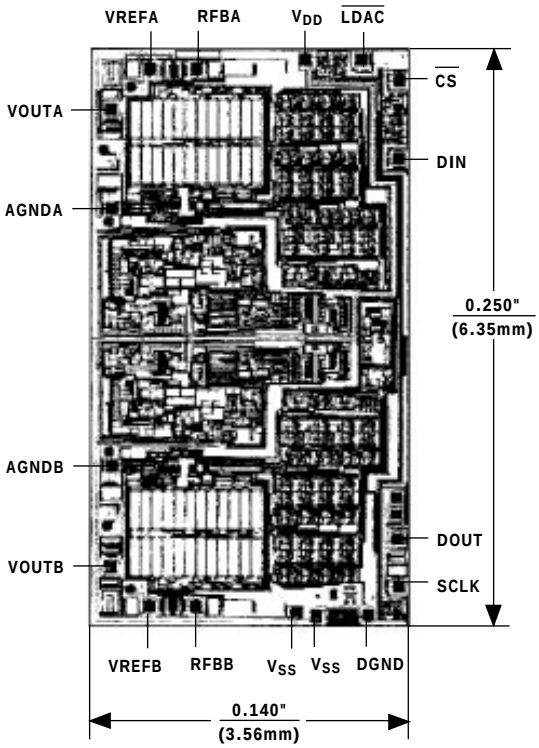
Dual, Serial-Input, Voltage-Output, 12-Bit MDAC

Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE	ERROR (LSBs)
MAX532AEPE	-40°C to +85°C	16 Plastic DIP	±1/2
MAX532BEPE	-40°C to +85°C	16 Plastic DIP	±1
MAX532AEWE	-40°C to +85°C	16 Wide SO	±1/2
MAX532BEWE	-40°C to +85°C	16 Wide SO	±1
MAX532AMJE	-55°C to +125°C	16 CERDIP**	±1/2
MAX532BMJE	-55°C to +125°C	16 CERDIP**	±1

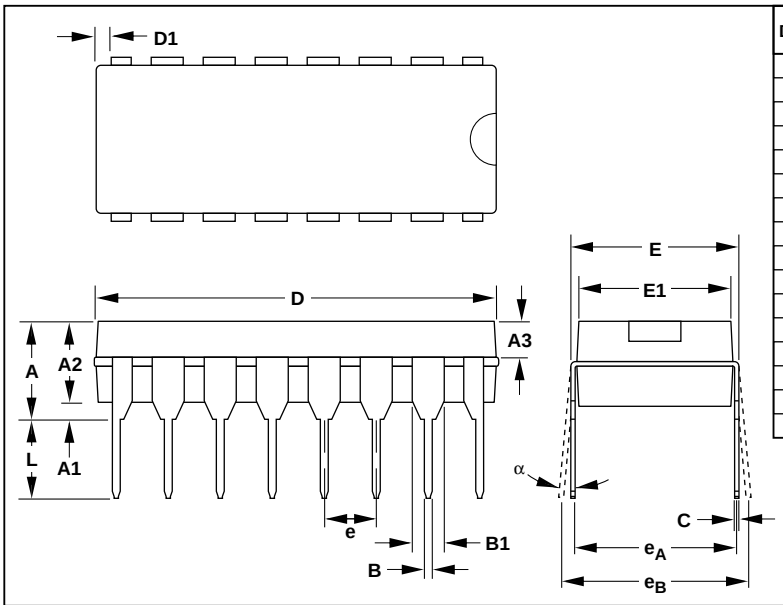
***Contact factory for availability and processing to MIL-STD-883B.*

Chip Topography



TRANSISTOR COUNT: 1324;
SUBSTRATE CONNECTED TO V_{DD}.

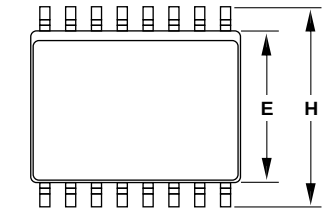
Package Information

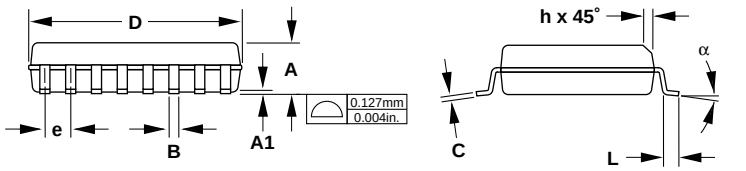


DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	–	0.200	–	5.08
A1	0.015	–	0.38	–
A2	0.125	0.150	3.18	3.81
A3	0.055	0.080	1.40	2.03
B	0.016	0.022	0.41	0.56
B1	0.050	0.065	1.27	1.65
C	0.008	0.012	0.20	0.30
D	0.745	0.765	18.92	19.43
D1	0.005	0.030	0.13	0.76
E	0.300	0.325	7.62	8.26
E1	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
e_A	0.300 BSC		7.62 BSC	
e_B	–	0.400	–	10.16
L	0.115	0.150	2.92	3.81
α	0°	15°	0°	15°

21-587A

16-PIN PLASTIC DUAL-IN-LINE PACKAGE





DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.093	0.104	2.35	2.65
A1	0.004	0.012	0.10	0.30
B	0.014	0.019	0.35	0.49
C	0.009	0.013	0.23	0.32
D	0.398	0.413	10.10	10.50
E	0.291	0.299	7.40	7.60
e	0.050 BSC		1.27 BSC	
H	0.394	0.419	10.00	10.65
h	0.010	0.030	0.25	0.75
L	0.016	0.050	0.40	1.27
α	0°	8°	0°	8°

21-589B

16-PIN PLASTIC SMALL-OUTLINE (WIDE) PACKAGE

Dual, Serial-Input, Voltage-Output, 12-Bit MDAC

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Analog Devices Inc.:

MAX532ACPE+ MAX532ACWE+ MAX532AEWE+ MAX532BCPE+ MAX532BCWE+ MAX532ACWE+T
MAX532AEPE+ MAX532AEWE+T MAX532BCWE+T MAX532BEPE+ MAX532BEWE+ MAX532BEWE+T