2N6387, 2N6388

Plastic Medium-Power Silicon Transistors

These devices are designed for general−purpose amplifier and low−speed switching applications.

Features

- High DC Current Gain – h_{FE} = 2500 (Typ) @ I_C = 4.0 Adc
- Collector−Emitter Sustaining Voltage – @ 100 mAdc
  $V_{CEO(sus)}$ = 60 Vdc (Min) – 2N6387
  $\quad\quad\quad$ = 80 Vdc (Min) – 2N6388
- Low Collector−Emitter Saturation Voltage –
  $V_{CE(sat)}$ = 2.0 Vdc (Max) @ I_C
  $\quad\quad\quad$ = 5.0 Adc – 2N6387, 2N6388
- Monolithic Construction with Built−In Base−Emitter Shunt Resistors
- TO−220AB Compact Package
- These Devices are Pb−Free and are RoHS Compliant*

MAXIMUM RATINGS (Note 1)

Rating		Symbol	Value	Unit
Collector−Emitter Voltage	2N6387 2N6388	V_{CEO}	60 80	Vdc
Collector−Base Voltage	2N6387 2N6388	V_{CB}	60 80	Vdc
Emitter−Base Voltage		V_{EB}	5.0	Vdc
Collector Current – Continuous – Peak		I_C	10 15	Adc
Base Current		I_B	250	mAdc
Total Power Dissipation @ T_C = 25°C Derate above 25°C		P_D	65 0.52	W W/°C
Total Power Dissipation @ T_A = 25°C Derate above 25°C		P_D	2.0 0.016	W W/°C
Operating and Storage Junction, Temperature Range		T_J, T_{stg}	−65 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. Indicates JEDEC Registered Data.

THERMAL CHARACTERISTICS

| Characteristics	Symbol	Max	Unit
Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	1.92	°C/W
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$	62.5	°C/W

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

DARLINGTON NPN SILICON POWER TRANSISTORS 8 AND 10 AMPERES 65 WATTS, 60 – 80 VOLTS
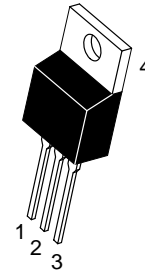
TO−220 CASE 221A STYLE 1

MARKING DIAGRAM

2N638xG
AYWW

2N638x = Device Code
$\quad\quad$ x = 7 or 8
G $\quad$ = Pb−Free Package
A $\quad$ = Assembly Location
Y $\quad$ = Year
WW $\quad$ = Work Week

ORDERING INFORMATION

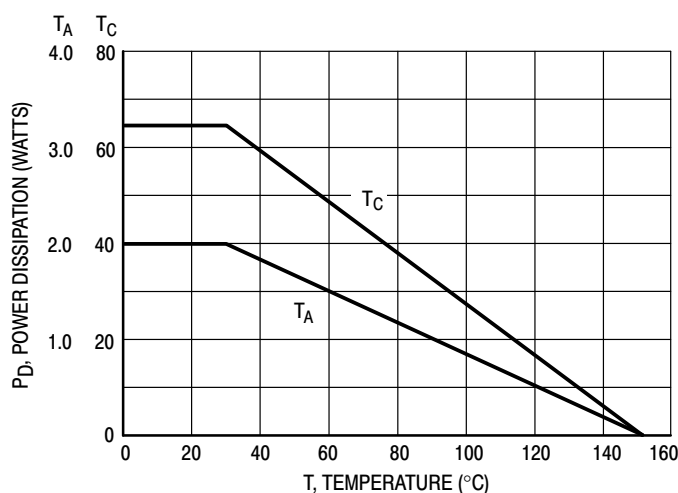| Device	Package	Shipping
2N6387G	TO−220 (Pb−Free)	50 Units / Rail
2N6388G	TO−220 (Pb−Free)	50 Units / Rail

November, 2014 – Rev. 15

1

Figure 1. Power Derating

ELECTRICAL CHARACTERISTICS ($T_C = 25°C$ unless otherwise noted) (Note 2)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector−Emitter Sustaining Voltage (Note 3) (I_C = 200 mAdc, I_B = 0) 2N6387 2N6388	$V_{CEO(sus)}$	 60 80	 − −	Vdc
Collector Cutoff Current (V_{CE} = 60 Vdc, I_B = 0) 2N6387 (V_{CE} = 80 Vdc, I_B = 0) 2N6388	I_{CEO}	 − −	 1.0 1.0	mAdc
Collector Cutoff Current (V_{CE} = 60 Vdc, $V_{EB(off)}$ = 1.5 Vdc) 2N6387 (V_{CE} − 80 Vdc, $V_{EB(off)}$ = 1.5 Vdc) 2N6388 (V_{CE} = 60 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 125°C) 2N6387 (V_{CE} = 80 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 125°C) 2N6388	I_{CEX}	 − − − −	 300 300 3.0 3.0	µAdc mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}	−	5.0	mAdc
ON CHARACTERISTICS (Note 3)				
DC Current Gain (I_C = 5.0 Adc, V_{CE} = 3.0 Vdc) 2N6387, 2N6388 (I_C = 1 0 Adc, V_{CE} = 3.0 Vdc) 2N6387, 2N6388	h_{FE}	 1000 100	 20,000 −	−
Collector−Emitter Saturation Voltage (I_C = 5.0 Adc, I_B = 0.01 Adc) 2N6387, 2N6388 (I_C = 10 Adc, I_B = 0.1 Adc) 2N6387, 2N6388	$V_{CE(sat)}$	 − −	 2.0 3.0	Vdc
Base−Emitter On Voltage (I_C = 5.0 Adc, V_{CE} = 3.0 Vdc) 2N6387, 2N6388 (I_C = 10 Adc, V_{CE} = 3.0 Vdc) 2N6387, 2N6388	$V_{BE(on)}$	 − −	 2.8 4.5	Vdc
DYNAMIC CHARACTERISTICS				
Small−Signal Current Gain (I_C = 1.0 Adc, V_{CE} = 5.0 Vdc, f_{test} = 1.0 MHz)	$|h_{fe}|$	20	−	−
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	−	200	pF
Small−Signal Current Gain (I_C = 1.0 Adc, V_{CE} = 5.0 Vdc, f = 1.0 kHz)	h_{fe}	1000	−	−

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
2. Indicates JEDEC Registered Data.
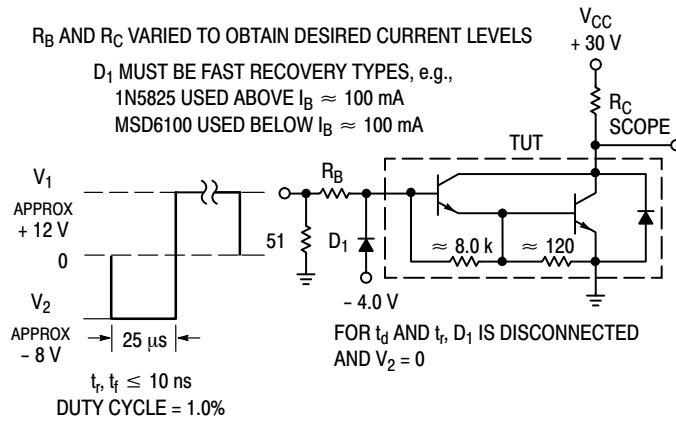3. Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2.0%.

2N6387, 2N6388

RB AND RC VARIED TO OBTAIN DESIRED CURRENT LEVELS

D1 MUST BE FAST RECOVERY TYPES, e.g.,
1N5825 USED ABOVE $I_B \approx$ 100 mA
MSD6100 USED BELOW $I_B \approx$ 100 mA

V_1 APPROX + 12 V

V_2 APPROX – 8 V

25 μs

t_r, $t_f \leq$ 10 ns
DUTY CYCLE = 1.0%

V_{CC} + 30 V

R_C

SCOPE

TUT

R_B

51

D_1

$\approx$ 8.0 k $\approx$ 120

– 4.0 V

FOR t_d AND t_r, D_1 IS DISCONNECTED
AND V_2 = 0

Figure 2. Switching Times Test Circuit

V_{CC} = 30 V
I_C/I_B = 250
$I_{B1} = I_{B2}$
$T_J = 25°C$

t, TIME (μs)

I_C, COLLECTOR CURRENT (AMPS)
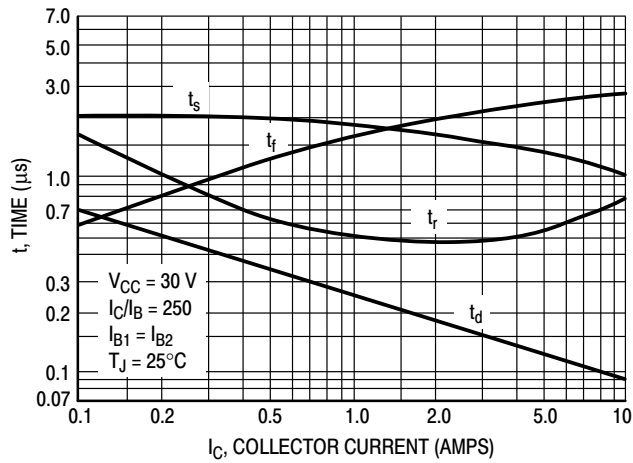
Figure 3. Switching Times

$Z_{\theta JC}$ (t) = r(t) $R_{\theta JC}$
$R_{\theta JC}$ = 1.92°C/W MAX
D CURVES APPLY FOR POWER
PULSE TRAIN SHOWN
READ TIME AT t_1
$T_{J(pk)} - T_C = P_{(pk)} Z_{\theta JC(t)}$

$P_{(pk)}$

t_1

t_2

DUTY CYCLE, D = t_1/t_2

r(t), TRANSIENT THERMAL RESISTANCE (NORMALIZED)

D = 0.5
0.2
0.1
0.05
0.02
0.01

SINGLE PULSE

t, TIME (ms)
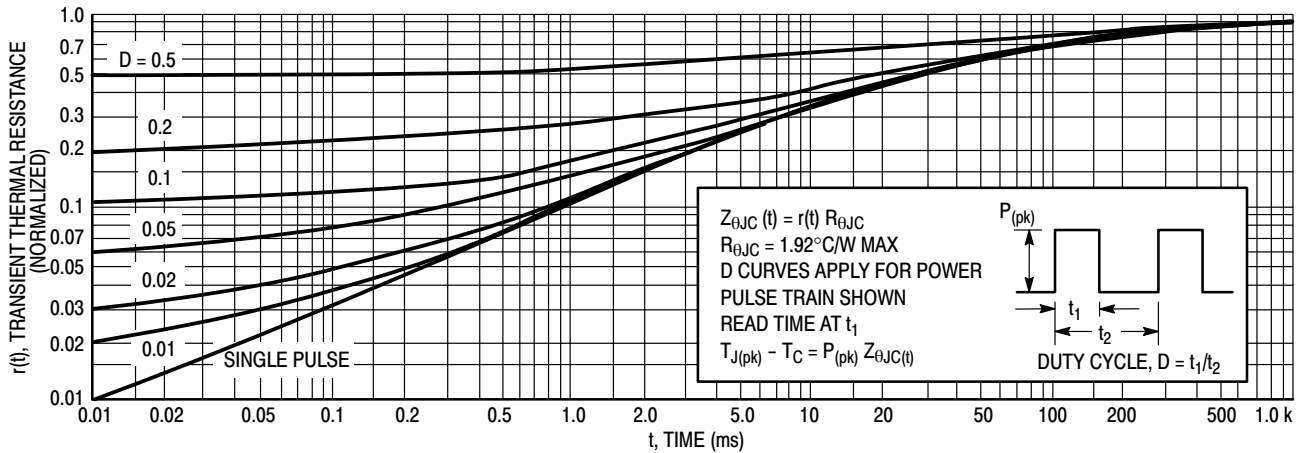
Figure 4. Thermal Response

2N6387, 2N6388
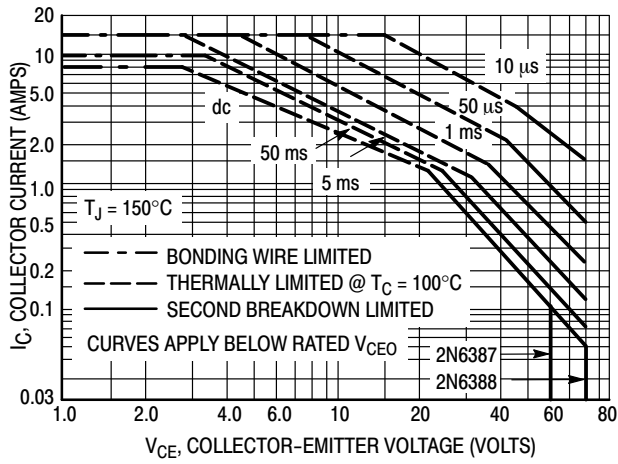
Figure 5. Active-Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown
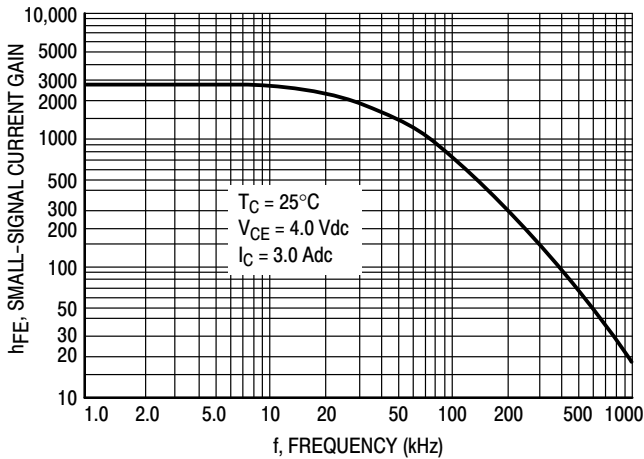
Figure 6. Small–Signal Current Gain
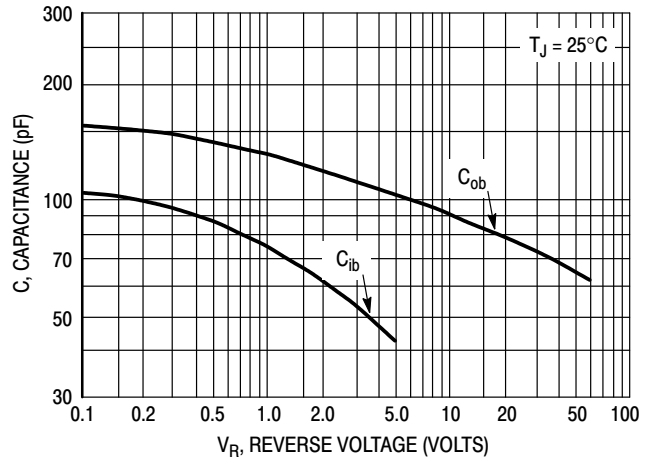
Figure 7. Capacitance
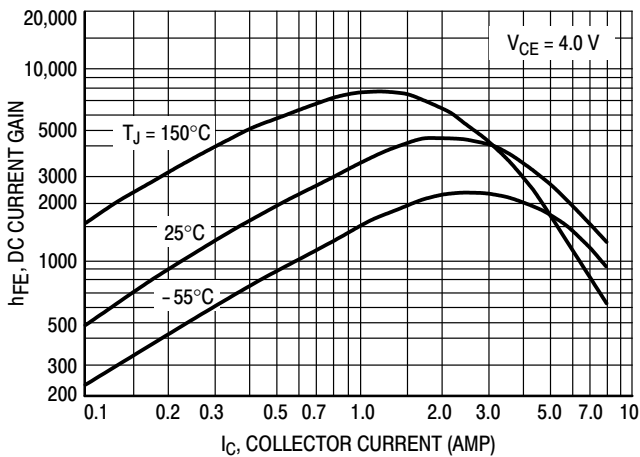
Figure 8. DC Current Gain
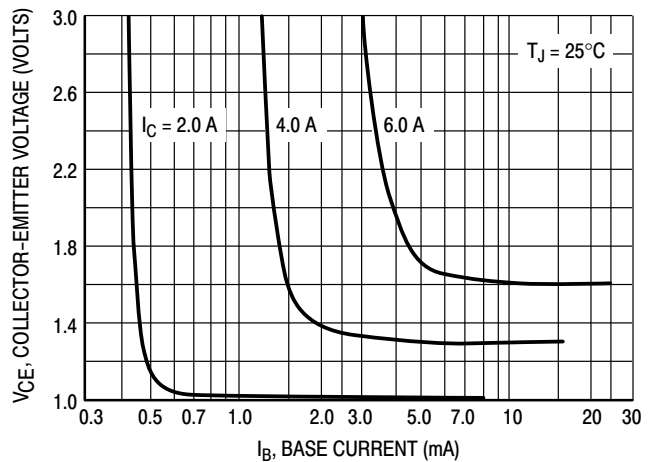
Figure 9. Collector Saturation Region
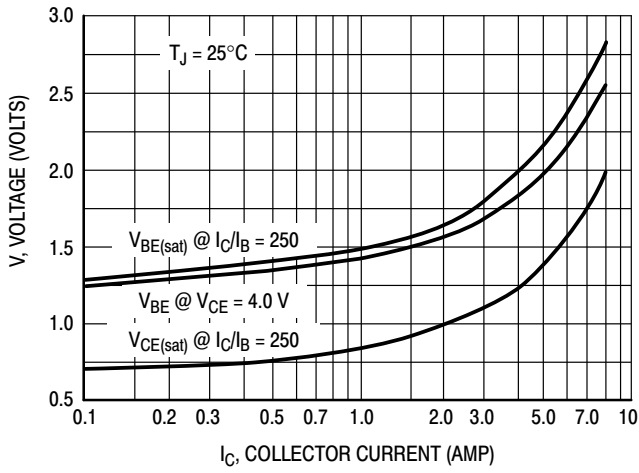
Figure 10. "On" Voltages
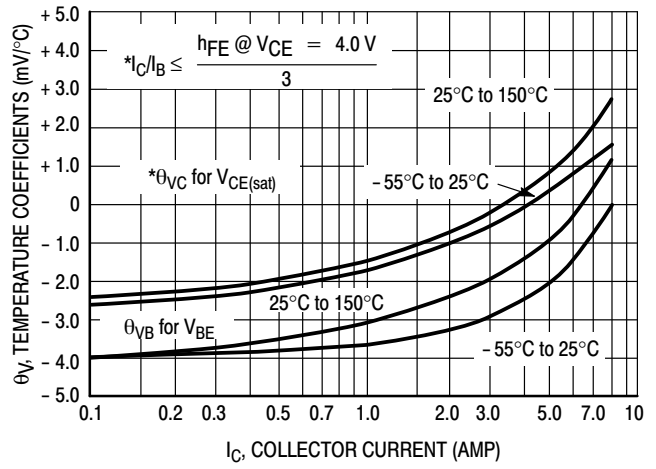
Figure 11. Temperature Coefficients
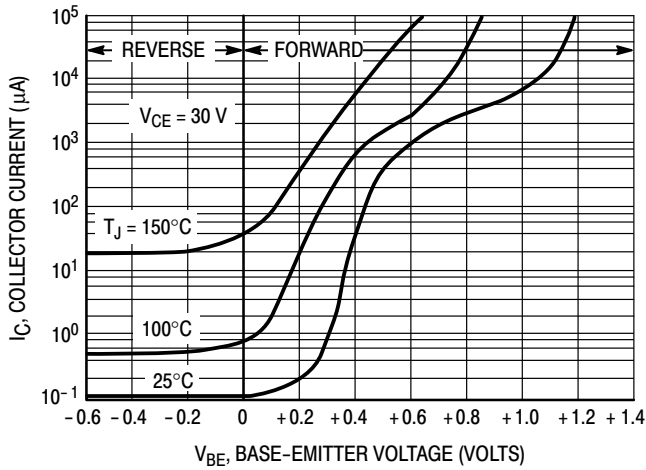
Figure 12. Collector Cut−Off Region
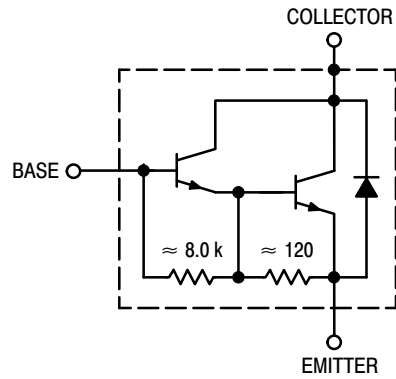
Figure 13. Darlington Schematic
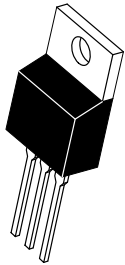
TO−220
CASE 221A
ISSUE AK

DATE 13 JAN 2022

SCALE 1:1

SEATING PLANE

SEE NOTE #4

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 2009.
2. CONTROLLING DIMENSION: INCHES
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.
4. MAX WIDTH FOR F102 DEVICE = 1.35MM

DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.
A	0.570	0.620	14.48	15.75
B	0.380	0.415	9.66	10.53
C	0.160	0.190	4.07	4.83
D	0.025	0.038	0.64	0.96
F	0.142	0.161	3.60	4.09
G	0.095	0.105	2.42	2.66
H	0.110	0.161	2.80	4.10
J	0.014	0.024	0.36	0.61
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.41
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	----	1.15	---
Z	----	0.080	---	2.04

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. BASE
2. EMITTER
3. COLLECTOR
4. EMITTER

STYLE 3:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 4:
PIN 1. MAIN TERMINAL 1
2. MAIN TERMINAL 2
3. GATE
4. MAIN TERMINAL 2

STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 6:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

STYLE 7:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. ANODE

STYLE 8:
PIN 1. CATHODE
2. ANODE
3. EXTERNAL TRIP/DELAY
4. ANODE

STYLE 9:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 10:
PIN 1. GATE
2. SOURCE
3. DRAIN
4. SOURCE

STYLE 11:
PIN 1. DRAIN
2. SOURCE
3. GATE
4. SOURCE

STYLE 12:
PIN 1. MAIN TERMINAL 1
2. MAIN TERMINAL 2
3. GATE
4. NOT CONNECTED

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DESCRIPTION:	TO−220		PAGE 1 OF 1

PUBLICATION ORDERING INFORMATION

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