MOSFET – Single, P-Channel, POWERTRENCH®
FDN352AP

V_{DSS}	$R_{DS(ON)}$ MAX	I_D MAX
–30 V	180 mΩ @ –10 V	–1.3 A
	300 mΩ @ –4.5 V	–1.1 A

General Description

This P−Channel Logic Level MOSFET is produced using **onsemi** advanced POWERTRENCH process that has been especially tailored to minimize the on−state resistance and yet maintain low gate charge for superior switching performance.

These devices are well suited for low voltage and battery powered applications where low in−line power loss is needed in a very small outline surface mount package.

Features

- –1.3 A, –30 V $R_{DS(ON)} = 180$ mΩ @ $V_{GS} = –10$ V
- –1.1 A, –30 V $R_{DS(ON)} = 300$ mΩ @ $V_{GS} = –4.5$ V
- High Performance Trench Technology for Extremely Low $R_{DS(ON)}$
- High Power Version of Industry Standard SOT−23 Package. Identical Pin−out to SOT−23 with 30% Higher Power Handling Capability
- This Device is Pb−Free, Halide Free and is RoHS Compliant

Applications

- Notebook Computer Power Management

SOT−23/SUPERSOT™−23, 3 LEAD, 1.4x2.9 CASE 527AG

MARKING DIAGRAM

52APM
o

52AP = Specific Device Code
M   = Date Code

PIN ASSIGNMENT

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted)

Symbol	Parameter		Value	Unit
V_{DSS}	Drain–Source Voltage		–30	V
V_{GSS}	Gate–Source Voltage		±25	V
I_D	Drain Current	Continuous (Note 1a)	–1.3	A
		Pulsed	–10	
P_D	Power Dissipation for Single Operation	(Note 1a)	0.5	W
		(Note 1b)	0.46	
T_J, T_{STG}	Operating and Storage Junction Temperature Range		–55 to 150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS (T_A = 25°C, unless otherwise noted)
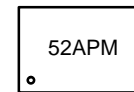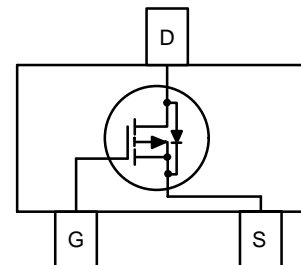
Symbol	Parameter	Max	Unit
$R_{\theta JA}$	Thermal Resistance, Junction–to–Ambient (Note 1a)	250	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction–to–Case (Note 1)	75	

1. $R_{\theta JA}$ is the sum of the junction−to−case and case−to−ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.
   a. $R_{\theta JA} = 250$°C/W when mounted on a 0.02 in² pad of 2 oz. copper.
   b. $R_{\theta JA} = 270$°C/W when mounted on a 0.001 in² pad of 2 oz. copper.

ORDERING INFORMATION

See detailed ordering and shipping information on page 5 of this data sheet.

FDN352AP

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain–Source Breakdown Voltage	V_{GS} = 0 V, I_D = –250 μA	–30	–	–	V
$\dfrac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = –250 μA, Referenced to 25°C	–	–17	–	mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = –24 V, V_{GS} = 0 V	–	–	–1	μA
I_{GSS}	Gate–Body Leakage	V_{GS} = ±25 V, V_{DS} = 0 V	–	–	±100	nA
ON CHARACTERISTICS (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = –250 μA	–0.8	–2.0	–2.5	V
$\dfrac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I_D = –250 μA, Referenced to 25°C	–	4	–	mV/°C
$R_{DS(on)}$	Static Drain–Source On–Resistance	V_{GS} = –10 V, I_D = –1.3 A	–	150	180	mΩ
		V_{GS} = –4.5 V, I_D = –1.1 A	–	250	300	
		V_{GS} = –4.5 V, I_D = –1.1 A, T_J = 125°C	–	330	400	
g_{FS}	Forward Transconductance	V_{DS} = –5 V, I_D = –0.9 A	–	2.0		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = –15 V, V_{GS} = 0 V, f = 1.0 MHz	–	150	–	pF
C_{oss}	Output Capacitance		–	40	–	pF
C_{rss}	Reverse Transfer Capacitance		–	20	–	pF
SWITCHING CHARACTERISTICS (Note 2)						
$t_{d(on)}$	Turn–On Delay Time	V_{DD} = –10 V, I_D = –1 A, V_{GS} = –10 V, R_{GEN} = 6 Ω	–	4	8	ns
t_r	Turn–On Rise Time		–	15	28	ns
$t_{d(off)}$	Turn–Off Delay Time		–	10	18	ns
t_f	Turn–Off Fall Time		–	1	2	ns
Q_g	Total Gate Charge	V_{DS} = –10 V, I_D = –0.9 A, V_{GS} = –4.5 V	–	1.4	1.9	nC
Q_{gs}	Gate–Source Charge		–	0.5	–	nC
Q_{gd}	Gate–Drain Charge		–	0.5	–	nC
DRAIN–SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I_S	Maximum Continuous Drain–Source Diode Forward Current		–	–	–0.42	A
V_{SD}	Drain–Source Diode Forward Voltage	V_{GS} = 0 V, I_S = –0.42 A (Note 2)	–	–0.8	–1.2	V
t_{rr}	Diode Reverse Recovery Time	I_F = –3.9 A, dI_F/dt = 100 A/μs	–	17	–	ns
Q_{rr}	Diode Reverse Recovery Charge		–	7	–	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
2. Pulse Test: Pulse Width ≤ 300 Ms, Duty Cycle ≤ 2.0%.

FDN352AP

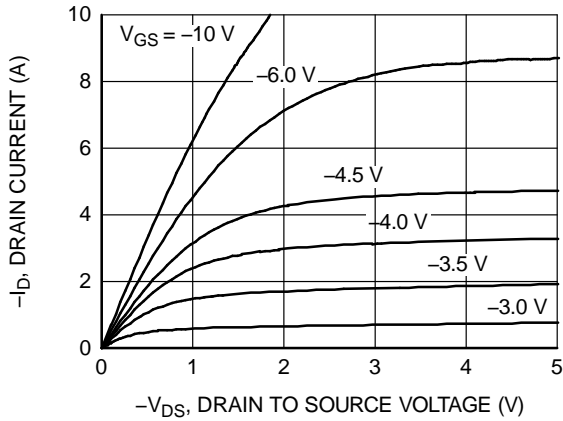## TYPICAL ELECTRICAL CHARACTERISTICS
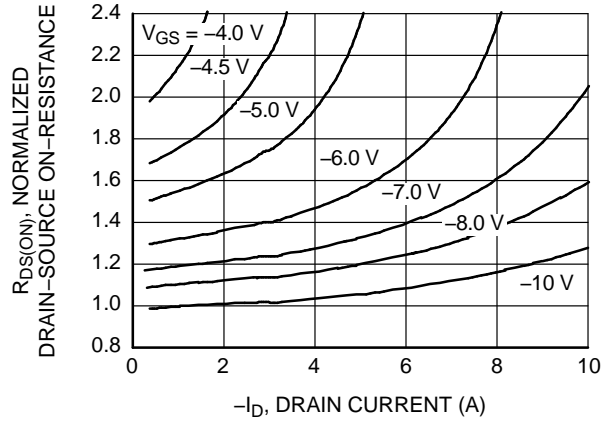
Figure 1. On−Region Characteristics

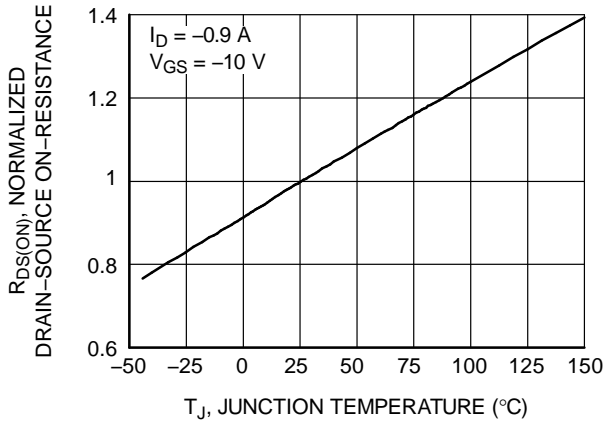**Figure 2. On−Resistance Variation with Drain Current and Gate Voltage**

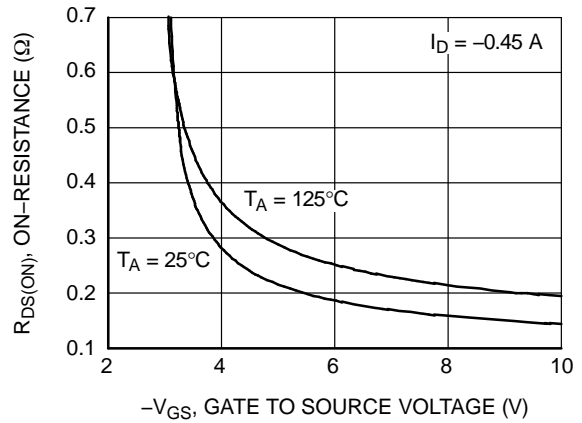**Figure 3. On−Resistance Variation with Temperature**

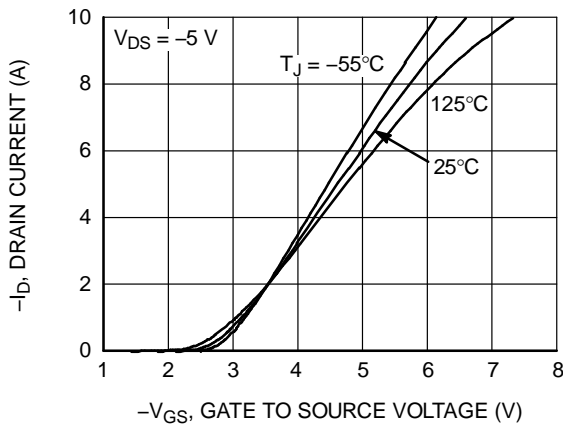**Figure 4. On−Resistance Variation with Gate−to−Source Voltage**
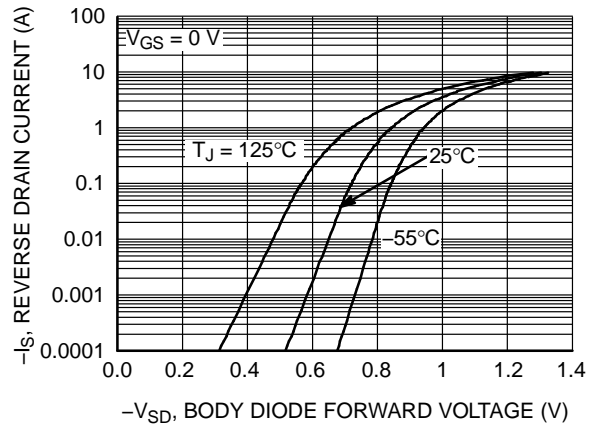
Figure 5. Transfer Characteristics

Figure 6. Diode Forward Voltage Variation with Source Current and Temperature
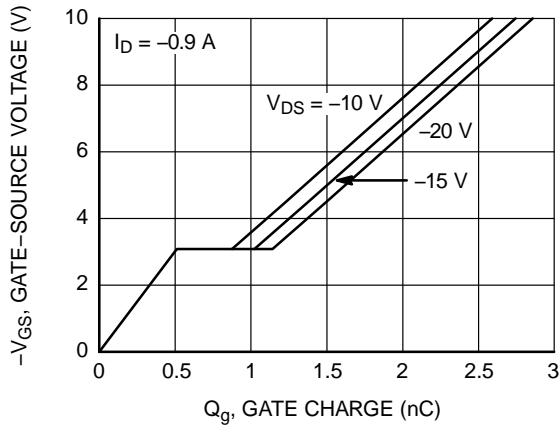
TYPICAL ELECTRICAL CHARACTERISTICS (continued)

Figure 7. Gate Charge Characteristics
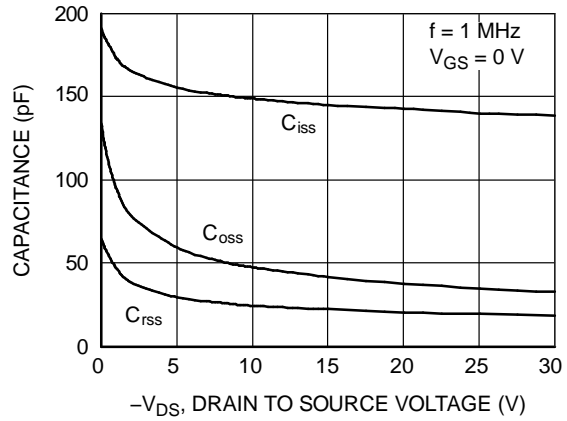
Figure 8. Capacitance Characteristics
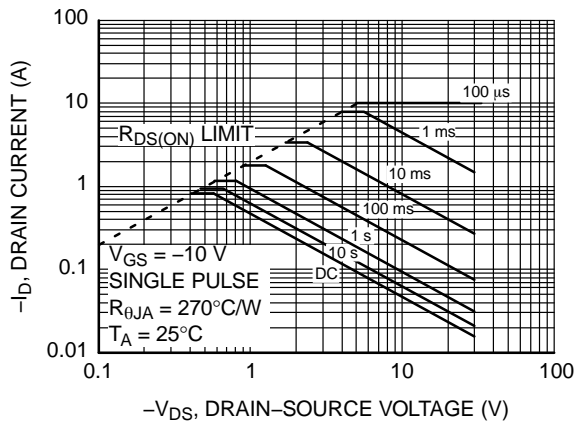
Figure 9. Maximum Safe Operating Area
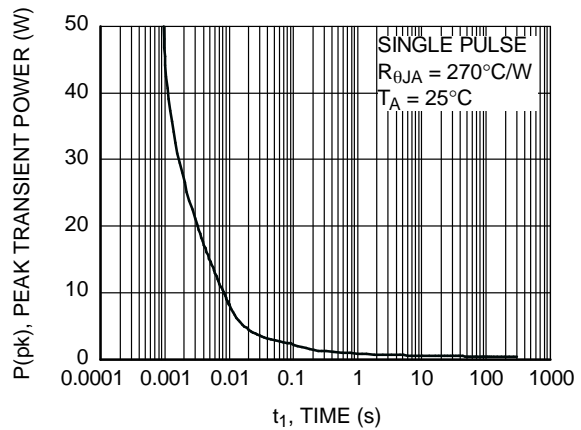
Figure 10. Single Pulse Maximum Power Dissipation
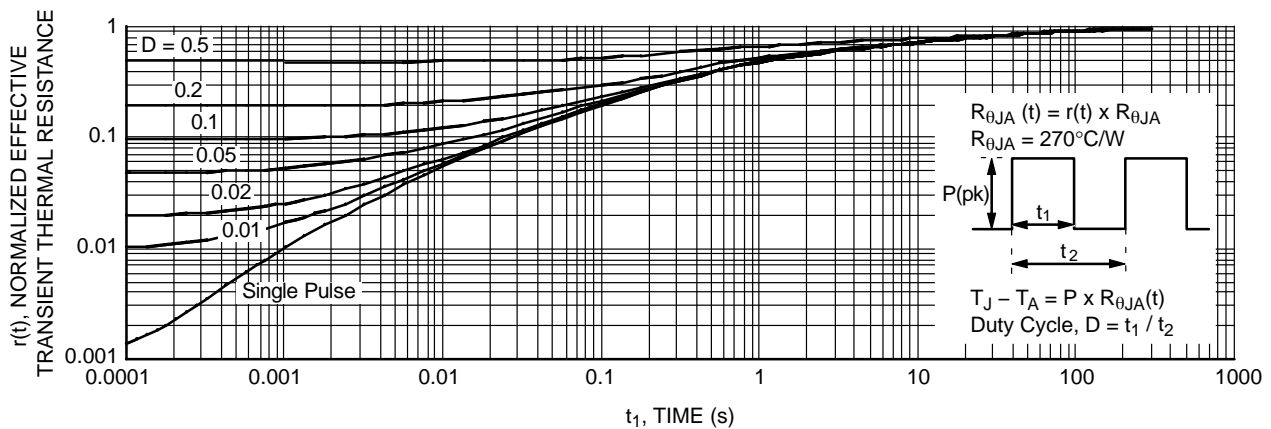
Figure 11. Transient Thermal Response Curve

Thermal characterization performed using the conditions described in Note 1b.
Transient thermal response will change depending on the circuit board design.

FDN352AP

PACKAGE MARKING AND ORDERING INFORMATION

Device	Device Marking	Package	Reel Size	Tape Width	Shipping[†]
FDN352AP	52AP	SOT–23/SUPERSOT–23, 3 LEAD, 1.4x2.9 (Pb–Free, Halide Free)	7"	8 mm	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

POWERTRENCH is registered trademark of Semiconductor Components Industries, LLC (SCILLC) or its subsidiaries in the United States and/or other countries.
SUPERSOT is trademark of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries.
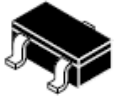
SOT−23/SUPERSOT™−23, 3 LEAD, 1.4x2.9
CASE 527AG
ISSUE A

DATE 09 DEC 2019
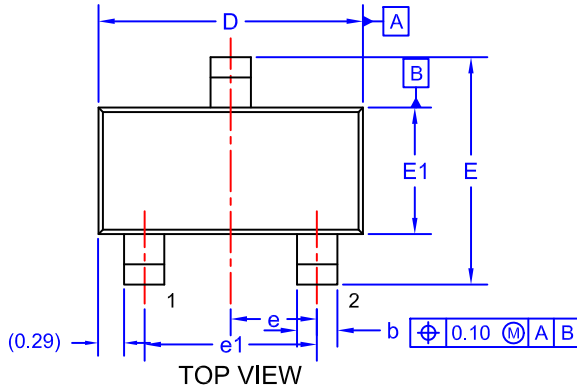
NOTES: UNLESS OTHERWISE SPECIFIED
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.

DIM	MIN.	NOM.	MAX.
A	0.85	0.95	1.12
A1	0.00	0.05	0.10
b	0.370	0.435	0.508
c	0.085	0.150	0.180
D	2.80	2.92	3.04
E	2.31	2.51	2.71
E1	1.20	1.40	1.52
e	0.95 BSC		
e1	1.90 BSC		
L	0.33	0.38	0.43

TOP VIEW

⊕ 0.10 Ⓜ A B

SIDE VIEW

⌒ 0.10 Ⓜ C

DETAIL A

GAGE PLANE

0.20

SEATING PLANE

SEE DETAIL A
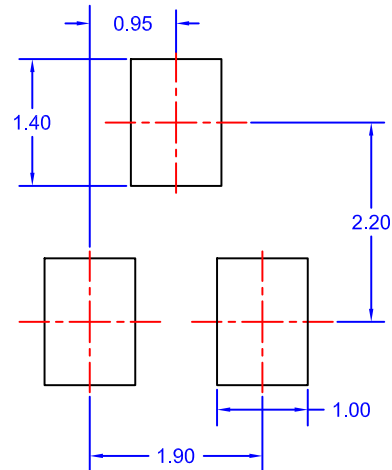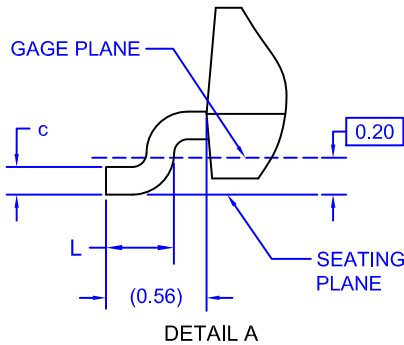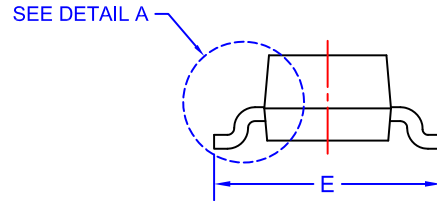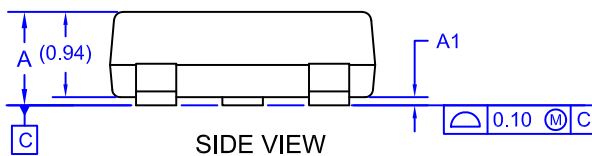
LAND PATTERN RECOMMENDATION*
*FOR ADDITIONAL INFORMATION ON OUR Pb−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

0.95
1.40
2.20
1.00
1.90

GENERIC MARKING DIAGRAM*

XXXM▪
▪
○

XXX = Specific Device Code
M = Month Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	98AON34319E	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	SOT−23/SUPERSOT−23, 3 LEAD, 1.4X2.9		PAGE 1 OF 1

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Email Requests to: orderlit@onsemi.com

onsemi Website: www.onsemi.com

TECHNICAL SUPPORT
North American Technical Support:
Voice Mail: 1 800−282−9855 Toll Free USA/Canada
Phone: 011 421 33 790 2910

Europe, Middle East and Africa Technical Support:
Phone: 00421 33 790 2910
For additional information, please contact your local Sales Representative

◊