PIC32MM0256GPM064 FAMILY

32-Bit Flash Microcontroller with MIPS32® microAptiv™ UC Core, Low Power and USB

Operating Conditions

- 2.0V to 3.6V, -40°C to +85°C, DC to 25 MHz

Low-Power Modes

- Low-Power modes:
  - Idle – CPU off, peripherals run from system clock
  - Sleep – CPU and peripherals off:
    - Fast wake-up Sleep with retention
    - Low-power Sleep with retention
- 0.65 µA Sleep current for RAM Retention Regulator mode and 5 µA for Regulator Standby mode
- On-Chip 1.8V Voltage Regulator (VREG)
- On-Chip Ultra Low-Power Retention Regulator

High-Performance 32-Bit RISC CPU

- microAptiv™ UC 32-Bit Core with 5-Stage Pipeline
- microMIPS™ Instruction Set for 35% Smaller Code and 98% Performance compared to MIPS32 Instructions
- 1.53 DMIPS/MHz (37 DMIPS) (Dhrystone 2.1) Performance
- 3.17 CoreMark®/MHz (79 CoreMark) Performance
- 16-Bit/32-Bit Wide Instructions with 32-Bit Wide Data Path
- Two Sets of 32 Core Register Files (32-bit) to Reduce Interrupt Latency
- Single-Cycle 32x16 Multiply and Two-Cycle 32x32 Multiply
- 64-Bit, Zero Wait State Flash with ECC to Maximize Endurance/Retention

Microcontroller Features

- Up to 256K Flash Memory
  - 20,000 Erase/Write Cycle Endurance
  - 20 Years Minimum Data Retention
  - Self-Programmable under Software Control
- Up to 32K SRAM Memory
- Multiple Interrupt Vectors with Individually Programmable Priority
- Fail-Safe Clock Monitor mode
- Configurable Watchdog Timer with On-Chip, Low-Power RC Oscillator
- Programmable Code Protection
- Selectable Oscillator Options Including:
  - High-precision, 8 MHz (FRC) internal RC oscillator – 2x/3x/4x/6x/12x/24x PLL, which can be clocked from FRC or the Primary Oscillator
  - Primary high-speed, crystal/resonator oscillator or external clock

Peripheral Features

- USB 2.0 Compliant Full-Speed and Low-Speed Device, Host and On-The-Go (OTG) Controller:
  - Dedicated DMA
  - Device mode operation from FRC oscillator; no crystal oscillator required
- Atomic Set, Clear and Invert Operation on Select Peripheral Registers
- High-Current Sink/Source
- Independent, Low-Power 32 kHz Timer Oscillator
- Three 4-Wire SPI modules:
  - 16-byte FIFO
  - Variable width
  - I^2S mode
- Three I^2C Master and Slave w/Address Masking and IPMI Support
- Three Enhanced Addressable UARTs:
  - RS-232, RS-485 and LIN/J2602 support
  - IrDA® with on-chip hardware encoder and decoder
- External Edge and Level Change Interrupt on All Ports
- Hardware Real-Time Clock and Calendar (RTCC)
- Up to 24 Peripheral Pin Select (PPS) Remappable Pins
- 21 Total 16-Bit Timers:
  - Three dedicated 16-bit timers/counters
  - Two can be concatenated to form a 32-bit timer
  - Two additional 16-bit timers in each MCCP and SCCP module, totaling 18
- Capture/Compare/PWM/Timer modules:
  - Two 16-bit timers or one 32-bit timer in each module
  - PWM resolution down to 21 ns
  - Three Multiple Output (MCCP) modules:
    - Flexible configuration as PWM, input capture, output compare or timers
    - Six PWM outputs
    - Programmable dead time
    - Auto-shutdown
  - Six Single Output (SCCP) modules:
    - Flexible configuration as PWM, input capture, output compare or timers
    - Single PWM output
- Reference Clock Output (REFO)
- Four Configurable Logic Cells (CLC) with Internal Connections to Select Peripherals and PPS
- 4-Channel Hardware DMA with Automatic Data Size Detection and CRC Engine

Debug Features

- Two Programming and Debugging Interfaces:
  - 2-wire ICSP™ interface with non-intrusive access and real-time data exchange with application
  - 4-wire MIPS® standard Enhanced JTAG interface
- IEEE Standard 1149.2 Compatible (JTAG) Boundary Scan

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Analog Features

- Three Analog Comparators with Input Multiplexing
- Programmable High/Low-Voltage Detect (HLVD)
- 5-Bit Comparator Voltage Reference DAC with Pin Output
- Up to 24-Channel, Software-Selectable 10/12-Bit SAR Analog-to-Digital Converter (ADC):
  - 12-bit 200K samples/second conversion rate (single Sample-and-Hold)
  - 10-bit 300k samples/second conversion rate (single Sample-and-Hold)
  - Sleep mode operation
  - Low-voltage boost for input
  - Band gap reference input feature
  - Windowed threshold compare feature
  - Auto-scan feature
- Brown-out Reset (BOR)

TABLE 1: PIC32MM0256GPM064 FAMILY DEVICES

Device	Pins	Program Memory (Kbytes)	Data Memory (Kbytes)	General Purpose I/O/PPS	16-Bit Timers Maximum	PWM Outputs Maximum	Remappable Peripherals: Dedicated 16-Bit Timers	Remappable Peripherals: UART(1)/LIN/J2602	Remappable Peripherals: MCCP(4)	Remappable Peripherals: SCCP(3)	Remappable Peripherals: CLC	Remappable Peripherals: SPI(2)/I2S	10/12-Bit ADC (External Channels)	Comparators	CRC	RTCC	I2C	USB	Packages
PIC32MM0064GPM028	28	64	16	21/18	21	18	3	3	3	6	4	3	12	3	Yes	Yes	3	Yes	SSOP/QFN/ UQFN
PIC32MM0128GPM028	28	128	16	21/18	21	18	3	3	3	6	4	3	12	3	Yes	Yes	3	Yes	SSOP/QFN/ UQFN
PIC32MM0256GPM028	28	256	32	21/18	21	18	3	3	3	6	4	3	12	3	Yes	Yes	3	Yes	SSOP/QFN/ UQFN
PIC32MM0064GPM036	36/40	64	16	27/20	21	20	3	3	3	6	4	3	15	3	Yes	Yes	3	Yes	VQFN/UQFN
PIC32MM0128GPM036	36/40	128	16	27/20	21	20	3	3	3	6	4	3	15	3	Yes	Yes	3	Yes	VQFN/UQFN
PIC32MM0256GPM036	36/40	256	32	27/20	21	20	3	3	3	6	4	3	15	3	Yes	Yes	3	Yes	VQFN/UQFN
PIC32MM0064GPM048	48	64	16	38/24	21	24	3	3	3	6	4	3	17	3	Yes	Yes	3	Yes	UQFN/TQFP
PIC32MM0128GPM048	48	128	16	38/24	21	24	3	3	3	6	4	3	17	3	Yes	Yes	3	Yes	UQFN/TQFP
PIC32MM0256GPM048	48	256	32	38/24	21	24	3	3	3	6	4	3	17	3	Yes	Yes	3	Yes	UQFN/TQFP
PIC32MM0064GPM064	64	64	16	52/24	21	24	3	3	3	6	4	3	20	3	Yes	Yes	3	Yes	QFN/TQFP
PIC32MM0128GPM064	64	128	16	52/24	21	24	3	3	3	6	4	3	20	3	Yes	Yes	3	Yes	QFN/TQFP
PIC32MM0256GPM064	64	256	32	52/24	21	24	3	3	3	6	4	3	20	3	Yes	Yes	3	Yes	QFN/TQFP

Note 1: UART1 has assigned pins. UART2 and UART3 are remappable.
2: SPI1 and SPI3 have assigned pins. SPI2 is remappable.
3: SCCP can be configured as a PWM with 1 output, input capture, output compare, 2 x 16-bit timers or 1 x 32-bit timer.
4: MCCP can be configured as a PWM with up to 6 outputs, input capture, output compare, 2 x 16-bit timers or 1 x 32-bit timer.

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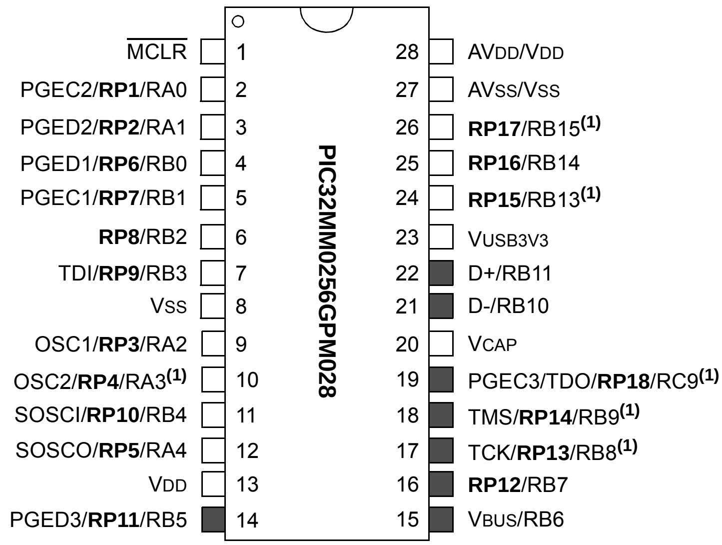
Pin Diagrams

28-Pin SSOP



Legend: Shaded pins are up to 5V tolerant.
Note 1: High drive strength pin.

TABLE 2: COMPLETE PIN FUNCTION DESCRIPTIONS FOR 28-PIN SSOP DEVICES

Pin	Function	Pin	Function
1	MCLR	15	VBUS/RB6
2	PGEC2/VREF+/CVREF+/AN0/**RP1**/OCM1E/INT3/RA0	16	**RP12**/SDA3/SDI3/OCM3F/RB7
3	PGED2/VREF-/AN1/**RP2**/OCM1F/RA1	17	TCK/**RP13**/SCL1/U1CTS/SCK1/OCM1A/RB8[1]
4	PGED1/AN2/C1IND/C2INB/C3INC/**RP6**/OCM2C/RB0	18	TMS/REFCLKI/**RP14**/SDA1/T1CK/T1G/T2CK/T2G/U1RTS/U1BCLK/SDO1/OCM1B/INT2/RB9[1]
5	PGEC1/AN3/C1INC/C2INA/**RP7**/OCM2D/RB1	19	PGEC3/TDO/**RP18**/ASCL1[2]/T3CK/T3G/USBOEN/SDO3/OCM2A/RC9[1]
6	AN4/C1INB/**RP8**/SDA2/OCM2E/RB2	20	VCAP
7	TDI/AN11/C1INA/**RP9**/SCL2/OCM2F/RB3	21	D-/RB10
8	VSS	22	D+/RB11
9	OSC1/CLKI/AN5/**RP3**/OCM1C/RA2	23	VUSB3V3
10	OSC2/CLKO/AN6/C3IND/**RP4**/OCM1D/RA3[1]	24	AN8/LVDIN/**RP15**/SCL3/SCK3/OCM3A/RB13[1]
11	SOSCI/AN7/**RP10**/OCM3C/RB4	25	CVREF/AN9/C3INB/**RP16**/RTCC/U1TX/VBUSON/SDI1/OCM3B/INT1/RB14
12	SOSCO/SCLKI/**RP5**/PWRLCLK/OCM3D/RA4	26	AN10/C3INA/REFCLKO/**RP17**/U1RX/SS1/FSYNC1/OCM2B/INT0/RB15[1]
13	VDD	27	AVSS/VSS
14	PGED3/**RP11**/ASDA1[2]/USBID/SS3/FSYNC3/OCM3E/RB5	28	AVDD/VDD

Note 1: High drive strength pin.
2: Alternate pin assignments for I2C1 as determined by the I2C1SEL Configuration bit.

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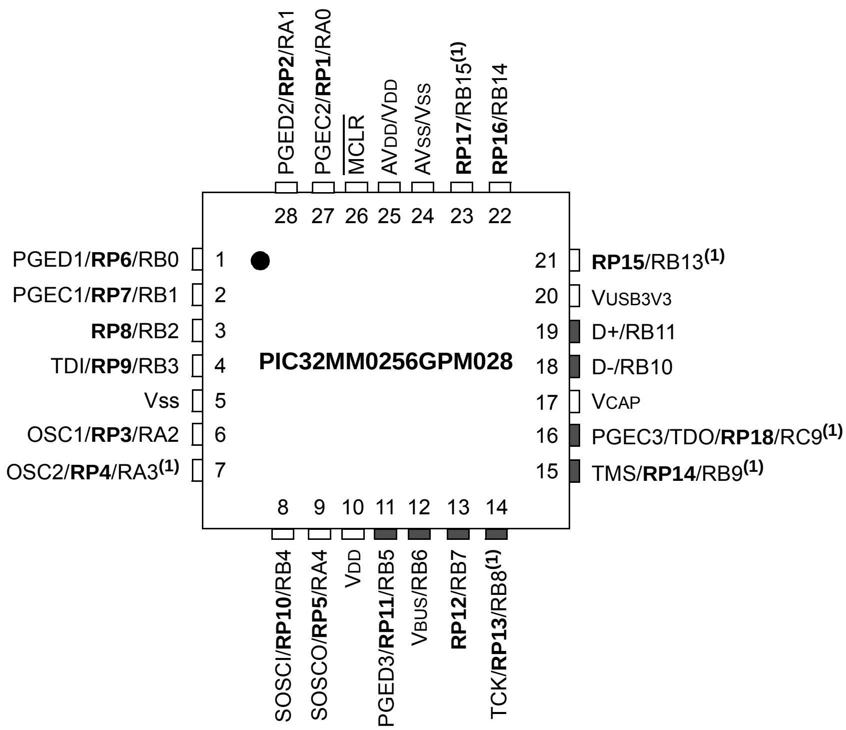
Pin Diagrams (Continued)

28-Pin QFN/UQFN



Legend: Shaded pins are up to 5V tolerant.

Note 1: High drive strength pin.

TABLE 3: COMPLETE PIN FUNCTION DESCRIPTIONS FOR 28-PIN QFN/UQFN DEVICES

Pin	Function	Pin	Function
1	PGED1/AN2/C1IND/C2INB/C3INC/**RP6**/OCM2C/RB0	15	TMS/REFCLKI/**RP14**/SDA1/T1CK/T1G/T2CK/T2G/U1RTS/U1BCLK/SDO1/OCM1B/INT2/RB9(1)
2	PGEC1/AN3/C1INC/C2INA/**RP7**/OCM2D/RB1	16	PGEC3/TDO/**RP18**/ASCL1(2)/T3CK/T3G/USBOEN/SDO3/OCM2A/RC9(1)
3	AN4/C1INB/**RP8**/SDA2/OCM2E/RB2	17	VCAP
4	TDI/AN11/C1INA/**RP9**/SCL2/OCM2F/RB3	18	D-/RB10
5	VSS	19	D+/RB11
6	OSC1/CLKI/AN5/**RP3**/OCM1C/RA2	20	VUSB3V3
7	OSC2/CLKO/AN6/C3IND/**RP4**/OCM1D/RA3(1)	21	AN8/LVDIN/**RP15**/SCL3/SCK3/OCM3A/RB13(1)
8	SOSCI/AN7/**RP10**/OCM3C/RB4	22	CVREF/AN9/C3INB/**RP16**/RTCC/U1TX/VBUSON/SDI1/OCM3B/INT1/RB14
9	SOSCO/SCLKI/**RP5**/PWRLCLK/OCM3D/RA4	23	AN10/C3INA/REFCLKO/**RP17**/U1RX/SS1/FSYNC1/OCM2B/INT0/RB15(1)
10	VDD	24	AVSS/VSS
11	PGED3/**RP11**/ASDA1(2)/USBID/SS3/FSYNC3/OCM3E/RB5	25	AVDD/VDD
12	VBUS/RB6	26	MCLR
13	**RP12**/SDA3/SDI3/OCM3F/RB7	27	PGEC2/VREF+/CVREF+/AN0/**RP1**/OCM1E/INT3/RA0
14	TCK/**RP13**/SCL1/U1CTS/SCK1/OCM1A/RB8(1)	28	PGED2/VREF-/AN1/**RP2**/OCM1F/RA1

Note 1: High drive strength pin.
2: Alternate pin assignments for I2C1 as determined by the I2C1SEL Configuration bit.

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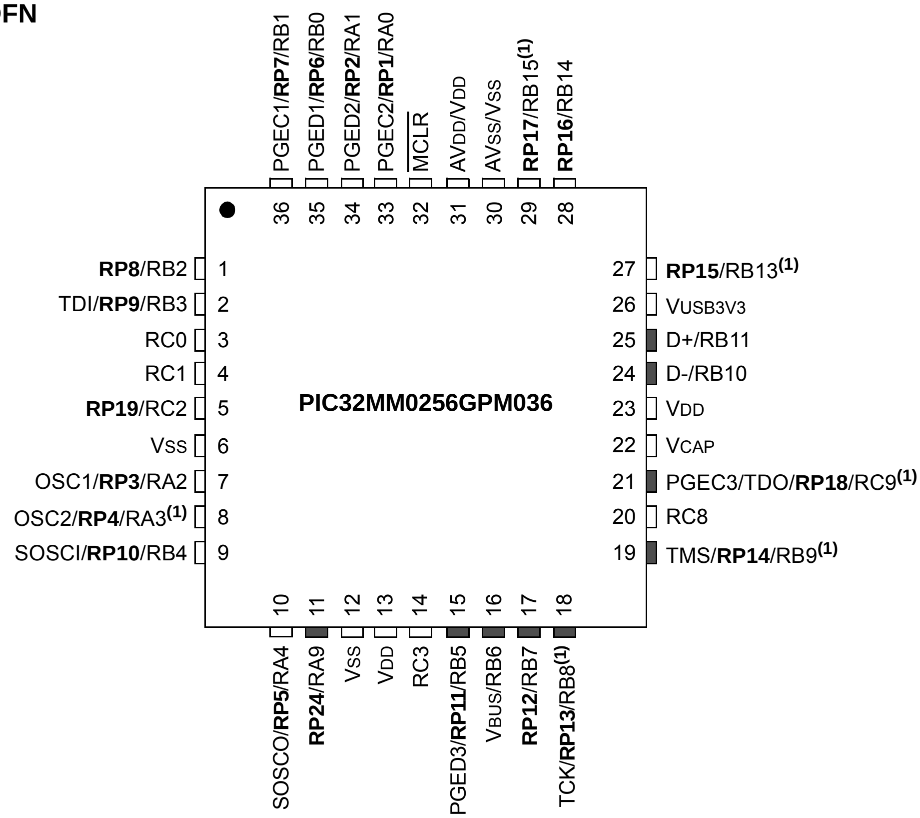
Pin Diagrams (Continued)

36-Pin QFN



Legend: Shaded pins are up to 5V tolerant.
Note 1: High drive strength pin.

TABLE 4: COMPLETE PIN FUNCTION DESCRIPTIONS FOR 36-PIN QFN DEVICES

Pin	Function	Pin	Function
1	AN4/C1INB/**RP8**/SDA2/OCM2E/RB2	19	TMS/REFCLKI/**RP14**/SDA1/T1CK/T1G/U1RTS/U1BCLK/SDO1/OCM1B/INT2/RB9[1]
2	TDI/AN11/C1INA/**RP9**/SCL2/OCM2F/RB3	20	AN14/LVDIN/C2INC/RC8
3	AN12/C2IND/T2CK/T2G/RC0	21	PGEC3/TDO/**RP18**/ASCL1[2]/USBOEN/SDO3/RC9[1]
4	AN13/T3CK/T3G/RC1	22	VCAP
5	**RP19**/OCM2A/RC2	23	VDD
6	VSS	24	D-/RB10
7	OSC1/CLKI/AN5/**RP3**/OCM1C/RA2	25	D+/RB11
8	OSC2/CLKO/AN6/C3IND/**RP4**/OCM1D/RA3[1]	26	VUSB3V3
9	SOSCI/AN7/**RP10**/OCM3C/RB4	27	AN8/**RP15**/SCL3/SCK3/RB13[1]
10	SOSCO/SCLKI/**RP5**/PWRLCLK/OCM3D/RA4	28	CVREF/AN9/C3INB/**RP16**/RTCC/U1TX/VBUSON/SDI1/OCM3B/INT1/RB14
11	**RP24**/OCM3A/RA9	29	AN10/C3INA/REFCLKO/**RP17**/U1RX/SS1/FSYNC1/OCM2B/INT0/RB15[1]
12	VSS	30	AVSS/VSS
13	VDD	31	AVDD/VDD
14	RC3	32	MCLR
15	PGED3/**RP11**/ASDA1[2]/USBID/SS3/FSYNC3/OCM3E/RB5	33	PGEC2/VREF+/CVREF+/AN0/**RP1**/OCM1E/INT3/RA0
16	VBUS/RB6	34	PGED2/VREF-/AN1/**RP2**/OCM1F/RA1
17	**RP12**/SDA3/SDI3/OCM3F/RB7	35	PGED1/AN2/C1IND/C2INB/C3INC/**RP6**/OCM2C/RB0
18	TCK/**RP13**/SCL1/U1CTS/SCK1/OCM1A/RB8[1]	36	PGEC1/AN3/C1INC/C2INA/**RP7**/OCM2D/RB1

Note 1: High drive strength pin.
2: Alternate pin assignments for I2C1 as determined by the I2C1SEL Configuration bit.

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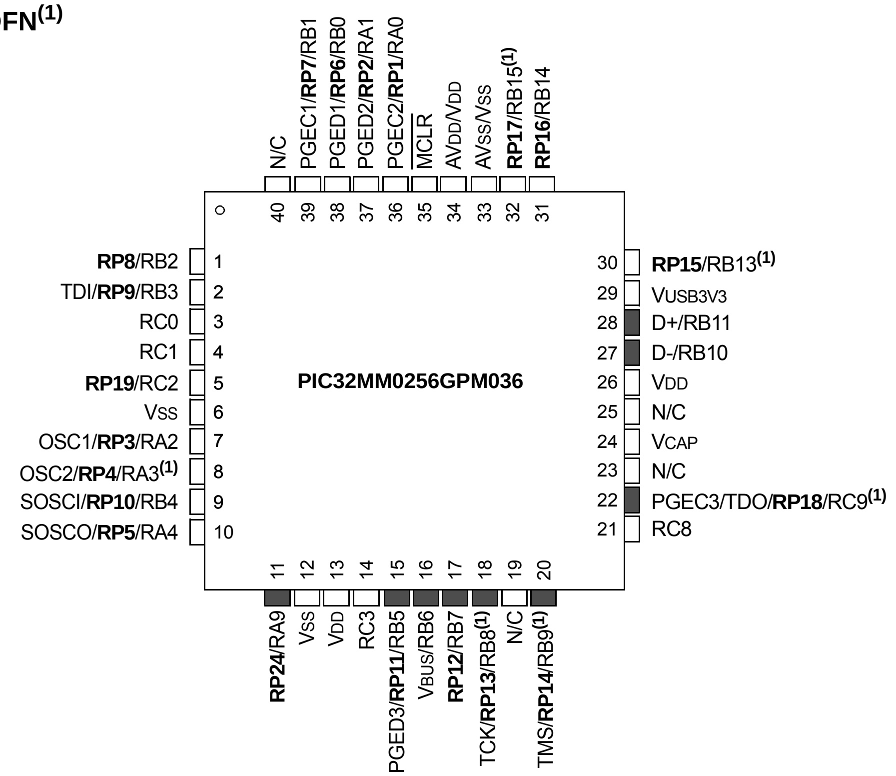
Pin Diagrams (Continued)

40-Pin UQFN[1]



Legend: Shaded pins are up to 5V tolerant.

Note 1: High drive strength pin.

TABLE 5: COMPLETE PIN FUNCTION DESCRIPTIONS FOR 40-PIN UQFN DEVICES

Pin	Function	Pin	Function
1	AN4/C1INB/**RP8**/SDA2/OCM2E/RB2	21	AN14/LVDIN/C2INC/RC8
2	TDI/AN11/C1INA/**RP9**/SCL2/OCM2F/RB3	22	PGEC3/TDO/**RP18**/ASCL1[2]/SDO3/USBOEN/RC9[1]
3	AN12/C2IND/T2CK/T2G/RC0	23	N/C
4	AN13/T3CK/T3G/RC1	24	VCAP
5	**RP19**/OCM2A/RC2	25	N/C
6	VSS	26	VDD
7	OSC1/CLKI/AN5/**RP3**/OCM1C/RA2	27	D-/RB10
8	OSC2/CLKO/AN6/C3IND/**RP4**/OCM1D/RA3[1]	28	D+/RB11
9	SOSCI/AN7/**RP10**/OCM3C/RB4	29	VUSB3V3
10	SOSCO/SCLKI/**RP5**/PWRLCLK/OCM3D/RA4	30	AN8/**RP15**/SCL3/SCK3/RB13[1]
11	**RP24**/OCM3A/RA9	31	CVREF/AN9/C3INB/**RP16**/RTCC/U1TX/VBUSON/SDI1/OCM3B/INT1/RB14
12	VSS	32	AN10/C3INA/REFCLKO/**RP17**/U1RX/SS1/FSYNC1/OCM2B/INT0/RB15[1]
13	VDD	33	AVSS/VSS
14	RC3	34	AVDD/VDD
15	PGED3/**RP11**/ASDA1[2]/USBID/SS3/FSYNC3/OCM3E/RB5	35	MCLR
16	VBUS/RB6	36	PGEC2/VREF+/CVREF+/AN0/**RP1**/OCM1E/INT3/RA0
17	**RP12**/SDA3/SDI3/OCM3F/RB7	37	PGED2/VREF-/AN1/**RP2**/OCM1F/RA1
18	TCK/**RP13**/SCL1/U1CTS/SCK1/OCM1A/RB8[1]	38	PGED1/AN2/C1IND/C2INB/C3INC/**RP6**/OCM2C/RB0
19	N/C	39	PGEC1/AN3/C1INC/C2INA/**RP7**/OCM2D/RB1
20	TMS/REFCLKI/**RP14**/SDA1/T1CK/T1G/U1RTS/U1BCLK/ SDO1/OCM1B/INT2/RB9[1]	40	N/C

Note 1: High drive strength pin.
2: Alternate pin assignments for I2C1 as determined by the I2C1SEL Configuration bit.

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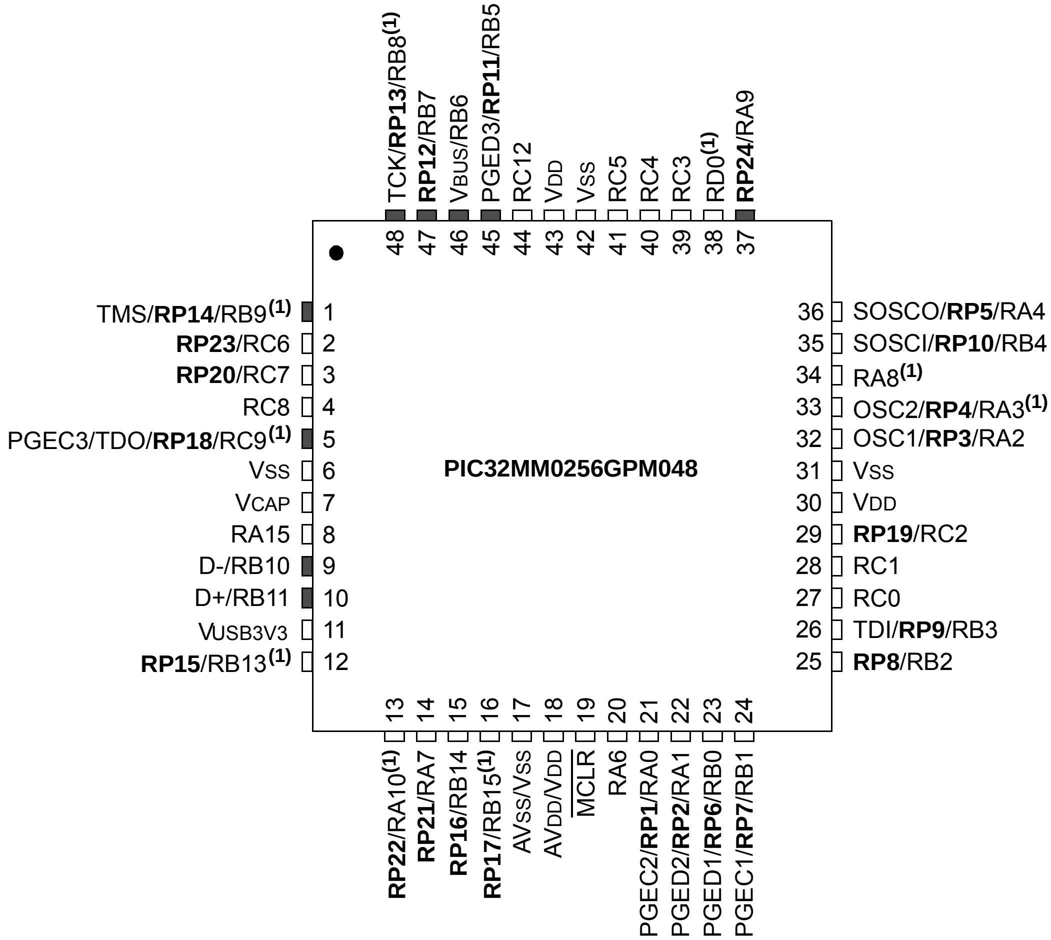
Pin Diagrams (Continued)

48-Pin UQFN, TQFP(1)



Legend: Shaded pins are up to 5V tolerant.

Note 1: High drive strength pin.

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TABLE 6: COMPLETE PIN FUNCTION DESCRIPTIONS FOR 48-PIN UQFN/TQFP DEVICES

Pin	Function	Pin	Function
1	TMS/**RP14**/SDA1/OCM1B/INT2/RB9(1)	25	AN4/C1INB/**RP8**/SDA2/OCM2E/RB2
2	**RP23**/RC6	26	TDI/AN11/C1INA/**RP9**/SCL2/OCM2F/RB3
3	**RP20**/RC7	27	AN12/C2IND/T2CK/T2G/RC0
4	AN14/LVDIN/C2INC/RC8	28	AN13/T3CK/T3G/RC1
5	PGEC3/TDO/**RP18**/ASCL1(2)/USBOEN/RC9(1)	29	**RP19**/OCM2A/RC2
6	VSS	30	VDD
7	VCAP	31	VSS
8	RTCC/RA15	32	OSC1/CLKI/AN5/**RP3**/OCM1C/RA2
9	D-/RB10	33	OSC2/CLKO/AN6/C3IND/**RP4**/RA3(1)
10	D+/RB11	34	SDO3/RA8(1)
11	VUSB3V3	35	SOSCI/AN7/**RP10**/OCM3C/RB4
12	AN8/**RP15**/SCL3/RB13(1)	36	SOSCO/SCLKI/**RP5**/PWRLCLK/OCM3D/RA4
13	**RP22**/SCK3/RA10(1)	37	**RP24**/OCM3A/RA9
14	**RP21**/SDI3/RA7	38	REFCLKI/T1CK/T1G/$\overline{\text{U1RTS}}$/U1BCLK/SDO1/RD0(1)
15	CVREF/AN9/C3INB/**RP16**/VBUSON/SDI1/OCM3B/INT1/RB14	39	OCM2B/RC3
16	AN10/C3INA/REFCLKO/**RP17**/$\overline{\text{SS1}}$/FSYNC1/INT0/RB15(1)	40	OCM1E/INT3/RC4
17	AVSS/VSS	41	AN15/OCM1D/RC5
18	AVDD/VDD	42	VSS
19	$\overline{\text{MCLR}}$	43	VDD
20	AN19/U1RX/RA6	44	U1TX/RC12
21	PGEC2/VREF+/CVREF+/AN0/**RP1**/RA0	45	PGED3/**RP11**/ASDA1(2)/USBID/$\overline{\text{SS3}}$/FSYNC3/OCM3E/RB5
22	PGED2/VREF-/AN1/**RP2**/OCM1F/RA1	46	VBUS/RB6
23	PGED1/AN2/C1IND/C2INB/C3INC/**RP6**/OCM2C/RB0	47	**RP12**/SDA3/OCM3F/RB7
24	PGEC1/AN3/C1INC/C2INA/**RP7**/OCM2D/RB1	48	TCK/**RP13**/SCL1/$\overline{\text{U1CTS}}$/SCK1/OCM1A/RB8(1)

Note 1: High drive strength pin.
2: Alternate pin assignments for I2C1 as determined by the I2C1SEL Configuration bit.

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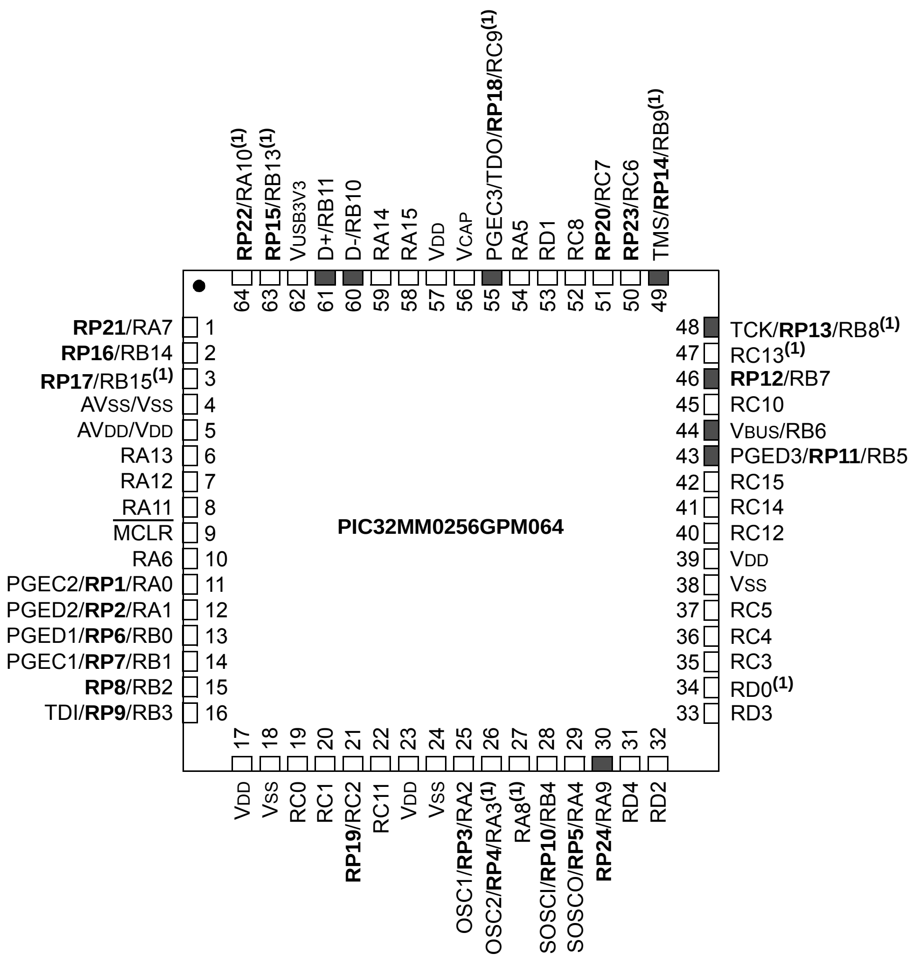
Pin Diagrams (Continued)

64-Pin QFN, TQFP(1)



Legend: Shaded pins are up to 5V tolerant.

Note 1: High drive strength pin.

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TABLE 7: COMPLETE PIN FUNCTION DESCRIPTIONS FOR 64-PIN QFN/TQFP DEVICES

Pin	Function	Pin	Function
1	**RP21**/SDI3/RA7	33	OCM3B/RD3
2	CVREF/AN9/C3INB/**RP16**/VBUSON/RB14	34	REFCLKI/T1CK/T1G/$\overline{\text{U1RTS}}$/U1BCLK/SDO1/RD0(1)
3	AN10/C3INA/REFCLKO/**RP17**/RB15(1)	35	OCM2B/RC3
4	AVSS	36	OCM1E/INT3/RC4
5	AVDD	37	AN15/OCM1D/RC5
6	AN16/$\overline{\text{U1CTS}}$/RA13	38	VSS
7	AN17/OCM1A/RA12	39	VDD
8	AN18/RA11	40	U1TX/RC12
9	$\overline{\text{MCLR}}$	41	OCM3D/RC14
10	AN19/U1RX/RA6	42	OCM3E/RC15
11	PGEC2/VREF+/CVREF+/AN0/**RP1**/RA0	43	PGED3/**RP11**/ASDA1(2)/USBID/RB5
12	PGED2/VREF-/AN1/**RP2**/OCM1F/RA1	44	VBUS/RB6
13	PGED1/AN2/C1IND/C2INB/C3INC/**RP6**/OCM2C/RB0	45	OCM3F/RC10
14	PGEC1/AN3/C1INC/C2INA/**RP7**/OCM2D/RB1	46	**RP12**/SDA3/RB7
15	AN4/C1INB/**RP8**/SDA2/OCM2E/RB2	47	SCK1/RC13(1)
16	TDI/AN11/C1INA/**RP9**/SCL2/OCM2F/RB3	48	TCK/**RP13**/SCL1/RB8(1)
17	VDD	49	TMS/**RP14**/SDA1/INT2/RB9(1)
18	VSS	50	**RP23**/RC6
19	AN12/C2IND/T2CK/T2G/RC0	51	**RP20**/RC7
20	AN13/T3CK/T3G/RC1	52	AN14/LVDIN/C2INC/RC8
21	**RP19**/OCM2A/RC2	53	OCM1B/RD1
22	$\overline{\text{SS3}}$/FSYNC3/RC11	54	OCM3A/RA5
23	VDD	55	PGEC3/TDO/**RP18**/ASCL1(2)/USBOEN/RC9(1)
24	VSS	56	VCAP
25	OSC1/CLKI/AN5/**RP3**/OCM1C/RA2	57	VDD
26	OSC2/CLKO/AN6/C3IND/**RP4**/RA3(1)	58	RTCC/RA15
27	SDO3/RA8(1)	59	OCM3C/RA14
28	SOSCI/AN7/**RP10**/RB4	60	D-/RB10
29	SOSCO/SCLKI/**RP5**/PWRLCLK/RA4	61	D+/RB11
30	**RP24**/RA9	62	VUSB3V3
31	SDI1/INT1/RD4	63	AN8/**RP15**/SCL3/RB13(1)
32	$\overline{\text{SS1}}$/FSYNC1/INT0/RD2	64	**RP22**/SCK3/RA10(1)

Note 1: High drive strength pin.
2: Alternate pin assignments for I2C1 as determined by the I2C1SEL Configuration bit.

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Referenced Sources

This device data sheet is based on the following individual sections of the *"PIC32 Family Reference Manual"*. These documents should be considered as the general reference for the operation of a particular module or device feature.

Note:	To access the documents listed below, browse the documentation section of the Microchip web site (www.microchip.com).

- **Section 1. "Introduction"** (DS60001127)
- **Section 5. "Flash Programming"** (DS60001121)
- **Section 7. "Resets"** (DS60001118)
- **Section 8. "Interrupts"** (DS61108)
- **Section 10. "Power-Saving Modes"** (DS60001130)
- **Section 12. "I/O Ports"** (DS60001120)
- **Section 14. "Timers"** (DS60001105)
- **Section 19. "Comparator"** (DS60001110)
- **Section 20. "Comparator Voltage Reference"** (DS61109)
- **Section 21. "UART"** (DS61107)
- **Section 23. "Serial Peripheral Interface (SPI)"** (DS61106)
- **Section 24. "Inter-Integrated Circuit™ (I^2C™)"** (DS61116)
- **Section 25. "12-Bit Analog-to-Digital Converter (ADC) with Threshold Detect"** (DS60001359)
- **Section 27. "USB On-The-Go (OTG)"** (DS61126)
- **Section 28. "RTCC with Timestamp"** (DS60001362)
- **Section 30. "Capture/Compare/PWM/Timer (MCCP and SCCP)"** (DS60001381)
- **Section 31. "DMA Controller"** (DS60001117)
- **Section 33. "Programming and Diagnostics"** (DS61129)
- **Section 36. "Configurable Logic Cell"** (DS60001363)
- **Section 48. "Memory Organization and Permissions"** (DS60001214)
- **Section 50. "CPU for Devices with MIPS32® microAptiv™ and M-Class Cores"** (DS60001192)
- **Section 59. "Oscillators with DCO"** (DS60001329)
- **Section 62. "Dual Watchdog Timer"** (DS60001365)

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1.0 DEVICE OVERVIEW

Note: This data sheet summarizes the features of the PIC32MM0256GPM064 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32). The information in this data sheet supersedes the information in the FRM.

This data sheet contains device-specific information for the PIC32MM0256GPM064 family devices.

Figure 1-1 illustrates a general block diagram of the core and peripheral modules in the PIC32MM0256GPM064 family of devices.

Table 1-1 lists the pinout I/O descriptions for the pins shown in the device pin tables.

FIGURE 1-1: PIC32MM0256GPM064 FAMILY BLOCK DIAGRAM

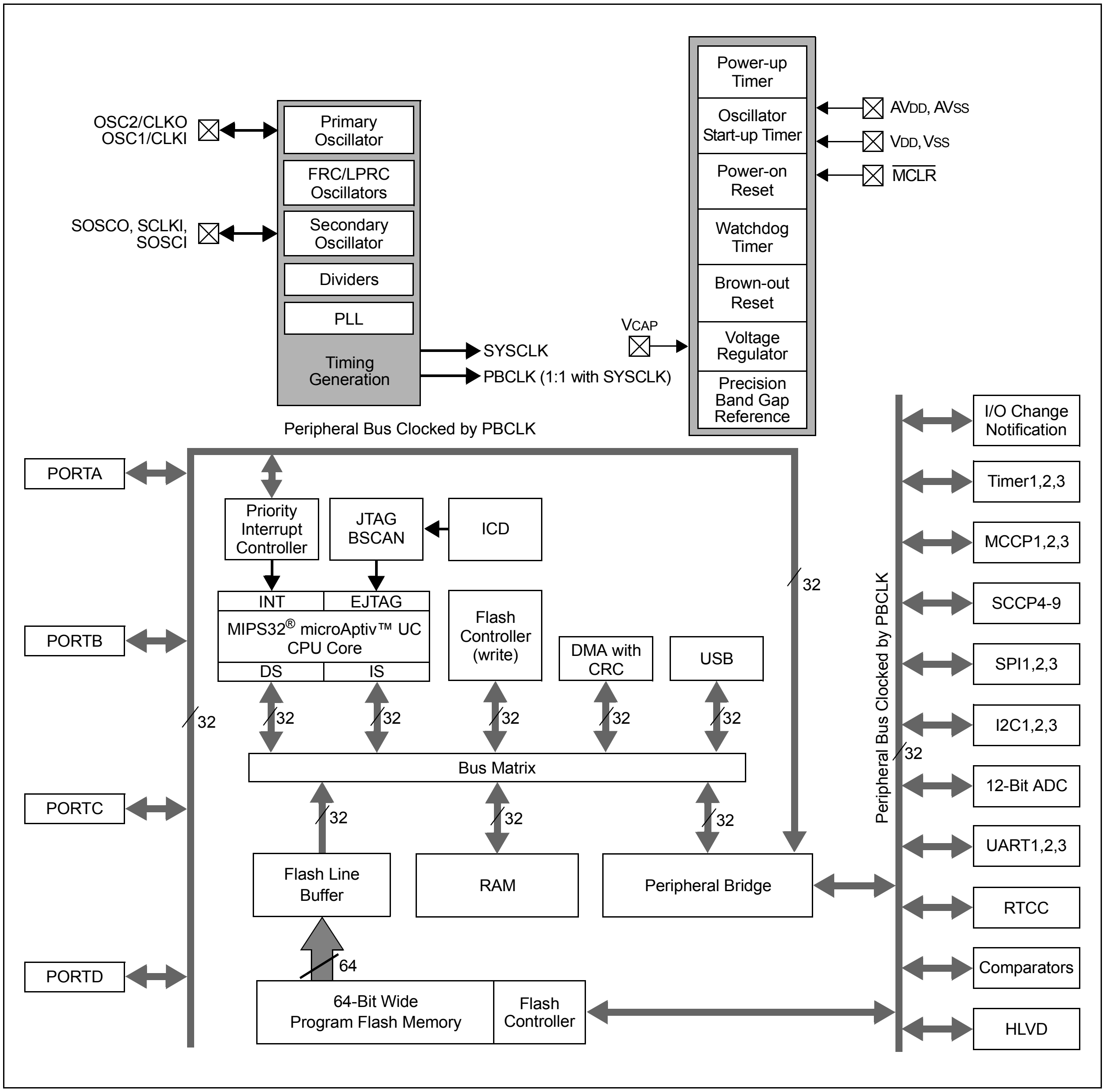

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TABLE 1-1: PIC32MM0256GPM064 FAMILY PINOUT DESCRIPTION

Pin Name	Pin Number						Pin Type	Buffer Type	Description
	28-Pin SSOP	28-Pin QFN/ UQFN	36-Pin QFN	40-Pin UQFN	48-Pin QFN/ TQFP	64-Pin QFN/ TQFP			
AN0	2	27	33	36	21	11	I	ANA	Analog-to-Digital Converter input channels
AN1	3	28	34	37	22	12	I	ANA	
AN2	4	1	35	38	23	13	I	ANA	
AN3	5	2	36	39	24	14	I	ANA	
AN4	6	3	1	1	25	15	I	ANA	
AN5	9	6	7	7	32	25	I	ANA	
AN6	10	7	8	8	33	26	I	ANA	
AN7	11	8	9	9	35	28	I	ANA	
AN8	24	21	27	30	12	63	I	ANA	
AN9	25	22	28	31	15	2	I	ANA	
AN10	26	23	29	32	16	3	I	ANA	
AN11	7	4	2	2	26	16	I	ANA	
AN12	—	—	3	3	27	19	I	ANA	
AN13	—	—	4	4	28	20	I	ANA	
AN14	—	—	20	21	4	52	I	ANA	
AN15	—	—	—	—	41	37	I	ANA	
AN16	—	—	—	—	—	6	I	ANA	
AN17	—	—	—	—	—	7	I	ANA	
AN18	—	—	—	—	—	8	I	ANA	
AN19	—	—	—	—	—	10	I	ANA	
AVDD	28	25	31	34	18	5	P	—	Analog modules power supply
AVSS	27	24	30	33	17	4	P	—	Analog modules ground
C1INA	7	4	2	2	26	16	I	ANA	Comparator 1 Input A
C1INB	6	3	1	1	25	15	I	ANA	Comparator 1 Input B
C1INC	5	2	36	39	24	14	I	ANA	Comparator 1 Input C
C1IND	4	1	35	38	23	13	I	ANA	Comparator 1 Input D
C2INA	5	2	36	39	24	14	I	ANA	Comparator 2 Input A
C2INB	4	1	35	38	23	13	I	ANA	Comparator 2 Input B
C2INC	—	—	20	21	4	52	I	ANA	Comparator 2 Input C
C2IND	—	—	3	3	27	19	I	ANA	Comparator 2 Input D
C3INA	26	23	29	32	16	3	I	ANA	Comparator 3 Input A
C3INB	25	22	28	31	15	2	I	ANA	Comparator 3 Input B
C3INC	4	1	35	38	23	13	I	ANA	Comparator 3 Input C
C3IND	10	7	8	8	33	26	I	ANA	Comparator 3 Input D
CLKI	9	6	7	7	32	25	I	ST	External Clock source input (EC mode)
CLKO	10	7	8	8	33	26	O	DIG	System clock output
CVREF	25	22	28	31	15	2	O	ANA	Comparator voltage reference output
CVREF+	2	27	33	36	21	11	I	ANA	Positive comparator voltage reference input
D+	22	19	25	28	10	61	I/O	—	USB transceiver differential plus line
D-	21	18	24	27	9	60	I/O	—	USB transceiver differential minus line
FSYNC1	26	23	29	32	16	32	I/O	ST/DIG	SPI1 frame signal input or output
FSYNC3	14	11	15	15	45	22	I/O	ST/DIG	SPI3 frame signal input or output

Legend: ST = Schmitt Trigger input buffer DIG = Digital input/output P = Power
I2C = I^2C/SMBus input buffer ANA = Analog level input/output

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TABLE 1-1: PIC32MM0256GPM064 FAMILY PINOUT DESCRIPTION (CONTINUED)

Pin Name	Pin Number						Pin Type	Buffer Type	Description
	28-Pin SSOP	28-Pin QFN/ UQFN	36-Pin QFN	40-Pin UQFN	48-Pin QFN/ TQFP	64-Pin QFN/ TQFP			
INT0	26	23	29	32	16	32	I	ST	External Interrupt 0
INT1	25	22	28	31	15	31	I	ST	External Interrupt 1
INT2	18	15	19	20	1	49	I	ST	External Interrupt 2
INT3	2	27	33	36	40	36	I	ST	External Interrupt 3
LVDIN	24	21	20	21	4	52	I	ANA	High/Low-Voltage Detect input
$\overline{\text{MCLR}}$	1	26	32	35	19	9	I	ST	Master Clear (device Reset)
OCM1A	17	14	18	18	48	7	O	DIG	MCCP1 Output A
OCM1B	18	15	19	20	1	53	O	DIG	MCCP1 Output B
OCM1C	9	6	7	7	32	25	O	DIG	MCCP1 Output C
OCM1D	10	7	8	8	41	37	O	DIG	MCCP1 Output D
OCM1E	2	27	33	36	40	36	O	DIG	MCCP1 Output E
OCM1F	3	28	34	37	22	12	O	DIG	MCCP1 Output F
OCM2A	19	16	5	5	29	21	O	DIG	MCCP2 Output A
OCM2B	26	23	29	32	39	35	O	DIG	MCCP2 Output B
OCM2C	4	1	35	38	23	13	O	DIG	MCCP2 Output C
OCM2D	5	2	36	39	24	14	O	DIG	MCCP2 Output D
OCM2E	6	3	1	1	25	15	O	DIG	MCCP2 Output E
OCM2F	7	4	2	2	26	16	O	DIG	MCCP2 Output F
OCM3A	24	21	11	11	37	54	O	DIG	MCCP3 Output A
OCM3B	25	22	28	31	15	33	O	DIG	MCCP3 Output B
OCM3C	11	8	9	9	35	59	O	DIG	MCCP3 Output C
OCM3D	12	9	10	10	36	41	O	DIG	MCCP3 Output D
OCM3E	14	11	15	15	45	42	O	DIG	MCCP3 Output E
OCM3F	16	13	17	17	47	45	O	DIG	MCCP3 Output F
OSC1	9	6	7	7	32	25	—	—	Primary Oscillator crystal
OSC2	10	7	8	8	33	26	—	—	Primary Oscillator crystal
PGEC1	5	2	36	39	24	14	I	ST	ICSP™ Port 1 programming clock input
PGEC2	2	27	33	36	21	11	I	ST	ICSP Port 2 programming clock input
PGEC3	19	16	21	22	5	55	I	ST	ICSP Port 3 programming clock input
PGED1	4	1	35	38	23	13	I/O	ST/DIG	ICSP Port 1 programming data
PGED2	3	28	34	37	22	12	I/O	ST/DIG	ICSP Port 2 programming data
PGED3	14	11	15	15	45	43	I/O	ST/DIG	ICSP Port 3 programming data
PWRLCLK	12	9	10	10	36	29	I	ST	Real-Time Clock 50/60 Hz clock input

Legend: ST = Schmitt Trigger input buffer DIG = Digital input/output P = Power
I2C = I^2C/SMBus input buffer ANA = Analog level input/output

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TABLE 1-1: PIC32MM0256GPM064 FAMILY PINOUT DESCRIPTION (CONTINUED)

Pin Name	Pin Number						Pin Type	Buffer Type	Description
	28-Pin SSOP	28-Pin QFN/ UQFN	36-Pin QFN	40-Pin UQFN	48-Pin QFN/ TQFP	64-Pin QFN/ TQFP			
RA0	2	27	33	36	21	11	I/O	ST/DIG	PORTA digital I/Os
RA1	3	28	34	37	22	12	I/O	ST/DIG	
RA2	9	6	7	7	32	25	I/O	ST/DIG	
RA3	10	7	8	8	33	26	I/O	ST/DIG	
RA4	12	9	10	10	36	29	I/O	ST/DIG	
RA5	—	—	—	—	—	54	I/O	ST/DIG	
RA6	—	—	—	—	20	10	I/O	ST/DIG	
RA7	—	—	—	—	14	1	I/O	ST/DIG	
RA8	—	—	—	—	34	27	I/O	ST/DIG	
RA9	—	—	11	11	37	30	I/O	ST/DIG	
RA10	—	—	—	—	13	64	I/O	ST/DIG	
RA11	—	—	—	—	—	8	I/O	ST/DIG	
RA12	—	—	—	—	—	7	I/O	ST/DIG	
RA13	—	—	—	—	—	6	I/O	ST/DIG	
RA14	—	—	—	—	—	59	I/O	ST/DIG	
RA15	—	—	—	—	8	58	I/O	ST/DIG	
RB0	4	1	35	38	23	13	I/O	ST/DIG	PORTB digital I/Os
RB1	5	2	36	39	24	14	I/O	ST/DIG	
RB2	6	3	1	1	25	15	I/O	ST/DIG	
RB3	7	4	2	2	26	16	I/O	ST/DIG	
RB4	11	8	9	9	35	28	I/O	ST/DIG	
RB5	14	11	15	15	45	43	I/O	ST/DIG	
RB6	15	12	16	16	46	44	I/O	ST/DIG	
RB7	16	13	17	17	47	46	I/O	ST/DIG	
RB8	17	14	18	18	48	48	I/O	ST/DIG	
RB9	18	15	19	20	1	49	I/O	ST/DIG	
RB10	21	18	24	27	9	60	I/O	ST/DIG	
RB11	22	19	25	28	10	61	I/O	ST/DIG	
RB13	24	21	27	30	12	63	I/O	ST/DIG	
RB14	25	22	28	31	15	2	I/O	ST/DIG	
RB15	26	23	29	32	16	3	I/O	ST/DIG	

Legend: ST = Schmitt Trigger input buffer; DIG = Digital input/output; P = Power
I2C = I^2C/SMBus input buffer; ANA = Analog level input/output

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TABLE 1-1: PIC32MM0256GPM064 FAMILY PINOUT DESCRIPTION (CONTINUED)

Pin Name	Pin Number						Pin Type	Buffer Type	Description
	28-Pin SSOP	28-Pin QFN/ UQFN	36-Pin QFN	40-Pin UQFN	48-Pin QFN/ TQFP	64-Pin QFN/ TQFP			
RC0	—	—	3	3	27	19	I/O	ST/DIG	PORTC digital I/Os
RC1	—	—	4	4	28	20	I/O	ST/DIG	
RC2	—	—	5	5	29	21	I/O	ST/DIG	
RC3	—	—	14	14	39	35	I/O	ST/DIG	
RC4	—	—	—	—	40	36	I/O	ST/DIG	
RC5	—	—	—	—	41	37	I/O	ST/DIG	
RC6	—	—	—	—	2	50	I/O	ST/DIG	
RC7	—	—	—	—	3	51	I/O	ST/DIG	
RC8	—	—	20	21	4	52	I/O	ST/DIG	
RC9	19	16	21	22	5	55	I/O	ST/DIG	
RC10	—	—	—	—	—	45	I/O	ST/DIG	
RC11	—	—	—	—	—	22	I/O	ST/DIG	
RC12	—	—	—	—	44	40	I/O	ST/DIG	
RC13	—	—	—	—	—	47	I/O	ST/DIG	
RC14	—	—	—	—	—	41	I/O	ST/DIG	
RC15	—	—	—	—	—	42	I/O	ST/DIG	
RD0	—	—	—	—	38	34	I/O	ST/DIG	PORTD digital I/Os
RD1	—	—	—	—	—	53	I/O	ST/DIG	
RD2	—	—	—	—	—	32	I/O	ST/DIG	
RD3	—	—	—	—	—	33	I/O	ST/DIG	
RD4	—	—	—	—	—	31	I/O	ST/DIG	
REFCLKI	18	15	19	20	38	34	I	ST	External reference clock input
REFCLKO	26	23	29	32	16	3	O	ST	External reference clock output
RP1	2	27	33	36	21	11	I/O	ST/DIG	Remappable peripherals (input or output)
RP2	3	28	34	37	22	12	I/O	ST/DIG	
RP3	9	6	7	7	32	25	I/O	ST/DIG	
RP4	10	7	8	8	33	26	I/O	ST/DIG	
RP5	12	9	10	10	36	29	I/O	ST/DIG	
RP6	4	1	35	38	23	13	I/O	ST/DIG	
RP7	5	2	36	39	24	14	I/O	ST/DIG	
RP8	6	3	1	1	25	15	I/O	ST/DIG	
RP9	7	4	2	2	26	16	I/O	ST/DIG	
RP10	11	8	9	9	35	28	I/O	ST/DIG	
RP11	14	11	15	15	45	43	I/O	ST/DIG	
RP12	16	13	17	17	47	46	I/O	ST/DIG	
RP13	17	14	18	18	48	48	I/O	ST/DIG	
RP14	18	15	19	20	1	49	I/O	ST/DIG	
RP15	24	21	27	30	12	63	I/O	ST/DIG	
RP16	25	22	28	31	15	2	I/O	ST/DIG	
RP17	26	23	29	32	16	3	I/O	ST/DIG	
RP18	19	16	21	22	5	55	I/O	ST/DIG	
RP19	—	—	5	5	29	21	I/O	ST/DIG	
RP20	—	—	—	—	3	51	I/O	ST/DIG	

Legend: ST = Schmitt Trigger input buffer; DIG = Digital input/output; P = Power; I2C = I^{2}C/SMBus input buffer; ANA = Analog level input/output

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TABLE 1-1: PIC32MM0256GPM064 FAMILY PINOUT DESCRIPTION (CONTINUED)

Pin Name	Pin Number						Pin Type	Buffer Type	Description
	28-Pin SSOP	28-Pin QFN/ UQFN	36-Pin QFN	40-Pin UQFN	48-Pin QFN/ TQFP	64-Pin QFN/ TQFP			
RP21	—	—	—	—	14	1	I/O	ST/DIG	Remappable peripherals (input or output)
RP22	—	—	—	—	13	64	I/O	ST/DIG	
RP23	—	—	—	—	2	50	I/O	ST/DIG	
RP24	—	—	11	11	37	30	I/O	ST/DIG	
RTCC	25	22	28	31	8	58	O	DIG	Real-Time Clock/Calendar alarm/seconds output
SCK1	17	14	18	18	48	47	I/O	ST/DIG	SPI1 clock (input or output)
SCK3	24	21	27	30	13	64	I/O	ST/DIG	SPI3 clock (input or output)
SCL1	17	14	18	18	48	48	I/O	I2C	I2C1 synchronous serial clock input/output
ASCL1	19	16	21	22	5	55	I/O	I2C	Alternate I2C1 synchronous serial clock input/ output
SCL2	7	4	2	2	26	16	I/O	I2C	I2C2 synchronous serial clock input/output
SCL3	24	21	27	30	12	63	I/O	I2C	I2C3 synchronous serial clock input/output
SCLKI	12	9	10	10	36	29	I	ST	Secondary Oscillator digital clock input
SDA1	18	15	19	20	1	49	I/O	I2C	I2C1 data input/output
ASDA1	14	11	15	15	45	43	I/O	I2C	Alternate I2C1 data input/output
SDA2	6	3	1	1	25	15	I/O	I2C	I2C2 data input/output
SDA3	16	13	17	17	47	46	I/O	I2C	I2C3 data input/output
SDI1	25	22	28	31	15	31	I	ST	SPI1 data input
SDI3	16	13	17	17	14	1	I	ST	SPI3 data input
SDO1	18	15	19	20	38	34	O	DIG	SPI1 data output
SDO3	19	16	21	22	34	27	O	DIG	SPI3 data output
SOSCI	11	8	9	9	35	28	—	—	Secondary Oscillator crystal
SOSCO	12	9	10	10	36	29	—	—	Secondary Oscillator crystal
$\overline{SS1}$	26	23	29	32	16	32	I	ST	SPI1 slave select input
$\overline{SS3}$	14	11	15	15	45	22	I	ST	SPI3 slave select input
T1CK	18	15	19	20	38	34	I	ST	Timer1 external clock input
T2CK	18	15	3	3	27	19	I	ST	Timer2 external clock input
T3CK	19	16	4	4	28	20	I	ST	Timer3 external clock input
T1G	18	15	19	20	38	34	I	ST	Timer1 clock gate input
T2G	18	15	3	3	27	19	I	ST	Timer2 clock gate input
T3G	19	16	4	4	28	20	I	ST	Timer3 clock gate input
TCK	17	14	18	18	48	48	I	ST	JTAG clock input
TDI	7	4	2	2	26	16	I	ST	JTAG data input
TDO	19	16	21	22	5	55	O	DIG	JTAG data output
TMS	18	15	19	20	1	49	I	ST	JTAG mode select input

Legend: ST = Schmitt Trigger input buffer; DIG = Digital input/output; P = Power
I2C = I^2C/SMBus input buffer; ANA = Analog level input/output

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TABLE 1-1: PIC32MM0256GPM064 FAMILY PINOUT DESCRIPTION (CONTINUED)

Pin Name	Pin Number						Pin Type	Buffer Type	Description
	28-Pin SSOP	28-Pin QFN/ UQFN	36-Pin QFN	40-Pin UQFN	48-Pin QFN/ TQFP	64-Pin QFN/ TQFP			
U1BCLK	18	15	19	20	38	34	O	DIG	UART1 IrDA® 16x baud clock output
$\overline{\text{U1CTS}}$	17	14	18	18	48	6	I	ST	UART1 Clear-to-Send
$\overline{\text{U1RTS}}$	18	15	19	20	38	34	O	DIG	UART1 Ready-to-Send
U1RX	26	23	29	32	20	10	I	ST	UART1 receive data input
U1TX	25	22	28	31	44	40	O	DIG	UART1 transmit data output
USBID	14	11	15	15	45	43	I	ST	USB OTG ID (OTG mode only)
USBOEN	19	16	21	22	5	55	O	—	USB transceiver output enable flag
VBUSON	25	22	28	31	15	2	O	—	USB host and On-The-Go (OTG) bus power control output
VBUS	15	12	16	16	46	44	P	—	USB VBUS connection (5V nominal)
VUSB3V3	23	20	26	29	11	62	P	—	USB transceiver power input (3.3V nominal)
VCAP	20	17	22	24	7	56	P	—	Core voltage regulator filter capacitor connection
VDD	13,28	10,25	13,23,31	13,26, 34	18,30, 43	17,23, 39,57	P	—	Digital modules power supply
VREF-	3	28	34	37	22	12	I	ANA	Analog-to-Digital Converter negative reference
VREF+	2	27	33	36	21	11	I	ANA	Analog-to-Digital Converter positive reference
VSS	8,27	5,24	6,12,30	6,12,33	6,17,31, 42	18,24, 38	P	—	Digital modules ground

Legend: ST = Schmitt Trigger input buffer DIG = Digital input/output P = Power
I2C = I²C/SMBus input buffer ANA = Analog level input/output

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2.0 GUIDELINES FOR GETTING STARTED WITH 32-BIT MICROCONTROLLERS

> **Note:** This data sheet summarizes the features of the PIC32MM0256GPM064 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32). The information in this data sheet supersedes the information in the FRM.

2.1 Basic Connection Requirements

Getting started with the PIC32MM0256GPM064 family of 32-bit Microcontrollers (MCUs) requires attention to a minimal set of device pin connections before proceeding with development. The following is a list of pin names, which must always be connected:

- All VDD and VSS pins (see **Section 2.2 "Decoupling Capacitors"**)
- All AVDD and AVSS pins, even if the ADC module is not used (see **Section 2.2 "Decoupling Capacitors"**)
- MCLR pin (see **Section 2.3 "Master Clear (MCLR) Pin"**)
- VCAP pin (see **Section 2.4 "Voltage Regulator Pin (VCAP)"**)
- PGECx/PGEDx pins, used for In-Circuit Serial Programming™ (ICSP™) and debugging purposes (see **Section 2.5 "ICSP Pins"**)
- OSC1 and OSC2 pins, when external oscillator source is used (see **Section 2.7 "External Oscillator Pins"**)
- VUSB3V3 pin, this pin must be powered for USB operation (see **Section 18.4 "Powering the USB Transceiver"**)

The following pin(s) may be required as well:

VREF+/VREF- pins, used when external voltage reference for the ADC module is implemented.

> **Note:** The AVDD and AVSS pins must be connected, regardless of ADC use and the ADC voltage reference source.

2.2 Decoupling Capacitors

The use of decoupling capacitors on power supply pins, such as VDD, VSS, AVDD and AVSS, is required. See Figure 2-1.

Consider the following criteria when using decoupling capacitors:

- **Value and type of capacitor:** A value of 0.1 µF (100 nF), 10-20V is recommended. The capacitor should be a low Equivalent Series Resistance (low-ESR) capacitor and have resonance frequency in the range of 20 MHz and higher. It is further recommended that ceramic capacitors be used.
- **Placement on the printed circuit board:** The decoupling capacitors should be placed as close to the pins as possible. It is recommended that the capacitors be placed on the same side of the board as the device. If space is constricted, the capacitor can be placed on another layer on the PCB using a via; however, ensure that the trace length from the pin to the capacitor is within one-quarter inch (6 mm) in length.
- **Handling high-frequency noise:** If the board is experiencing high-frequency noise, upward of tens of MHz, add a second ceramic-type capacitor in parallel to the above described decoupling capacitor. The value of the second capacitor can be in the range of 0.01 µF to 0.001 µF. Place this second capacitor next to the primary decoupling capacitor. In high-speed circuit designs, consider implementing a decade pair of capacitances, as close to the power and ground pins as possible. For example, 0.1 µF in parallel with 0.001 µF.
- **Maximizing performance:** On the board layout from the power supply circuit, run the power and return traces to the decoupling capacitors first, and then to the device pins. This ensures that the decoupling capacitors are first in the power chain. Equally important is to keep the trace length between the capacitor and the power pins to a minimum, thereby reducing PCB track inductance.

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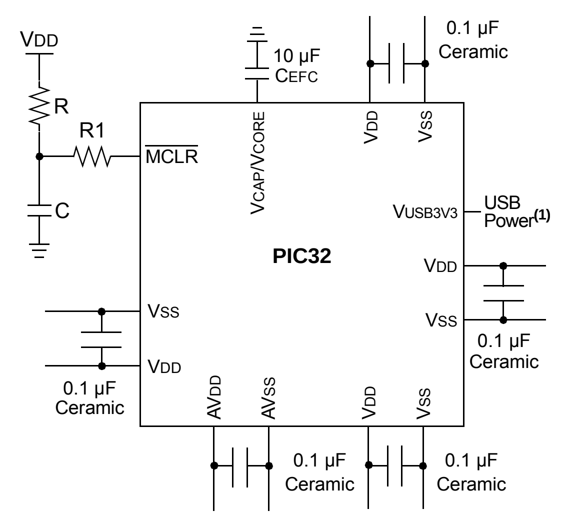
FIGURE 2-1: RECOMMENDED MINIMUM CONNECTION



Note 1: Refer to **Section 18.4 "Powering the USB Transceiver"** for requirements of this pin.

2.2.1 BULK CAPACITORS

The use of a bulk capacitor is recommended to improve power supply stability. Typical values range from 4.7 µF to 47 µF. This capacitor should be located as close to the device as possible.

2.3 Master Clear (MCLR) Pin

The MCLR pin provides for two specific device functions:

- Device Reset
- Device Programming and Debugging

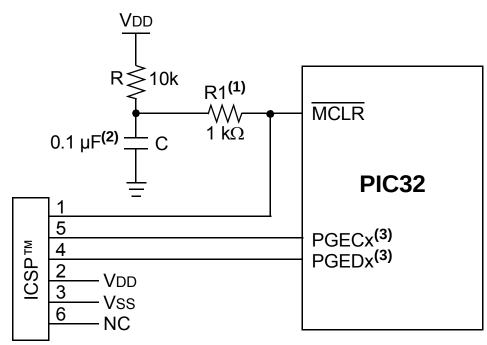
Pulling The MCLR pin low generates a device Reset. Figure 2-2 illustrates a typical MCLR circuit. During device programming and debugging, the resistance and capacitance that can be added to the pin must be considered. Device programmers and debuggers drive the MCLR pin. Consequently, specific voltage levels (VIH and VIL) and fast signal transitions must not be adversely affected. Therefore, specific values of R and C will need to be adjusted based on the application and PCB requirements.

Note:	When MCLR is used to wake the device from Retention Sleep, a POR Reset will occur.

For example, as illustrated in Figure 2-2, it is recommended that the capacitor, C, be isolated from the MCLR pin during programming and debugging operations.

Place the components illustrated in Figure 2-2 within one-quarter inch (6 mm) from the MCLR pin.

FIGURE 2-2: EXAMPLE OF MCLR PIN CONNECTIONS(1,2,3)



Note 1: 470Ω ≤ R1 ≤ 1 kΩ will limit any current flowing into MCLR from the external capacitor, C, in the event of MCLR pin breakdown, due to Electrostatic Discharge (ESD) or Electrical Overstress (EOS). Ensure that the MCLR pin VIH and VIL specifications are met without interfering with the debugger/programmer tools.

2: The capacitor can be sized to prevent unintentional Resets from brief glitches or to extend the device Reset period during POR.

3: No pull-ups or bypass capacitors are allowed on active debug/program PGECx/PGEDx pins.

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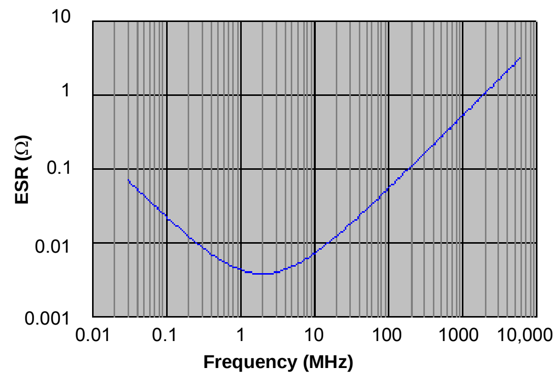
2.4 Voltage Regulator Pin (VCAP)

A low-ESR (< 5Ω) capacitor is required on the VCAP pin to stabilize the output voltage of the on-chip voltage regulator. The VCAP pin must not be connected to VDD and must use a capacitor of 10 µF connected to ground. The type can be ceramic or tantalum. Suitable examples of capacitors are shown in Table 2-1. Capacitors with equivalent specification can be used.

The placement of this capacitor should be close to VCAP. It is recommended that the trace length not exceed 0.25 inch (6 mm). Refer to **Section 29.0 "Electrical Characteristics"** for additional information.

Designers may use Figure 2-3 to evaluate ESR equivalence of candidate devices.

FIGURE 2-3: FREQUENCY vs. ESR PERFORMANCE FOR SUGGESTED VCAP



Note: Typical data measurement at +25°C, 0V DC bias.

TABLE 2-1: SUITABLE CAPACITOR EQUIVALENTS

Make	Part #	Nominal Capacitance	Base Tolerance	Rated Voltage	Temp. Range
TDK	C3216X7R1C106K	10 µF	±10%	16V	-55 to +125ºC
TDK	C3216X5R1C106K	10 µF	±10%	16V	-55 to +85ºC
Panasonic	ECJ-3YX1C106K	10 µF	±10%	16V	-55 to +125ºC
Panasonic	ECJ-4YB1C106K	10 µF	±10%	16V	-55 to +85ºC
Murata	GRM319R61C106KE15D	10 µF	±10%	16V	-55 to +85ºC

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2.4.1 CONSIDERATIONS FOR CERAMIC CAPACITORS

In recent years, large value, low-voltage, surface-mount ceramic capacitors have become very cost effective in sizes up to a few tens of microfarad. The low-ESR, small physical size and other properties make ceramic capacitors very attractive in many types of applications.

Ceramic capacitors are suitable for use with the internal voltage regulator of this microcontroller. However, some care is needed in selecting the capacitor to ensure that it maintains sufficient capacitance over the intended operating range of the application.

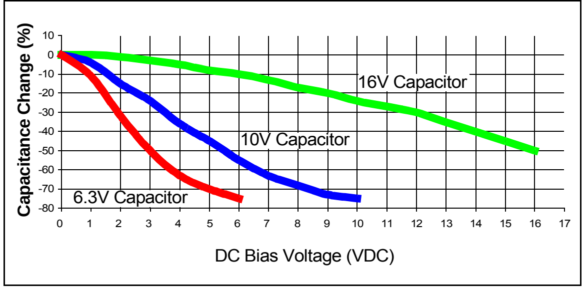
Typical low-cost, 10 μF ceramic capacitors are available in X5R, X7R and Y5V dielectric ratings (other types are also available, but are less common). The initial tolerance specifications for these types of capacitors are often specified as ±10% to ±20% (X5R and X7R) or -20%/+80% (Y5V). However, the effective capacitance that these capacitors provide in an application circuit will also vary based on additional factors, such as the applied DC bias voltage and the temperature. The total in-circuit tolerance is, therefore, much wider than the initial tolerance specification.

The X5R and X7R capacitors typically exhibit satisfactory temperature stability (ex: ±15% over a wide temperature range, but consult the manufacturer's data sheets for exact specifications). However, Y5V capacitors typically have extreme temperature tolerance specifications of +22%/-82%. Due to the extreme temperature tolerance, a 10 μF nominal rated Y5V type capacitor may not deliver enough total capacitance to meet minimum internal voltage regulator stability and transient response requirements. Therefore, Y5V capacitors are not recommended for use with the internal regulator.

In addition to temperature tolerance, the effective capacitance of large value ceramic capacitors can vary substantially, based on the amount of DC voltage applied to the capacitor. This effect can be very significant, but is often overlooked or is not always documented.

Typical DC bias voltage vs. capacitance graph for X7R type capacitors is shown in Figure 2-4.

FIGURE 2-4: DC BIAS VOLTAGE vs. CAPACITANCE CHARACTERISTICS



When selecting a ceramic capacitor to be used with the internal voltage regulator, it is suggested to select a high-voltage rating, so that the operating voltage is a small percentage of the maximum rated capacitor voltage. The minimum DC rating for the ceramic capacitor on V_{CAP} is 16V. Suggested capacitors are shown in Table 2-1.

2.5 ICSP Pins

The PGECx and PGEDx pins are used for In-Circuit Serial Programming™ (ICSP™) and debugging purposes. It is recommended to keep the trace length between the ICSP connector and the ICSP pins on the device as short as possible. If the ICSP connector is expected to experience an ESD event, a series resistor is recommended, with the value in the range of a few tens of Ohms, not to exceed 100 Ohms.

Pull-up resistors, series diodes and capacitors on the PGECx and PGEDx pins are not recommended as they will interfere with the programmer/debugger communications to the device. If such discrete components are an application requirement, they should be removed from the circuit during programming and debugging. Alternatively, refer to the AC/DC characteristics and timing requirements information in the respective device Flash programming specification for information on capacitive loading limits and pin Input Voltage High (V_{IH}) and Input Voltage Low (V_{IL}) requirements.

Ensure that the "Communication Channel Select" (i.e., PGECx/PGEDx pins) programmed into the device matches the physical connections for the ICSP to MPLAB® ICD 3 or MPLAB REAL ICE™ In-Circuit Emulator.

For more information on MPLAB® ICD 3 and REAL ICE connection requirements, refer to the following documents that are available from the Microchip web site.

- *"Using MPLAB® ICD 3"* (poster) (DS51765)
- *"Development Tools Design Advisory"* (DS51764)
- *"MPLAB® REAL ICE™ In-Circuit Emulator User's Guide"* (DS51616)
- *"Using MPLAB® REAL ICE™ In-Circuit Emulator"* (poster) (DS51749)

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2.6 JTAG

The TMS, TDO, TDI and TCK pins are used for testing and debugging according to the Joint Test Action Group (JTAG) standard. It is recommended to keep the trace length between the JTAG connector, and the JTAG pins on the device, as short as possible. If the JTAG connector is expected to experience an ESD event, a series resistor is recommended, with the value in the range of a few tens of Ohms, not to exceed 100 Ohms.

Pull-up resistors, series diodes and capacitors on the TMS, TDO, TDI and TCK pins are not recommended as they will interfere with the programmer/debugger communications to the device. If such discrete components are an application requirement, they should be removed from the circuit during programming and debugging. Alternatively, refer to the AC/DC characteristics and timing requirements information in the respective device Flash programming specification for information on capacitive loading limits, and pin Input Voltage High (V_{IH}) and Input Voltage Low (V_{IL}) requirements.

2.7 External Oscillator Pins

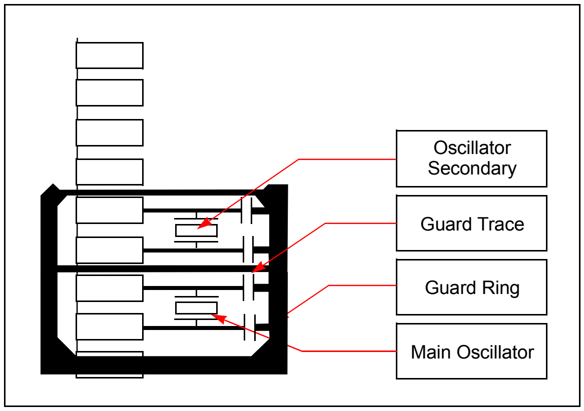
This family of devices has options for two external oscillators: a high-frequency Primary Oscillator and a low-frequency Secondary Oscillator (refer to **Section 9.0 "Oscillator Configuration"** for details).

The oscillator circuit should be placed on the same side of the board as the device. Also, place the oscillator circuit close to the respective oscillator pins, not exceeding one-half inch (12 mm) distance between them. The load capacitors should be placed next to the oscillator itself, on the same side of the board. Use a grounded copper pour around the oscillator circuit to isolate them from surrounding circuits. The grounded copper pour should be routed directly to the MCU ground. Do not run any signal traces or power traces inside the ground pour. Also, if using a two-sided board, avoid any traces on the other side of the board where the crystal is placed. A suggested layout is illustrated in Figure 2-5.

For additional information and design guidance on oscillator circuits, please refer to these Microchip Application Notes, available at the corporate web site: (www.microchip.com).

- AN826, *"Crystal Oscillator Basics and Crystal Selection for rfPIC™ and PICmicro® Devices"*
- AN849, *"Basic PICmicro® Oscillator Design"*
- AN943, *"Practical PICmicro® Oscillator Analysis and Design"*
- AN949, *"Making Your Oscillator Work"*

FIGURE 2-5: SUGGESTED OSCILLATOR CIRCUIT PLACEMENT



2.8 Unused I/Os

To minimize power consumption, unused I/O pins should not be allowed to float as inputs. They can be configured as outputs and driven to a logic low or logic high state.

Alternatively, inputs can be reserved by ensuring the pin is always configured as an input and externally connecting the pin to V_{SS} or V_{DD}. A current-limiting resistor may be used to create this connection if there is any risk of inadvertently configuring the pin as an output with the logic output state opposite of the chosen power rail.

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NOTES:

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3.0 CPU

Note:	This data sheet summarizes the features of the PIC32MM0256GPM064 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 50. "CPU for Devices with MIPS32® microAptiv™ and M-Class Cores"** (DS60001192) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32). MIPS32® microAptiv™ UC microprocessor core resources are available at: www.imgtec.com. The information in this data sheet supersedes the information in the FRM.

The MIPS32® microAptiv™ UC microprocessor core is the heart of the PIC32MM0256GPM064 family devices. The CPU fetches instructions, decodes each instruction, fetches source operands, executes each instruction and writes the results of the instruction execution to the proper destinations.

3.1 Features

The PIC32MM0256GPM064 family processor core key features include:

- 5-Stage Pipeline
- 32-Bit Address and Data Paths
- MIPS32 Enhanced Architecture:
  - Multiply-add and multiply-subtract instructions.
  - Targeted multiply instruction.
  - Zero and one detect instructions.
  - `WAIT` instruction.
  - Conditional move instructions.
  - Vectored interrupts.
  - Atomic interrupt enable/disable.
  - One GPR shadow set to minimize latency of interrupts.
  - Bit field manipulation instructions.
- microMIPS™ Instruction Set:
  - microMIPS allows improving the code size density over MIPS32, while maintaining MIPS32 performance.
  - microMIPS supports all MIPS32 instructions (except for branch-likely instructions) with new optimized 32-bit encoding. Frequent MIPS32 instructions are available as 16-bit instructions.
  - Added seventeen new and thirty-five MIPS32® corresponding, commonly used instructions in 16-bit opcode format.
  - Stack Pointer implicit in instruction.
  - MIPS32 assembly and ABI compatible.
- Memory Management Unit with Simple Fixed Mapping Translation (FMT) Mechanism
- Multiply/Divide Unit (MDU):
  - Configurable using high-performance multiplier array.
  - Maximum issue rate of one 32x16 multiply per clock.
  - Maximum issue rate of one 32x32 multiply every other clock.
  - Early-in iterative divide. Minimum 11 and maximum 33 clock latency (dividend (rs) sign extension dependent).
- Power Control:
  - No minimum frequency: 0 MHz.
  - Power-Down mode (triggered by `WAIT` instruction).
- EJTAG Debug/Profiling:
  - CPU control with start, stop and single stepping.
  - Software breakpoints via the `SDBBP` instruction.
  - Simple hardware breakpoints on virtual addresses, 4 instruction and 2 data breakpoints.
  - PC and/or load/store address sampling for profiling.
  - Performance counters.
  - Supports Fast Debug Channel (FDC).

A block diagram of the PIC32MM0256GPM064 family processor core is shown in Figure 3-1.

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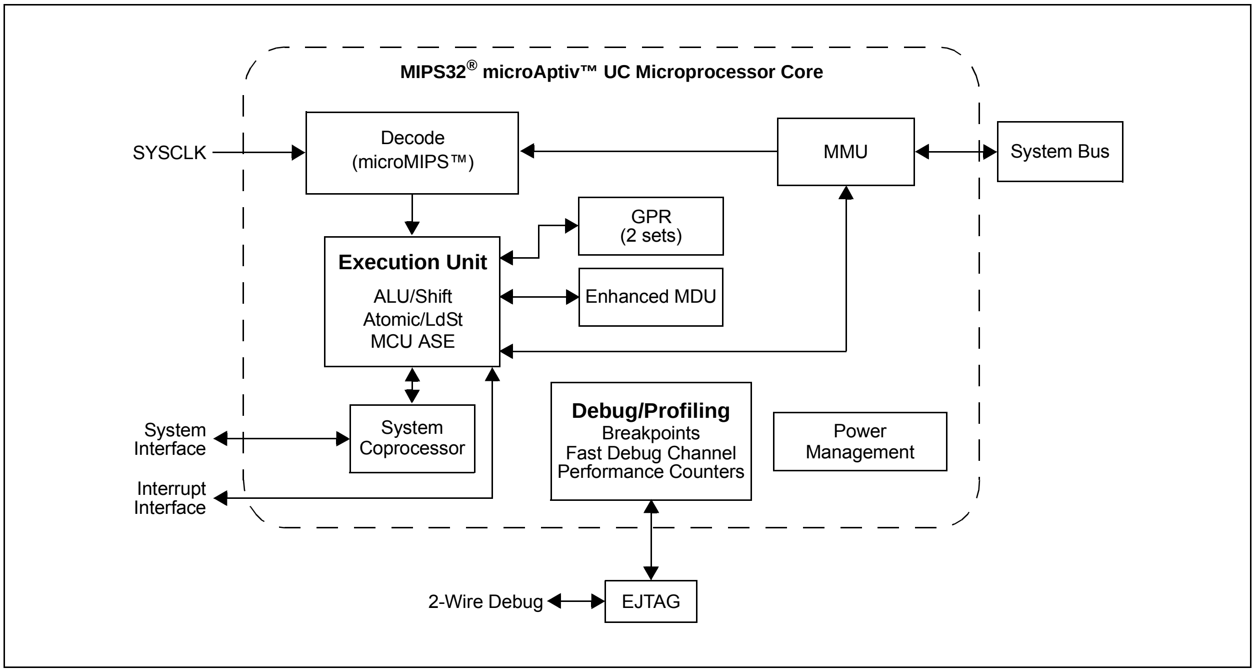
FIGURE 3-1: PIC32MM0256GPM064 FAMILY MICROPROCESSOR CORE BLOCK DIAGRAM



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3.2 Architecture Overview

The MIPS32® microAptiv™ UC microprocessor core in the PIC32MM0256GPM064 family devices contains several logic blocks, working together in parallel, providing an efficient high-performance computing engine. The following blocks are included with the core:

- Execution Unit
- General Purpose Register (GPR)
- Multiply/Divide Unit (MDU)
- System Control Coprocessor (CP0)
- Memory Management Unit (MMU)
- Power Management
- microMIPS Instructions Decoder
- Enhanced JTAG (EJTAG) Controller

3.2.1 EXECUTION UNIT

The processor core execution unit implements a load/store architecture with single-cycle ALU operations (logical, shift, add, subtract) and an autonomous Multiply/Divide Unit (MDU). The core contains thirty-two 32-bit General Purpose Registers (GPRs) used for integer operations and address calculation. One additional register file shadow set (containing thirty-two registers) is added to minimize context switching overhead during interrupt/exception processing. The register file consists of two read ports and one write port, and is fully bypassed to minimize operation latency in the pipeline.

The execution unit includes:

- 32-bit adder used for calculating the data address
- Address unit for calculating the next instruction address
- Logic for branch determination and branch target address calculation
- Load aligner
- Bypass multiplexers used to avoid Stalls when executing instruction streams where data producing instructions are followed closely by consumers for their results
- Leading zero/one detect unit for implementing the `CLZ` and `CLO` instructions
- Arithmetic Logic Unit (ALU) for performing arithmetic and bitwise logical operations
- Shifter and store aligner

3.2.2 MULTIPLY/DIVIDE UNIT (MDU)

The microAptiv UC core includes a Multiply/Divide Unit (MDU) that contains a separate pipeline for multiply and divide operations. This pipeline operates in parallel with the Integer Unit (IU) pipeline and does not stall when the IU pipeline stalls. This allows the long-running MDU operations to be partially masked by system Stalls and/or other Integer Unit instructions.

The high-performance MDU consists of a 32x16 booth recoded multiplier, Result/Accumulation registers (HI and LO), a divide state machine, and the necessary multiplexers and control logic. The first number shown ('32' of 32x16) represents the rs operand. The second number ('16' of 32x16) represents the rt operand. The microAptiv UC core only checks the value of the rt operand to determine how many times the operation must pass through the multiplier. The 16x16 and 32x16 operations pass through the multiplier once. A 32x32 operation passes through the multiplier twice.

The MDU supports execution of one 16x16 or 32x16 multiply operation every clock cycle; 32x32 multiply operations can be issued every other clock cycle. Appropriate interlocks are implemented to stall the issuance of back-to-back, 32x32 multiply operations. The multiply operand size is automatically determined by logic built into the MDU. Divide operations are implemented with a simple 1-bit-per-clock iterative algorithm. An early-in detection checks the sign extension of the dividend (rs) operand. If rs is 8 bits wide, 23 iterations are skipped. For a 16-bit wide rs, 15 iterations are skipped, and for a 24-bit wide rs, 7 iterations are skipped. Any attempt to issue a subsequent MDU instruction while a divide is still active causes an IU pipeline Stall until the divide operation has completed.

Table 3-1 lists the repeat rate (peak issue rate of cycles until the operation can be re-issued), and latency (number of cycles until a result is available) for the microAptiv UC core multiply and divide instructions. The approximate latency and repeat rates are listed in terms of pipeline clocks.

TABLE 3-1: MULTIPLY/DIVIDE UNIT LATENCIES AND REPEAT RATES

Opcode	Operand Size (mul *rt*) (div *rs*)	Latency	Repeat Rate
`MULT/MULTU`, `MADD/MADDU`, `MSUB/MSUBU`	16 bits	1	1
	32 bits	2	2
`MUL` (GPR destination)	16 bits	2	1
	32 bits	3	2
`DIV/DIVU`	8 bits	12	11
	16 bits	19	18
	24 bits	26	25
	32 bits	33	32

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The MIPS® architecture defines that the result of a multiply or divide operation be placed in the HI and LO registers. Using the Move-From-HI (MFHI) and Move-From-LO (MFLO) instructions, these values can be transferred to the general purpose register file.

In addition to the HI/LO targeted operations, the MIPS architecture also defines a Multiply instruction, MUL, which places the least significant results in the primary register file instead of the HI/LO register pair. By avoiding the explicit MFLO instruction, required when using the LO register, and by supporting multiple destination registers, the throughput of multiply-intensive operations is increased.

Two other instructions, Multiply-Add (MADD) and Multiply-Subtract (MSUB), are used to perform the multiply-accumulate and multiply-subtract operations. The MADD instruction multiplies two numbers and then adds the product to the current contents of the HI and LO registers. Similarly, the MSUB instruction multiplies two operands and then subtracts the product from the HI and LO registers. The MADD and MSUB operations are commonly used in DSP algorithms.

3.2.3 SYSTEM CONTROL COPROCESSOR (CP0)

In the MIPS architecture, CP0 is responsible for the virtual-to-physical address translation, the exception control system, the processor's diagnostics capability, the operating modes (Kernel, User and Debug) and whether interrupts are enabled or disabled. These configuration options and other system information are available by accessing the CP0 registers listed in Table 3-2.

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TABLE 3-2: COPROCESSOR 0 REGISTERS

Register Number	Register Name	Function
0-3	Reserved	Reserved in the microAptiv™ UC.
4	UserLocal	User information that can be written by privileged software and read via `RDHWR` Register 29.
5-6	Reserved	Reserved in the microAptiv UC.
7	HWREna	Enables access via the `RDHWR` instruction to selected hardware registers in Non-Privileged mode.
8	BadVAddr(1)	Reports the address for the most recent address related exception.
9	Count(1)	Processor cycle count.
10	Reserved	Reserved in the microAptiv UC.
11	Compare(1)	Timer interrupt control.
12	Status/ IntCtl/ SRSCtl/ SRSMap1/ View_IPL/ SRSMAP2	Processor status and control; interrupt control and shadow set control.
13	Cause(1)/ View_RIPL	Cause of last exception.
14	EPC(1)	Program Counter at last exception.
15	PRId/ EBase/ CDMMBase	Processor identification and revision; exception base address; Common Device Memory Map Base register.
16	CONFIG/ CONFIG1/ CONFIG2/ CONFIG3/ CONFIG7	Configuration registers.
7-22	Reserved	Reserved in the microAptiv UC.
23	Debug/ Debug2/ TraceControl/ TraceControl2/ UserTraceData1/ TraceBPC(2)	EJTAG Debug register. EJTAG Debug Register 2. EJTAG Trace Control register. EJTAG Trace Control Register 2. EJTAG User Trace Data 1 register. EJTAG Trace Breakpoint register.
24	DEPC(2)/ UserTraceData2	Program Counter at last debug exception. EJTAG User Trace Data 2 register.
25	PerfCtl0/ PerfCnt0/ PerfCtl1/ PerfCnt1	Performance Counter 0 control. Performance Counter 0. Performance Counter 1 control. Performance Counter 1.
26	ErrCtl	Software parity check enable.
27	CacheErr	Records information about SRAM parity errors.
28-29	Reserved	Reserved in the PIC32 core.
30	ErrorEPC(1)	Program Counter at last error.
31	DeSAVE(2)	Debug Handler Scratchpad register.

Note 1: Registers used in exception processing.
2: Registers used in debug.

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3.3 Power Management

The processor core offers a number of power management features, including low-power design, active power management and Power-Down modes of operation. The core is a static design that supports slowing or halting of the clocks, which reduces system power consumption during Idle periods.

The mechanism for invoking Power-Down mode is implemented through execution of the `WAIT` instruction, used to initiate Sleep or Idle. The majority of the power consumed by the processor core is in the clock tree and clocking registers. The PIC32MM family makes extensive use of local gated clocks to reduce this dynamic power consumption.

3.4 EJTAG Debug Support

The microAptiv UC core has an Enhanced JTAG (EJTAG) interface for use in the software debug. In addition to the standard mode of operation, the microAptiv UC core provides a Debug mode that is entered after a debug exception (derived from a hardware breakpoint, single-step exception, etc.) is taken and continues until a Debug Exception Return (`DERET`) instruction is executed. During this time, the processor executes the debug exception handler routine.

The EJTAG interface operates through the Test Access Port (TAP), a serial communication port used for transferring test data in and out of the microAptiv UC core. In addition to the standard JTAG instructions, special instructions defined in the EJTAG specification specify which registers are selected and how they are used.

3.5 MIPS32® microAptiv™ UC Core Configuration

Register 3-1 through Register 3-4 show the default configuration of the microAptiv UC core, which is included on PIC32MM0256GPM064 family devices.

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REGISTER 3-1: CONFIG: CONFIGURATION REGISTER; CP0 REGISTER 16, SELECT 0

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	r-1	R/W-0	R/W-1	R/W-0	R/W-0	R/W-1	R/W-0	r-0
	—	K23<2:0>			KU<2:0>[(1)]			—
23:16	r-0	R-0	R-1	R-0	r-0	r-0	r-0	R-1
	—	UDI	SB	MDU	—	—	—	DS
15:8	R-0	R-0	R-0	R-0	R-0	R-1	R-0	R-1
	BE	AT<1:0>		AR<2:0>			MT<2:1>	
7:0	R-1	r-0	r-0	r-0	r-0	R/W-0	R/W-1	R/W-0
	MT<0>	—	—	—	—	K0<2:0>		

Legend:	r = Reserved bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **Reserved:** This bit is hardwired to '1' to indicate the presence of the CONFIG1 register

bit 30-28 **K23<2:0>:** Cacheability of the kseg2 and kseg3 Segments bits
`010` = Cache is not implemented

bit 27-25 **KU<2:0>:** Cacheability of the kuseg and useg Segments bits[(1)]
`010` = Cache is not implemented

bit 24-23 **Reserved:** Must be written as zeros; returns zeros on reads

bit 22 **UDI:** User-Defined bit
`0` = CorExtend user-defined instructions are not implemented

bit 21 **SB:** SimpleBE bit
`1` = Only Simple Byte Enables are allowed on the internal bus interface

bit 20 **MDU:** Multiply/Divide Unit bit
`0` = Fast, high-performance MDU

bit 19-17 **Reserved:** Must be written as zeros; returns zeros on reads

bit 16 **DS:** Dual SRAM Interface bit
`1` = Dual instruction/data SRAM interface

bit 15 **BE:** Endian Mode bit
`0` = Little-endian

bit 14-13 **AT<1:0>:** Architecture Type bits
`00` = MIPS32®

bit 12-10 **AR<2:0>:** Architecture Revision Level bits
`001` = MIPS32 Release 2

bit 9-7 **MT<2:0>:** MMU Type bits
`011` = Fixed mapping

bit 6-3 **Reserved:** Must be written as zeros; returns zeros on reads

bit 2-0 **K0<2:0>:** kseg0 Coherency Algorithm bits
`010` = Cache is not implemented

Note 1: The KU<2:0> bits are not usable as this device does not support User mode.

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REGISTER 3-2: CONFIG1: CONFIGURATION REGISTER 1; CP0 REGISTER 16, SELECT 1

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	r-1	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	R-1	R-0	R-0	R-1	R-0
	—	—	—	PC	WR	CA	EP	FP

Legend:	r = Reserved bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31 **Reserved:** This bit is hardwired to ‘1’ to indicate the presence of the CONFIG2 register

bit 30-5 **Unimplemented:** Read as ‘0’

bit 4 **PC:** Performance Counter bit
1 = The processor core contains performance counters

bit 3 **WR:** Watch Register Presence bit
0 = No Watch registers are present

bit 2 **CA:** Code Compression Implemented bit
0 = No MIPS16e® are present

bit 1 **EP:** EJTAG Present bit
1 = Core implements EJTAG

bit 0 **FP:** Floating Point Unit bit
0 = Floating point unit is not implemented

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REGISTER 3-3: CONFIG3: CONFIGURATION REGISTER 3; CP0 REGISTER 16, SELECT 3

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	r-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	R-0	R-1	R-0	R-0	R-0	R-1	R-1
	—	IPLW<1:0>		MMAR<2:0>			MCU	ISAONEXC
15:8	R-0	R-1	R-1	R-1	U-0	U-0	U-0	R-0
	ISA<1:0>		ULRI	RXI	—	—	—	ITL
7:0	U-0	R-1	R-1	R-0	R-1	U-0	U-0	R-0
	—	VEIC	VINT	SP	CDMM	—	—	TL

Legend:	r = Reserved bit	y = Value set from Configuration bits on POR	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **Reserved:** This bit is hardwired as '0'

bit 30-23 **Unimplemented:** Read as '0'

bit 22-21 **IPLW<1:0>:** Width of the Status IPL and Cause RIPL bits
01 = IPL and RIPL bits are 8 bits in width

bit 20-18 **MMAR<2:0>:** microMIPS™ Architecture Revision Level bits
000 = Release 1

bit 17 **MCU:** MIPS® MCU ASE Implemented bit
1 = MCU ASE is implemented

bit 16 **ISAONEXC:** ISA on Exception bit
1 = microMIPS is used on entrance to an exception vector

bit 15-14 **ISA<1:0>:** Instruction Set Availability bits
01 = Only microMIPS is implemented

bit 13 **ULRI:** UserLocal Register Implemented bit
1 = UserLocal Coprocessor 0 register is implemented

bit 12 **RXI:** RIE and XIE Implemented in PageGrain bit
1 = RIE and XIE bits are implemented

bit 11-9 **Unimplemented:** Read as '0'

bit 8 **ITL:** Indicates that iFlowtrace™ Hardware is Present bit
0 = The iFlowtrace hardware is not implemented in the core

bit 7 **Unimplemented:** Read as '0'

bit 6 **VEIC:** External Vector Interrupt Controller bit
1 = Support for an external interrupt controller is implemented.

bit 5 **VINT:** Vector Interrupt bit
1 = Vector interrupts are implemented

bit 4 **SP:** Small Page bit
0 = 4-Kbyte page size

bit 3 **CDMM:** Common Device Memory Map bit
1 = CDMM is implemented

bit 2-1 **Unimplemented:** Read as '0'

bit 0 **TL:** Trace Logic bit
0 = Trace logic is not implemented

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REGISTER 3-4: CONFIG5: CONFIGURATION REGISTER 5; CP0 REGISTER 16, SELECT 5

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	R-1
	—	—	—	—	—	—	—	NF

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-1 **Unimplemented:** Read as ‘0’

bit 0 **NF:** Nested Fault bit

1 = Nested Fault feature is implemented

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4.0 MEMORY ORGANIZATION

PIC32MM microcontrollers provide 4 GBytes of unified virtual memory address space. All memory regions, including program memory, data memory, SFRs and Configuration registers, reside in this address space at their respective unique addresses. The data memory can be made executable, allowing the CPU to execute code from data memory.

Key features include:

- 32-Bit Native Data Width
- Separate Boot Flash Memory (BFM) for Protected Code
- Robust Bus Exception Handling to Intercept Runaway Code
- Simple Memory Mapping with Fixed Mapping Translation (FMT) Unit

The PIC32MM0256GPM064 family devices implement two address spaces: virtual and physical. All hardware resources, such as program memory, data memory and peripherals, are located at their respective physical addresses. Virtual addresses are exclusively used by the CPU to fetch and execute instructions. Physical addresses are used by peripherals, such as Flash controllers, that access memory independently of the CPU.

The virtual address space is divided into two segments of 512 Mbytes each, labeled kseg0 and kseg1. The Program Flash Memory (PFM) and Data RAM Memory (DRM) are accessible from either kseg0 or kseg1, while the Boot Flash Memory (BFM) and peripheral SFRs are accessible only from kseg1.

The Fixed Mapping Translation (FMT) unit translates the memory segments into corresponding physical address regions. Figure 4-1 through Figure 4-3 illustrate the fixed mapping scheme, implemented by the PIC32MM0256GPM064 family core, between the virtual and physical address space.

The mapping of the memory segments depends on the CPU error level, set by the ERL bit in the CPU STATUS register. Error level is set (ERL = 1) by the CPU on a Reset, Soft Reset or Non-Maskable Interrupt (NMI). In this mode, the CPU can access memory by the physical address. This mode is provided for compatibility with other MIPS processor cores that use a TLB-based MMU. The C start-up code clears the ERL bit to zero, so that when application software starts up, it sees the proper virtual to physical memory mapping.

4.1 Alternate Configuration Bits Space

Every Configuration Word has an associated Alternate Word (designated by the letter A as the first letter in the name of the word). During device start-up, Primary Words are read, and if uncorrectable ECC errors are found, the BCFGERR (RCON<27>) flag is set and Alternate Words are used. If uncorrectable ECC errors are found in Primary and Alternate Words, the BCFGFAIL (RCON<26>) flag is set, and the default configuration is used. The Primary Configuration bits' area is located at the address range, from 0x1FC01780 to 0x1FC017E8. The Alternate Configuration bits' area is located at the address range, from 0x1FC01700 to 0x1FC01768.

4.2 Bus Matrix (BMX)

The BMX is a switch fabric that connects the system bus initiators (Flash controller, CPU instruction, CPU data, system DMA and USB) to bus targets (RAM, Flash and peripherals without integrated DMA). All data and instructions are transferred through this bus. Only one initiator can connect to a given target at a time. Multiple initiators can be active at one time provided each one has a separate target. Multiple priority modes (Round Robin, Fixed CPU Highest and Fixed CPU Lowest) are available to allow the priority to be tailored to the application needs. Mode 0 is a Fixed Priority mode with the CPU having the highest priority (refer to Table 4-1). For most applications, this mode should be sufficient; however, it is possible for the CPU to generate sufficient bus traffic to 'starve' the other initiators attempting to access Flash memory, preventing them from performing transfers in the required time limit. If this 'starvation' occurs, the Round Robin or CPU Lowest mode should be chosen.

Mode 1 is a Fixed Priority mode with the CPU having the lowest priority (refer to Table 4-1). This mode can reduce the latency of DMA transfers because the DMA engines have a higher priority than the CPU.

Mode 2 is a Round Robin or Rotating Priority mode. The initiator's priority for each target rotates with every access. This ensures, not that the initiator is starved, but the latency for accesses changes with every access; this makes the latency variable.

The Arbitration mode is selected by the BMXARB<1:0> bits (CFGCON<25:24>).

Note:	The CPU has two initiators: one for data and the other for instructions. In all Arbitration modes, the CPU data initiator has higher priority than the CPU instruction initiator.

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TABLE 4-1: FIXED MODES ORDER OF PRIORITY

Mode 1	Mode 0
CPU Lowest	**CPU Highest**
Highest Priority	
Flash Controller	Flash Controller
DMA	CPU
USB	USB
CPU	DMA
Lowest Priority	

Note: The Arbitration mode chosen only has an effect on system performance when a contention for a target occurs.

The Flash controller, when programming memory, always has the highest priority regardless of the priority mode setting.

Refer to **Section 48. "Memory Organization and Permissions"** (DS60001214) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32) for more information regarding Bus Matrix operation.

4.3 Flash Line Buffer

The Flash line buffer is a buffer that resides between the Bus Matrix and the Flash memory. When a Flash fetch is generated, an aligned double word (64 bits) is read. This is then placed in the Flash line buffer. If the next initiator requested address's data is contained in the Flash line buffer, it is read directly without requiring another Flash fetch; if it is not in the Flash line buffer, a Flash fetch is generated.

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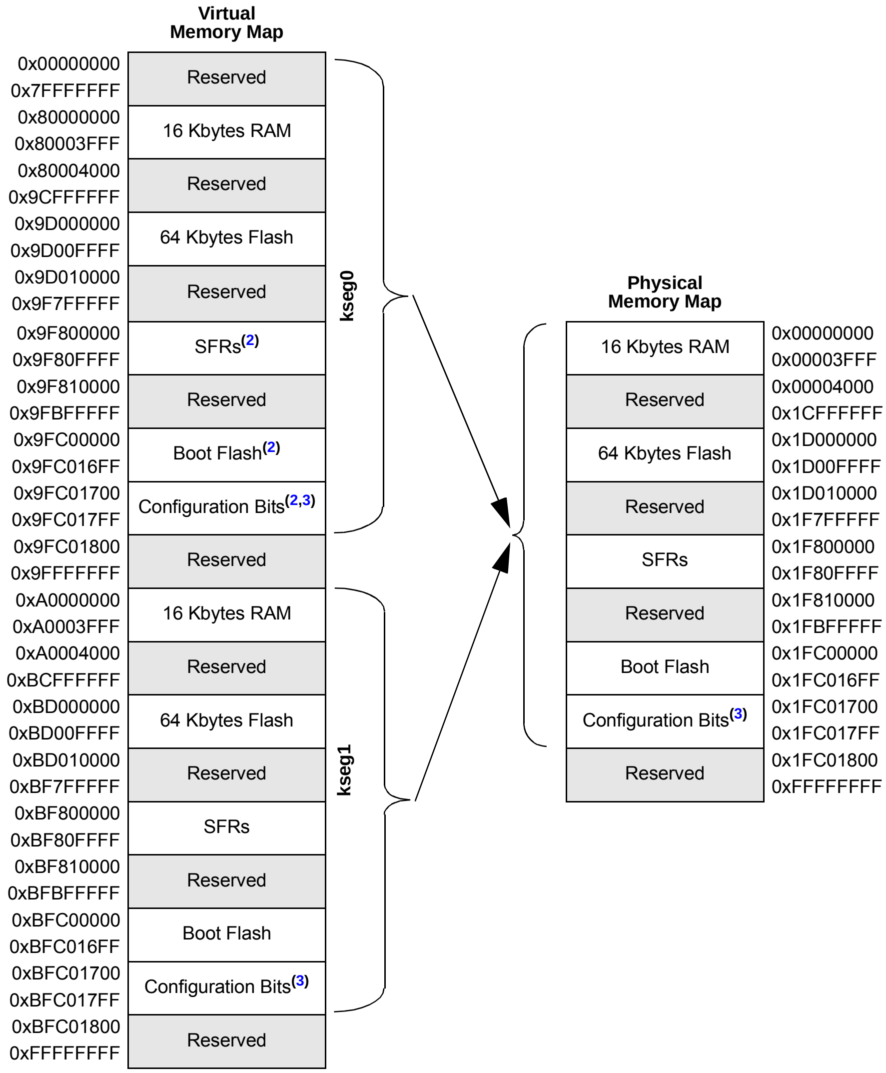
FIGURE 4-1: MEMORY MAP FOR DEVICES WITH 64 Kbytes OF PROGRAM MEMORY[1]



Note 1: Memory areas are not shown to scale.

2: This region should be accessed from kseg1 space only.

3: Primary Configuration bits' area is located at the address range, from 0x1FC01780 to 0x1FC017E8. Alternate Configuration bits' area is located at the address range, from 0x1FC01700 to 0x1FC01768. Refer to **Section 4.1 "Alternate Configuration Bits Space"** for more information.

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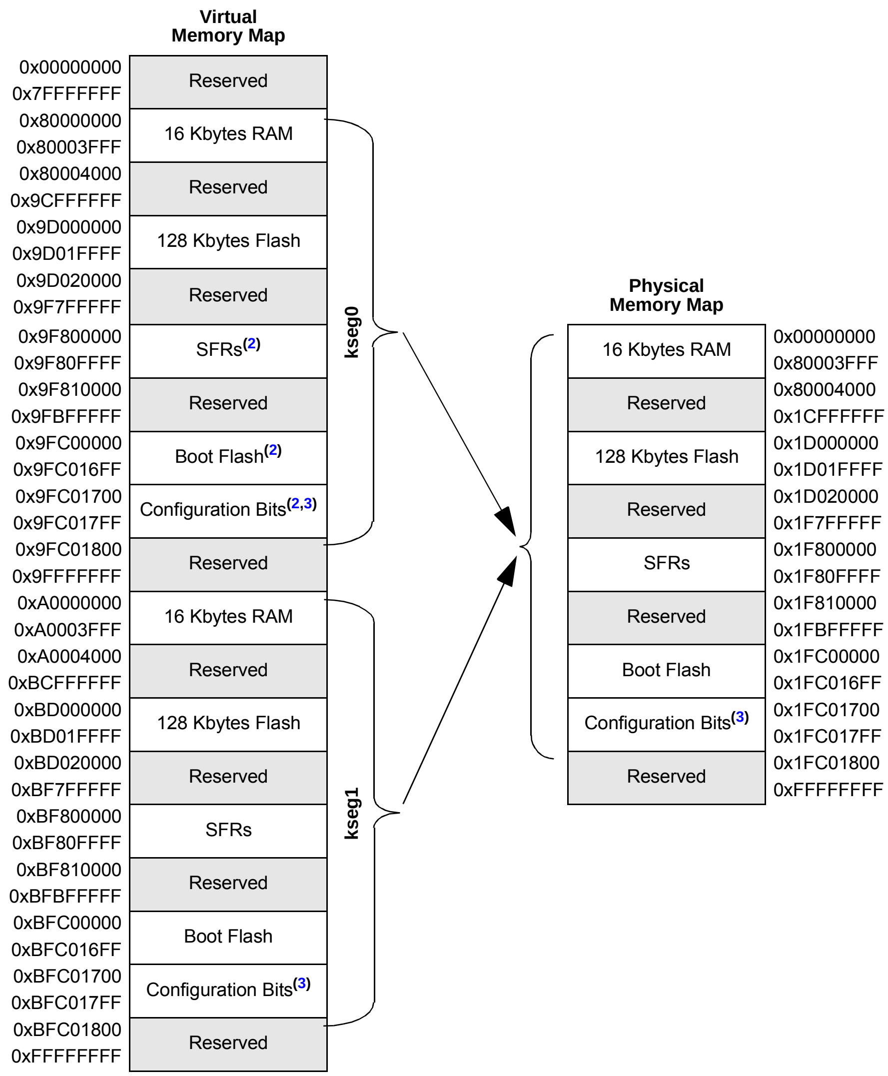
FIGURE 4-2: MEMORY MAP FOR DEVICES WITH 128 Kbytes OF PROGRAM MEMORY[1]



Note 1: Memory areas are not shown to scale.
2: This region should be accessed from kseg1 space only.
3: Primary Configuration bits' area is located at the address range, from 0x1FC01780 to 0x1FC017E8. Alternate Configuration bits' area is located at the address range, from 0x1FC01700 to 0x1FC01768. Refer to **Section 4.1 "Alternate Configuration Bits Space"** for more information.

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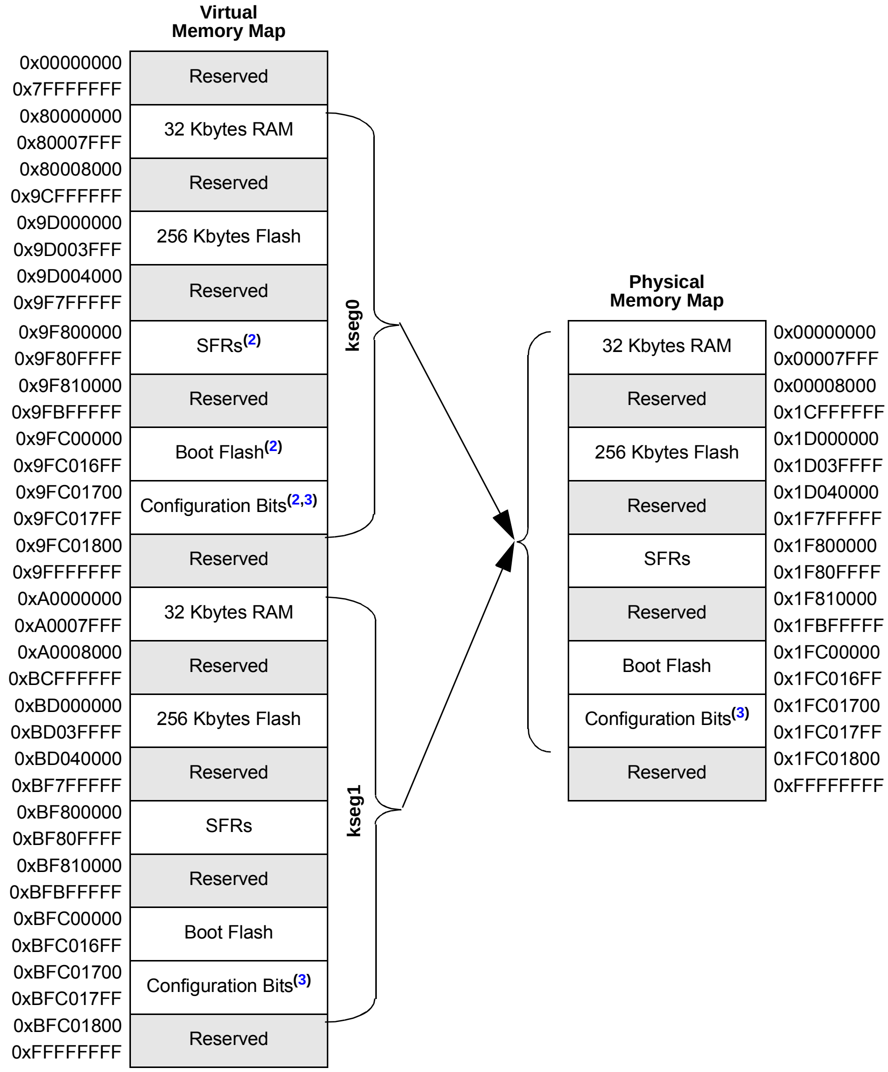
FIGURE 4-3: MEMORY MAP FOR DEVICES WITH 256 Kbytes OF PROGRAM MEMORY[1]



Note 1: Memory areas are not shown to scale.

2: This region should be accessed from kseg1 space only.

3: Primary Configuration bits' area is located at the address range, from 0x1FC01780 to 0x1FC017E8. Alternate Configuration bits' area is located at the address range, from 0x1FC01700 to 0x1FC01768. Refer to **Section 4.1 "Alternate Configuration Bits Space"** for more information.

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NOTES:

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5.0 FLASH PROGRAM MEMORY

Note:	This data sheet summarizes the features of the PIC32MM0256GPM064 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 5. "Flash Programming"** (DS60001121) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32). The information in this data sheet supersedes the information in the FRM.

PIC32MM0256GPM064 family devices contain an internal Flash program memory for executing user code. The program and Boot Flash can be write-protected. The erase page size is 512 32-bit words. The program row size is 64 32-bit words. The memory can be programmed by rows or by two 32-bit words, called double-words.

Note:	Double-words must be 64-bit aligned.

The devices implement a 6-bit Error Correcting Code (ECC). The memory control block contains a logic to write and read ECC bits to and from the Flash memory. The Flash is programmed at the same time as the corresponding ECC bits. The ECC provides improved resistance to Flash errors. The ECC single-bit error generates an interrupt and can be transparently corrected. The ECC double-bit error results in a bus error exception.

There are three methods by which the user can program this memory:

- Run-Time Self-Programming (RTSP)
- EJTAG Programming
- In-Circuit Serial Programming™ (ICSP™)

RTSP is performed by software executing from either Flash or RAM memory. Information about RTSP techniques is described in **Section 5. "Flash Programming"** (DS60001121) in the *"PIC32 Family Reference Manual"*. EJTAG programming is performed using the JTAG port of the device. ICSP programming requires fewer connections than for EJTAG programming. The EJTAG and ICSP methods are described in the *"PIC32 Flash Programming Specification"* (DS60001145), which is available for download from the Microchip web site.

5.1 Flash Controller Registers Write Protection

The NVMPWP and NVMBWP registers, and the WR bit in the NVMCON register are protected (locked) from an accidental write. Each time a special unlock sequence is required to modify the content of these registers or bits. To unlock, the following steps should be done:

1. Disable interrupts prior to the unlock sequence.
2. Execute the system unlock sequence by writing the key values of 0xAA996655 and 0x556699AA to the NVMKEY register.
3. Write the new value to the required bits.
4. Re-enable interrupts.
5. Relock the system.

Refer to Example 5-1.

EXAMPLE 5-1:

```
// unlock sequence
NVMKEY = AA996655;
NVMKEY = 556699AA;


// relock
NVMKEY = 0;
```


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5.2 Flash Control Registers

TABLE 5-1: FLASH CONTROLLER REGISTER MAP

Virtual Address (BF80_#)	Register Name	Bit Range	Bits 31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
2930	NVMCON[1]	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	WR	WREN	WRERR	LVDERR	r	—	—	—	—	—	—	—	NVMOP<3:0>				0000
2940	NVMKEY	31:16	NVMKEY<31:0>																0000
		15:0																	0000
2950	NVMADDR[1]	31:16	NVMADDR<31:0>																0000
		15:0																	0000
2960	NVMDATA0	31:16	NVMDATA0<31:0>																0000
		15:0																	0000
2970	NVMDATA1	31:16	NVMDATA1<31:0>																0000
		15:0																	0000
2980	NVMSRCADDR	31:16	NVMSRCADDR<31:0>																0000
		15:0																	0000
2990	NVMPWP[1]	31:16	PWPULOCK	—	—	—	—	—	—	—	PWP<23:16>								8000
		15:0	PWP<15:0>																0000
29A0	NVMBWP[1]	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	BWPULOCK	—	—	—	—	BWP2	BWP1	BWP0	—	—	—	—	—	—	—	—	8700

Legend: — = unimplemented, read as '0'; r = Reserved bit. Reset values are shown in hexadecimal.

Note 1: These registers have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively.

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REGISTER 5-1: NVMCON: PROGRAMMING CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0, HC	R/W-0	R-0, HS, HC	R-0, HS, HC	r-0	U-0	U-0	U-0
	WR[1,3]	WREN[1]	WRERR[1,2]	LVDERR[1,2]	—	—	—	—
7:0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	NVMOP<3:0>			

Legend:	HS = Hardware Settable bit	HC = Hardware Clearable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	r = Reserved bit

bit 31-16 **Unimplemented:** Read as ‘0’

bit 15 **WR:** Write Control bit[1,3]

This bit cannot be cleared and can be set only when WREN = 1, and the unlock sequence has been performed.
1 = Initiates a Flash operation
0 = Flash operation is complete or inactive

bit 14 **WREN:** Write Enable bit[1]

1 = Enables writes to the WR bit and disables writes to the NVMOP<3:0> bits
0 = Disables writes to the WR bit and enables writes to the NVMOP<3:0> bits

bit 13 **WRERR:** Write Error bit[1,2]

This bit can be cleared only by setting the NVMOP<3:0> bits = 0000 and initiating a Flash operation.
1 = Program or erase sequence did not complete successfully
0 = Program or erase sequence completed normally

bit 12 **LVDERR:** Low-Voltage Detect Error bit[1,2]

This bit can be cleared only by setting the NVMOP<3:0> bits = 0000 and initiating a Flash operation.
1 = Low-voltage is detected (possible data corruption if WRERR is set)
0 = Voltage level is acceptable for programming

bit 11 **Reserved:** Maintain as ‘0’

bit 10-4 **Unimplemented:** Read as ‘0’

Note 1: These bits are only reset by a Power-on Reset (POR) and are not affected by other Reset sources.
2: These bits are cleared by setting NVMOP<3:0> = 0000 and initiating a Flash operation (i.e., WR).
3: This bit is only writable when the NVMKEY unlock sequence is followed. Refer to Example 5-1.

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REGISTER 5-1: NVMCON: PROGRAMMING CONTROL REGISTER (CONTINUED)

bit 3-0 **NVMOP<3:0>:** NVM Operation bits
These bits are only writable when WREN = `0`.
`1111` = Reserved
•
•
•
`1000` = Reserved
`0111` = Program Erase Operation: Erases all of Program Flash Memory (all pages must be unprotected, PWP<23:0> = 0x000000, Boot Flash Memory is not erased)
`0110` = Reserved
`0101` = Reserved
`0100` = Page Erase Operation: Erases page selected by NVMADDR if it is not write-protected
`0011` = Row Program Operation: Programs row selected by NVMADDR if it is not write-protected
`0010` = Double-Word Program Operation: Programs two words to address selected by NVMADDR if it is not write-protected
`0001` = Reserved
`0000` = No operation (clears the WRERR and LVDERR status bits when executed)

Note 1: These bits are only reset by a Power-on Reset (POR) and are not affected by other Reset sources.
2: These bits are cleared by setting NVMOP<3:0> = `0000` and initiating a Flash operation (i.e., WR).
3: This bit is only writable when the NVMKEY unlock sequence is followed. Refer to Example 5-1.

REGISTER 5-2: NVMKEY: PROGRAMMING UNLOCK REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0
	NVMKEY<31:24>							
23:16	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0
	NVMKEY<23:16>							
15:8	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0
	NVMKEY<15:8>							
7:0	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0
	NVMKEY<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **NVMKEY<31:0>:** Programming Unlock Register bits
These bits are write-only and read as '`0`' on any read.

Note: This register is used as part of the unlock sequence to prevent inadvertent writes to the PFM. Refer to Example 5-1.

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REGISTER 5-3: NVMADDR: FLASH ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NVMADDR<31:24>(1)							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NVMADDR<23:16>(1)							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NVMADDR<15:8>(1)							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NVMADDR<7:0>(1)							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **NVMADDR<31:0>:** Flash Address bits[1]

NVMOP<3:0> Selection	Flash Address Bits (NVMADDR<31:0>)
Page Erase	Address identifies the page to erase (NVMADDR<10:0> are ignored).
Row Program	Address identifies the row to program (NVMADDR<7:0> are ignored).
Double-Word Program	Address identifies the double-word (64-bit) to program (NVMADDR<2:0> bits are ignored). **Note:** Must be 64-bit aligned.

Note 1: For all other NVMOP<3:0> bits settings, the Flash address is ignored. See the NVMCON register (Register 5-1) for additional information on these bits.

Note:	The bits in this register are only reset by a Power-on Reset (POR) and are not affected by other Reset sources.

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REGISTER 5-4: NVMDATAx: FLASH DATA x REGISTER (x = 0-1)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NVMDATAx<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NVMDATAx<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NVMDATAx<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NVMDATAx<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-0 **NVMDATAx<31:0>:** Flash Data x bits
Double-Word Program: Writes NVMDATA1:NVMDATA0 to the target Flash address defined in NVMADDR. NVMDATA0 contains the least significant instruction word.

Note: The bits in this register are only reset by a Power-on Reset (POR) and are not affected by other Reset sources.

REGISTER 5-5: NVMSRCADDR: SOURCE DATA ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NVMSRCADDR<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NVMSRCADDR<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NVMSRCADDR<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NVMSRCADDR<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-0 **NVMSRCADDR<31:0>:** Source Data Address bits
The system physical address of the data to be programmed into the Flash when the NVMOP<3:0> bits (NVMCON<3:0>) are set to perform row programming.

Note: The bits in this register are only reset by a Power-on Reset (POR) and are not affected by other Reset sources.

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REGISTER 5-6: NVMPWP: PROGRAM FLASH WRITE-PROTECT REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-1	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	PWPULOCK	—	—	—	—	—	—	—
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PWP<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PWP<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PWP<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31 **PWPULOCK:** Program Flash Memory Page Write-Protect Unlock bit
1 = Register is not locked and can be modified
0 = Register is locked and cannot be modified
This bit is only clearable and cannot be set except by any Reset.

bit 30-24 **Unimplemented:** Read as ‘0’

bit 23-0 **PWP<23:0>:** Flash Program Write-Protect (Page) Address bits
Physical memory below address, 0x1DXXXXXX, is write-protected, where ‘XXXXXX’ is specified by PWP<23:0>. When the PWP<23:0> bits have a value of ‘0’, write protection is disabled for the entire Program Flash Memory. If the specified address falls within the page, the entire page and all pages below the current page will be protected.

Note: The bits in this register are only writable when the NVMKEY unlock sequence is followed. Refer to Example 5-1.

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REGISTER 5-7: NVMBWP: BOOT FLASH (PAGE) WRITE-PROTECT REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-1	U-0	U-0	U-0	U-0	R/W-1	R/W-1	R/W-1
	BWPULOCK	—	—	—	—	BWP2(1)	BWP1(1)	BWP0(1)
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **BWPULOCK:** Boot Alias Write-Protect Unlock bit
1 = BWPx bits are not locked and can be modified
0 = BWPx bits are locked and cannot be modified
This bit is only clearable and cannot be set except by any Reset.

bit 14-11 **Unimplemented:** Read as '0'

bit 10 **BWP2:** Boot Alias Page 2 Write-Protect bit(1)
1 = Write protection for physical address, 0x01FC08000 through 0x1FC0BFFF, is enabled
0 = Write protection for physical address, 0x01FC08000 through 0x1FC0BFFF, is disabled

bit 9 **BWP1:** Boot Alias Page 1 Write-Protect bit(1)
1 = Write protection for physical address, 0x01FC04000 through 0x1FC07FFF, is enabled
0 = Write protection for physical address, 0x01FC04000 through 0x1FC07FFF, is disabled

bit 8 **BWP0:** Boot Alias Page 0 Write-Protect bit(1)
1 = Write protection for physical address, 0x01FC00000 through 0x1FC03FFF, is enabled
0 = Write protection for physical address, 0x01FC00000 through 0x1FC03FFF, is disabled

bit 7-0 **Unimplemented:** Read as '0'

Note 1: These bits are only available when the NVMKEY unlock sequence is performed and the associated Lock bit (BWPULOCK) is set.

Note: The bits in this register are only writable when the NVMKEY unlock sequence is followed. Refer to Example 5-1.

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6.0 RESETS

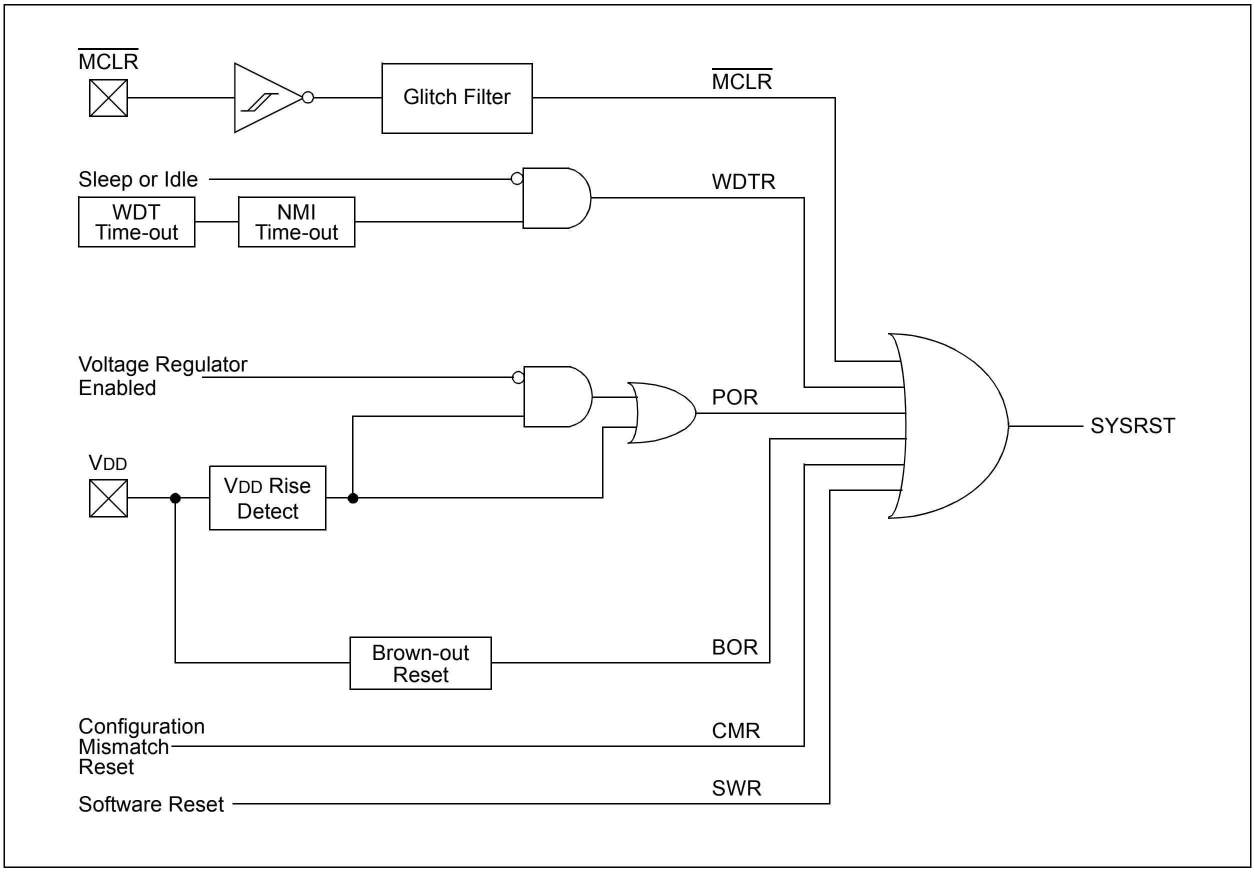
Note: This data sheet summarizes the features of the PIC32MM0256GPM064 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 7. "Resets"** (DS60001118) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32). The information in this data sheet supersedes the information in the FRM.

The Reset module combines all Reset sources and controls the device Master Reset Signal, SYSRST. The device Reset sources are as follows:

- Power-on Reset (POR)
- Master Clear Reset Pin (MCLR)
- Software Reset (SWR)
- Watchdog Timer Reset (WDTR)
- Brown-out Reset (BOR)
- Configuration Mismatch Reset (CMR)

A simplified block diagram of the Reset module is illustrated in Figure 6-1.

FIGURE 6-1: SYSTEM RESET BLOCK DIAGRAM



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6.1 Reset Control Registers

TABLE 6-1: RESETS REGISTER MAP

Virtual Address (BF80_#)	Register Name(1)	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
26E0	RCON	31:16	PORIO	PORCORE	—	—	BCFGERR	BCFGFAIL	—	—	—	—	—	—	—	—	—	—	C000
		15:0	—	—	—	—	—	—	CMR	—	EXTR	SWR	—	WDTO	SLEEP	IDLE	BOR	POR	0003
26F0	RSWRST	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SWRST	0000
2700	RNMICON	31:16	—	—	—	—	—	—	—	WDTR	SWNMI	—	—	—	GNMI	—	CF	WDTS	0000
		15:0	NMICNT<15:0>																0000
2710	PWRCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	SBOREN	RETEN	VREGS	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively.

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REGISTER 6-1: RCON: RESET CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-1, HS	R/W-1, HS	U-0	U-0	R/W-0, HS	R/W-0, HS	U-0	U-0
	PORIO	PORCORE	—	—	BCFGERR	BCFGFAIL	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0, HS	U-0
	—	—	—	—	—	—	CMR	—
7:0	R/W-0, HS	R/W-0, HS	U-0	R/W-0, HS	R/W-0, HS	R/W-0, HS	R/W-1, HS	R/W-1, HS
	EXTR[(1)]	SWR[(1)]	—	WDTO[(1)]	SLEEP[(1)]	IDLE[(1,2)]	BOR[(1)]	POR[(1)]

Legend:	HS = Hardware Settable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **PORIO:** VDD POR Flag bit
Set by hardware at detection of a VDD POR event.
1 = A Power-on Reset has occurred due to VDD voltage
0 = A Power-on Reset has not occurred due to VDD voltage

bit 30 **PORCORE:** Core Voltage POR Flag bit
Set by hardware at detection of a core POR event.
1 = A Power-on Reset has occurred due to core voltage
0 = A Power-on Reset has not occurred due to core voltage

bit 29-28 **Unimplemented:** Read as '0'

bit 27 **BCFGERR:** Primary Configuration Registers Error Flag bit
1 = An error occurred during a read of the Primary Configuration registers
0 = No error occurred during a read of the Primary Configuration registers

bit 26 **BCFGFAIL:** Primary/Alternate Configuration Registers Error Flag bit
1 = An error occurred during a read of the Primary and Alternate Configuration registers
0 = No error occurred during a read of the Primary and Alternate Configuration registers

bit 25-10 **Unimplemented:** Read as '0'

bit 9 **CMR:** Configuration Mismatch Reset Flag bit
1 = A Configuration Mismatch Reset has occurred
0 = A Configuration Mismatch Reset has not occurred

bit 8 **Unimplemented:** Read as '0'

bit 7 **EXTR:** External Reset ($\overline{\text{MCLR}}$) Pin Flag bit[(1)]
1 = Master Clear (pin) Reset has occurred
0 = Master Clear (pin) Reset has not occurred

bit 6 **SWR:** Software Reset Flag bit[(1)]
1 = Software Reset was executed
0 = Software Reset was not executed

bit 5 **Unimplemented:** Read as '0'

bit 4 **WDTO:** Watchdog Timer Time-out Flag bit[(1)]
1 = WDT time-out has occurred
0 = WDT time-out has not occurred

Note 1: User software must clear these bits to view the next detection.
2: The IDLE bit will also be set when the device wakes from Sleep.

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REGISTER 6-1: RCON: RESET CONTROL REGISTER (CONTINUED)

bit 3 **SLEEP:** Wake from Sleep Flag bit[1]
1 = Device was in Sleep mode
0 = Device was not in Sleep mode

bit 2 **IDLE:** Wake from Idle Flag bit[1,2]
1 = Device was in Idle mode
0 = Device was not in Idle mode

bit 1 **BOR:** Brown-out Reset Flag bit[1]
1 = Brown-out Reset has occurred
0 = Brown-out Reset has not occurred

bit 0 **POR:** Power-on Reset Flag bit[1]
1 = Power-on Reset has occurred
0 = Power-on Reset has not occurred

Note 1: User software must clear these bits to view the next detection.
2: The IDLE bit will also be set when the device wakes from Sleep.

REGISTER 6-2: RSWRST: SOFTWARE RESET REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	W-0, HC
	—	—	—	—	—	—	—	SWRST[1,2]

Legend:	HC = Hardware Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-1 **Unimplemented:** Read as '0'

bit 0 **SWRST:** Software Reset Trigger bit[1,2]
1 = Enables Software Reset event
0 = No effect

Note 1: The system unlock sequence must be performed before the SWRST bit can be written. Refer to **Section 26.4 "System Registers Write Protection"** for details.
2: Once this bit is set, any read of the RSWRST register will cause a Reset to occur.

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REGISTER 6-3: RNMICON: NON-MASKABLE INTERRUPT (NMI) CONTROL REGISTER[(2)]

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
	—	—	—	—	—	—	—	WDTR
23:16	R/W-0	U-0	U-0	U-0	R/W-0	U-0	R/W-0	R/W-0
	SWNMI	—	—	—	GNMI	—	CF	WDTS
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NMICNT<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NMICNT<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-25 **Unimplemented:** Read as ‘0’

bit 24 **WDTR:** Watchdog Timer Time-out Flag bit
1 = A Run mode WDT time-out has occurred and caused an NMI
0 = WDT time-out has not occurred
Setting this bit will cause a WDT NMI event and NMICNT will begin counting.

bit 23 **SWNMI:** Software NMI Trigger bit
1 = An NMI has been generated
0 = An NMI has not been generated

bit 22-20 **Unimplemented:** Read as ‘0’

bit 19 **GNMI:** Software General NMI Trigger bit
1 = A general NMI has been generated
0 = A general NMI has not been generated

bit 18 **Unimplemented:** Read as ‘0’

bit 17 **CF:** Clock Fail Detect bit
1 = FSCM has detected clock failure and caused an NMI
0 = FSCM has not detected clock failure
Setting this bit will cause a CF NMI event, but will not cause a clock switch to the FRC.

bit 16 **WDTS:** Watchdog Timer Time-out in Sleep Mode Flag bit
1 = WDT time-out has occurred during Sleep mode and caused a wake-up from Sleep
0 = WDT time-out has not occurred during Sleep mode
Setting this bit will cause a WDT NMI.

bit 15-0 **NMICNT<15:0>:** NMI Reset Counter Value bits
These bits specify the reload value used by the NMI Reset counter.
0xFFFF-0x0001 = Number of SYSCLK cycles before a device Reset occurs[(1)]
0x0000 = No delay between NMI assertion and device Reset event

Note 1: If a Watchdog Timer NMI event (when not in Sleep or Idle mode) is cleared before this counter reaches ‘0’, no device Reset is asserted. This NMI Reset counter is only applicable to the Watchdog Timer NMI event.

2: The system unlock sequence must be performed before the RNMICON register can be written. Refer to **Section 26.4 “System Registers Write Protection”** for details.

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REGISTER 6-4: PWRCON: POWER CONTROL REGISTER[2]

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	—	SBOREN	RETEN[1]	VREGS

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-3 **Unimplemented:** Read as ‘0’

bit 2 **SBOREN:** BOR Enable bit
Enables the BOR for select BOREN Configuration bit settings.
1 = Writing a ‘1’ to this bit enables the BOR for select BOREN configuration values
0 = Writing a ‘0’ to this bit enables the BOR for select BOREN configuration values

bit 1 **RETEN:** Output Level of the Regulator During Sleep Selection bit[1]
1 = Writing a ‘1’ to this bit will cause the main regulator to be put in a low-power state during Sleep mode[3]
0 = Writing a ‘0’ to this bit will have no effect

bit 0 **VREGS:** Voltage Regulator Standby Enable bit
1 = Voltage regulator will remain active during Sleep mode
0 = Voltage regulator will go into Standby mode during Sleep mode

Note 1: Refer to **Section 25.0 “Power-Saving Features”** for details.
2: The SYSKEY register is used to unlock this register.
3: The RETEN bit in the device configuration must also be set to enable this mode.

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7.0 CPU EXCEPTIONS AND INTERRUPT CONTROLLER

Note:	This data sheet summarizes the features of the PIC32MM0256GPM064 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 8. "Interrupts"** (DS61108) and **Section 50. "CPU for Devices with MIPS32® microAptiv™ and M-Class Cores"** (DS60001192) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32). The information in this data sheet supersedes the information in the FRM.

PIC32MM0256GPM064 family devices generate interrupt requests in response to interrupt events from peripheral modules. The interrupt control module exists externally to the CPU logic and prioritizes the interrupt events before presenting them to the CPU.

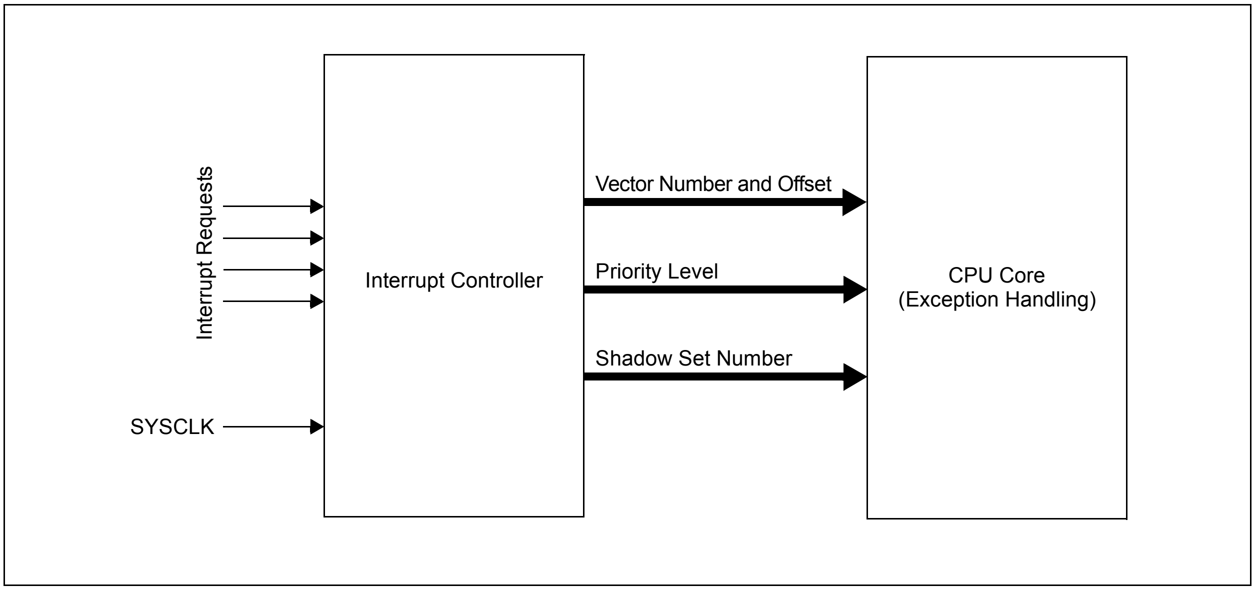
The CPU handles interrupt events as part of the exception handling mechanism, which is described in **Section 7.1 "CPU Exceptions"**.

The PIC32MM0256GPM064 family device interrupt module includes the following features:

- Single Vector or Multivector Mode Operation
- Five External Interrupts with Edge Polarity Control
- Interrupt Proximity Timer
- Module Freeze in Debug mode
- Seven User-Selectable Priority Levels for Each Vector
- Four User-Selectable Subpriority Levels within Each Priority
- One Shadow Register Set that can be Used for Any Priority Level, Eliminating Software Context Switch and Reducing Interrupt Latency
- Software can Generate any Interrupt
- User-Configurable Interrupt Vectors' Offset and Vector Table Location

Figure 7-1 shows the block diagram for the interrupt controller and CPU exceptions.

FIGURE 7-1: CPU EXCEPTIONS AND INTERRUPT CONTROLLER MODULE BLOCK DIAGRAM



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7.1 CPU Exceptions

CPU Coprocessor 0 contains the logic for identifying and managing exceptions. Exceptions can be caused by a variety of sources, including boundary cases in data, external events or program errors. Table 7-1 lists the exception types in order of priority.

TABLE 7-1: MIPS32® microAptiv™ UC MICROPROCESSOR CORE EXCEPTION TYPES

Exception Type (In Order of Priority)	Description	Branches to	Status Bits Set	Debug Bits Set	EXCCODE	XC32 Function Name
Highest Priority						
Reset	Assertion of $\overline{MCLR}$.	0xBFC0_0000	BEV, ERL	—	—	`_on_reset`
Soft Reset	Execution of a RESET instruction.	0xBFC0_0000	BEV, SR, ERL	—	—	`_on_reset`
DSS	EJTAG debug single step.	0xBFC0_0480 (ProbEn = 0 in ECR) 0xBFC0_0200 (ProbEn = 1 in ECR)	—	DSS	—	—
DINT	EJTAG debug interrupt. Caused by setting the EjtagBrk bit in the ECR register.	0xBFC0_0480 (ProbEn = 0 in ECR) 0xBFC0_0200 (ProbEn = 1 in ECR)	—	DINT	—	—
NMI	Non-Maskable Interrupt.	0xBFC0_0000	BEV, NMI, ERL	—	—	`_nmi_handler`
Interrupt	Assertion of unmasked hardware or software interrupt signal.	See Table 7-2	IPL<2:0>	—	Int (0x00)	See Table 7-2
DIB	EJTAG debug hardware instruction break matched.	0xBFC0_0480 (ProbEn = 0 in ECR) 0xBFC0_0200 (ProbEn = 1 in ECR)	—	DIB	—	—
AdEL	Load address alignment error.	EBASE + 0x180	EXL	—	ADEL (0x04)	`_general_exception_handler`
IBE	Instruction fetch bus error.	EBASE + 0x180	EXL	—	IBE (0x06)	`_general_exception_handler`
DBp	EJTAG breakpoint (execution of SDBBP instruction).	0xBFC0_0480 (ProbEn = 0 in ECR) 0xBFC0_0200 (ProbEn = 1 in ECR)	DBp	—	—	—
Sys	Execution of SYSCALL instruction.	EBASE + 0x180	EXL	—	Sys (0x08)	`_general_exception_handler`
Bp	Execution of BREAK instruction.	EBASE + 0x180	EXL	—	Bp (0x09)	`_general_exception_handler`

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TABLE 7-1: MIPS32® microAptiv™ UC MICROPROCESSOR CORE EXCEPTION TYPES (CONTINUED)

Exception Type (In Order of Priority)	Description	Branches to	Status Bits Set	Debug Bits Set	EXCCODE	XC32 Function Name
CpU	Execution of a coprocessor instruction for a coprocessor that is not enabled.	EBASE + 0x180	CU, EXL	—	CpU (0x0B)	`_general_exception_handler`
RI	Execution of a reserved instruction.	EBASE + 0x180	EXL	—	RI (0x0A)	`_general_exception_handler`
Ov	Execution of an arithmetic instruction that overflowed.	EBASE + 0x180	EXL	—	Ov (0x0C)	`_general_exception_handler`
Tr	Execution of a trap (when trap condition is true).	EBASE + 0x180	EXL	—	Tr (0x0D)	`_general_exception_handler`
DDBL	EJTAG data address break (address only) or EJTAG data value break on load (address and value).	0xBFC0_0480 (ProbEn = 0 in ECR) 0xBFC0_0200 (ProbEn = 1 in ECR)	—	DDBL for a load instruction or DDBS for a store instruction	—	—
DDBS	EJTAG data address break (address only) or EJTAG data value break on store (address and value).	0xBFC0_0480 (ProbEn = 0 in ECR) 0xBFC0_0200 (ProbEn = 1 in ECR)	—	DDBL for a load instruction or DDBS for a store instruction	—	—
AdES	Store address alignment error.	EBASE + 0x180	EXL	—	ADES (0x05)	`_general_exception_handler`
DBE	Load or store bus error.	EBASE + 0x180	EXL	—	DBE (0x07)	`_general_exception_handler`
CBrk	EJTAG complex breakpoint.	0xBFC0_0480 (ProbEn = 0 in ECR) 0xBFC0_0200 (ProbEn = 1 in ECR)	—	DIBImpr, DDBLImpr and/or DDBSImpr	—	—
Lowest Priority						

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7.2 Interrupts

The PIC32MM0256GPM064 family uses fixed offset for vector spacing. For details, refer to **Section 8. "Interrupts"** (DS61108) in the *"PIC32 Family Reference Manual"*. Table 7-2 provides the interrupt related vectors and bits information.

TABLE 7-2: INTERRUPTS

Interrupt Source	MPLAB® XC32 Vector Name	Vector Number	Interrupt Related Bits Location				Persistent Interrupt
			Flag	Enable	Priority	Subpriority	
Core Timer	_CORE_TIMER_VECTOR	0	IFS0<0>	IEC0<0>	IPC0<4:2>	IPC0<1:0>	No
Core Software 0	_CORE_SOFTWARE_0_VECTOR	1	IFS0<1>	IEC0<1>	IPC0<12:10>	IPC0<9:8>	No
Core Software 1	_CORE_SOFTWARE_1_VECTOR	2	IFS0<2>	IEC0<2>	IPC0<20:18>	IPC0<17:16>	No
External 0	_EXTERNAL_0_VECTOR	3	IFS0<3>	IEC0<3>	IPC0<28:26>	IPC0<25:24>	No
External 1	_EXTERNAL_1_VECTOR	4	IFS0<4>	IEC0<4>	IPC1<4:2>	IPC1<1:0>	No
External 2	_EXTERNAL_2_VECTOR	5	IFS0<5>	IEC0<5>	IPC1<12:10>	IPC1<9:8>	No
External 3	_EXTERNAL_3_VECTOR	6	IFS0<6>	IEC0<6>	IPC1<20:18>	IPC1<17:16>	No
External 4	_EXTERNAL_4_VECTOR	7	IFS0<7>	IEC0<7>	IPC1<28:26>	IPC1<25:24>	No
PORTA Change Notification	_CHANGE_NOTICE_A_VECTOR	8	IFS0<8>	IEC0<8>	IPC2<4:2>	IPC2<1:0>	No
PORTB Change Notification	_CHANGE_NOTICE_B_VECTOR	9	IFS0<9>	IEC0<9>	IPC2<12:10>	IPC2<9:8>	No
PORTC Change Notification	_CHANGE_NOTICE_C_VECTOR	10	IFS0<10>	IEC0<10>	IPC2<20:18>	IPC2<17:16>	No
PORTD Change Notification	_CHANGE_NOTICE_D_VECTOR	11	IFS0<11>	IEC0<11>	IPC2<28:26>	IPC2<25:24>	No
RESERVED		12	IFS0<12>	IEC0<12>	IPC3<4:2>	IPC3<1:0>	No
RESERVED		13	IFS0<13>	IEC0<13>	IPC3<12:10>	IPC3<9:8>	No
RESERVED		14	IFS0<14>	IEC0<14>	IPC3<20:18>	IPC3<17:16>	No
RESERVED		15	IFS0<15>	IEC0<15>	IPC3<28:26>	IPC3<25:24>	No
RESERVED		16	IFS0<16>	IEC0<16>	IPC4<4:2>	IPC4<1:0>	No
Timer1	_TIMER_1_VECTOR	17	IFS0<17>	IEC0<17>	IPC4<12:10>	IPC4<9:8>	No
Timer2	_TIMER_2_VECTOR	18	IFS0<18>	IEC0<18>	IPC4<20:18>	IPC4<17:16>	No
Timer3	_TIMER_3_VECTOR	19	IFS0<19>	IEC0<19>	IPC4<28:26>	IPC4<25:24>	No
RESERVED		20	IFS0<20>	IEC0<20>	IPC5<4:2>	IPC5<1:0>	No
RESERVED		21	IFS0<21>	IEC0<21>	IPC5<12:10>	IPC5<9:8>	No
RESERVED		22	IFS0<22>	IEC0<22>	IPC5<20:18>	IPC5<17:16>	No
Comparator 1	_COMPARATOR_1_VECTOR	23	IFS0<23>	IEC0<23>	IPC5<28:26>	IPC5<25:24>	No
Comparator 2	_COMPARATOR_2_VECTOR	24	IFS0<24>	IEC0<24>	IPC6<4:2>	IPC6<1:0>	No
Comparator 3	_COMPARATOR_3_VECTOR	25	IFS0<25>	IEC0<25>	IPC6<12:10>	IPC6<9:8>	No

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TABLE 7-2: INTERRUPTS (CONTINUED)

Interrupt Source	MPLAB® XC32 Vector Name	Vector Number	Interrupt Related Bits Location				Persistent Interrupt
			Flag	Enable	Priority	Subpriority	
RESERVED		26	IFS0<26>	IEC0<26>	IPC6<20:18>	IPC6<17:16>	No
RESERVED		27	IFS0<27>	IEC0<27>	IPC6<28:26>	IPC6<25:24>	No
RESERVED		28	IFS0<28>	IEC0<28>	IPC7<4:2>	IPC7<1:0>	No
USB	_USB_VECTOR	29	IFS0<29>	IEC0<29>	IPC7<12:10>	IPC7<9:8>	No
RESERVED		30	IFS0<30>	IEC0<30>	IPC7<20:18>	IPC7<17:16>	No
RESERVED		31	IFS0<31>	IEC0<31>	IPC7<28:26>	IPC7<25:24>	No
Real-Time Clock Alarm	_RTCC_VECTOR	32	IFS1<0>	IEC1<0>	IPC8<4:2>	IPC8<1:0>	No
ADC Conversion	_ADC_VECTOR	33	IFS1<1>	IEC1<1>	IPC8<12:10>	IPC8<9:8>	No
RESERVED		34	IFS1<2>	IEC1<2>	IPC8<20:18>	IPC8<17:16>	No
RESERVED		35	IFS1<3>	IEC1<3>	IPC8<28:26>	IPC8<25:24>	No
High/Low-Voltage Detect	_HLVD_VECTOR	36	IFS1<4>	IEC1<4>	IPC9<4:2>	IPC9<1:0>	Yes
Logic Cell 1	_CLC1_VECTOR	37	IFS1<5>	IEC1<5>	IPC9<12:10>	IPC9<9:8>	No
Logic Cell 2	_CLC2_VECTOR	38	IFS1<6>	IEC1<6>	IPC9<20:18>	IPC9<17:16>	No
Logic Cell 3	_CLC3_VECTOR	39	IFS1<7>	IEC1<7>	IPC9<28:26>	IPC9<25:24>	No
Logic Cell 4	_CLC4_VECTOR	40	IFS1<8>	IEC1<8>	IPC10<4:2>	IPC10<1:0>	No
SPI1 Error	_SPI1_ERR_VECTOR	41	IFS1<9>	IEC1<9>	IPC10<12:10>	IPC10<9:8>	Yes
SPI1 Transmission	_SPI1_TX_VECTOR	42	IFS1<10>	IEC1<10>	IPC10<20:18>	IPC10<17:16>	Yes
SPI1 Reception	_SPI1_RX_VECTOR	43	IFS1<11>	IEC1<11>	IPC10<28:26>	IPC10<25:24>	Yes
SPI2 Error	_SPI2_ERR_VECTOR	44	IFS1<12>	IEC1<12>	IPC11<4:2>	IPC11<1:0>	Yes
SPI2 Transmission	_SPI2_TX_VECTOR	45	IFS1<13>	IEC1<13>	IPC11<12:10>	IPC11<9:8>	Yes
SPI2 Reception	_SPI2_RX_VECTOR	46	IFS1<14>	IEC1<14>	IPC11<20:18>	IPC11<17:16>	Yes
SPI3 Error	_SPI3_ERR_VECTOR	47	IFS1<15>	IEC1<15>	IPC11<28:26>	IPC11<25:24>	Yes
SPI3 Transmission	_SPI3_TX_VECTOR	48	IFS1<16>	IEC1<16>	IPC12<4:2>	IPC12<1:0>	Yes
SPI3 Reception	_SPI3_RX_VECTOR	49	IFS1<17>	IEC1<17>	IPC12<12:10>	IPC12<9:8>	Yes
RESERVED		50	IFS1<18>	IEC1<18>	IPC12<20:18>	IPC12<17:16>	No
RESERVED		51	IFS1<19>	IEC1<19>	IPC12<28:26>	IPC12<25:24>	No
RESERVED		52	IFS1<20>	IEC1<20>	IPC13<4:2>	IPC13<1:0>	No
UART1 Reception	_UART1_RX_VECTOR	53	IFS1<21>	IEC1<21>	IPC13<12:10>	IPC13<9:8>	Yes
UART1 Transmission	_UART1_TX_VECTOR	54	IFS1<22>	IEC1<22>	IPC13<20:18>	IPC13<17:16>	Yes
UART1 Error	_UART1_ERR_VECTOR	55	IFS1<23>	IEC1<23>	IPC13<28:26>	IPC13<25:24>	Yes

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TABLE 7-2: INTERRUPTS (CONTINUED)

Interrupt Source	MPLAB® XC32 Vector Name	Vector Number	Interrupt Related Bits Location				Persistent Interrupt
			Flag	Enable	Priority	Subpriority	
UART2 Reception	_UART2_RX_VECTOR	56	IFS1<24>	IEC1<24>	IPC14<4:2>	IPC14<1:0>	Yes
UART2 Transmission	_UART2_TX_VECTOR	57	IFS1<25>	IEC1<25>	IPC14<12:10>	IPC14<9:8>	Yes
UART2 Error	_UART2_ERR_VECTOR	58	IFS1<26>	IEC1<26>	IPC14<20:18>	IPC14<17:16>	Yes
UART3 Reception	_UART3_RX_VECTOR	59	IFS1<27>	IEC1<27>	IPC14<28:26>	IPC14<25:24>	Yes
UART3 Transmission	_UART3_TX_VECTOR	60	IFS1<28>	IEC1<28>	IPC15<4:2>	IPC15<1:0>	Yes
UART3 Error	_UART3_ERR_VECTOR	61	IFS1<29>	IEC1<29>	IPC15<12:10>	IPC15<9:8>	Yes
RESERVED		62	IFS1<30>	IEC1<30>	IPC15<20:18>	IPC15<17:16>	No
RESERVED		63	IFS1<31>	IEC1<31>	IPC15<28:26>	IPC15<25:24>	No
RESERVED		64	IFS2<0>	IEC2<0>	IPC16<4:2>	IPC16<1:0>	No
I2C1 Slave	_I2C1_SLAVE_VECTOR	65	IFS2<1>	IEC2<1>	IPC16<12:10>	IPC16<9:8>	Yes
I2C1 Master	_I2C1_MASTER_VECTOR	66	IFS2<2>	IEC2<2>	IPC16<20:18>	IPC16<17:16>	Yes
I2C1 Bus Collision	_I2C1_BUS_VECTOR	67	IFS2<3>	IEC2<3>	IPC16<28:26>	IPC16<25:24>	Yes
I2C2 Slave	_I2C2_SLAVE_VECTOR	68	IFS2<4>	IEC2<4>	IPC17<4:2>	IPC17<1:0>	Yes
I2C2 Master	_I2C2_MASTER_VECTOR	69	IFS2<5>	IEC2<5>	IPC17<12:10>	IPC17<9:8>	Yes
I2C2 Bus Collision	_I2C2_BUS_VECTOR	70	IFS2<6>	IEC2<6>	IPC17<20:18>	IPC17<17:16>	Yes
I2C3 Slave	_I2C3_SLAVE_VECTOR	71	IFS2<7>	IEC2<7>	IPC17<28:26>	IPC17<25:24>	Yes
I2C3 Master	_I2C3_MASTER_VECTOR	72	IFS2<8>	IEC2<8>	IPC18<4:2>	IPC18<1:0>	Yes
I2C3 Bus Collision	_I2C3_BUS_VECTOR	73	IFS2<9>	IEC2<9>	IPC18<12:10>	IPC18<9:8>	Yes
CCP1 Input Capture or Output Compare	_CCP1_VECTOR	74	IFS2<10>	IEC2<10>	IPC18<20:18>	IPC18<17:16>	No
CCP1 Timer	_CCT1_VECTOR	75	IFS2<11>	IEC2<11>	IPC18<28:26>	IPC18<25:24>	No
CCP2 Input Capture or Output Compare	_CCP2_VECTOR	76	IFS2<12>	IEC2<12>	IPC19<4:2>	IPC19<1:0>	No
CCP2 Timer	_CCT2_VECTOR	77	IFS2<13>	IEC2<13>	IPC19<12:10>	IPC19<9:8>	No
CCP3 Input Capture or Output Compare	_CCP3_VECTOR	78	IFS2<14>	IEC2<14>	IPC19<20:18>	IPC19<17:16>	No
CCP3 Timer	_CCT3_VECTOR	79	IFS2<15>	IEC2<15>	IPC19<28:26>	IPC19<25:24>	No
CCP4 Input Capture or Output Compare	_CCP4_VECTOR	80	IFS2<16>	IEC2<16>	IPC20<4:2>	IPC20<1:0>	No
CCP4 Timer	_CCT4_VECTOR	81	IFS2<17>	IEC2<17>	IPC20<12:10>	IPC20<9:8>	No
CCP5 Input Capture or Output Compare	_CCP5_VECTOR	82	IFS2<18>	IEC2<18>	IPC20<20:18>	IPC20<17:16>	No
CCP5 Timer	_CCT5_VECTOR	83	IFS2<19>	IEC2<19>	IPC20<28:26>	IPC20<25:24>	No
CCP6 Input Capture or Output Compare	_CCP6_VECTOR	84	IFS2<20>	IEC2<20>	IPC21<4:2>	IPC21<1:0>	No
CCP6 Timer	_CCT6_VECTOR	85	IFS2<21>	IEC2<21>	IPC21<12:10>	IPC21<9:8>	No
CCP7 Input Capture or Output Compare	_CCP7_VECTOR	86	IFS2<22>	IEC2<22>	IPC21<20:18>	IPC21<17:16>	No
CCP7 Timer	_CCT7_VECTOR	87	IFS2<23>	IEC2<23>	IPC21<28:26>	IPC21<25:24>	No

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TABLE 7-2: INTERRUPTS (CONTINUED)

Interrupt Source	MPLAB® XC32 Vector Name	Vector Number	Interrupt Related Bits Location				Persistent Interrupt
			Flag	Enable	Priority	Subpriority	
CCP8 Input Capture or Output Compare	_CCP8_VECTOR	88	IFS2<24>	IEC2<24>	IPC22<4:2>	IPC22<1:0>	No
CCP8 Timer	_CCT8_VECTOR	89	IFS2<25>	IEC2<25>	IPC22<12:10>	IPC22<9:8>	No
CCP9 Input Capture or Output Compare	_CCP9_VECTOR	90	IFS2<26>	IEC2<26>	IPC22<20:18>	IPC22<17:16>	No
CCP9 Timer	_CCT9_VECTOR	91	IFS2<27>	IEC2<27>	IPC22<28:26>	IPC22<25:24>	No
FRC Auto-Tune	_FRC_TUNE	92	IFS2<28>	IEC2<28>	IPC23<4:2>	IPC23<1:0>	No
NVM Program or Erase Complete	_NVM_VECTOR	94	IFS2<30>	IEC2<30>	IPC23<20:18>	IPC23<17:16>	Yes
Core Performance Counter	_PERFORMANCE_COUNTER_VECTOR	95	IFS2<31>	IEC2<31>	IPC23<28:26>	IPC23<25:24>	No
RESERVED		96	IFS3<0>	IEC3<0>	IPC24<4:2>	IPC24<1:0>	No
Single-Bit ECC Error	_ECCSB_ERR_VECTOR	97	IFS3<1>	IEC3<1>	IPC24<12:10>	IPC24<9:8>	No
DMA Channel 0	_DMA0_VECTOR	98	IFS3<2>	IEC3<2>	IPC24<20:18>	IPC24<17:16>	No
DMA Channel 1	_DMA1_VECTOR	99	IFS3<3>	IEC3<3>	IPC24<28:26>	IPC24<25:24>	No
DMA Channel 2	_DMA2_VECTOR	100	IFS3<4>	IEC3<4>	IPC25<4:2>	IPC25<1:0>	No
DMA Channel 3	_DMA3_VECTOR	101	IFS3<5>	IEC3<5>	IPC25<12:10>	IPC25<9:8>	No

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TABLE 7-3: INTERRUPT REGISTER MAP

Virtual Address (BF80_#)	Register Name[(1)]	Bit Range	Bits 31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
F000	INTCON	31:16	—	—	—	—	—	—	—	—	—	VS<6:0>							0000
		15:0	—	—	—	MVEC	—	TPC<2:0>			—	—	—	INT4EP	INT3EP	INT2EP	INT1EP	INT0EP	0000
F010	PRISS	31:16	PRI7SS<3:0>				PRI6SS<3:0>				PRI5SS<3:0>				PRI4SS<3:0>				0000
		15:0	PRI3SS<3:0>				PRI2SS<3:0>				PRI1SS<3:0>				—	—	—	SS0	0000
F020	INTSTAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	SRIPL<2:0>			SIRQ<7:0>								0000
F030	IPTMR	31:16	IPTMR<31:0>																0000
		15:0																	0000
F040	IFS0	31:16	—	USBIF	—	—	—	—	CMP3IF	CMP2IF	CMP1IF	—	—	—	T3IF	T2IF	T1IF	—	0000
		15:0	—	—	—	—	CNDIF	CNCIF	CNBIF	CNAIF	INT4IF	INT3IF	INT2IF	INT1IF	INT0IF	CS1IF	CS0IF	CTIF	0000
F050	IFS1	31:16	—	—	U3EIF	U3TXIF	U3RXIF	U2EIF	U2TXIF	U2RXIF	U1EIF	U1TXIF	U1RXIF	—	—	—	SPI3RXIF	SPI3TXIF	0000
		15:0	SPI3EIF	SPI2RXIF	SPI2TXIF	SPI2EIF	SPI1RXIF	SPI1TXIF	SPI1EIF	CLC4IF	CLC3IF	CLC2IF	CLC1IF	LVDIF	—	—	AD1IF	RTCCIF	0000
F060	IFS2	31:16	CPCIF	NVMIF	—	FSTIF	CCT9IF	CCP9IF	CCT8IF	CCP8IF	CCT7IF	CCP7IF	CCT6IF	CCP6IF	CCT5IF	CCP5IF	CCT4IF	CCP4IF	0000
		15:0	CCT3IF	CCP3IF	CCT2IF	CCP2IF	CCT1IF	CCP1IF	I2C3BCIF	I2C3MIF	I2C3SIF	I2C2BCIF	I2C2MIF	I2C2SIF	I2C1BCIF	I2C1MIF	I2C1SIF	—	0000
F070	IFS3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	DMA3IF	DMA2IF	DMA1IF	DMA0IF	ECCBEIF	—	0000
F080	IEC0	31:16	—	USBIE	—	—	—	—	CMP3IE	CMP2IE	CMP1IE	—	—	—	T3IE	T2IE	T1IE	—	0000
		15:0	—	—	—	—	CNDIE	CNCIE	CNBIE	CNAIE	INT4IE	INT3IE	INT2IE	INT1IE	INT0IE	CS1IE	CS0IE	CTIE	0000
F090	IEC1	31:16	—	—	U3EIE	U3TXIE	U3RXIE	U2EIE	U2TXIE	U2RXIE	U1EIE	U1TXIE	U1RXIE	—	—	—	SPI3RXIE	SPI3TXIE	0000
		15:0	SPI3EIE	SPI2RXIE	SPI2TXIE	SPI2EIE	SPI1RXIE	SPI1TXIE	SPI1EIE	CLC4IE	CLC3IE	CLC2IE	CLC1IE	LVDIE	—	—	AD1IE	RTCCIE	0000
F0A0	IEC2	31:16	CPCIE	NVMIE	—	FSTIE	CCT9IE	CCP9IE	CCT8IE	CCP8IE	CCT7IE	CCP7IE	CCT6IE	CCP6IE	CCT5IE	CCP5IE	CCT4IE	CCP4IE	0000
		15:0	CCT3IE	CCP3IE	CCT2IE	CCP2IE	CCT1IE	CCP1IE	I2C3BCIE	I2C3MIE	I2C3SIE	I2C2BCIE	I2C2MIE	I2C2SIE	I2C1BCIE	I2C1MIE	I2C1SIE	—	0000
F0B0	IEC3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	DMA3IE	DMA2IE	DMA1IE	DMA0IE	ECCBEIE	—	0000
F0C0	IPC0	31:16	—	—	—	INT0IP<2:0>			INT0IS<1:0>		—	—	—	CS1IP<2:0>			CS1IS<1:0>		0000
		15:0	—	—	—	CS0IP<2:0>			CS0IS<1:0>		—	—	—	CTIP<2:0>			CTIS<1:0>		0000
F0D0	IPC1	31:16	—	—	—	INT4IP<2:0>			INT4IS<1:0>		—	—	—	INT3IP<2:0>			INT3IS<1:0>		0000
		15:0	—	—	—	INT2IP<2:0>			INT2IS<1:0>		—	—	—	INT1IP<2:0>			INT1IS<1:0>		0000
F0E0	IPC2	31:16	—	—	—	CNDIP<2:0>			CNDIS<1:0>		—	—	—	CNCIP<2:0>			CNCIS<1:0>		0000
		15:0	—	—	—	CNBIP<2:0>			CNBIS<1:0>		—	—	—	CNAIP<2:0>			CNAIS<1:0>		0000
F0F0	IPC3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively.

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TABLE 7-3: INTERRUPT REGISTER MAP (CONTINUED)

Virtual Address (BF80_#)	Register Name[1]	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
F100	IPC4	31:16	—	—	—	T3IP<2:0>			T3IS<1:0>		—	—	—	T2IP<2:0>			T2IS<1:0>		0000
		15:0	—	—	—	T1IP<2:0>			T1IS<1:0>		—	—	—	—	—	—	—	—	0000
F110	IPC5	31:16	—	—	—	CMP1IP<2:0>			CMP1IS<1:0>		—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
F120	IPC6	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	CMP3IP<2:0>			CMP3IS<1:0>		—	—	—	CMP2IP<2:0>			CMP2IS<1:0>		0000
F130	IPC7	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	USBIP<2:0>			USBIS<1:0>		—	—	—	—	—	—	—	—	0000
F140	IPC8	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	AD1IP<2:0>			AD1IS<1:0>		—	—	—	RTCCIP<2:0>			RTCCIS<1:0>		0000
F150	IPC9	31:16	—	—	—	CLC3IP<2:0>			CLC3IS<1:0>		—	—	—	CLC2IP<2:0>			CLC2IS<1:0>		0000
		15:0	—	—	—	CLC1IP<2:0>			CLC1IS<1:0>		—	—	—	LVDIP<2:0>			LVDIS<1:0>		0000
F160	IPC10	31:16	—	—	—	SPI1RXIP<2:0>			SPI1RXIS<1:0>		—	—	—	SPI1TXIP<2:0>			SPI1TXIS<1:0>		0000
		15:0	—	—	—	SPI1EIP<2:0>			SPI1EIS<1:0>		—	—	—	CLC4IP<2:0>			CLC4IS<1:0>		0000
F170	IPC11	31:16	—	—	—	SPI3EIP<2:0>			SPI3EIS<1:0>		—	—	—	SPI2RXIP<2:0>			SPI2RXIS<1:0>		0000
		15:0	—	—	—	SPI2TXIP<2:0>			SPI2TXIS<1:0>		—	—	—	SPI2EIP<2:0>			SPI2EIS<1:0>		0000
F180	IPC12	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	SPI3RXIP<2:0>			SPI3RXIS<1:0>		—	—	—	SPI3TXIP<2:0>			SPI3TXIS<1:0>		0000
F190	IPC13	31:16	—	—	—	U1EIP<2:0>			U1EIS<1:0>		—	—	—	U1TXIP<2:0>			U1TXIS<1:0>		0000
		15:0	—	—	—	U1RXIP<2:0>			U1RXIS<1:0>		—	—	—	—	—	—	—	—	0000
F1A0	IPC14	31:16	—	—	—	U3RXIP<2:0>			U3RXIS<1:0>		—	—	—	U2EIP<2:0>			U2EIS<1:0>		0000
		15:0	—	—	—	U2TXIP<2:0>			U2TXIS<1:0>		—	—	—	U2RXIP<2:0>			U2RXIS<1:0>		0000
F1B0	IPC15	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	U3EIP<2:0>			U3EIS<1:0>		—	—	—	U3TXIP<2:0>			U3TXIS<1:0>		0000
F1C0	IPC16	31:16	—	—	—	I2C1BCIP<2:0>			I2C1BCIS<1:0>		—	—	—	I2C1MIP<2:0>			I2C1MIS<1:0>		0000
		15:0	—	—	—	I2C1SIP<2:0>			I2C1SIS<1:0>		—	—	—	—	—	—	—	—	0000
F1D0	IPC17	31:16	—	—	—	I2C3SIP<2:0>			I2C3SIS<1:0>		—	—	—	I2C2BCIP<2:0>			I2C2BCIS<1:0>		0000
		15:0	—	—	—	I2C2MIP<2:0>			I2C2MIS<1:0>		—	—	—	I2C2SIP<2:0>			I2C2SIS<1:0>		0000
F1E0	IPC18	31:16	—	—	—	CCT1IP<2:0>			CCT1IS<1:0>		—	—	—	CCP1IP<2:0>			CCP1IS<1:0>		0000
		15:0	—	—	—	I2C3BCIP<2:0>			I2C3BCIS<1:0>		—	—	—	I2C3MIP<2:0>			I2C3MIS<1:0>		0000
F1F0	IPC19	31:16	—	—	—	CCT3IP<2:0>			CCT3IS<1:0>		—	—	—	CCP3IP<2:0>			CCP3IS<1:0>		0000
		15:0	—	—	—	CCT2IP<2:0>			CCT2IS<1:0>		—	—	—	CCP2IP<2:0>			CCP2IS<1:0>		0000

Legend: — = unimplemented, read as ‘0’. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively.

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TABLE 7-3: INTERRUPT REGISTER MAP (CONTINUED)

Virtual Address (BF80_#)	Register Name[1]	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
F200	IPC20	31:16	—	—	—	CCT5IP<2:0>			CCT5IS<1:0>		—	—	—	CCP5IP<2:0>			CCP5IS<1:0>		0000
		15:0	—	—	—	CCT4IP<2:0>			CCT4IS<1:0>		—	—	—	CCP4IP<2:0>			CCP4IS<1:0>		0000
F210	IPC21	31:16	—	—	—	CCT7IP<2:0>			CCT7IS<1:0>		—	—	—	CCP7IP<2:0>			CCP7IS<1:0>		0000
		15:0	—	—	—	CCT6IP<2:0>			CCT6IS<1:0>		—	—	—	CCP6IP<2:0>			CCP6IS<1:0>		0000
F220	IPC22	31:16	—	—	—	CCT9IP<2:0>			CCT9IS<1:0>		—	—	—	CCP9IP<2:0>			CCP9IS<1:0>		0000
		15:0	—	—	—	CCT8IP<2:0>			CCT8IS<1:0>		—	—	—	CCP8IP<2:0>			CCP8IS<1:0>		0000
F230	IPC23	31:16	—	—	—	CPCIP<2:0>			CPCIS<1:0>		—	—	—	NVMIP<2:0>			NVMIS<1:0>		0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	FSTIP<2:0>			FSTIS<1:0>		0000
F240	IPC24	31:16	—	—	—	DMA1IP<2:0>			DMA1IS<1:0>		—	—	—	DMA0IP<2:0>			DMA0IS<1:0>		0000
		15:0	—	—	—	ECCBEIP<2:0>			ECCBEIS<1:0>		—	—	—	—	—	—	—	—	0000
F250	IPC25	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	DMA3IP<2:0>			DMA3IS<1:0>		—	—	—	DMA2IP<2:0>			DMA2IS<1:0>		0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively.

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REGISTER 7-1: INTCON: INTERRUPT CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	VS<6:0>						
15:8	U-0	U-0	U-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0
	—	—	—	MVEC	—	TPC<2:0>		
7:0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	INT4EP	INT3EP	INT2EP	INT1EP	INT0EP

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-23 **Unimplemented:** Read as ‘0’

bit 22-16 **VS<6:0>**: Vector Spacing bits

Spacing Between Vectors:
0000000 = 0 Bytes
0000001 = 8 Bytes
0000010 = 16 Bytes
0000100 = 32 Bytes
0001000 = 64 Bytes
0010000 = 128 Bytes
0100000 = 256 Bytes
1000000 = 512 Bytes
All other values are reserved. The operation of this device is undefined if a reserved value is written to this field. If MVEC = 0, this field is ignored.

bit 15-13 **Unimplemented:** Read as ‘0’

bit 12 **MVEC:** Multivector Configuration bit
1 = Interrupt controller is configured for Multivectored mode
0 = Interrupt controller is configured for Single Vectored mode

bit 11 **Unimplemented:** Read as ‘0’

bit 10-8 **TPC<2:0>:** Interrupt Proximity Timer Control bits
111 = Interrupts of Group Priority 7 or lower start the interrupt proximity timer
110 = Interrupts of Group Priority 6 or lower start the interrupt proximity timer
101 = Interrupts of Group Priority 5 or lower start the interrupt proximity timer
100 = Interrupts of Group Priority 4 or lower start the interrupt proximity timer
011 = Interrupts of Group Priority 3 or lower start the interrupt proximity timer
010 = Interrupts of Group Priority 2 or lower start the interrupt proximity timer
001 = Interrupts of Group Priority 1 start the interrupt proximity timer
000 = Disables interrupt proximity timer

bit 7-5 **Unimplemented:** Read as ‘0’

bit 4 **INT4EP:** External Interrupt 4 Edge Polarity Control bit
1 = Rising edge
0 = Falling edge

bit 3 **INT3EP:** External Interrupt 3 Edge Polarity Control bit
1 = Rising edge
0 = Falling edge

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REGISTER 7-1: INTCON: INTERRUPT CONTROL REGISTER (CONTINUED)

bit 2 **INT2EP:** External Interrupt 2 Edge Polarity Control bit
1 = Rising edge
0 = Falling edge

bit 1 **INT1EP:** External Interrupt 1 Edge Polarity Control bit
1 = Rising edge
0 = Falling edge

bit 0 **INT0EP:** External Interrupt 0 Edge Polarity Control bit
1 = Rising edge
0 = Falling edge

REGISTER 7-2: PRISS: PRIORITY SHADOW SELECT REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PRI7SS<3:0>(1)				PRI6SS<3:0>(1)			
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PRI5SS<3:0>(1)				PRI4SS<3:0>(1)			
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PRI3SS<3:0>(1)				PRI2SS<3:0>(1)			
7:0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	R/W-0
	PRI1SS<3:0>(1)				—	—	—	SS0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-28 **PRI7SS<3:0>:** Interrupt with Priority Level 7 Shadow Set bits(1)
1111 = Reserved
•
•
•
0010 = Reserved
0001 = Interrupt with a priority level of 7 uses Shadow Set 1
0000 = Interrupt with a priority level of 7 uses Shadow Set 0

bit 27-24 **PRI6SS<3:0>:** Interrupt with Priority Level 6 Shadow Set bits(1)
1111 = Reserved
•
•
•
0010 = Reserved
0001 = Interrupt with a priority level of 6 uses Shadow Set 1
0000 = Interrupt with a priority level of 6 uses Shadow Set 0

Note 1: These bits are ignored if the MVEC bit (INTCON<12>) = 0.

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REGISTER 7-2: PRISS: PRIORITY SHADOW SELECT REGISTER (CONTINUED)

bit 23-20 **PRI5SS<3:0>:** Interrupt with Priority Level 5 Shadow Set bits[(1)]

1111 = Reserved
•
•
•
0010 = Reserved
0001 = Interrupt with a priority level of 5 uses Shadow Set 1
0000 = Interrupt with a priority level of 5 uses Shadow Set 0

bit 19-16 **PRI4SS<3:0>:** Interrupt with Priority Level 4 Shadow Set bits[(1)]

1111 = Reserved
•
•
•
0010 = Reserved
0001 = Interrupt with a priority level of 4 uses Shadow Set 1
0000 = Interrupt with a priority level of 4 uses Shadow Set 0

bit 15-12 **PRI3SS<3:0>:** Interrupt with Priority Level 3 Shadow Set bits[(1)]

1111 = Reserved
•
•
•
0010 = Reserved
0001 = Interrupt with a priority level of 3 uses Shadow Set 1
0000 = Interrupt with a priority level of 3 uses Shadow Set 0

bit 11-8 **PRI2SS<3:0>:** Interrupt with Priority Level 2 Shadow Set bits[(1)]

1111 = Reserved
•
•
•
0010 = Reserved
0001 = Interrupt with a priority level of 2 uses Shadow Set 1
0000 = Interrupt with a priority level of 2 uses Shadow Set 0

bit 7-4 **PRI1SS<3:0>:** Interrupt with Priority Level 1 Shadow Set bits[(1)]

1111 = Reserved
•
•
•
0010 = Reserved
0001 = Interrupt with a priority level of 1 uses Shadow Set 1
0000 = Interrupt with a priority level of 1 uses Shadow Set 0

bit 3-1 **Unimplemented:** Read as ‘0’

bit 0 **SS0:** Single Vector Shadow Register Set bit

1 = Single vector is presented with a shadow set
0 = Single vector is not presented with a shadow set

Note 1: These bits are ignored if the MVEC bit (INTCON<12>) = 0.

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REGISTER 7-3: INTSTAT: INTERRUPT STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC
	—	—	—	—	—	SRIPL<2:0>(1)		
7:0	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC
	SIRQ<7:0>							

Legend:	HS = Hardware Settable bit	HC = Hardware Clearable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-11 **Unimplemented:** Read as ‘0’

bit 10-8 **SRIPL<2:0>:** Requested Priority Level for Single Vector Mode bits[1]
`111-000` = The priority level of the latest interrupt presented to the CPU

bit 7-0 **SIRQ<7:0>:** Last Interrupt Request Serviced Status bits
`11111111-00000000` = The last interrupt request number serviced by the CPU

Note 1: This value should only be used when the interrupt controller is configured for Single Vector mode.

REGISTER 7-4: IPTMR: INTERRUPT PROXIMITY TIMER REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IPTMR<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IPTMR<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IPTMR<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IPTMR<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-0 **IPTMR<31:0>:** Interrupt Proximity Timer Reload bits
Used by the interrupt proximity timer as a reload value when the interrupt proximity timer is triggered by an interrupt event.

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REGISTER 7-5: IFSx: INTERRUPT FLAG STATUS REGISTER x

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IFS<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IFS<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IFS<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IFS<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-0 **IFS<31:0>:** Interrupt Flag Status bits
1 = Interrupt request has occurred
0 = No interrupt request has occurred

Note: This register represents a generic definition of the IFSx register. Refer to Table 7-3 for the exact bit definitions.

REGISTER 7-6: IECx: INTERRUPT ENABLE CONTROL REGISTER x

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IEC<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IEC<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IEC<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IEC<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-0 **IEC<31-0>:** Interrupt Enable bits
1 = Interrupt is enabled
0 = Interrupt is disabled

Note: This register represents a generic definition of the IECx register. Refer to Table 7-3 for the exact bit definitions.

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REGISTER 7-7: IPCx: INTERRUPT PRIORITY CONTROL REGISTER x

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	IP3<2:0>			IS3<1:0>	
23:16	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	IP2<2:0>			IS2<1:0>	
15:8	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	IP1<2:0>			IS1<1:0>	
7:0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	IP0<2:0>			IS0<1:0>	

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-29 **Unimplemented:** Read as '0'

bit 28-26 **IP3<2:0>:** Interrupt Priority 3 bits
`111` = Interrupt priority is 7
•
•
•
`010` = Interrupt priority is 2
`001` = Interrupt priority is 1
`000` = Interrupt is disabled

bit 25-24 **IS3<1:0>:** Interrupt Subpriority 3 bits
`11` = Interrupt subpriority is 3
`10` = Interrupt subpriority is 2
`01` = Interrupt subpriority is 1
`00` = Interrupt subpriority is 0

bit 23-21 **Unimplemented:** Read as '0'

bit 20-18 **IP2<2:0>:** Interrupt Priority 2 bits
`111` = Interrupt priority is 7
•
•
•
`010` = Interrupt priority is 2
`001` = Interrupt priority is 1
`000` = Interrupt is disabled

bit 17-16 **IS2<1:0>:** Interrupt Subpriority 2 bits
`11` = Interrupt subpriority is 3
`10` = Interrupt subpriority is 2
`01` = Interrupt subpriority is 1
`00` = Interrupt subpriority is 0

bit 15-13 **Unimplemented:** Read as '0'

Note: This register represents a generic definition of the IPCx register. Refer to Table 7-3 for the exact bit definitions.

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REGISTER 7-7: IPCx: INTERRUPT PRIORITY CONTROL REGISTER x (CONTINUED)

bit 12-10 **IP1<2:0>:** Interrupt Priority 1 bits
`111` = Interrupt priority is 7
•
•
•
`010` = Interrupt priority is 2
`001` = Interrupt priority is 1
`000` = Interrupt is disabled

bit 9-8 **IS1<1:0>:** Interrupt Subpriority 1 bits
`11` = Interrupt subpriority is 3
`10` = Interrupt subpriority is 2
`01` = Interrupt subpriority is 1
`00` = Interrupt subpriority is 0

bit 7-5 **Unimplemented:** Read as ‘`0`’

bit 4-2 **IP0<2:0>:** Interrupt Priority 0 bits
`111` = Interrupt priority is 7
•
•
•
`010` = Interrupt priority is 2
`001` = Interrupt priority is 1
`000` = Interrupt is disabled

bit 1-0 **IS0<1:0>:** Interrupt Subpriority 0 bits
`11` = Interrupt subpriority is 3
`10` = Interrupt subpriority is 2
`01` = Interrupt subpriority is 1
`00` = Interrupt subpriority is 0

Note:	This register represents a generic definition of the IPCx register. Refer to Table 7-3 for the exact bit definitions.

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NOTES:

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8.0 DIRECT MEMORY ACCESS (DMA) CONTROLLER

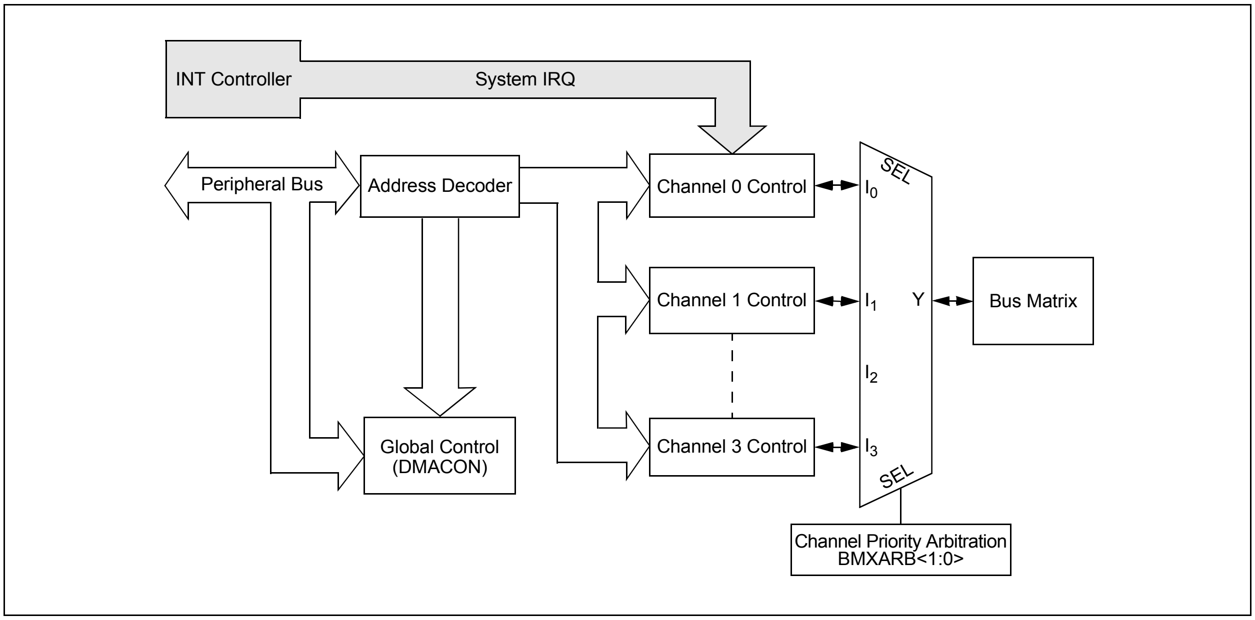
Note 1:	This data sheet summarizes the features of the PIC32MM0256GPM064 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 31. "DMA Controller"** (DS60001117) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

The Direct Memory Access (DMA) Controller is a bus master module useful for data transfers between peripherals and memory without CPU intervention. The source and destination of a DMA transfer can be any of the memory-mapped modules, that do not have a dedicated DMA, existent in the PIC32 (such as SPI, UART, PMP, etc.) or the memory itself.

The following are some of the key features of the DMA Controller module:

- Four Identical Channels, Each Featuring:
  - Auto-Increment Source and Destination Address registers
  - Source and Destination Pointers
  - Memory to memory and memory to peripheral transfers
- Automatic Word Size Detection:
  - Transfer granularity, down to byte level
  - Bytes need not be word-aligned at source and destination
- Fixed Priority Channel Arbitration
- Flexible DMA Channel Operating modes:
  - Manual (software) or automatic (interrupt) DMA requests
  - One-Shot or Auto-Repeat Block Transfer modes
  - Channel-to-channel chaining
- Flexible DMA Requests:
  - A DMA request can be selected from any of the peripheral interrupt sources
  - Each channel can select any (appropriate) observable interrupt as its DMA request source
  - A DMA transfer abort can be selected from any of the peripheral interrupt sources
  - Pattern (data) match transfer termination
- Multiple DMA Channel Status Interrupts:
  - DMA channel block transfer complete
  - Source empty or half empty
  - Destination full or half full
  - DMA transfer aborted due to an external event
  - Invalid DMA address generated
- DMA Debug Support Features:
  - Most recent address accessed by a DMA channel
  - Most recent DMA channel to transfer data
- CRC Generation module:
  - CRC module can be assigned to any of the available channels
  - CRC module is highly configurable
- User Selectable Bus Arbitration Priority (refer to **Section 4.2 "Bus Matrix (BMX)"**)
- 8 System Clocks Per Cell Transfer

FIGURE 8-1: DMA BLOCK DIAGRAM



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8.1 DMA Control Registers

TABLE 8-1: DMA CONTROLLER REGISTER MAP

Virtual Address (BF88_#)	Register Name[1]	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
8900	DMACON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	SUSPEND	DMABUSY	—	—	—	—	—	—	—	—	—	—	—	0000
8910	DMASTAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RDWR	DMACH<2:0>			0000
8920	DMAADDR	31:16	DMAADDR<31:0>																0000
		15:0																	0000
8930	DCRCCON	31:16	—	—	BYTO<1:0>		WBO	—	—	BITO	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	PLEN<4:0>					CRCEN	CRCAPP	CRCTYP	—	—	CRCCH<2:0>			0000
8940	DCRCDATA	31:16	DCRCDATA<31:0>																0000
		15:0																	0000
8950	DCRCXOR	31:16	DCRCXOR<31:0>																0000
		15:0																	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 10.1 "CLR, SET and INV Registers"** for more information.

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TABLE 8-2: DMA CHANNELS 0-3 REGISTER MAP

Virtual Address (BF88_#)	Register Name[1]	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
8960	DCH0CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHBUSY	—	—	—	—	—	—	CHCHNS	CHEN	CHAED	CHCHN	CHAEN	—	CHEDET	CHPRI<1:0>		0000
8970	DCH0ECON	31:16	—	—	—	—	—	—	—	—	CHAIRQ<7:0>								00FF
		15:0	CHSIRQ<7:0>								CFORCE	CABORT	PATEN	SIRQEN	AIRQEN	—	—	—	FF00
8980	DCH0INT	31:16	—	—	—	—	—	—	—	—	CHSDIE	CHSHIE	CHDDIE	CHDHIE	CHBCIE	CHCCIE	CHTAIE	CHERIE	0000
		15:0	—	—	—	—	—	—	—	—	CHSDIF	CHSHIF	CHDDIF	CHDHIF	CHBCIF	CHCCIF	CHTAIF	CHERIF	0000
8990	DCH0SSA	31:16	CHSSA<31:0>																0000
		15:0																	0000
89A0	DCH0DSA	31:16	CHDSA<31:0>																0000
		15:0																	0000
89B0	DCH0SSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSSIZ<15:0>																0000
89C0	DCH0DSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDSIZ<15:0>																0000
89D0	DCH0SPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSPTR<15:0>																0000
89E0	DCH0DPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDPTR<15:0>																0000
89F0	DCH0CSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCSIZ<15:0>																0000
8A00	DCH0CPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCPTR<15:0>																0000
8A10	DCH0DAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	CHPDAT<7:0>								0000
8A20	DCH1CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHBUSY	—	—	—	—	—	—	CHCHNS	CHEN	CHAED	CHCHN	CHAEN	—	CHEDET	CHPRI<1:0>		0000
8A30	DCH1ECON	31:16	—	—	—	—	—	—	—	—	CHAIRQ<7:0>								00FF
		15:0	CHSIRQ<7:0>								CFORCE	CABORT	PATEN	SIRQEN	AIRQEN	—	—	—	FF00
8A40	DCH1INT	31:16	—	—	—	—	—	—	—	—	CHSDIE	CHSHIE	CHDDIE	CHDHIE	CHBCIE	CHCCIE	CHTAIE	CHERIE	0000
		15:0	—	—	—	—	—	—	—	—	CHSDIF	CHSHIF	CHDDIF	CHDHIF	CHBCIF	CHCCIF	CHTAIF	CHERIF	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 10.1 "CLR, SET and INV Registers"** for more information.

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TABLE 8-2: DMA CHANNELS 0-3 REGISTER MAP (CONTINUED)

Virtual Address (BF88_#)	Register Name(1)	Bit Range	Bits 31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
8A50	DCH1SSA	31:16	CHSSA<31:0>																0000
		15:0																	0000
8A60	DCH1DSA	31:16	CHDSA<31:0>																0000
		15:0																	0000
8A70	DCH1SSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSSIZ<15:0>																0000
8A80	DCH1DSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDSIZ<15:0>																0000
8A90	DCH1SPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSPTR<15:0>																0000
8AA0	DCH1DPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDPTR<15:0>																0000
8AB0	DCH1CSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCSIZ<15:0>																0000
8AC0	DCH1CPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCPTR<15:0>																0000
8AD0	DCH1DAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	CHPDAT<7:0>								0000
8AE0	DCH2CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHBUSY	—	—	—	—	—	—	CHCHNS	CHEN	CHAED	CHCHN	CHAEN	—	CHEDET	CHPRI<1:0>		0000
8AF0	DCH2ECON	31:16	—	—	—	—	—	—	—	—	CHAIRQ<7:0>								00FF
		15:0	CHSIRQ<7:0>								CFORCE	CABORT	PATEN	SIRQEN	AIRQEN	—	—	—	FF00
8B00	DCH2INT	31:16	—	—	—	—	—	—	—	—	CHSDIE	CHSHIE	CHDDIE	CHDHIE	CHBCIE	CHCCIE	CHTAIE	CHERIE	0000
		15:0	—	—	—	—	—	—	—	—	CHSDIF	CHSHIF	CHDDIF	CHDHIF	CHBCIF	CHCCIF	CHTAIF	CHERIF	0000
8B10	DCH2SSA	31:16	CHSSA<31:0>																0000
		15:0																	0000
8B20	DCH2DSA	31:16	CHDSA<31:0>																0000
		15:0																	0000
8B30	DCH2SSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSSIZ<15:0>																0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 10.1 "CLR, SET and INV Registers"** for more information.

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TABLE 8-2: DMA CHANNELS 0-3 REGISTER MAP (CONTINUED)

Virtual Address (BF88_#)	Register Name[1]	Bit Range	Bits 31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
8B40	DCH2DSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDSIZ<15:0>																0000
8B50	DCH2SPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSPTR<15:0>																0000
8B60	DCH2DPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDPTR<15:0>																0000
8B70	DCH2CSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCSIZ<15:0>																0000
8B80	DCH2CPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCPTR<15:0>																0000
8B90	DCH2DAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	CHPDAT<7:0>								0000
8BA0	DCH3CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHBUSY	—	—	—	—	—	—	CHCHNS	CHEN	CHAED	CHCHN	CHAEN	—	CHEDET	CHPRI<1:0>		0000
8BB0	DCH3ECON	31:16	—	—	—	—	—	—	—	—	CHAIRQ<7:0>								00FF
		15:0	CHSIRQ<7:0>								CFORCE	CABORT	PATEN	SIRQEN	AIRQEN	—	—	—	FF00
8BC0	DCH3INT	31:16	—	—	—	—	—	—	—	—	CHSDIE	CHSHIE	CHDDIE	CHDHIE	CHBCIE	CHCCIE	CHTAIE	CHERIE	0000
		15:0	—	—	—	—	—	—	—	—	CHSDIF	CHSHIF	CHDDIF	CHDHIF	CHBCIF	CHCCIF	CHTAIF	CHERIF	0000
8BD0	DCH3SSA	31:16	CHSSA<31:0>																0000
		15:0																	0000
8BE0	DCH3DSA	31:16	CHDSA<31:0>																0000
		15:0																	0000
8BF0	DCH3SSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSSIZ<15:0>																0000
8C00	DCH3DSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDSIZ<15:0>																0000
8C10	DCH3SPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSPTR<15:0>																0000
8C20	DCH3DPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDPTR<15:0>																0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 10.1 "CLR, SET and INV Registers"** for more information.

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TABLE 8-2: DMA CHANNELS 0-3 REGISTER MAP (CONTINUED)

Virtual Address (BF88_#)	Register Name[1]	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
8C30	DCH3CSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCSIZ<15:0>																0000
8C40	DCH3CPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCPTR<15:0>																0000
8C50	DCH3DAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	CHPDAT<7:0>								0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 10.1 "CLR, SET and INV Registers"** for more information.

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REGISTER 8-1: DMACON: DMA CONTROLLER CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	U-0	R/W-0	R/W-0	U-0	U-0	U-0
	ON(1)	—	—	SUSPEND	DMABUSY	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as ‘0’

bit 15 **ON:** DMA On bit(1)
- 1 = DMA module is enabled
- 0 = DMA module is disabled

bit 14-13 **Unimplemented:** Read as ‘0’

bit 12 **SUSPEND:** DMA Suspend bit
- 1 = DMA transfers are suspended to allow CPU uninterrupted access to data bus
- 0 = DMA operates normally

bit 11 **DMABUSY:** DMA Module Busy bit
- 1 = DMA module is active
- 0 = DMA module is disabled and not actively transferring data

bit 10-0 **Unimplemented:** Read as ‘0’

Note 1: The user’s software should not read/write the peripheral’s SFRs in the SYSCLK cycle immediately following the instruction that clears the module’s ON bit.

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REGISTER 8-2: DMASTAT: DMA STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	R-0	R-0	R-0	R-0
	—	—	—	—	RDWR	DMACH<2:0>		

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-4 **Unimplemented:** Read as '0'

bit 3 **RDWR:** DMA Read/Write Status bit
1 = Last DMA bus access was a read
0 = Last DMA bus access was a write

bit 2-0 **DMACH<2:0>:** DMA Channel bits
These bits contain the value of the most recent active DMA channel.

REGISTER 8-3: DMAADDR: DMA ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	DMAADDR<31:24>							
23:16	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	DMAADDR<23:16>							
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	DMAADDR<15:8>							
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	DMAADDR<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **DMAADDR<31:0>:** DMA Module Address bits
These bits contain the address of the most recent DMA access.

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REGISTER 8-4: DCRCCON: DMA CRC CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0
	—	—	BYTO<1:0>		WBO[1]	—	—	BITO
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	PLEN<4:0>				
7:0	R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	CRCEN	CRCAPP[1]	CRCTYP	—	—	CRCCH<2:0>		

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-30 **Unimplemented:** Read as '0'

bit 29-28 **BYTO<1:0>:** CRC Byte Order Selection bits
- 11 = Endian byte swap on half-word boundaries (source half-word order with reverse source byte order per half-word)
- 10 = Swap half-words on word boundaries (reverse source half-word order with source byte order per half-word)
- 01 = Endian byte swap on word boundaries (reverse source byte order)
- 00 = No swapping (source byte order)

bit 27 **WBO:** CRC Write Byte Order Selection bit[1]
- 1 = Source data is written to the destination re-ordered, as defined by BYTO<1:0>
- 0 = Source data is written to the destination unaltered

bit 26-25 **Unimplemented:** Read as '0'

bit 24 **BITO:** CRC Bit Order Selection bit

<u>When CRCTYP (DCRCCON<5>) = 1 (CRC module is in IP Header mode):</u>
- 1 = The IP header checksum is calculated Least Significant bit (LSb) first (reflected)
- 0 = The IP header checksum is calculated Most Significant bit (MSb) first (not reflected)

<u>When CRCTYP (DCRCCON<5>) = 0 (CRC module is in LFSR mode):</u>
- 1 = The LFSR CRC is calculated Least Significant bit first (reflected)
- 0 = The LFSR CRC is calculated Most Significant bit first (not reflected)

bit 23-13 **Unimplemented:** Read as '0'

bit 12-8 **PLEN<4:0>:** Polynomial Length bits

<u>When CRCTYP (DCRCCON<5>) = 1 (CRC module is in IP Header mode):</u>
These bits are unused.

<u>When CRCTYP (DCRCCON<5>) = 0 (CRC module is in LFSR mode):</u>
Denotes the length of the polynomial – 1.

bit 7 **CRCEN:** CRC Enable bit
- 1 = CRC module is enabled and channel transfers are routed through the CRC module
- 0 = CRC module is disabled and channel transfers proceed normally

bit 6 **CRCAPP:** CRC Append Mode bit[1]
- 1 = The DMA transfers data from the source into the CRC but not to the destination; when a block transfer completes, the DMA writes the calculated CRC value to the location given by CHxDSA
- 0 = The DMA transfers data from the source through the CRC, obeying WBO as it writes the data to the destination

Note 1: When WBO = 1, unaligned transfers are not supported and the CRCAPP bit cannot be set.

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REGISTER 8-4: DCRCCON: DMA CRC CONTROL REGISTER (CONTINUED)

bit 5 **CRCTYP:** CRC Type Selection bit
1 = The CRC module will calculate an IP header checksum
0 = The CRC module will calculate an LFSR CRC

bit 4-3 **Unimplemented:** Read as '0'

bit 2-0 **CRCCH<2:0>:** CRC Channel Select bits
111 = CRC is assigned to Channel 7
110 = CRC is assigned to Channel 6
101 = CRC is assigned to Channel 5
100 = CRC is assigned to Channel 4
011 = CRC is assigned to Channel 3
010 = CRC is assigned to Channel 2
001 = CRC is assigned to Channel 1
000 = CRC is assigned to Channel 0

Note 1: When WBO = 1, unaligned transfers are not supported and the CRCAPP bit cannot be set.

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REGISTER 8-5: DCRCDATA: DMA CRC DATA REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DCRCDATA<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DCRCDATA<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DCRCDATA<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DCRCDATA<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-0 **DCRCDATA<31:0>:** CRC Data Register bits

Writing to this register will seed the CRC generator. Reading from this register will return the current value of the CRC. Bits greater than PLEN will return ‘0’ on any read.

When CRCTYP (DCRCCON<5>) = 1 (CRC module is in IP Header mode):
Only the lower 16 bits contain IP header checksum information. The upper 16 bits are always ‘0’. Data written to this register is converted and read back in ‘1’s complement form (current IP header checksum value).

When CRCTYP (DCRCCON<5>) = 0 (CRC module is in LFSR mode):
Bits greater than PLEN will return ‘0’ on any read.

REGISTER 8-6: DCRCXOR: DMA CRCXOR ENABLE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DCRCXOR<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DCRCXOR<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DCRCXOR<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DCRCXOR<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-0 **DCRCXOR<31:0>:** CRC XOR Register bits

When CRCTYP (DCRCCON<5>) = 1 (CRC module is in IP Header mode):
This register is unused.

When CRCTYP (DCRCCON<5>) = 0 (CRC module is in LFSR mode):
1 = Enables the XOR input to the Shift register
0 = Disables the XOR input to the Shift register; data is shifted in directly from the previous stage in the register

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REGISTER 8-7: DCHxCON: DMA CHANNEL x CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
	CHBUSY	—	—	—	—	—	—	CHCHNS(1)
7:0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R-0	R/W-0	R/W-0
	CHEN(2)	CHAED	CHCHN	CHAEN	—	CHEDET	CHPRI<1:0>	

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as ‘0’

bit 15 **CHBUSY:** Channel Busy bit
1 = Channel is active or has been enabled
0 = Channel is inactive or has been disabled

bit 14-9 **Unimplemented:** Read as ‘0’

bit 8 **CHCHNS:** Chain Channel Selection bit(1)
1 = Chain to channel lower in natural priority (CH1 will be enabled by CH2 transfer complete)
0 = Chain to channel higher in natural priority (CH1 will be enabled by CH0 transfer complete)

bit 7 **CHEN:** Channel Enable bit(2)
1 = Channel is enabled
0 = Channel is disabled

bit 6 **CHAED:** Channel Allow Events if Disabled bit
1 = Channel start/abort events will be registered, even if the channel is disabled
0 = Channel start/abort events will be ignored if the channel is disabled

bit **CHCHN:** Channel Chain Enable bit
1 = Allows channel to be chained
0 = Does not allow channel to be chained

bit 4 **CHAEN:** Channel Automatic Enable bit
1 = Channel is continuously enabled and not automatically disabled after a block transfer is complete
0 = Channel is disabled on a block transfer complete

bit 3 **Unimplemented:** Read as ‘0’

bit 2 **CHEDET:** Channel Event Detected bit
1 = An event has been detected
0 = No events have been detected

bit 1-0 **CHPRI<1:0>:** Channel Priority bits
11 = Channel has Priority 3 (highest)
10 = Channel has Priority 2
01 = Channel has Priority 1
00 = Channel has Priority 0

Note 1: The chain selection bit takes effect when chaining is enabled (CHCHN = 1).
2: When the channel is suspended by clearing this bit, the user application should poll the CHBUSY bit (if available on the device variant) to see when the channel is suspended, as it may take some clock cycles to complete a current transaction before the channel is suspended.

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REGISTER 8-8: DCHxECON: DMA CHANNEL x EVENT CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
	CHAIRQ<7:0>(1)							
15:8	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
	CHSIRQ<7:0>(1)							
7:0	S-0	S-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0
	CFORCE	CABORT	PATEN	SIRQEN	AIRQEN	—	—	—

Legend:	S = Settable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-24 **Unimplemented:** Read as ‘0’

bit 23-16 **CHAIRQ<7:0>:** Channel Transfer Abort IRQ bits(1)

11111111 = Interrupt 255 will abort any transfers in progress and sets the CHTAIF flag
•
•
•
00000001 = Interrupt 1 will abort any transfers in progress and sets the CHTAIF flag
00000000 = Interrupt 0 will abort any transfers in progress and sets the CHTAIF flag

bit 15-8 **CHSIRQ<7:0>:** Channel Transfer Start IRQ bits(1)

11111111 = Interrupt 255 will initiate a DMA transfer
•
•
•
00000001 = Interrupt 1 will initiate a DMA transfer
00000000 = Interrupt 0 will initiate a DMA transfer

bit 7 **CFORCE:** DMA Forced Transfer bit

1 = A DMA transfer is forced to begin when this bit is written to a ‘1’
0 = This bit always reads ‘0’

bit 6 **CABORT:** DMA Abort Transfer bit

1 = A DMA transfer is aborted when this bit is written to a ‘1’
0 = This bit always reads ‘0’

bit 5 **PATEN:** Channel Pattern Match Abort Enable bit

1 = Aborts transfer and clears CHEN on pattern match
0 = Pattern match is disabled

bit 4 **SIRQEN:** Channel Start IRQ Enable bit

1 = Starts channel cell transfer if an interrupt matching CHSIRQx occurs
0 = Interrupt number CHSIRQx is ignored and does not start a transfer

bit 3 **AIRQEN:** Channel Abort IRQ Enable bit

1 = Channel transfer is aborted if an interrupt matching CHAIRQx occurs
0 = Interrupt number CHAIRQx is ignored and does not terminate a transfer

bit 2-0 **Unimplemented:** Read as ‘0’

Note 1: See Table 7-2 for the list of available interrupt IRQ sources.

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REGISTER 8-9: DCHxINT: DMA CHANNEL x INTERRUPT CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHSDIE	CHSHIE	CHDDIE	CHDHIE	CHBCIE	CHCCIE	CHTAIE	CHERIE
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHSDIF	CHSHIF	CHDDIF	CHDHIF	CHBCIF	CHCCIF	CHTAIF	CHERIF

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-24 **Unimplemented:** Read as ‘0’

bit 23 **CHSDIE:** Channel Source Done Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 22 **CHSHIE:** Channel Source Half Empty Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 21 **CHDDIE:** Channel Destination Done Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 20 **CHDHIE:** Channel Destination Half Full Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 19 **CHBCIE:** Channel Block Transfer Complete Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 18 **CHCCIE:** Channel Cell Transfer Complete Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 17 **CHTAIE:** Channel Transfer Abort Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 16 **CHERIE:** Channel Address Error Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 15-8 **Unimplemented:** Read as ‘0’

bit 7 **CHSDIF:** Channel Source Done Interrupt Flag bit
1 = Channel Source Pointer has reached end of source (CHSPTRx = CHSSIZx)
0 = No interrupt is pending

bit 6 **CHSHIF:** Channel Source Half Empty Interrupt Flag bit
1 = Channel Source Pointer has reached midpoint of source (CHSPTRx = CHSSIZx/2)
0 = No interrupt is pending

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REGISTER 8-9: DCHxINT: DMA CHANNEL x INTERRUPT CONTROL REGISTER (CONTINUED)

bit 5 **CHDDIF:** Channel Destination Done Interrupt Flag bit
1 = Channel Destination Pointer has reached end of destination (CHDPTRx = CHDSIZx)
0 = No interrupt is pending

bit 4 **CHDHIF:** Channel Destination Half Full Interrupt Flag bit
1 = Channel Destination Pointer has reached midpoint of destination (CHDPTRx = CHDSIZx/2)
0 = No interrupt is pending

bit 3 **CHBCIF:** Channel Block Transfer Complete Interrupt Flag bit
1 = A block transfer has been completed (the larger of CHSSIZx/CHDSIZx bytes has been transferred) or a pattern match event occurs
0 = No interrupt is pending

bit 2 **CHCCIF:** Channel Cell Transfer Complete Interrupt Flag bit
1 = A cell transfer has been completed (CHCSIZx bytes have been transferred)
0 = No interrupt is pending

bit 1 **CHTAIF:** Channel Transfer Abort Interrupt Flag bit
1 = An interrupt matching CHAIRQx has been detected and the DMA transfer has been aborted
0 = No interrupt is pending

bit 0 **CHERIF:** Channel Address Error Interrupt Flag bit
1 = A channel address error has been detected (either the source or the destination address is invalid)
0 = No interrupt is pending

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REGISTER 8-10: DCHxSSA: DMA CHANNEL x SOURCE START ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHSSA<31:24>(1)							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHSSA<23:16>(1)							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHSSA<15:8>(1)							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHSSA<7:0>(1)							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-0 **CHSSA<31:0>** Channel Source Start Address bits(1)
Channel source start address.

Note 1: This must be the physical address of the source.

REGISTER 8-11: DCHxDSA: DMA CHANNEL x DESTINATION START ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHDSA<31:24>(1)							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHDSA<23:16>(1)							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHDSA<15:8>(1)							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHDSA<7:0>(1)							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-0 **CHDSA<31:0>:** Channel Destination Start Address bits(1)
Channel destination start address.

Note 1: This must be the physical address of the source.

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REGISTER 8-12: DCHxSSIZ: DMA CHANNEL x SOURCE SIZE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHSSIZ<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHSSIZ<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as ‘0’

bit 15-0 **CHSSIZ<15:0>:** Channel Source Size bits
`1111111111111111` = 65,535-byte source size
•
•
•
`0000000000000010` = 2-byte source size
`0000000000000001` = 1-byte source size
`0000000000000000` = 65,536-byte source size

REGISTER 8-13: DCHxDSIZ: DMA CHANNEL x DESTINATION SIZE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHDSIZ<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHDSIZ<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as ‘0’

bit 15-0 **CHDSIZ<15:0>:** Channel Destination Size bits
`1111111111111111` = 65,535-byte destination size
•
•
•
`0000000000000010` = 2-byte destination size
`0000000000000001` = 1-byte destination size
`0000000000000000` = 65,536-byte destination size

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REGISTER 8-14: DCHxSPTR: DMA CHANNEL x SOURCE POINTER REGISTER[1]

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	CHSPTR<15:8>							
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	CHSPTR<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as ‘0’

bit 15-0 **CHSPTR<15:0>:** Channel Source Pointer bits

`1111111111111111` = Points to Byte 65,535 of the source
•
•
•
`0000000000000001` = Points to Byte 1 of the source
`0000000000000000` = Points to Byte 0 of the source

Note 1: When in Pattern Detect mode, this register is reset on a pattern detect.

REGISTER 8-15: DCHxDPTR: DMA CHANNEL x DESTINATION POINTER REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	CHDPTR<15:8>							
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	CHDPTR<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as ‘0’

bit 15-0 **CHDPTR<15:0>:** Channel Destination Pointer bits

`1111111111111111` = Points to Byte 65,535 of the destination
•
•
•
`0000000000000001` = Points to Byte 1 of the destination
`0000000000000000` = Points to Byte 0 of the destination

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REGISTER 8-16: DCHxCSIZ: DMA CHANNEL x CELL SIZE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHCSIZ<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHCSIZ<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as ‘0’

bit 15-0 **CHCSIZ<15:0>:** Channel Cell Size bits

1111111111111111 = 65,535 bytes are transferred on an event
•
•
•
0000000000000010 = 2 bytes are transferred on an event
0000000000000001 = 1 byte is transferred on an event
0000000000000000 = 65,536 bytes are transferred on an event

REGISTER 8-17: DCHxCPTR: DMA CHANNEL x CELL POINTER REGISTER(1)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	CHCPTR<15:8>							
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	CHCPTR<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as ‘0’

bit 15-0 **CHCPTR<7:0>:** Channel Cell Progress Pointer bits

1111111111111111 = 65,535 bytes have been transferred since the last event
•
•
•
0000000000000001 = 1 byte has been transferred since the last event
0000000000000000 = 0 bytes have been transferred since the last event

Note 1: When in Pattern Detect mode, this register is reset on a pattern detect.

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REGISTER 8-18: DCHxDAT: DMA CHANNEL x PATTERN DATA REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHPDAT<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as ‘0’

bit 7-0 **CHPDAT<7:0>:** Channel Data Register bits

Pattern Terminate mode:
Data to be matched must be stored in this register to allow terminate on match.

All Other modes:
Unused.

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9.0 OSCILLATOR CONFIGURATION

> **Note:** This data sheet summarizes the features of the PIC32MM0256GPM064 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 59. "Oscillators with DCO"** (DS60001329) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32). The information in this data sheet supersedes the information in the FRM.

The PIC32MM0256GPM064 family oscillator system has the following modules and features:

- A Total of Five External and Internal Oscillator Options as Clock Sources
- On-Chip PLL with User-Selectable Multiplier and Output Divider to Boost Operating Frequency on Select Internal and External Oscillator Sources
- On-Chip User-Selectable Divisor Postscaler on Select Oscillator Sources
- Software-Controllable Switching between Various Clock Sources
- A Fail-Safe Clock Monitor (FSCM) that Detects Clock Failure and Permits Safe Application Recovery or Shutdown
- Flexible Reference Clock Output

A block diagram of the oscillator system is provided in Figure 9-1.

9.1 Fail-Safe Clock Monitor (FSCM)

The PIC32MM0256GPM064 family oscillator system includes a Fail-Safe Clock Monitor (FSCM). The FSCM monitors the SYSCLK for continuous operation. If it detects that the SYSCLK has failed, it switches the SYSCLK over to the FRC oscillator and triggers a Non-Maskable Interrupt (NMI). When the NMI is executed, software can attempt to restart the main oscillator or shut down the system.

In Sleep mode, both the SYSCLK and the FSCM halt, which prevents FSCM detection.

9.2 Clock Switching Operation

With few limitations, applications are free to switch between any of the four clock sources (POSC, SOSC, FRC and LPRC) under software control and at any time. To limit the possible side effects that could result from this flexibility, PIC32 devices have a safeguard lock built into the switching process.

> **Note:** The Primary Oscillator mode has three different submodes (XT, HS and EC), which are determined by the POSCMOD<1:0> Configuration bits. While an application can switch to and from Primary Oscillator mode in software, it cannot switch between the different primary submodes without reprogramming the device.

9.2.1 ENABLING CLOCK SWITCHING

To enable clock switching, the FCKSM1 Configuration bit in FOSC must be programmed to '0'. (Refer to **Section 26.1 "Configuration Bits"** for further details.) If the FCKSM1 Configuration bit is unprogrammed ('1'), the clock switching function and Fail-Safe Clock Monitor function are disabled; this is the default setting.

The NOSC<2:0> control bits (OSCCON<10:8>) do not control the clock selection when clock switching is disabled. However, the COSC<2:0> bits (OSCCON<14:12>) will reflect the clock source selected by the FNOSC<2:0> Configuration bits.

The OSWEN control bit (OSCCON<0>) has no effect when clock switching is disabled; it is held at '0' at all times.

9.2.2 OSCILLATOR SWITCHING SEQUENCE

At a minimum, performing a clock switch requires this basic sequence:

1. If desired, read the COSC<2:0> bits (OSCCON<14:12>) to determine the current oscillator source.
2. Perform the unlock sequence to allow a write to the OSCCON register.
3. Write the appropriate value to the NOSC<2:0> bits (OSCCON<10:8>) for the new oscillator source.
4. Set the OSWEN bit to initiate the oscillator switch.

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Once the basic sequence is completed, the system clock hardware responds automatically as follows:

1. The clock switching hardware compares the COSCx bits with the new value of the NOSCx bits. If they are the same, then the clock switch is a redundant operation. In this case, the OSWEN bit is cleared automatically and the clock switch is aborted.
2. If a valid clock switch has been initiated, the LOCK (OSCTUN<11>) and CF (OSCCON<3>) bits are cleared.
3. The new oscillator is turned on by the hardware if it is not currently running. If a crystal oscillator must be turned on, the hardware will wait until the OST expires. If the new source is using the PLL, then the hardware waits until a PLL lock is detected (LOCK = 1).
4. The hardware waits for 10 clock cycles from the new clock source and then performs the clock switch.
5. The hardware clears the OSWEN bit to indicate a successful clock transition. In addition, the NOSC<2:0> bits values are transferred to the COSC<2:0> bits.
6. The old clock source is turned off if it is not being used by a peripheral, or enabled by device configuration or a control register.

> **Note 1:** The processor will continue to execute code throughout the clock switching sequence. Timing-sensitive code should not be executed during this time.
>
> **2:** Direct clock switches between any Primary Oscillator mode with PLL and FRCPLL mode are not permitted. This applies to clock switches in either direction. In these instances, the application must switch to FRC mode as a transitional clock source between the two PLL modes.

A recommended code sequence for a clock switch includes the following:

1. Disable interrupts during the OSCCON register unlock and write sequence.
2. Execute the unlock sequence for OSCCON by writing 0xAA996655 and 0x556699AA to the SYSKEY register.
3. Write the new oscillator source to the NOSC<2:0> bits.
4. Set the OSWEN bit.
5. Relock the OSCCON register.
6. Continue to execute code that is not clock-sensitive (optional).

The core sequence for unlocking the OSCCON register and initiating a clock switch is shown in Example 9-1.

EXAMPLE 9-1: BASIC CODE SEQUENCE FOR CLOCK SWITCHING

```
SYSKEY = 0x00000000;        // force lock
SYSKEY = 0xAA996655;        // unlock
SYSKEY = 0x556699AA;

OSCCONbits.NOSC = 3;        // select the new
                               clock source

OSCCONSET = 1;              // set the OSWEN bit

SYSKEY = 0x00000000;        // force lock

while (OSCCONbits.OSWEN);   // optional wait for
                               switch operation
BSET  OSCCON, #0
```

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9.3 FRC Active Clock Tuning

PIC32MM0256GPM064 family devices include an automatic mechanism to calibrate the FRC during run time. This system uses active clock tuning from a source of known accuracy to maintain the FRC within a very narrow margin of its nominal 8 MHz frequency. This allows for a frequency accuracy that is well within the requirements of the *"USB 2.0 Specification"* regarding full-speed USB devices.

> **Note:** The self-tune feature maintains sufficient accuracy for operation in USB Device mode. For applications that function as a USB host, a high-accuracy clock source (±0.05%) is still required.

The self-tune system is controlled by the bits in the upper half of the OSCTUN register. Setting the ON bit (OSCTUN<15>) enables the self-tuning feature, allowing the hardware to calibrate to a source selected by the SRC bit (OSCTUN<12>). When SRC = `1`, the system uses the Start-of-Frame (SOF) packets from an external USB host for its source. When SRC = `0`, the system uses the crystal-controlled SOSC for its calibration source. Regardless of the source, the system uses the TUN<5:0> bits (OSCTUN<5:0>) to change the FRC Oscillator's frequency. Frequency monitoring and adjustment is dynamic, occurring continuously during run time. While the system is active, the TUNx bits cannot be written to by software.

> **Note:** To use the USB as a reference clock tuning source (SRC = `1`), the microcontroller must be configured for USB device operation and connected to a non-suspended USB host or hub port.
>
> If the SOSC is to be used as the reference clock tuning source (SRC = `0`), the SOSC must also be enabled for clock tuning to occur.

The self-tune system can generate a hardware interrupt, FSTIF. The interrupt can result from a drift of the FRC from the reference, by greater than 0.2% in either direction, or whenever the frequency deviation is beyond the ability of the TUNx bits to correct (i.e., greater than 1.5%). The LOCK and ORNG status bits (OSCTUN<11,9>) are used to indicate these conditions.

The POL and ORPOL bits (OSCTUN<10,8>) configure the FSTIF interrupt to occur in the presence or the absence of the conditions. It is the user's responsibility to monitor both the LOCK and ORNG bits to determine the exact cause of the interrupt.

> **Note:** The POL and ORPOL bits should be ignored when the self-tune system is disabled (ON = `0`).

> **Note:** After exiting out of self-tune, 6 writes may be required to update the TUN<5:0> bits.

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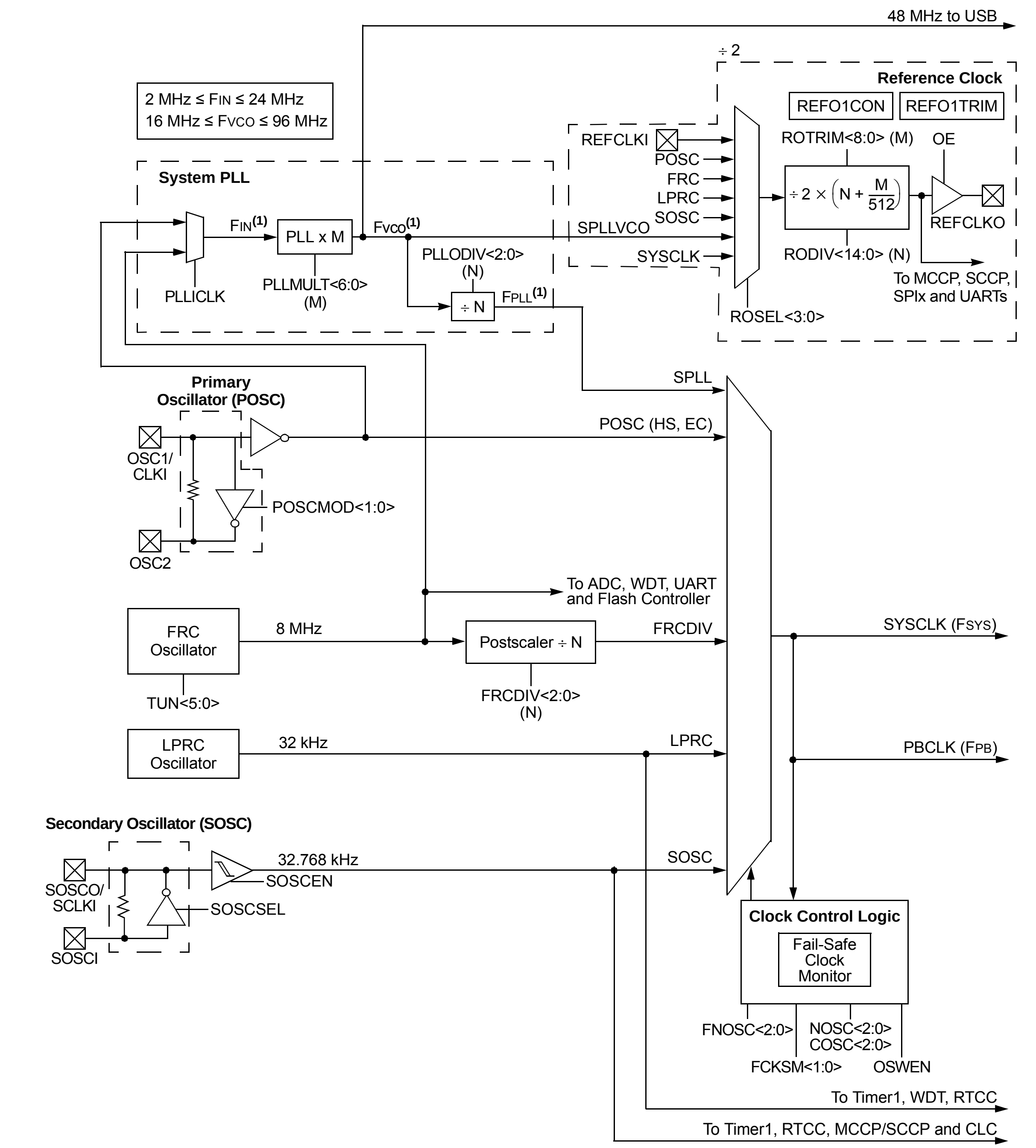
FIGURE 9-1: PIC32MM0256GPM064 FAMILY OSCILLATOR DIAGRAM[(1)]



Note 1: Refer to Table 29-19 in **Section 29.0 "Electrical Characteristics"** for frequency limitations.

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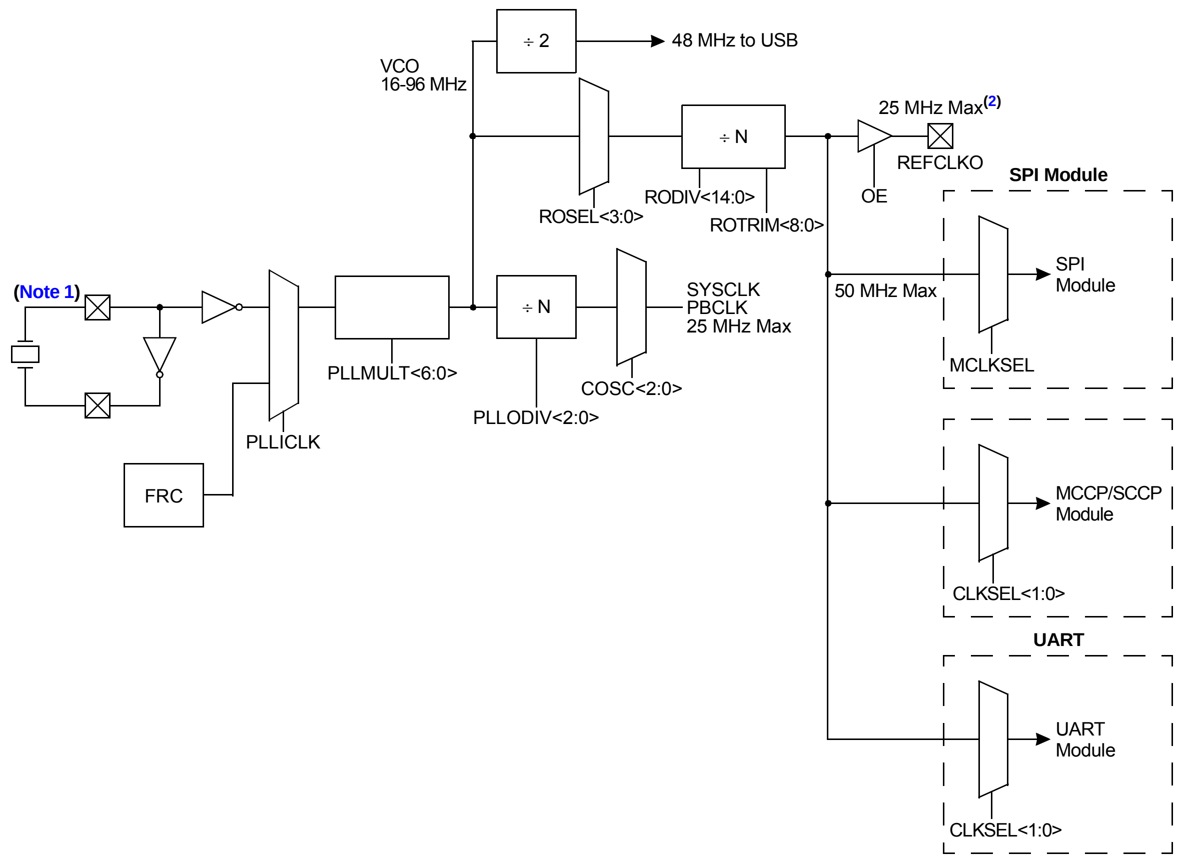
FIGURE 9-2: REFERENCE OSCILLATOR



Note 1: Support circuitry for crystal is not shown.
2: In Retention mode, the maximum peripheral output frequency to an I/O pin must be limited to 33 kHz or less.

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9.4 Oscillator Control Registers

TABLE 9-1: OSCILLATOR CONFIGURATION REGISTER MAP

Virtual Address (BF80_#)	Register Name[2]	Bit Range	Bits 31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets[1]
2680	OSCCON	31:16	—	—	—	—	—	FRCDIV<2:0>			—	—	—	—	—	—	—	—	0000
		15:0	—	COSC<2:0>			—	NOSC<2:0>			CLKLOCK	—	—	SLPEN	CF	—	SOSCEN	OSWEN	xx0x
26A0	SPLLCON	31:16	—	—	—	—	—	PLLODIV<2:0>			—	PLLMULT<6:0>							0001
		15:0	—	—	—	—	—	—	—	—	PLLICLK	r	—	—	—	—	—	—	0000
2720	REFO1CON	31:16	—	RODIV<14:0>															0000
		15:0	ON	—	SIDL	OE	RSLP	—	DIVSWEN	ACTIVE	—	—	—	—	ROSEL<3:0>				0000
2730	REFO1TRIM	31:16	ROTRIM<8:0>									—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
2770	CLKSTAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	r	SPLLRDY	USBRDY	LPRCRDY	SOSCRDY	r	POSCRDY	SPDIVRDY	FRCRDY	0000
2880	OSCTUN	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	r	SIDL	SRC	LOCK	POL	ORNG	ORPOL	—	—	TUN<5:0>						0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'; r = reserved bit. Reset values are shown in hexadecimal.

Note 1: Reset values are dependent on the FOSCSEL Configuration bits and the type of Reset.

2: All registers in this table have corresponding CLR, SET and INV registers at their virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively.

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REGISTER 9-1: OSCCON: OSCILLATOR CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	—	FRCDIV<2:0>		
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	R-y	R-y	R-y	U-0	R/W-y	R/W-y	R/W-y
	—	COSC<2:0>			—	NOSC<2:0>		
7:0	R/W-0	U-0	U-0	R/W-0	R/W-0, HS	U-0	R/W-y	R/W-y
	CLKLOCK	—	—	SLPEN	CF	—	SOSCEN	OSWEN(1)

Legend:	HS = Hardware Settable bit	y = Value set from Configuration bits on POR	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-27 **Unimplemented:** Read as ‘0’

bit 26-24 **FRCDIV<2:0>:** Internal Fast RC (FRC) Oscillator Clock Divider bits
111 = FRC divided by 256
110 = FRC divided by 64
101 = FRC divided by 32
100 = FRC divided by 16
011 = FRC divided by 8
010 = FRC divided by 4
001 = FRC divided by 2
000 = FRC divided by 1 (default setting)

bit 23-15 **Unimplemented:** Read as ‘0’

bit 14-12 **COSC<2:0>:** Current Oscillator Selection bits
111-110 = Reserved (selects internal Fast RC (FRC) Oscillator divided by FRCDIV<2:0> bits (FRCDIV))
101 = Internal Low-Power RC (LPRC) Oscillator
100 = Secondary Oscillator (SOSC)
011 = Reserved
010 = Primary Oscillator (POSC) (XT, HS or EC)
001 = System PLL (SPLL)
000 = Internal Fast RC (FRC) Oscillator divided by FRCDIV<2:0> bits (FRCDIV)

bit 11 **Unimplemented:** Read as ‘0’

bit 10-8 **NOSC<2:0>:** New Oscillator Selection bits
111-110 = Reserved (selects internal Fast RC (FRC) Oscillator divided by FRCDIV<2:0> bits (FRCDIV))
101 = Internal Low-Power RC (LPRC) Oscillator
100 = Secondary Oscillator (SOSC)
011 = Reserved
010 = Primary Oscillator (POSC) (XT, HS or EC)
001 = System PLL (SPLL)
000 = Internal Fast RC (FRC) Oscillator divided by FRCDIV<2:0> bits (FRCDIV)
On Reset, these bits are set to the value of the FNOSC<2:0> Configuration bits (FOSCSEL<2:0>).

Note 1: The Reset value for this bit depends on the setting of the IESO (FOSCSEL<7>) bit. When IESO = 1, the Reset value is ‘1’. When IESO = 0, the Reset value is ‘0’.

Note: Writes to this register require an unlock sequence. Refer to **Section 26.4 “System Registers Write Protection”** for details.

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REGISTER 9-1: OSCCON: OSCILLATOR CONTROL REGISTER (CONTINUED)

bit 7 **CLKLOCK:** Clock Selection Lock Enable bit
1 = Clock and PLL selections are locked
0 = Clock and PLL selections are not locked and may be modified

bit 6-5 **Unimplemented:** Read as '0'

bit 4 **SLPEN:** Sleep Mode Enable bit
1 = Device will enter Sleep mode when a WAIT instruction is executed
0 = Device will enter Idle mode when a WAIT instruction is executed

bit 3 **CF:** Clock Fail Detect bit
1 = FSCM has detected a clock failure
0 = No clock failure has been detected

bit 2 **Unimplemented:** Read as '0'

bit 1 **SOSCEN:** Secondary Oscillator (SOSC) Enable bit
1 = Enables the Secondary Oscillator
0 = Disables the Secondary Oscillator

bit 0 **OSWEN:** Oscillator Switch Enable bit[1]
1 = Initiates an oscillator switch to a selection specified by the NOSC<2:0> bits
0 = Oscillator switch is complete

Note 1: The Reset value for this bit depends on the setting of the IESO (FOSCSEL<7>) bit. When IESO = 1, the Reset value is '1'. When IESO = 0, the Reset value is '0'.

Note: Writes to this register require an unlock sequence. Refer to **Section 26.4 "System Registers Write Protection"** for details.

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REGISTER 9-2: SPLLCON: SYSTEM PLL CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	—	PLLODIV<2:0>		
23:16	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1
	—	PLLMULT<6:0>						
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-y	r-0	U-0	U-0	U-0	U-0	U-0	U-0
	PLLICLK	—	—	—	—	—	—	—

Legend:	r = Reserved bit	y = Values set from Configuration bits on POR	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-27 **Unimplemented:** Read as '0'

bit 26-24 **PLLODIV<2:0>:** System PLL Output Clock Divider bits
111 = PLL divide-by-256
110 = PLL divide-by-64
101 = PLL divide-by-32
100 = PLL divide-by-16
011 = PLL divide-by-8
010 = PLL divide-by-4
001 = PLL divide-by-2
000 = PLL divide-by-1 (default setting)

bit 23 **Unimplemented:** Read as '0'

bit 22-16 **PLLMULT<6:0>:** System PLL Multiplier bits
111111-0000111 = Reserved
0000110 = 24x
0000101 = 12x
0000100 = 8x
0000011 = 6x
0000010 = 4x
0000001 = 3x (default setting)
0000000 = 2x

bit 15-8 **Unimplemented:** Read as '0'

bit 7 **PLLICLK:** System PLL Input Clock Source bit
1 = FRC is selected as the input to the system PLL (not divided)
0 = POSC is selected as the input to the system PLL; the POR default value is specified by the PLLSRC bit
The POR default value is specified by the PLLSRC Configuration bit in the FOSCSEL register. Refer to Register 26-9 in **Section 26.0 "Special Features"** for more information.

bit 6 **Reserved:** Maintain as '0'

bit 5-0 **Unimplemented:** Read as '0'

Note 1: Writes to this register require an unlock sequence. Refer to **Section 26.4 "System Registers Write Protection"** for details.

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REGISTER 9-3: REFO1CON: REFERENCE OSCILLATOR CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	RODIV<14:8>						
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	RODIV<7:0>							
15:8	R/W-0	U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0, HC	R-0, HS, HC
	ON(1)	—	SIDL	OE	RSLP(2)	—	DIVSWEN	ACTIVE(1)
7:0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	ROSEL<3:0>(3)			

Legend:	HC = Hardware Clearable bit	HS = Hardware Settable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31 **Unimplemented:** Read as ‘0’

bit 30-16 **RODIV<14:0>:** Reference Clock Divider bits
The value selects the reference clock divider bits (see Figure 9-1 for details). A value of ‘0’ selects no divider.

bit 15 **ON:** Reference Oscillator Output Enable bit(1)
1 = Reference oscillator module is enabled
0 = Reference oscillator module is disabled

bit 14 **Unimplemented:** Read as ‘0’

bit 13 **SIDL:** Peripheral Stop in Idle Mode bit
1 = Discontinues module operation when device enters Idle mode
0 = Continues module operation in Idle mode

bit 12 **OE:** Reference Clock Output Enable bit
1 = Reference clock is driven out on the REFO1 pin
0 = Reference clock is not driven out on the REFO1 pin

bit 11 **RSLP:** Reference Oscillator Module Run in Sleep bit(2)
1 = Reference oscillator module output continues to run in Sleep
0 = Reference oscillator module output is disabled in Sleep

bit 10 **Unimplemented:** Read as ‘0’

bit 9 **DIVSWEN:** Divider Switch Enable bit
1 = Divider switch is in progress
0 = Divider switch is complete

bit 8 **ACTIVE:** Reference Clock Request Status bit(1)
1 = Reference clock request is active
0 = Reference clock request is not active

bit 7-4 **Unimplemented:** Read as ‘0’

Note 1: Do not write to this register when the ON bit is not equal to the ACTIVE bit.
2: This bit is ignored when the ROSEL<3:0> bits = 0000.
3: The ROSEL<3:0> bits should not be written while the ACTIVE bit is ‘1’, as undefined behavior may result.

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REGISTER 9-3: REFO1CON: REFERENCE OSCILLATOR CONTROL REGISTER (CONTINUED)

bit 3-0 **ROSEL<3:0>:** Reference Clock Source Select bits(3)

1111 = Reserved
•
•
•
0111 = System PLL VCO output (not divided)
0110 = Reserved
0101 = SOSC
0100 = LPRC
0011 = FRC
0010 = POSC
0001 = Reserved
0000 = SYSCLK

Note 1: Do not write to this register when the ON bit is not equal to the ACTIVE bit.
2: This bit is ignored when the ROSEL<3:0> bits = 0000.
3: The ROSEL<3:0> bits should not be written while the ACTIVE bit is '1', as undefined behavior may result.

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REGISTER 9-4: REFO1TRIM: REFERENCE OSCILLATOR TRIM REGISTER[1,2,3]

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ROTRIM<8:1>							
23:16	R/W-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	ROTRIM<0>	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-23 **ROTRIM<8:0>:** Reference Oscillator Trim bits

111111111 = 511/512 divisor added to the RODIVx value
111111110 = 510/512 divisor added to the RODIVx value
•
•
•
100000000 = 256/512 divisor added to the RODIVx value
•
•
•
000000010 = 2/512 divisor added to the RODIVx value
000000001 = 1/512 divisor added to the RODIVx value
000000000 = 0 divisor added to the RODIVx value

bit 22-0 **Unimplemented:** Read as ‘0’

Note 1: While the ON bit (REFO1CON<15>) is ‘1’, writes to this register do not take effect until the DIVSWEN bit is also set to ‘1’.

2: Do not write to this register when the ON bit (REFO1CON<15>) is not equal to the ACTIVE bit (REFO1CON<8>).

3: Specified values in this register do not take effect if RODIV<14:0> (REFO1CON<30:16>) = 0.

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REGISTER 9-5: CLKSTAT: CLOCK STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	r-1
	—	—	—	—	—	—	—	—
7:0	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC	r-0	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC
	SPLLRDY	USBRDY	LPRCRDY	SOSCRDY	—	POSCRDY	SPDIVRDY	FRCRDY

Legend:	HS = Hardware Settable bit	HC = Hardware Clearable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	r = Reserved bit

bit 31-9 **Unimplemented:** Read as ‘0’

bit 8 **Reserved:** Read as ‘1’

bit 7 **SPLLRDY**: PLL Lock bit
1 = PLL is locked and ready
0 = PLL is not locked

bit 6 **USBRDY**: USB Oscillator Ready bit
1 = USB oscillator is running
0 = USB oscillator is not running

bit 5 **LPRCRDY:** LPRC Oscillator Ready bit
1 = LPRC oscillator is enabled
0 = LPRC oscillator is not enabled

bit 4 **SOSCRDY:** Secondary Oscillator (SOSC) Ready bit
1 = SOSC is enabled and the Oscillator Start-up Timer (OST) has expired
0 = SOSC is not enabled or the Oscillator Start-up Timer has not expired

bit 3 **Reserved:** Read as ‘0’

bit 2 **POSCRDY:** Primary Oscillator (POSC) Ready bit
1 = POSC is enabled and the Oscillator Start-up Timer has expired
0 = POSC is not enabled or the Oscillator Start-up Timer has not expired

bit 1 **SPDIVRDY:** System PLL (with postscaler, SPLLDIV) Clock Ready Status bit
1 = SPLLDIV is enabled and the PLL start-up timer has expired
0 = SPLLDIV is not enabled or the PLL start-up timer has not expired

bit 0 **FRCRDY:** Fast RC (FRC) Oscillator Ready bit
1 = FRC oscillator is enabled
0 = FRC oscillator is not enabled

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REGISTER 9-6: OSCTUN: FRC TUNING REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	R-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	r-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ON	—	SIDL	SRC	LOCK	POL	ORNG	ORPOL
7:0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	TUN<5:0>(1)					

Legend:	r = Reserved bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as ‘0’

bit 15 **ON:** Self-Tune Enable bit
1 = FRC self-tuning is enabled; the TUNx bits are controlled by hardware
0 = FRC self-tuning is disabled; the TUNx bits are readable and writable

bit 14 **Reserved:** Used by debugger

bit 13 **SIDL:** FRC Self-Tune Stop in Idle bit
1 = Self-tuning stops during Idle mode
0 = Self-tuning continues during Idle mode

bit 12 **SRC:** FRC Self-Tune Reference Clock Source bit
1 = The USB host clock is used to tune the FRC
0 = The 32.768 kHz SOSC clock is used to tune the FRC

bit 11 **LOCK:** FRC Self-Tune Lock Status bit
1 = FRC accuracy is currently within ±0.2% of the SRC reference accuracy
0 = FRC accuracy may not be within ±0.2% of the SRC reference accuracy

bit 10 **POL:** FRC Self-Tune Lock Interrupt Polarity bit
1 = A self-tune lock interrupt is generated when LOCK is ‘0’
0 = A self-tune lock interrupt is generated when LOCK is ‘1’

bit 9 **ORNG:** FRC Self-Tune Out of Range Status bit
1 = SRC reference clock error is beyond the range of TUN<5:0>; no tuning is performed
0 = SRC reference clock is within the tunable range; tuning is performed

bit 8 **ORPOL:** FRC Self-Tune Out of Range Interrupt Polarity bit
1 = A self-tune out of range interrupt is generated when STOR is ‘0’
0 = A self-tune out of range interrupt is generated when STOR is ‘1’

bit 7-6 **Unimplemented:** Read as ‘0’

Note 1: OSCTUN functionality has been provided to help customers compensate for temperature effects on the FRC frequency over a wide range of temperatures. The tuning step-size is an approximation and is neither characterized, nor tested.

Note: Writes to this register require an unlock sequence. Refer to **Section 26.4 “System Registers Write Protection”** for details.

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REGISTER 9-6: OSCTUN: FRC TUNING REGISTER (CONTINUED)

bit 5-0 **TUN<5:0>:** FRC Oscillator Tuning bits[(1)]

`100000` = Center frequency – 1.50%
`100001` =
•
•
•
`111111` =
`000000` = Center frequency; oscillator runs at a nominal frequency (8 MHz)
`000001` =
•
•
•
`011110` =
`011111` = Center frequency + 1.453%

Note 1: OSCTUN functionality has been provided to help customers compensate for temperature effects on the FRC frequency over a wide range of temperatures. The tuning step-size is an approximation and is neither characterized, nor tested.

Note:	Writes to this register require an unlock sequence. Refer to **Section 26.4 "System Registers Write Protection"** for details.

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NOTES:

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10.0 I/O PORTS

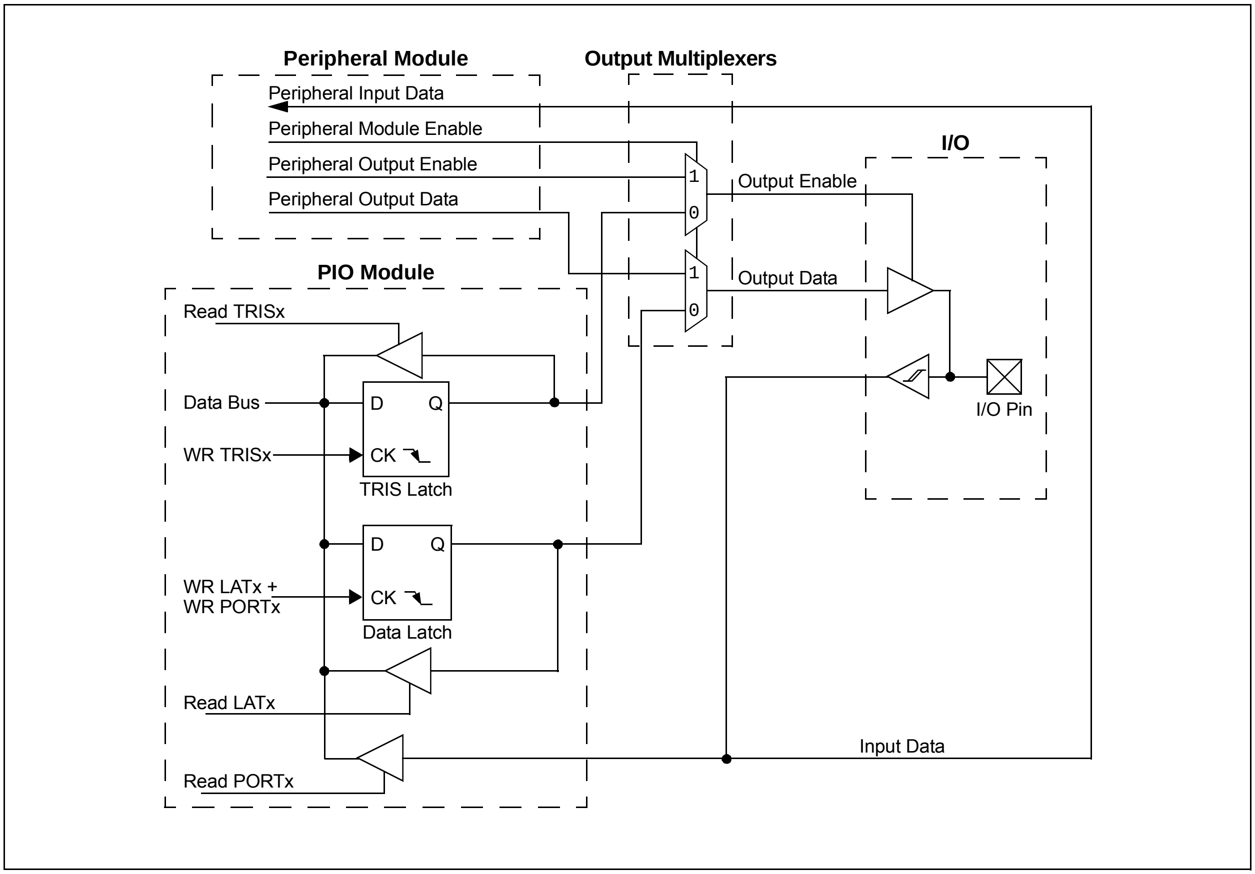
> **Note:** This data sheet summarizes the features of the PIC32MM0256GPM064 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 12. "I/O Ports"** (DS60001120) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32). The information in this data sheet supersedes the information in the FRM.

Many of the device pins are shared among the peripherals and the Parallel I/O (PIO) ports. All I/O input ports feature Schmitt Trigger inputs for improved noise immunity. Some pins in the devices are 5V tolerant pins. Some of the key features of the I/O ports are:

- Individual Output Pin Open-Drain Enable/Disable
- Individual Input Pin Weak Pull-up and Pull-Down
- Monitor Selective Inputs and Generate Interrupt when Change in Pin State is Detected
- Operation during Sleep and Idle modes
- Fast Bit Manipulation using the CLR, SET and INV Registers

Figure 10-1 illustrates a block diagram of a typical multiplexed I/O port.

FIGURE 10-1: BLOCK DIAGRAM OF A TYPICAL SHARED PORT STRUCTURE



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10.1 CLR, SET and INV Registers

Every I/O module register has a corresponding CLR (Clear), SET (Set) and INV (Invert) register designed to provide fast atomic bit manipulations. As the name of the register implies, a value written to a SET, CLR or INV register effectively performs the implied operation, but only on the corresponding base register and only bits specified as '1' are modified. Bits specified as '0' are not modified.

Reading SET, CLR and INV registers returns undefined values. To see the effects of a write operation to a SET, CLR or INV register, the base register must be read.

10.2 Parallel I/O (PIO) Ports

All port pins have 14 registers directly associated with their operation as digital I/Os. The Data Direction register (TRISx) determines whether the pin is an input or an output. If the data direction bit is a '1', then the pin is an input. All port pins are defined as inputs after a Reset. The LATx register controls the pin level when it is configured as an output. Reads from the PORTx register read the port pins, while writes to the port pins write the latch, LATx.

10.3 Open-Drain Configuration

In addition to the PORTx, LATx and TRISx registers for data control, the port pins can also be individually configured for either digital or open-drain outputs. This is controlled by the Open-Drain Control x register, ODCx, associated with each port. Setting any of the bits configures the corresponding pin to act as an open-drain output.

The open-drain feature allows the generation of outputs higher than VDD (e.g., 5V), on any desired 5V tolerant pins, by using external pull-up resistors. The maximum open-drain voltage allowed is the same as the maximum VIH specification.

10.4 Configuring Analog and Digital Port Pins

When the PORTx register is read, all pins configured as analog input channels are read as cleared (a low level).

Pins configured as digital inputs do not convert an analog input. Analog levels on any pin defined as a digital input (including the ANx pins) can cause the input buffer to consume current that exceeds the device specifications. The ANSELx register controls the operation of the analog port pins. The port pins that are to function as analog inputs must have their corresponding ANSELx and TRISx bits set. In order to use port pins for I/O functionality with digital modules, such as timers, UARTs, etc., the corresponding ANSELx bit must be cleared. The ANSELx register has a default value of 0xFFFF. Therefore, all pins that share analog functions are analog (not digital) by default. If the TRISx bit is cleared (output) while the ANSELx bit is set, the digital output level (VOH or VOL) is used by an analog peripheral, such as the ADC or comparator module.

10.5 I/O Port Write/Read Timing

One instruction cycle is required between a port direction change or port write operation and a read operation of the same port. Typically, this instruction would be a NOP.

There is a three-instruction cycle delay in the port read synchronizer. When a port or port bit is read, the returned value is the value that was present on the port three system clocks prior.

10.6 GPIO Port Merging

Port merging creates a 32-bit wide port from two GPIO ports. When the PORT32 bit is set, the next I/O port is mapped to the upper 16 bits of the lower port.

Only the next higher letter port can be merged to a given port (i.e., PORTA can only be merged with PORTB).

Note: All 32 pins may not be available. Refer to the pin diagrams for information regarding GPIO port pin availability.

10.7 Input Change Notification (ICN)

The Input Change Notification function of the I/O ports allows the PIC32MM devices to generate interrupt requests to the processor in response to a Change-of-State (COS) on the input pins. This feature can detect input Change-of-States, even in Sleep mode, when the clocks are disabled. Every I/O port pin can be selected (enabled) for generating an interrupt request on a Change-of-State. Five control registers are associated with the Change Notification (CN) functionality of each I/O port. To enable the Change Notification feature for the port, the ON bit (CNCONx<15>) must be set.

The CNEN0x and CNEN1x registers contain the CN interrupt enable control bits for each of the input pins. The setting of these bits enables a CN interrupt for the corresponding pins. Also, these bits, in combination with the CNSTYLE bit (CNCONx<11>), define a type of transition when the interrupt is generated. Possible CN event options are listed in Table 10-1.

TABLE 10-1: CHANGE NOTIFICATION EVENT OPTIONS

CNSTYLE Bit (CNCONx<11>)	CNEN1x Bit	CNEN0x Bit	Change Notification Event Description
0	Does not matter	0	Disabled
0	Does not matter	1	Detects a mismatch between the last read state and the current state of the pin
1	0	0	Disabled
1	0	1	Detects a positive transition only (from '0' to '1')
1	1	0	Detects a negative transition only (from '1' to '0')
1	1	1	Detects both positive and negative transitions

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The CNSTATx register indicates whether a change occurred on the corresponding pin since the last read of the PORTx bit. In addition to the CNSTATx register, the CNFx register is implemented for each port. This register contains flags for Change Notification events. These flags are set if the valid transition edge, selected in the CNEN0x and CNEN1x registers, is detected. CNFx stores the occurrence of the event. CNFx bits must be cleared in software to get the next Change Notification interrupt. The CN interrupt is generated only for the I/Os configured as inputs (corresponding TRISx bits must be set).

10.8 Pin Pull-up and Pull-Down

Each I/O pin also has a weak pull-up and a weak pull-down connected to it. The pull-ups act as a current source, or sink source, connected to the pin and eliminate the need for external resistors when push button or keypad devices are connected. The pull-ups and pull-downs are enabled separately using the CNPUx and the CNPDx registers, which contain the control bits for each of the pins. Setting any of the control bits enables the weak pull-ups and/or pull-downs for the corresponding pins.

10.9 Peripheral Pin Select (PPS)

A major challenge in general purpose devices is providing the largest possible set of peripheral features while minimizing the conflict of features on I/O pins. The challenge is even greater on low pin count devices. In an application where more than one peripheral needs to be assigned to a single pin, inconvenient work arounds in application code, or a complete redesign, may be the only option.

PPS configuration provides an alternative to these choices by enabling peripheral set selection and their placement on a wide range of I/O pins. By increasing the pinout options available on a particular device, users can better tailor the device to their entire application, rather than trimming the application to fit the device.

The PPS configuration feature operates over a fixed subset of digital I/O pins. Users may independently map the input and/or output of most digital peripherals to these I/O pins. PPS is performed in software and generally does not require the device to be reprogrammed. Hardware safeguards are included that prevent accidental or spurious changes to the peripheral mapping once it has been established.

10.9.1 AVAILABLE PINS

The number of available pins is dependent on the particular device and its pin count. Pins that support the PPS feature include the designation, “RPn”, in their full pin designation, where “RP” designates a Remappable Peripheral and “n” is the remappable port number.

10.9.2 AVAILABLE PERIPHERALS

The peripherals managed by the PPS are all digital only peripherals. These include general serial communications (UART and SPI), general purpose timer clock inputs, timer-related peripherals (MCCP, SCCP) and others.

In comparison, some digital only peripheral modules are never included in the PPS feature. This is because the peripheral’s function requires special I/O circuitry on a specific port and cannot be easily connected to multiple pins. These modules include I^2C among others. A similar requirement excludes all modules with analog inputs, such as the Analog-to-Digital Converter (ADC).

A key difference between remappable and non-remappable peripherals is that remappable peripherals are not associated with a default I/O pin. The peripheral must always be assigned to a specific I/O pin before it can be used. In contrast, non-remappable peripherals are always available on a default pin, assuming that the peripheral is active and not conflicting with another peripheral.

When a remappable peripheral is active on a given I/O pin, it takes priority over all other digital I/Os and digital communication peripherals associated with the pin. Priority is given regardless of the type of peripheral that is mapped. Remappable peripherals never take priority over any analog functions associated with the pin.

10.9.3 CONTROLLING PPS

PPS features are controlled through two sets of SFRs: one to map peripheral inputs and one to map outputs. Because they are separately controlled, a particular peripheral’s input and output (if the peripheral has both) can be placed on any selectable function pin without constraint.

The association of a peripheral to a peripheral-selectable pin is handled in two different ways, depending on whether an input or output is being mapped.

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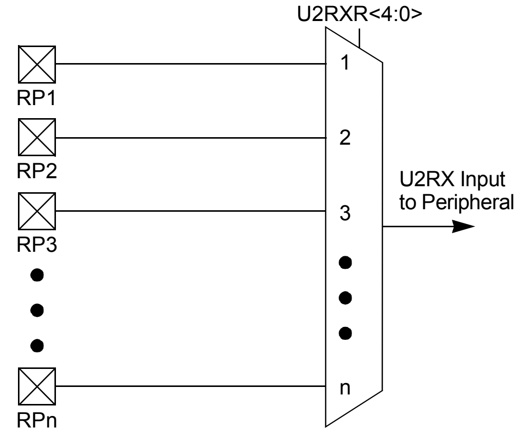
10.9.4 INPUT MAPPING

The inputs of the PPS options are mapped on the basis of the peripheral. That is, a control register associated with a peripheral dictates the pin it will be mapped to. The RPINRx registers (refer to the peripheral pins listed in Table 10-2) are used to configure peripheral input mapping (see Register 10-1). Each register contains sets of 5-bit fields. Programming these bits with a number of the remappable pin will connect the peripheral to this RPn pin (refer to Table 10-3). For any given device, the valid range of values for any bit field is shown in Table 10-2.

For example, Figure 10-2 illustrates the remappable pin selection for the U2RX input.

FIGURE 10-2: REMAPPABLE INPUT EXAMPLE FOR U2RX



Note: For input only, PPS functionality does not have priority over TRISx settings. Therefore, when configuring an RPn pin for input, the corresponding bit in the TRISx register must also be configured for input (set to '1').

TABLE 10-2: INPUT PIN SELECTION

Input Name	Function Name	Register	Function Bits
External Interrupt 4	INT4	RPINR1	INT4R<4:0>
MCCP1 Input Capture	ICM1	RPINR2	ICM1R<4:0>
MCCP2 Input Capture	ICM2	RPINR2	ICM2R<4:0>
MCCP3 Input Capture	ICM3	RPINR3	ICM3R<4:0>
SCCP4 Input Capture	ICM4	RPINR3	ICM4R<4:0>
Output Compare Fault A	OCFA	RPINR5	OCFAR<4:0>
Output Compare Fault B	OCFB	RPINR5	OCFBR<4:0>
CCP Clock Input A	TCKIA	RPINR6	TCKIAR<4:0>
CCP Clock Input B	TCKIB	RPINR6	TCKIBR<4:0>
SCCP5 Input Capture	ICM5	RPINR7	ICM5R<4:0>
SCCP6 Input Capture	ICM6	RPINR7	ICM6R<4:0>
SCCP7 Input Capture	ICM7	RPINR7	ICM7R<4:0>
SCCP8 Input Capture	ICM8	RPINR7	ICM8R<4:0>
SCCP9 Input Capture	ICM9	RPINR8	ICM9R<4:0>
UART3 Receive	U3RX	RPINR8	U3RXR<4:0>
UART2 Receive	U2RX	RPINR9	U2RXR<4:0>
UART2 Clear-to-Send	$\overline{\text{U2CTS}}$	RPINR9	U2CTSR<4:0>
UART3 Clear-to-Send	$\overline{\text{U3CTS}}$	RPINR10	U3CTSR<4:0>
SPI2 Data Input	SDI2	RPINR11	SDI2R<4:0>
SPI2 Clock Input	SCK2IN	RPINR11	SCK2INR<4:0>
SPI2 Slave Select Input	SS2IN	RPINR11	SS2INR<4:0>
CLC Input A	CLCINA	RPINR12	CLCINAR<4:0>
CLC Input B	CLCINB	RPINR12	CLCINBR<4:0>

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TABLE 10-3: REMAPPABLE INPUT SOURCES PIN ASSIGNMENTS[(1)]

Value	RPn Pins	Pin Assignment	Value	RPn Pins	Pin Assignment
00001	RP1	RA0 Pin	01110	RP14	RB9 Pin
00010	RP2	RA1 Pin	01111	RP15	RB13 Pin
00011	RP3	RA2 Pin	10000	RP16	RB14 Pin
00100	RP4	RA3 Pin	10001	RP17	RB15 Pin
00101	RP5	RA4 Pin	10010	RP18	RC9 Pin
00110	RP6	RB0 Pin	10011	RP19	RC2 Pin
00111	RP7	RB1 Pin	10100	RP20	RC7 Pin
01000	RP8	RB2 Pin	10101	RP21	RA7 Pin
01001	RP9	RB3 Pin	10110	RP22	RA10 Pin
01010	RP10	RB4 Pin	10111	RP23	RC6 Pin
01011	RP11	RB5 Pin	11000	RP24	RA9 Pin
01100	RP12	RB7 Pin	11001-11111	Reserved	
01101	RP13	RB8 Pin			

Note 1: All RPx pins are not available on all packages.

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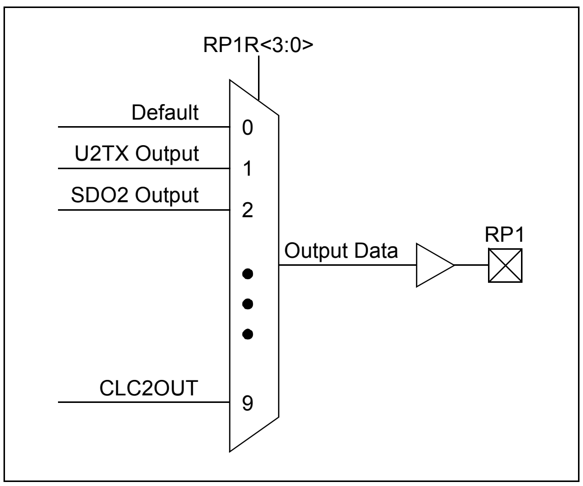
10.9.5 OUTPUT MAPPING

In contrast to inputs, the outputs of the PPS options are mapped on the basis of the pin. In this case, a control register associated with a particular pin dictates the peripheral output to be mapped. The RPORx registers are used to control output mapping. Like the RPINRx registers, each register contains sets of 4-bit fields. The value of the bit field corresponds to one of the peripherals and that peripheral's output is mapped to the pin (see Table 10-4 and Figure 10-3).

A null output is associated with the output register Reset value of '0'. This is done to ensure that remappable outputs remain disconnected from all output pins by default.

FIGURE 10-3: EXAMPLE OF MULTIPLEXING OF REMAPPABLE OUTPUT FOR RP0



10.9.6 CONTROLLING CONFIGURATION CHANGES

Because peripheral remapping can be changed during run time, some restrictions on peripheral remapping are needed to prevent accidental configuration changes. PIC32MM0256GPM064 family devices include two features to prevent alterations to the peripheral map:

- Control register lock sequence
- Configuration bit select lock

10.9.6.1 Control Register Lock

Under normal operation, writes to the RPORx and RPINRx registers are not allowed. Attempted writes appear to execute normally, but the contents of the registers remain unchanged. To change these registers, they must be unlocked in hardware. The register lock is controlled by the IOLOCK bit in the RPCON register. Clearing IOLOCK prevents writes to the control registers; setting IOLOCK allows writes.

To set or clear the IOLOCK bit, an unlock sequence must be executed. Refer to **Section 26.4 "System Registers Write Protection"** for details.

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TABLE 10-4: OUTPUT PIN SELECTION

Output Function Number	Function	Output Name
0	None	Not Connected
1	C1OUT	Comparator 1 Output
2	C2OUT	Comparator 2 Output
3	C3OUT	Comparator 3 Output
4	U2TX	UART2 Transmit
5	$\overline{\text{U2RTS}}$	UART2 Request-to-Send
6	U3TX	UART3 Transmit
7	$\overline{\text{U3RTS}}$	UART3 Request-to-Send
8	SDO2	SPI2 Data Output
9	SCK2OUT	SPI2 Clock Output
10	SS2OUT	SPI2 Slave Select Output
11	OCM4	SCCP4 Output Compare Output
12	OCM5	SCCP5 Output Compare Output
13	OCM6	SCCP6 Output Compare Output
14	OCM7	SCCP7 Output Compare Output
15	OCM8	SCCP8 Output Compare Output
16	OCM9	SCCP9 Output Compare Output
17	CLC1OUT	CLC1 Output
18	CLC2OUT	CLC2 Output
19	CLC3OUT	CLC3 Output
20	CLC4OUT	CLC4 Output

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10.10 I/O Ports Control Registers

TABLE 10-5: PORTA REGISTER MAP

Virtual Address (BF80_#)	Register Name[1]	Bit Range	Bits 31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
2BB0	ANSELA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	ANSA<13:11>[2]			—	—	—	—	ANSA6[2]	—	—	ANSA<3:0>				000F
2BC0	TRISA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TRISA<15:0>[3]																021F
2BD0	PORTA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	RA<15:0>[3]																xxxx
2BE0	LATA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	LATA<15:0>[3]																0000
2BF0	ODCA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ODCA<15:0>[3]																0000
2C00	CNPUA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNPUA<15:0>[3]																0000
2C10	CNPDA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNPDA<15:0>[4]																0000
2C20	CNCONA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	CNSTYLE	PORT32	—	—	—	—	—	—	—	—	—	—	0000
2C30	CNEN0A	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNIE0A<15:0>[3]																0000
2C40	CNSTATA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNSTATA<15:0>[3]																0000
2C50	CNEN1A	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNIE1A<15:0>[3]																0000
2C60	CNFA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNFA<15:0>[3]																0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively.

2: These bits are not available on 48, 36 or 28-pin devices.

3: Bits<14:11> are not available on 48-pin devices; bits<15:10> and bits<8:5> are not available on 36-pin devices.

4: Bits<15:5> are not available on 28-pin devices.

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TABLE 10-6: PORTB REGISTER MAP

Virtual Address (BF80_#)	Register Name[1]	Bit Range	Bits 31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
2CB0	ANSELB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	ANSB<13:11>[2]			—	—	—	—	ANSB6[2]	—	ANSB<4:0>					E01F
2CC0	TRISB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TRISB<15:0>																FFFF
2CD0	PORTB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	RB<15:0>																0000
2CE0	LATB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	LATB<15:0>																0000
2CF0	ODCB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ODCB<15:0>																0000
2D00	CNPUB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNPUB<15:0>																0000
2D10	CNPDB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNPDB<15:0>																0000
2D20	CNCONB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	CNSTYLE	PORT32	—	—	—	—	—	—	—	—	—	—	0000
2D30	CNEN0B	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNIE0B<15:0>																0000
2D40	CNSTATB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNSTATB<15:0>																0000
2D50	CNEN1B	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNIE1B<15:0>																0000
2D60	CNFB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNFB<15:0>																0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively.

2: The ANSB<13:11> and ANSB6 bits are not available on 48, 36 or 28-pin devices.

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TABLE 10-7: PORTC REGISTER MAP

Virtual Address (BF80_#)	Register Name[1]	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
2DB0	ANSELC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	ANSC8[2]	—	—	ANSC5[2]	—	—	—	ANSC<1:0>[2]		0003
2DC0	TRISC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TRISC<15:0>[3]																FFFF
2DD0	PORTC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	RC<15:0>[3]																0000
2DE0	LATC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	LATC<15:0>[3]																0000
2DF0	ODCC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ODCC<15:0>[3]																0000
2E00	CNPUC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNPUC<15:0>[3]																0000
2E10	CNPDC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNPDC<15:0>[3]																0000
2E20	CNCONC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	CNSTYLE	PORT32	—	—	—	—	—	—	—	—	—	—	0000
2E30	CNEN0C	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNIE0C<15:0>[3]																0000
2E40	CNSTATC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNSTATC<15:0>[3]																0000
2E50	CNEN1C	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNIE1C<15:0>[3]																0000
2E60	CNFC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CNFC<15:0>[3]																0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively.

2: Bit<8> is not available on 28-pin devices; bit<5> is not available on 36 or 28-pin devices; bits<1:0> are not available on 28-pin devices.

3: Bits<15:13> and bits<11:10> are not available on 48-pin devices; bits<15:10> and bits<7:5> are not available on 36-pin devices; bits<15:10> and bits<8:0> are not available on 28-pin devices.

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TABLE 10-8: PORTD REGISTER MAP

Virtual Address (BF80_#)	Register Name[2]	Bit Range	Bits 31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
2EB0	ANSELD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
2EC0	TRISD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	TRISD<3:0>[1]				030F
2ED0	PORTD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RD<3:0>[1]				0000
2EE0	LATD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	LATD<3:0>[1]				0000
2EF0	ODCD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	ODCD<3:0>[1]				0000
2F00	CNPUD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	CNPUD<3:0>[1]				0000
2F10	CNPDD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	CNPDD<3:0>[1]				0000
2F20	CNCOND	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	—	CNSTYLE	PORT32	—	—	—	—	—	—	—	—	—	—	0000
2F30	CNEN0D	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	CNIE0D<3:0>[1]				0000
2F40	CNSTATD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	CNSTATD<3:0>[1]				0000
2F50	CNEN1D	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	CNIE1D<3:0>[1]				0000
2F60	CNFD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	CNFD<3:0>[1]				0000
2F70	SR0D	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	SR0D<3:0>[1]				0000
2F80	SR1D	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	SR1D<3:0>[1]				0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: Bits<3:1> are not available on 48-pin devices; bits are not available on 36 and 28-pin devices.

2: All registers in this table have corresponding CLR, SET and INV registers at their virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively.

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TABLE 10-9: PERIPHERAL PIN SELECT REGISTER MAP

Virtual Address (BF80_#)	Register Name[1]	Bit Range	Bits 31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
2A00	RPCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	IOLOCK	—	—	—	—	—	—	—	—	—	—	—	0000
2A20	RPINR1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0												INT4R<4:0>					0000
2A30	RPINR2	31:16	—	—	—	ICM2R<4:0>					—	—	—	ICM1R<4:0>					0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
2A40	RPINR3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	ICM3R<4:0>					0000
2A60	RPINR5	31:16	—	—	—	OCFBR<4:0>					—	—	—	OCFAR<4:0>					0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
2A70	RPINR6	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	TCKIBR<4:0>					—	—	—	TCKIAR<4:0>					0000
2A80	RPINR7	31:16	—	—	—	ICM8R<4:0>					—	—	—	ICM7R<4:0>					0000
		15:0	—	—	—	ICM6R<4:0>					—	—	—	ICM5R<4:0>					0000
2A90	RPINR8	31:16	—	—	—	U3RXR<4:0>					—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	ICM9R<4:0>					0000
2AA0	RPINR9	31:16	—	—	—	U2CTSR<4:0>					—	—	—	U2RXR<4:0>					0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
2AB0	RPINR10	31:16	—	—	—	U3RTSR<4:0>					—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
2AC0	RPINR11	31:16	—	—	—	—	—	—	—	—	—	—	—	SS2INR<4:0>					0000
		15:0	—	—	—	SCK2INR<4:0>					—	—	—	SDI2R<4:0>					0000
2AD0	RPINR12	31:16	—	—	—	CLCINBR<4:0>					—	—	—	CLCINAR<4:0>					0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
2B10	RPOR0	31:16	—	—	—	RP4R<4:0>					—	—	—	RP3R<4:0>					0000
		15:0	—	—	—	RP2R<4:0>					—	—	—	RP1R<4:0>					0000
2B20	RPOR1	31:16	—	—	—	RP8R<4:0>					—	—	—	RP7R<4:0>					0000
		15:0	—	—	—	RP6R<4:0>					—	—	—	RP5R<4:0>					0000
2B30	RPOR2	31:16	—	—	—	RP12R<4:0>					—	—	—	RP11R<4:0>					0000
		15:0	—	—	—	RP10R<4:0>					—	—	—	RP9R<4:0>					0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively.

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TABLE 10-9: PERIPHERAL PIN SELECT REGISTER MAP (CONTINUED)

Virtual Address (BF80_#)	Register Name(1)	Bit Range	Bits 31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
2B40	RPOR3	31:16	—	—	—	RP16R<4:0>					—	—	—	RP15R<4:0>					0000
		15:0	—	—	—	RP14R<4:0>					—	—	—	RP13R<4:0>					0000
2B50	RPOR4	31:16	—	—	—	RP20R<4:0>					—	—	—	RP19R<4:0>					0000
		15:0	—	—	—	RP18R<4:0>					—	—	—	RP17R<4:0>					0000
2B60	RPOR5	31:16	—	—	—	RP24R<4:0>					—	—	—	RP23R<4:0>					0000
		15:0	—	—	—	RP22R<4:0>					—	—	—	—	—	—	—	—	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively.

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REGISTER 10-1: CNCONx: CHANGE NOTIFICATION CONTROL FOR PORTx REGISTER (x = A-D)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0	U-0	U-0
	ON	—	—	—	CNSTYLE	PORT32	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as ‘0’

bit 15 **ON:** Change Notification (CN) Control On bit
1 = CN is enabled
0 = CN is disabled

bit 14-12 **Unimplemented:** Read as ‘0’

bit 11 **CNSTYLE:** Change Notification Style Selection bit
1 = Edge style (detects edge transitions, CNFx bits are used for a Change Notice event)
0 = Mismatch style (detects change from last port read, CNSTATx bits are used for a Change Notification event)

bit 10 **PORT32:** Merge Ports bit
Maps the next higher GPIO’s control and status registers to the upper half, bits<31:16>, of this port.
1 = Merging of this port and the next port is enabled
0 = Merging is disabled; all ports are accessed through their registers

bit 9-0 **Unimplemented:** Read as ‘0’

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11.0 TIMER1

> **Note:** This data sheet summarizes the features of the PIC32MM0256GPM064 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 14. "Timers"** (DS60001105) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32). The information in this data sheet supersedes the information in the FRM.

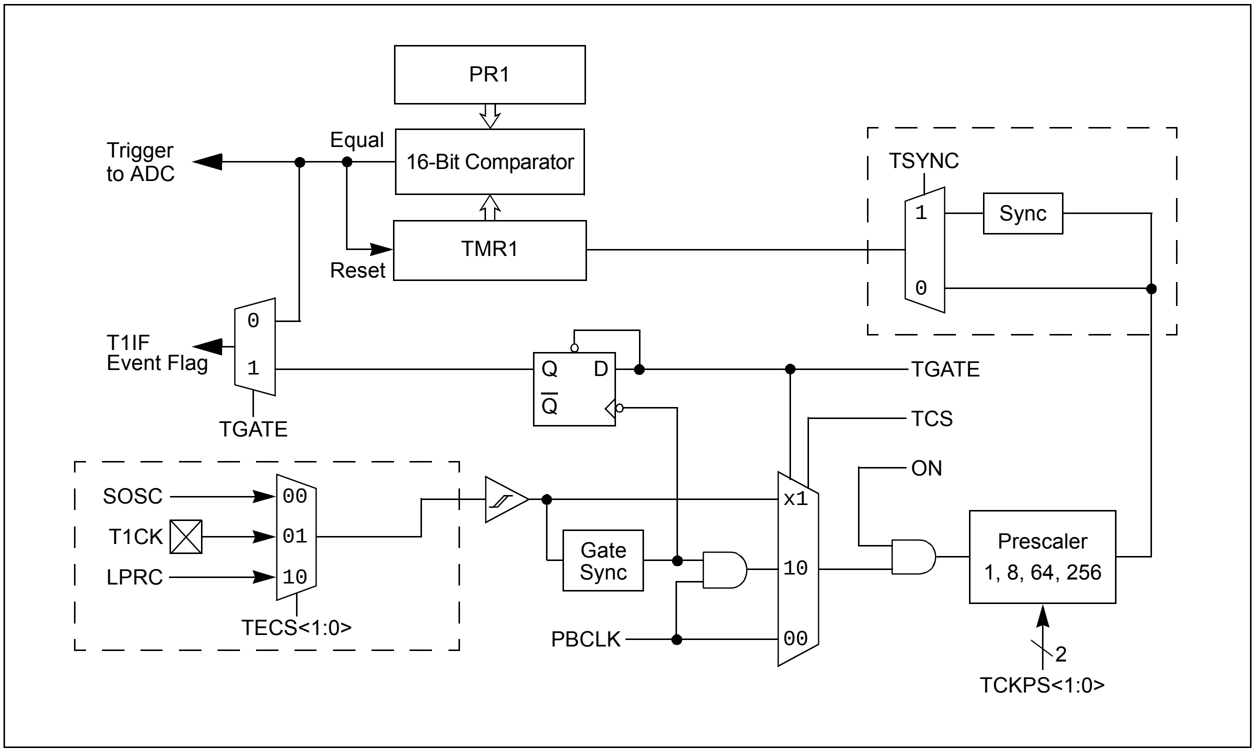
PIC32MM0256GPM064 family devices feature one synchronous/asynchronous 16-bit timer that can operate as a free-running interval timer for various timing applications and counting external events. This timer can be clocked from different sources, such as the Peripheral Bus Clock (PBCLK), Secondary Oscillator (SOSC), T1CK pin or LPRC oscillator.

The following modes are supported by Timer1:

- Synchronous Internal Timer
- Synchronous Internal Gated Timer
- Synchronous External Timer
- Asynchronous External Timer

The timer has a selectable clock prescaler and can operate in Sleep and Idle modes.

FIGURE 11-1: TIMER1 BLOCK DIAGRAM



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11.1 Timer1 Control Register

TABLE 11-1: TIMER1 REGISTER MAP

Virtual Address (BF80_#)	Register Name[1]	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
8000	T1CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	TWDIS	TWIP	—	TECS<1:0>		TGATE	—	TCKPS<1:0>		—	TSYNC	TCS	—	0000
8010	TMR1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TMR1<15:0>																0000
8020	PR1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PR1<15:0>[2]																FFFF

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively.

2: PR1 values of '0' and '1' are reserved.

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REGISTER 11-1: T1CON: TIMER1 CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	R/W-0	R/W-0	R-0	U-0	R/W-0	R/W-0
	ON	—	SIDL	TWDIS	TWIP	—	TECS<1:0>	
7:0	R/W-0	U-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	U-0
	TGATE	—	TCKPS<1:0>		—	TSYNC	TCS	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as ‘0’

bit 15 **ON:** Timer1 On bit
1 = Timer1 is enabled
0 = Timer1 is disabled

bit 14 **Unimplemented:** Read as ‘0’

bit 13 **SIDL:** Timer1 Stop in Idle Mode bit
1 = Discontinues operation when device enters Idle mode
0 = Continues operation even in Idle mode

bit 12 **TWDIS:** Asynchronous Timer1 Write Disable bit
1 = Writes to TMR1 are ignored until pending write operation completes
0 = Back-to-back writes are enabled (Legacy Asynchronous Timer mode functionality)

bit 11 **TWIP:** Asynchronous Timer1 Write in Progress bit
In Asynchronous Timer1 mode:
1 = Asynchronous write to TMR1 register is in progress
0 = Asynchronous write to TMR1 register is complete
In Synchronous Timer1 mode:
This bit is read as ‘0’.

bit 10 **Unimplemented:** Read as ‘0’

bit 9-8 **TECS<1:0>:** Timer1 External Clock Selection bits
11 = Reserved
10 = External clock comes from the LPRC
01 = External clock comes from the T1CK Pin
00 = External clock comes from the Secondary Oscillator (SOSC)

bit 7 **TGATE:** Timer1 Gated Time Accumulation Enable bit
When TCS = 1:
This bit is ignored.
When TCS = 0:
1 = Gated time accumulation is enabled
0 = Gated time accumulation is disabled

bit 6 **Unimplemented:** Read as ‘0’

bit 5-4 **TCKPS<1:0>:** Timer1 Input Clock Prescale Select bits
11 = 1:256 prescale value
10 = 1:64 prescale value
01 = 1:8 prescale value
00 = 1:1 prescale value

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REGISTER 11-1: T1CON: TIMER1 CONTROL REGISTER (CONTINUED)

bit 3 **Unimplemented:** Read as '0'

bit 2 **TSYNC:** Timer1 External Clock Input Synchronization Selection bit

When TCS = 1:
1 = External clock input is synchronized
0 = External clock input is not synchronized

When TCS = 0:
This bit is ignored.

bit 1 **TCS:** Timer1 Clock Source Select bit

1 = External clock is defined by the TECS<1:0> bits
0 = Internal peripheral clock

bit 0 **Unimplemented:** Read as '0'

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12.0 TIMER2 AND TIMER3

Note: This data sheet summarizes the features of the PIC32MM0256GPM064 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 14. "Timers"** (DS60001105) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32). The information in this data sheet supersedes the information in the FRM.

This family of PIC32 devices features four synchronous 16-bit timers (default) that can operate as a free-running interval timer for various timing applications and counting external events. The following modes are supported:

- Synchronous Internal 16-Bit Timer
- Synchronous Internal 16-Bit Gated Timer
- Synchronous External 16-Bit Timer

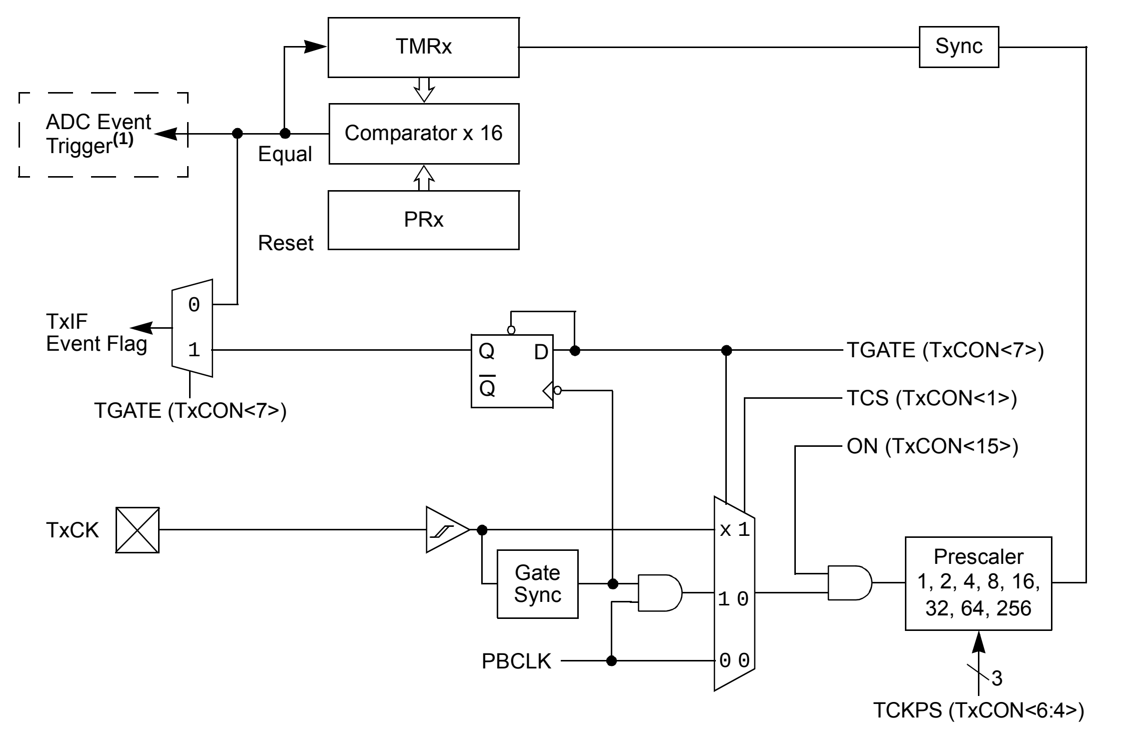
A single 32-bit synchronous timer is available by combining Timer2 with Timer3. The resulting 32-bit timer can operate in three modes:

- Synchronous Internal 32-Bit Timer
- Synchronous Internal 32-Bit Gated Timer
- Synchronous External 32-Bit

12.1 Additional Supported Features

- Selectable Clock Prescaler
- Timers Operational during CPU Idle
- ADC Event Trigger (only Timer3)
- Fast Bit Manipulation using CLR, SET and INV Registers

FIGURE 12-1: TIMER2 AND TIMER3 BLOCK DIAGRAM (TYPE A, 16-BIT)



Note 1: ADC Event Trigger is only available on Timer3.

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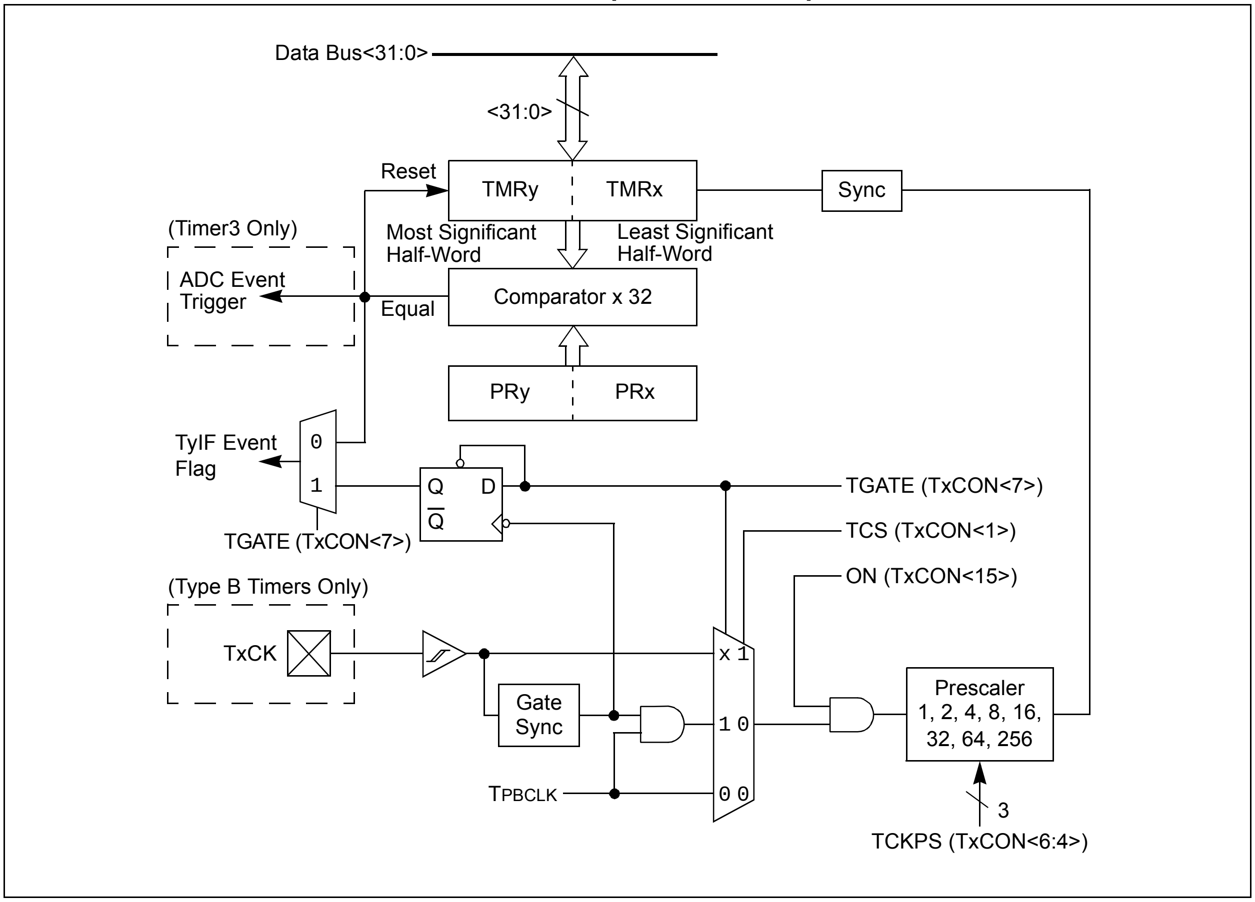
FIGURE 12-2: TIMER2/3 BLOCK DIAGRAM (TYPE B, 32-BIT)



Note: The timer configuration bit, T32 (T2CON<3>), must be set to '1' for a 32-bit timer/counter operation. All control bits are respective to the T2CON register and interrupt bits are respective to the T3CON register.

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12.2 Timer2/3 Control Registers

TABLE 12-1: TIMER2/3 REGISTER MAP

Virtual Address (BF80_#)	Register Name[1]	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
8040	T2CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	TGATE	TCKPS<2:0>			T32	—	TCS	—	0000
8050	TMR2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TMR2<15:0>																0000
8060	PR2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PR2<15:0>[2]																FFFF
8080	T3CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	TGATE	TCKPS<2:0>			—	—	TCS	—	0000
8090	TMR3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TMR3<15:0>																0000
80A0	PR3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PR3<15:0>[2]																FFFF

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively.

2: PR2 and PR3 values of '0' and '1' are reserved.

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12.3 Control Register

REGISTER 12-1: T2CON: TIMER2 CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
	ON[1,3]	—	SIDL[4]	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	U-0
	TGATE[3]	TCKPS<2:0>[3]			T32[2]	—	TCS[3]	—

Legend:
R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Timer2 On bit[1,3]
1 = Module is enabled
0 = Module is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Timer2 Stop in Idle Mode bit[4]
1 = Discontinues operation when device enters Idle mode
0 = Continues operation when device is in Idle mode

bit 12-8 **Unimplemented:** Read as '0'

bit 7 **TGATE:** Timer Gated Time Accumulation Enable bit[3]
When TCS = 1:
This bit is ignored and is read as '0'.
When TCS = 0:
1 = Gated time accumulation is enabled
0 = Gated time accumulation is disabled

bit 6-4 **TCKPS<2:0>:** Timer Input Clock Prescale Select bits[3]
111 = 1:256 prescale value
110 = 1:64 prescale value
101 = 1:32 prescale value
100 = 1:16 prescale value
011 = 1:8 prescale value
010 = 1:4 prescale value
001 = 1:2 prescale value
000 = 1:1 prescale value

Note 1: The user's software should not read/write the peripheral SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.
2: This bit is only available on even numbered timers (Timer2).
3: While operating in 32-bit mode, this bit has no effect for odd numbered timers (Timer1). All timer functions are set through the even numbered timers.
4: While operating in 32-bit mode, this bit must be cleared on odd numbered timers to enable the 32-bit timer in Idle mode.

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REGISTER 12-1: T2CON: TIMER2 CONTROL REGISTER (CONTINUED)

bit 3 **T32:** 32-Bit Timer Mode Select bit(2)
1 = Odd numbered and even numbered timers form a 32-bit timer
0 = Odd numbered and even numbered timers form a separate 16-bit timer

bit 2 **Unimplemented:** Read as ‘0’

bit 1 **TCS:** Timer Clock Source Select bit(3)
1 = External clock from T2CK pin
0 = Internal peripheral clock

bit 0 **Unimplemented:** Read as ‘0’

Note 1: The user’s software should not read/write the peripheral SFRs in the SYSCLK cycle immediately following the instruction that clears the module’s ON bit.
2: This bit is only available on even numbered timers (Timer2).
3: While operating in 32-bit mode, this bit has no effect for odd numbered timers (Timer1). All timer functions are set through the even numbered timers.
4: While operating in 32-bit mode, this bit must be cleared on odd numbered timers to enable the 32-bit timer in Idle mode.

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REGISTER 12-2: T3CON: TIMER3 CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
	ON	—	SIDL	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0	U-0
	TGATE	TCKPS<2:0>			—	—	TCS	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Timer3 On bit
1 = Timer3 is enabled
0 = Timer3 is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Timer3 Stop in Idle Mode bit
1 = Discontinues operation when device enters Idle mode
0 = Continues operation even in Idle mode

bit 12-8 **Unimplemented:** Read as '0'

bit 7 **TGATE:** Timer3 Gated Time Accumulation Enable bit
When TCS = 1:
This bit is ignored.
When TCS = 0:
1 = Gated time accumulation is enabled
0 = Gated time accumulation is disabled

bit 6-4 **TCKPS<2:0>:** Timer3 Input Clock Prescale Select bits
111 = 1:256 prescale value
110 = 1:64 prescale value
101 = 1:32 prescale value
100 = 1:16 prescale value
011 = 1:8 prescale value
010 = 1:4 prescale value
001 = 1:2 prescale value
000 = 1:1 prescale value

bit 3-2 **Unimplemented:** Read as '0'

bit 1 **TCS:** Timer3 Clock Source Select bit
1 = External clock is from the T3CK pin
0 = Internal peripheral clock

bit 0 **Unimplemented:** Read as '0'

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13.0 WATCHDOG TIMER (WDT)

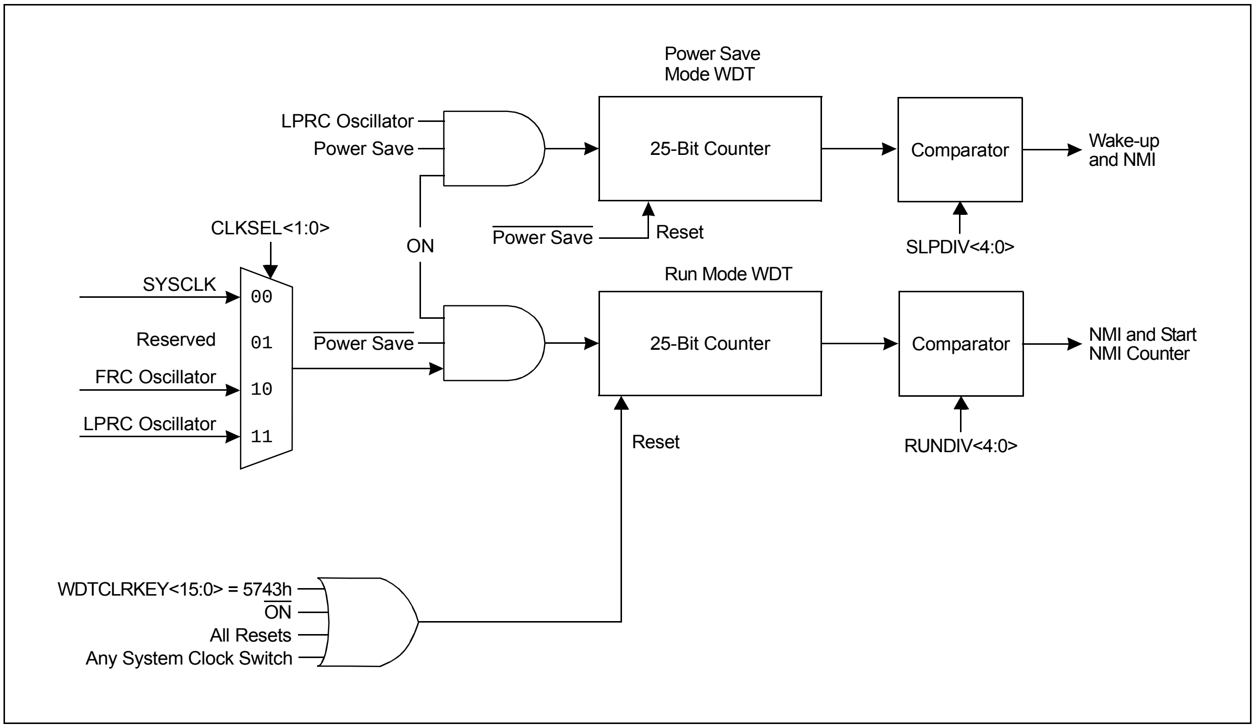
Note:	This data sheet summarizes the features of the PIC32MM0256GPM064 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 62. "Dual Watchdog Timer"** (DS60001365) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32). The information in this data sheet supersedes the information in the FRM.

When enabled, the Watchdog Timer (WDT) can be used to detect system software malfunctions by resetting the device if the WDT is not cleared periodically in software. Various WDT time-out periods can be selected using the WDT postscaler. The WDT can also be used to wake the device from Sleep or Idle mode.

Some of the key features of the WDT module are:

- Configuration or Software Controlled
- User-Configurable Time-out Period
- Different Time-out Periods for Run and Sleep/Idle modes
- Operates from LPRC Oscillator in Sleep/Idle modes
- Different Clock Sources for Run mode
- Can Wake the Device from Sleep or Idle

FIGURE 13-1: WATCHDOG TIMER BLOCK DIAGRAM



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13.1 Watchdog Timer Control Registers

TABLE 13-1: WATCHDOG TIMER REGISTER MAP

Virtual Address (BF80_#)	Register Name	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
3990	WDTCON[1]	31:16	WDTCLRKEY<15:0>																0000
		15:0	ON	—	—	RUNDIV<4:0>					CLKSEL<1:0>		SLPDIV<4:0>					WDTWINEN	xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register has corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively.

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REGISTER 13-1: WDTCON: WATCHDOG TIMER CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0
	WDTCLRKEY<15:8>							
23:16	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0
	WDTCLRKEY<7:0>							
15:8	R/W-0	U-0	U-0	R-y	R-y	R-y	R-y	R-y
	ON(1)	—	—	RUNDIV<4:0>				
7:0	R-y	R-y	R-y	R-y	R-y	R-y	R-y	R/W-y
	CLKSEL<1:0>		SLPDIV<4:0>					WDTWINEN

Legend:	y = Values set from Configuration bits on Reset		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-16 **WDTCLRKEY<15:0>:** Watchdog Timer Clear Key bits
To clear the Watchdog Timer to prevent a time-out, software must write the value, 0x5743, to the upper 16 bits of this register address using a single 16-bit write.

bit 15 **ON:** Watchdog Timer Enable bit(1)
1 = The WDT is enabled
0 = The WDT is disabled

bit 14-13 **Unimplemented:** Read as ‘0’

bit 12-8 **RUNDIV<4:0>:** Shadow Copy of Watchdog Timer Postscaler Value for Run Mode from Configuration bits
On Reset, these bits are set to the values of the RWDTPS<4:0> Configuration bits in FWDT.

bit 7-6 **CLKSEL<1:0>:** Shadow Copy of Watchdog Timer Clock Selection Value for Run Mode from Configuration bits
On Reset, these bits are set to the values of the RCLKSEL<1:0> Configuration bits in FWDT.

bit 5-1 **SLPDIV<4:0>:** Shadow Copy of Watchdog Timer Postscaler Value for Sleep/Idle Mode from Configuration bits
On Reset, these bits are set to the values of the SWDTPS<4:0> Configuration bits in FWDT.

bit 0 **WDTWINEN:** Watchdog Timer Window Enable bit
On Reset, this bit is set to the inverse of the value of the WINDIS Configuration bit in FWDT.
1 = Windowed mode is enabled
0 = Windowed mode is disabled

Note 1: This bit only has control when FWDTEN (FWDT<15>) = 0.

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NOTES:

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14.0 CAPTURE/COMPARE/PWM/ TIMER MODULES (MCCP AND SCCP)

Note: This data sheet summarizes the features of the PIC32MM0256GPM064 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 30. "Capture/Compare/PWM/ Timer (MCCP and SCCP)"** (DS60001381) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32). The information in this data sheet supersedes the information in the FRM.

14.1 Introduction

PIC32MM0256GPM064 family devices include nine Capture/Compare/PWM/Timer (CCP) modules. These modules are similar to the multipurpose timer modules found on many other 32-bit microcontrollers. They also provide the functionality of the comparable input capture, output compare and general purpose timer peripherals found in all earlier PIC32 devices.

CCP modules can operate in one of three major modes:

- General Purpose Timer
- Input Capture
- Output Compare/PWM

There are two different forms of the module, distinguished by the number of PWM outputs that the module can generate. Single Capture/Compare/PWM/Timer (SCCPs) output modules provide only one PWM output. Multiple Capture/Compare/PWM/Timer (MCCPs) output modules can provide up to six outputs and an extended range of output control features, depending on the pin count of the particular device.

All modules (SCCP and MCCP) include these features:

- User-Selectable Clock Inputs, including System Clock and External Clock Input Pins
- Input Clock Prescaler for Time Base
- Output Postscaler for module Interrupt Events or Triggers
- Synchronization Output Signal for coordinating other MCCP/SCCP modules with User-Configurable Alternate and Auxiliary Source Options
- Fully Asynchronous Operation in all modes and in Low-Power Operation
- Special Output Trigger for ADC Conversions
- 16-Bit and 32-Bit General Purpose Timer modes with Optional Gated Operation for Simple Time Measurements
- Capture modes:
    - Backward compatible with previous input capture peripherals of the PIC32 family
    - 16-bit or 32-bit capture of time base on external event
    - Up to four-level deep FIFO capture buffer
    - Capture source input multiplexer
    - Gated capture operation to reduce noise-induced false captures
- Output Compare/PWM modes:
    - Backward compatible with previous output compare peripherals of the PIC32 family
    - Single Edge and Dual Edge Compare modes
    - Center-Aligned Compare mode
    - Variable Frequency Pulse mode
    - External Input mode

MCCP modules also include these extended PWM features:

- Single Output Steerable mode
- Brush DC Motor (Forward and Reverse) modes
- Half-Bridge with Dead-Time Delay mode
- Push-Pull PWM mode
- Output Scan mode
- Auto-Shutdown with Programmable Source and Shutdown State
- Programmable Output Polarity

The SCCP and MCCP modules can be operated in only one of the three major modes (Capture, Compare or Timer) at any time. The other modes are not available unless the module is reconfigured.

A conceptual block diagram for the module is shown in Figure 14-1. All three modes use the time base generator and the common Timer register pair (CCPxTMR). Other shared hardware components, such as comparators and buffer registers, are activated and used as a particular mode requires.

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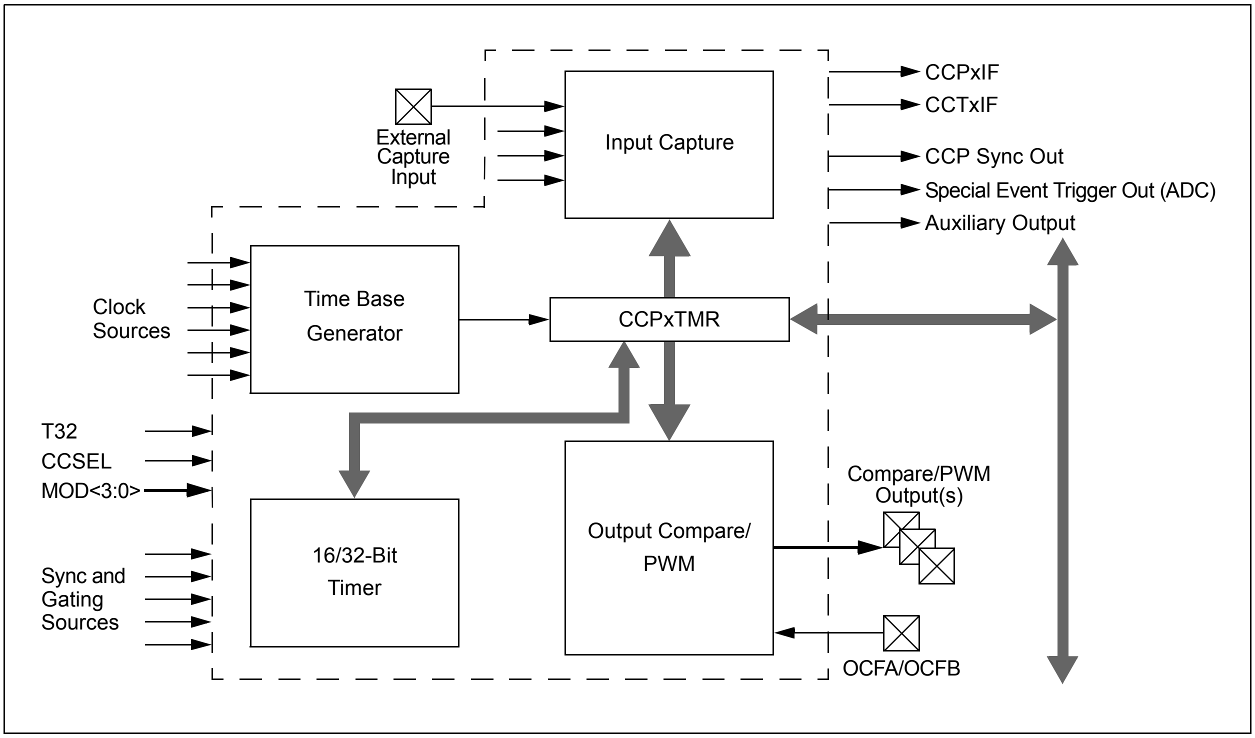
FIGURE 14-1: MCCP/SCCP CONCEPTUAL BLOCK DIAGRAM



14.2 Registers

Each MCCP/SCCP module has up to seven control and status registers:

- CCPxCON1 (Register 14-1) controls many of the features common to all modes, including input clock selection, time base prescaling, timer synchronization, Trigger mode operations and postscaler selection for all modes. The module is also enabled and the operational mode is selected from this register.
- CCPxCON2 (Register 14-2) controls auto-shutdown and restart operation, primarily for PWM operations, and also configures other input capture and output compare features, and configures auxiliary output operation.
- CCPxCON3 (Register 14-3) controls multiple output PWM dead time, controls the output of the output compare and PWM modes, and configures the PWM Output mode for the MCCP modules.
- CCPxSTAT (Register 14-4) contains read-only status bits showing the state of module operations.

Each module also includes eight buffer/counter registers that serve as Timer Value registers or data holding buffers:

- CCPxTMR is the 32-Bit Timer/Counter register
- CCPxPR is the 32-Bit Timer Period register
- CCPxR is the 32-bit primary data buffer for output compare operations
- CCPxBUF(H/L) is the 32-Bit Buffer register pair, which is used in input capture FIFO operations

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TABLE 14-1: MCCP/SCCP REGISTER MAP

Virtual Address (BF80_#)	Register Name[1]	Bit Range	Bits 31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
0100	CCP1CON1	31:16	OPSSRC	RTRGEN	—	—	OPS<3:0>				TRIGEN	ONESHOT	ALTSYNC	SYNC<4:0>					0000
		15:0	ON	—	SIDL	CCPSLP	TMRSYNC	CLKSEL<2:0>			TMRPS<1:0>		T32	CCSEL	MOD<3:0>				0000
0110	CCP1CON2	31:16	OENSYNC	—	OCFEN	OCEEN	OCDEN	OCCEN	OCBEN	OCAEN	ICGSM<1:0>		—	AUXOUT<1:0>		ICS<2:0>			0100
		15:0	PWMRSEN	ASDGM	—	SSDG	—	—	—	—	ASDG<7:0>								0000
0120	CCP1CON3	31:16	OETRIG	OSCNT<2:0>			—	OUTM<2:0>			—	—	POLACE	POLBDF	PSSACE<1:0>		PSSBDF<1:0>		0000
		15:0	—	—	—	—	—	—	—	—	—	—	DT<5:0>						0000
0130	CCP1STAT	31:16	—	—	—	—	—	—	—	—	—	—	—	PRLWIP	TMRHWIP	TMRLWIP	RBWIP	RAWIP	0000
		15:0	—	—	—	—	—	ICGARM	—	—	CCPTRIG	TRSET	TRCLR	ASEVT	SCEVT	ICDIS	ICOV	ICBNE	0000
0140	CCP1TMR	31:16	TMRH<15:0>																0000
		15:0	TMRL<15:0>																0000
0150	CCP1PR	31:16	PRH<15:0>																0000
		15:0	PRL<15:0>																0000
0160	CCP1RA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CMPA<15:0>																0000
0170	CCP1RB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CMPB<15:0>																0000
0180	CCP1BUF	31:16	BUFH<15:0>																0000
		15:0	BUFL<15:0>																0000
0200	CCP2CON1	31:16	OPSSRC	RTRGEN	—	—	OPS<3:0>				TRIGEN	ONESHOT	ALTSYNC	SYNC<4:0>					0000
		15:0	ON	—	SIDL	CCPSLP	TMRSYNC	CLKSEL<2:0>			TMRPS<1:0>		T32	CCSEL	MOD<3:0>				0000
0210	CCP2CON2	31:16	OENSYNC	—	OCFEN	OCEEN	OCDEN	OCCEN	OCBEN	OCAEN	ICGSM<1:0>		—	AUXOUT<1:0>		ICS<2:0>			0100
		15:0	PWMRSEN	ASDGM	—	SSDG	—	—	—	—	ASDG<7:0>								0000
0220	CCP2CON3	31:16	OETRIG	OSCNT<2:0>			—	OUTM<2:0>			—	—	POLACE	POLBDF	PSSACE<1:0>		PSSBDF<1:0>		0000
		15:0	—	—	—	—	—	—	—	—	—	—	DT<5:0>						0000
0230	CCP2STAT	31:16	—	—	—	—	—	—	—	—	—	—	—	PRLWIP	TMRHWIP	TMRLWIP	RBWIP	RAWIP	0000
		15:0	—	—	—	—	—	ICGARM	—	—	CCPTRIG	TRSET	TRCLR	ASEVT	SCEVT	ICDIS	ICOV	ICBNE	0000
0240	CCP2TMR	31:16	TMRH<15:0>																0000
		15:0	TMRL<15:0>																0000
0250	CCP2PR	31:16	PRH<15:0>																0000
		15:0	PRL<15:0>																0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively.

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TABLE 14-1: MCCP/SCCP REGISTER MAP (CONTINUED)

Virtual Address (BF80_#)	Register Name[1]	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0260	CCP2RA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CMPA<15:0>																0000
0270	CCP2RB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CMPB<15:0>																0000
0280	CCP2BUF	31:16	BUFH<15:0>																0000
		15:0	BUFL<15:0>																0000
0300	CCP3CON1	31:16	OPSSRC	RTRGEN	—	—	OPS<3:0>				TRIGEN	ONESHOT	ALTSYNC	SYNC<4:0>					0000
		15:0	ON	—	SIDL	CCPSLP	TMRSYNC	CLKSEL<2:0>			TMRPS<1:0>		T32	CCSEL	MOD<3:0>				0000
0310	CCP3CON2	31:16	OENSYNC	—	OCFEN	OCEEN	OCDEN	OCCEN	OCBEN	OCAEN	ICGSM<1:0>		—	AUXOUT<1:0>		ICS<2:0>			0100
		15:0	PWMRSEN	ASDGM	—	SSDG	—	—	—	—	ASDG<7:0>								0000
0320	CCP3CON3	31:16	OETRIG	OSCNT<2:0>			—	OUTM<2:0>			—	—	POLACE	POLBDF	PSSACE<1:0>		PSSBDF<1:0>		0000
		15:0	—	—	—	—	—	—	—	—	—	—	DT<5:0>						0000
0330	CCP3STAT	31:16	—	—	—	—	—	—	—	—	—	—	—	PRLWIP	TMRHWIP	TMRLWIP	RBWIP	RAWIP	0000
		15:0	—	—	—	—	—	ICGARM	—	—	CCPTRIG	TRSET	TRCLR	ASEVT	SCEVT	ICDIS	ICOV	ICBNE	0000
0340	CCP3TMR	31:16	TMRH<15:0>																0000
		15:0	TMRL<15:0>																0000
0350	CCP3PR	31:16	PRH<15:0>																0000
		15:0	PRL<15:0>																0000
0360	CCP3RA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CMPA<15:0>																0000
0370	CCP3RB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CMPB<15:0>																0000
0380	CCP3BUF	31:16	BUFH<15:0>																0000
		15:0	BUFL<15:0>																0000
0400	CCP4CON1	31:16	OPSSRC	RTRGEN	—	—	OPS<3:0>				TRIGEN	ONESHOT	ALTSYNC	SYNC					0000
		15:0	ON	—	SIDL	CCPSLP	TMRSYNC	CLKSEL<2:0>			TMRPS<1:0>		T32	CCSEL	MOD<3:0>				0000
0410	CCP4CON2	31:16	OENSYNC	—	—	—	—	—	—	OCAEN	ICGSM<1:0>		—	AUXOUT<1:0>		ICS<2:0>			0100
		15:0	PWMRSEN	ASDGM	—	SSDG	—	—	—	—	ASDG<7:0>								0000
0420	CCP4CON3	31:16	OETRIG	OSCNT<2:0>			—	—	—	—	—	—	POLACE	—	PSSACE<1:0>		—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively.

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TABLE 14-1: MCCP/SCCP REGISTER MAP (CONTINUED)

Virtual Address (BF80_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0430	CCP4STAT	31:16	—	—	—	—	—	—	—	—	—	—	—	PRLWIP	TMRHWIP	TMRLWIP	RBWIP	RAWIP	0000
		15:0	—	—	—	—	—	ICGARM	—	—	CCPTRIG	TRSET	TRCLR	ASEVT	SCEVT	ICDIS	ICOV	ICBNE	0000
0440	CCP4TMR	31:16	TMRH<15:0>																0000
		15:0	TMRL<15:0>																0000
0450	CCP4PR	31:16	PRH<15:0>																0000
		15:0	PRL<15:0>																0000
0460	CCP4RA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CMPA<15:0>																0000
0470	CCP4RB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CMPB<15:0>																0000
0480	CCP4BUF	31:16	BUFH<15:0>																0000
		15:0	BUFL<15:0>																0000
0500	CCP5CON1	31:16	OPSSRC	RTRGEN	—	—	OPS<3:0>				TRIGEN	ONESHOT	ALTSYNC	SYNC<4:0>					0000
		15:0	ON	—	SIDL	CCPSLP	TMRSYNC	CLKSEL<2:0>			TMRPS<1:0>		T32	CCSEL	MOD<3:0>				0000
0510	CCP5CON2	31:16	OENSYNC	—	OCFEN	OCEEN	OCDEN	OCCEN	OCBEN	OCAEN	ICGSM<1:0>		—	AUXOUT<1:0>		ICS<2:0>			0100
		15:0	PWMRSEN	ASDGM	—	SSDG	—	—	—	—	ASDG<7:0>								0000
0520	CCP5CON3	31:16	OETRIG	OSCNT<2:0>			—	—	—	—	—	—	POLACE	—	PSSACE<1:0>		—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
0530	CCP5STAT	31:16	—	—	—	—	—	—	—	—	—	—	—	PRLWIP	TMRHWIP	TMRLWIP	RBWIP	RAWIP	0000
		15:0	—	—	—	—	—	ICGARM	—	—	CCPTRIG	TRSET	TRCLR	ASEVT	SCEVT	ICDIS	ICOV	ICBNE	0000
0540	CCP5TMR	31:16	TMRH<15:0>																0000
		15:0	TMRL<15:0>																0000
0550	CCP5PR	31:16	PRH<15:0>																0000
		15:0	PRL<15:0>																0000
0560	CCP5RA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CMPA<15:0>																0000
0570	CCP5RB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CMPB<15:0>																0000
0580	CCP5BUF	31:16	BUFH<15:0>																0000
		15:0	BUFL<15:0>																0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively.

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TABLE 14-1: MCCP/SCCP REGISTER MAP (CONTINUED)

Virtual Address (BF80_#)	Register Name[(1)]	Bit Range	Bits 31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
0600	CCP6CON1	31:16	OPSSRC	RTRGEN	—	—	OPS<3:0>				TRIGEN	ONESHOT	ALTSYNC	SYNC<4:0>					0000
		15:0	ON	—	SIDL	CCPSLP	TMRSYNC	CLKSEL<2:0>			TMRPS<1:0>		T32	CCSEL	MOD<3:0>				0000
0610	CCP6CON2	31:16	OENSYNC	—	OCFEN	OCEEN	OCDEN	OCCEN	OCBEN	OCAEN	ICGSM<1:0>		—	AUXOUT<1:0>		ICS<2:0>			0100
		15:0	PWMRSEN	ASDGM	—	SSDG	—	—	—	—	ASDG<7:0>								0000
0620	CCP6CON3	31:16	OETRIG	OSCNT<2:0>			—	—	—	—	—	—	POLACE	—	PSSACE<1:0>		—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
0630	CCP6STAT	31:16	—	—	—	—	—	—	—	—	—	—	—	PRLWIP	TMRHWIP	TMRLWIP	RBWIP	RAWIP	0000
		15:0	—	—	—	—	—	ICGARM	—	—	CCPTRIG	TRSET	TRCLR	ASEVT	SCEVT	ICDIS	ICOV	ICBNE	0000
0640	CCP6TMR	31:16	TMRH<15:0>																0000
		15:0	TMRL<15:0>																0000
0650	CCP6PR	31:16	PRH<15:0>																0000
		15:0	PRL<15:0>																0000
0660	CCP6RA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CMPA<15:0>																0000
0670	CCP6RB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CMPB<15:0>																0000
0680	CCP6BUF	31:16	BUFH<15:0>																0000
		15:0	BUFL<15:0>																0000
0700	CCP7CON1	31:16	OPSSRC	RTRGEN	—	—	OPS<3:0>				TRIGEN	ONESHOT	ALTSYNC	SYNC<4:0>					0000
		15:0	ON	—	SIDL	CCPSLP	TMRSYNC	CLKSEL<2:0>			TMRPS<1:0>		T32	CCSEL	MOD<3:0>				0000
0710	CCP7CON2	31:16	OENSYNC	—	OCFEN	OCEEN	OCDEN	OCCEN	OCBEN	OCAEN	ICGSM<1:0>		—	AUXOUT<1:0>		ICS<2:0>			0100
		15:0	PWMRSEN	ASDGM	—	SSDG	—	—	—	—	ASDG<7:0>								0000
0720	CCP7CON3	31:16	OETRIG	OSCNT<2:0>			—	—	—	—	—	—	POLACE	—	PSSACE<1:0>		—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
0730	CCP7STAT	31:16	—	—	—	—	—	—	—	—	—	—	—	PRLWIP	TMRHWIP	TMRLWIP	RBWIP	RAWIP	0000
		15:0	—	—	—	—	—	ICGARM	—	—	CCPTRIG	TRSET	TRCLR	ASEVT	SCEVT	ICDIS	ICOV	ICBNE	0000
0740	CCP7TMR	31:16	TMRH<15:0>																0000
		15:0	TMRL<15:0>																0000
0750	CCP7PR	31:16	PRH<15:0>																0000
		15:0	PRL<15:0>																0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively.

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TABLE 14-1: MCCP/SCCP REGISTER MAP (CONTINUED)

Virtual Address (BF80_#)	Register Name[1]	Bit Range	Bits 31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
0760	CCP7RA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CMPA<15:0>																0000
0770	CCP7RB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CMPB<15:0>																0000
0780	CCP7BUF	31:16	BUFH<15:0>																0000
		15:0	BUFL<15:0>																0000
0800	CCP8CON1	31:16	OPSSRC	RTRGEN	—	—	OPS<3:0>				TRIGEN	ONESHOT	ALTSYNC	SYNC<4:0>					0000
		15:0	ON	—	SIDL	CCPSLP	TMRSYNC	CLKSEL<2:0>			TMRPS<1:0>		T32	CCSEL	MOD<3:0>				0000
0810	CCP8CON2	31:16	OENSYNC	—	OCFEN	OCEEN	OCDEN	OCCEN	OCBEN	OCAEN	ICGSM<1:0>		—	AUXOUT<1:0>		ICS<2:0>			0100
		15:0	PWMRSEN	ASDGM	—	SSDG	—	—	—	—	ASDG<7:0>								0000
0820	CCP8CON3	31:16	OETRIG	OSCNT<2:0>			—	—	—	—	—	—	POLACE	—	PSSACE<1:0>		—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
0830	CCP8STAT	31:16	—	—	—	—	—	—	—	—	—	—	—	PRLWIP	TMRHWIP	TMRLWIP	RBWIP	RAWIP	0000
		15:0	—	—	—	—	—	ICGARM	—	—	CCPTRIG	TRSET	TRCLR	ASEVT	SCEVT	ICDIS	ICOV	ICBNE	0000
0840	CCP8TMR	31:16	TMRH<15:0>																0000
		15:0	TMRL<15:0>																0000
0850	CCP8PR	31:16	PRH<15:0>																0000
		15:0	PRL<15:0>																0000
0860	CCP8RA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CMPA<15:0>																0000
0870	CCP8RB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CMPB<15:0>																0000
0880	CCP8BUF	31:16	BUFH<15:0>																0000
		15:0	BUFL<15:0>																0000
0900	CCP9CON1	31:16	OPSSRC	RTRGEN	—	—	OPS<3:0>				TRIGEN	ONESHOT	ALTSYNC	SYNC<4:0>					0000
		15:0	ON	—	SIDL	CCPSLP	TMRSYNC	CLKSEL<2:0>			TMRPS<1:0>		T32	CCSEL	MOD<3:0>				0000
0910	CCP9CON2	31:16	OENSYNC	—	OCFEN	OCEEN	OCDEN	OCCEN	OCBEN	OCAEN	ICGSM<1:0>		—	AUXOUT<1:0>		ICS<2:0>			0100
		15:0	PWMRSEN	ASDGM	—	SSDG	—	—	—	—	ASDG<7:0>								0000
0920	CCP9CON3	31:16	OETRIG	OSCNT<2:0>			—	—	—	—	—	—	POLACE	—	PSSACE<1:0>		—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively.

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TABLE 14-1: MCCP/SCCP REGISTER MAP (CONTINUED)

Virtual Address (BF80_#)	Register Name[1]	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
0930	CCP9STAT	31:16	—	—	—	—	—	—	—	—	—	—	—	PRLWIP	TMRHWIP	TMRLWIP	RBWIP	RAWIP	0000
		15:0	—	—	—	—	—	ICGARM	—	—	CCPTRIG	TRSET	TRCLR	ASEVT	SCEVT	ICDIS	ICOV	ICBNE	0000
0940	CCP9TMR	31:16	TMRH<15:0>																0000
		15:0	TMRL<15:0>																0000
0950	CCP9PR	31:16	PRH<15:0>																0000
		15:0	PRL<15:0>																0000
0960	CCP9RA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CMPA<15:0>																0000
0970	CCP9RB	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CMPB<15:0>																0000
0980	CCP9BUF	31:16	BUFH<15:0>																0000
		15:0	BUFL<15:0>																0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively.

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REGISTER 14-1: CCPxCON1: CAPTURE/COMPARE/PWMx CONTROL 1 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	OPSSRC(1)	RTRGEN(2)	—	—	OPS<3:0>(3)			
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	TRIGEN	ONESHOT	ALTSYNC	SYNC<4:0>				
15:8	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ON(1)	—	SIDL	CCPSLP	TMRSYNC	CLKSEL<2:0>		
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	TMRPS<1:0>		T32	CCSEL	MOD<3:0>			

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31 **OPSSRC:** Output Postscaler Source Select bit(1)
1 = Output postscaler scales the Special Event Trigger output events
0 = Output postscaler scales the timer interrupt events

bit 30 **RTRGEN:** Retrigger Enable bit(2)
1 = Time base can be retriggered when CCPTRIG = 1
0 = Time base may not be retriggered when CCPTRIG = 1

bit 29-28 **Unimplemented:** Read as ‘0’

bit 27-24 **OPS<3:0>:** CCPx Interrupt Output Postscale Select bits(3)
1111 = Interrupt every 16th time base period match
1110 = Interrupt every 15th time base period match
. . .
0100 = Interrupt every 5th time base period match
0011 = Interrupt every 4th time base period match or 4th input capture event
0010 = Interrupt every 3rd time base period match or 3rd input capture event
0001 = Interrupt every 2nd time base period match or 2nd input capture event
0000 = Interrupt after each time base period match or input capture event

bit 23 **TRIGEN:** CCPx Triggered Enable bit
1 = Triggered operation of the timer is enabled
0 = Triggered operation of the timer is disabled

bit 22 **ONESHOT:** One-Shot Mode Enable bit
1 = One-Shot Triggered mode is enabled; trigger duration is set by OSCNT<2:0>
0 = One-Shot Triggered mode is disabled

bit 21 **ALTSYNC:** CCPx Clock Select bit
1 = An alternate signal is used as the module synchronization output signal
0 = The module synchronization output signal is the Time Base Reset/rollover event

Note 1: This control bit has no function in Input Capture modes.
2: This control bit has no function when TRIGEN = 0.
3: Values greater than ‘0011’ will cause a FIFO buffer overflow in Input Capture mode.

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REGISTER 14-1: CCPxCON1: CAPTURE/COMPARE/PWMx CONTROL 1 REGISTER (CONTINUED)

bit 20-16 **SYNC<4:0>:** CCPx Synchronization Source Select bits
11111 = Off
11110 = Reserved
. . .
11100 = Reserved
11011 = Time base is synchronized to the start of ADC conversion
11010 = Time base is synchronized to Comparator 3
11001 = Time base is synchronized to Comparator 2
11000 = Time base is synchronized to Comparator 1
10111 = Reserved
. . .
10010 = Reserved
10011 = Time base is synchronized to CLC4
10010 = Time base is synchronized to CLC3
10001 = Time base is synchronized to CLC2
10001 = Time base is synchronized to CLC1
01111 = Time base is synchronized to SCCP9
01110 = Time base is synchronized to SCCP8
01101 = Time base is synchronized to the INT4 Pin (Remappable)
01100 = Time base is synchronized to the INT3 Pin
01011 = Time base is synchronized to the INT2 Pin
01010 = Time base is synchronized to the INT1 Pin
01001 = Time base is synchronized to the INT0 Pin
01000 = Reserved
. . .
00101 = Reserved
00100 = Time base is synchronized to SCCP3
00011 = Time base is synchronized to SCCP2
00010 = Time base is synchronized to MCCP1
00001 = Time base is synchronized to this MCCP/SCCP
00000 = No external synchronization; timer rolls over at FFFFh or matches with the Timer Period register

bit 15 **ON:** CCPx Module Enable bit(1)
1 = Module is enabled with the operating mode specified by the MOD<3:0> bits
0 = Module is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** CCPx Stop in Idle Mode bit
1 = Discontinues module operation when device enters Idle mode
0 = Continues module operation in Idle mode

bit 12 **CCPSLP:** CCPx Sleep Mode Enable bit
1 = Module continues to operate in Sleep modes
0 = Module does not operate in Sleep modes

bit 11 **TMRSYNC:** Time Base Clock Synchronization bit
1 = Module time base clock is synchronized to internal system clocks; timing restrictions apply
0 = Module time base clock is not synchronized to internal system clocks

Note 1: This control bit has no function in Input Capture modes.
2: This control bit has no function when TRIGEN = 0.
3: Values greater than '0011' will cause a FIFO buffer overflow in Input Capture mode.

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REGISTER 14-1: CCPxCON1: CAPTURE/COMPARE/PWMx CONTROL 1 REGISTER (CONTINUED)

bit 10-8 **CLKSEL<2:0>:** CCPx Time Base Clock Select bits
111 = TCKIA pin (remappable)
110 = TCKIB pin (remappable)
101 = Reserved
100 = Reserved
011 = CLC1 output for MCCP1
CLC2 output for MCCP2
CLC3 output for MCCP3
CLC1 output for SCCP4
CLC2 output for SCCP5
CLC3 output for SCCP6
CLC4 output for SCCP7
CLC1 output for SCCP8
CLC1 output for SCCP9
010 = Secondary Oscillator (SOSC) clock
001 = REFO1 output clock
000 = System clock (T_{CY})

bit 7-6 **TMRPS<1:0>:** CCPx Time Base Prescale Select bits
11 = 1:64 prescaler
10 = 1:16 prescaler
01 = 1:4 prescaler
00 = 1:1 prescaler

bit 5 **T32:** 32-Bit Time Base Select bit
1 = 32-bit time base for timer, single edge output compare or input capture function
0 = 16-bit time base for timer, single edge output compare or input capture function

bit 4 **CCSEL:** Capture/Compare Mode Select bit
1 = Input Capture mode
0 = Output Compare/PWM or Timer mode (exact function is selected by the MOD<3:0> bits)

bit 3-0 **MOD<3:0>:** CCPx Mode Select bits
CCSEL = 1 (Input Capture modes):
1xxx = Reserved
011x = Reserved
0101 = Capture every 16th rising edge
0100 = Capture every 4th rising edge
0011 = Capture every rising and falling edge
0010 = Capture every falling edge
0001 = Capture every rising edge
0000 = Capture every rising and falling edge (Edge Detect mode)
CCSEL = 0 (Output Compare modes):
1111 = External Input mode: Pulse generator is disabled, source is selected by ICS<2:0>
1110 = Reserved
110x = Reserved
10xx = Reserved
0111 = Variable Frequency Pulse mode
0110 = Center-Aligned Pulse Compare mode, buffered
0101 = Dual Edge Compare mode, buffered
0100 = Dual Edge Compare mode
0011 = 16-Bit/32-Bit Single Edge mode: Toggles output on compare match
0010 = 16-Bit/32-Bit Single Edge mode: Drives output low on compare match
0001 = 16-Bit/32-Bit Single Edge mode: Drives output high on compare match
0000 = 16-Bit/32-Bit Timer mode: Output functions are disabled

Note 1: This control bit has no function in Input Capture modes.
2: This control bit has no function when TRIGEN = 0.
3: Values greater than ‘0011’ will cause a FIFO buffer overflow in Input Capture mode.

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REGISTER 14-2: CCPxCON2: CAPTURE/COMPARE/PWMx CONTROL 2 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1
	OENSYNC	—	OCFEN(1)	OCEEN(1)	OCDEN(1)	OCCEN(1)	OCBEN(1)	OCAEN
23:16	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ICGSM<1:0>		—	AUXOUT<1:0>		ICS<2:0>		
15:8	R/W-0	R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0
	PWMRSEN	ASDGM	—	SSDG	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ASDG<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31 **OENSYNC:** Output Enable Synchronization bit
1 = Update by output enable bits occurs on the next Time Base Reset or rollover
0 = Update by output enable bits occurs immediately

bit 30 **Unimplemented:** Read as ‘0’

bit 29-24 **OC<F:A>EN:** Output Enable/Steering Control bits(1)
1 = OCx pin is controlled by the CCPx module and produces an output compare or PWM signal
0 = OCx pin is not controlled by the CCPx module; the pin is available to the port logic or another peripheral multiplexed on the pin

bit 23-22 **ICGSM<1:0>:** Input Capture Gating Source Mode Control bits
11 = Reserved
10 = One-Shot mode: Falling edge from gating source disables future capture events (ICDIS = 1)
01 = One-Shot mode: Rising edge from gating source enables future capture events (ICDIS = 0)
00 = Level-Sensitive mode: A high level from gating source will enable future capture events; a low level will disable future capture events

bit 21 **Unimplemented:** Read as ‘0’

bit 20-19 **AUXOUT<1:0>:** Auxiliary Output Signal on Event Selection bits
11 = Input capture or output compare event; no signal in Timer mode
10 = Signal output depends on module operating mode
01 = Time base rollover event (all modes)
00 = Disabled

bit 18-16 **ICS<2:0>:** Input Capture Source Select bits
111 = CLC4 output
110 = CLC3 output
101 = CLC2 output
100 = CLC1 output
011 = Comparator 3 output
010 = Comparator 2 output
001 = Comparator 1 output
000 = ICMx pin(2)

bit 15 **PWMRSEN:** CCPx PWM Restart Enable bit
1 = ASEVT bit clears automatically at the beginning of the next PWM period, after the shutdown input has ended
0 = ASEVT must be cleared in software to resume PWM activity on output pins

Note 1: OCFEN through OCBEN (bits<29:25>) are implemented in MCCP modules only.
2: This pin is remappable from SCCP modules.

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REGISTER 14-2: CCPxCON2: CAPTURE/COMPARE/PWMx CONTROL 2 REGISTER (CONTINUED)

bit 14 **ASDGM:** CCPx Auto-Shutdown Gate Mode Enable bit
1 = Waits until the next Time Base Reset or rollover for shutdown to occur
0 = Shutdown event occurs immediately

bit 13 **Unimplemented:** Read as '0'

bit 12 **SSDG:** CCPx Software Shutdown/Gate Control bit
1 = Manually forces auto-shutdown, timer clock gate or input capture signal gate event (setting the ASDGM bit still applies)
0 = Normal module operation

bit 11-8 **Unimplemented:** Read as '0'

bit 7-0 **ASDG<7:0>:** CCPx Auto-Shutdown/Gating Source Enable bits
1xxx xxxx = Auto-shutdown is controlled by the OCFB pin (remappable)
x1xx xxxx = Auto-shutdown is controlled by the OCFA pin (remappable)
xx1x xxxx = Auto-shutdown is controlled by CLC1 for MCCP1
Auto-shutdown is controlled by CLC2 for MCCP2
Auto-shutdown is controlled by CLC3 for MCCP3
Auto-shutdown is controlled by CLC1 for SCCP4
Auto-shutdown is controlled by CLC2 for SCCP5
Auto-shutdown is controlled by CLC3 for SCCP6
Auto-shutdown is controlled by CLC4 for SCCP7
Auto-shutdown is controlled by CLC1 for SCCP8
Auto-shutdown is controlled by CLC2 for SCCP9
xxx1 xxxx = Auto-shutdown is controlled by the SCCP4 output for MCCP1/MCCP2/MCCP3
Auto-shutdown is controlled by the MCCP1 output for SCCP4/SCCP5/SCCP6/SCCP7/SCCP8/SCCP9
xxxx 1xxx = Auto-shutdown is controlled by the SCCP5 output for MCCP1/MCCP2/MCCP3
Auto-shutdown is controlled by the MCCP2 output for SCCP4/SCCP5/SCCP6/SCCP7/SCCP8/SCCP9
xxxx x1xx = Auto-shutdown is controlled by Comparator 3
xxxx xx1x = Auto-shutdown is controlled by Comparator 2
xxxx xxx1 = Auto-shutdown is controlled by Comparator 1

Note 1: OCFEN through OCBEN (bits<29:25>) are implemented in MCCP modules only.
2: This pin is remappable from SCCP modules.

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REGISTER 14-3: CCPxCON3: CAPTURE/COMPARE/PWMx CONTROL 3 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0
	OETRIG	OSCNT<2:0>			—	OUTM<2:0>[1]		
23:16	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	POLACE	POLBDF[1]	PSSACE<1:0>		PSSBDF<1:0>[1]	
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	DT<5:0>[1]					

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31 **OETRIG:** PWM Dead-Time Select bit
1 = For Triggered mode (TRIGEN = 1), the module does not drive enabled output pins until triggered
0 = Normal output pin operation

bit 30-28 **OSCNT<2:0>:** One-Shot Event Count bits
Extends the duration of a one-shot trigger event by an additional n clock cycles (n + 1 total cycles).
111 = 7 timer count periods (8 cycles total)
110 = 6 timer count periods (7 cycles total)
101 = 5 timer count periods (6 cycles total)
100 = 4 timer count periods (5 cycles total)
011 = 3 timer count periods (4 cycles total)
010 = 2 timer count periods (3 cycles total)
001 = 1 timer count period (2 cycles total)
000 = Does not extend the one-shot trigger event (the event takes 1 timer count period)

bit 27 **Unimplemented:** Read as ‘0’

bit 26-24 **OUTM<2:0>:** PWMx Output Mode Control bits[1]
111 = Reserved
110 = Output Scan mode
101 = Brush DC Output mode, forward
100 = Brush DC Output mode, reverse
011 = Reserved
010 = Half-Bridge Output mode
001 = Push-Pull Output mode
000 = Steerable Single Output mode

bit 23-22 **Unimplemented:** Read as ‘0’

bit 21 **POLACE:** CCPx Output Pins, OCxA, OCxC and OCxE, Polarity Control bit
1 = Output pin polarity is active-low
0 = Output pin polarity is active-high

bit 20 **POLBDF:** CCPx Output Pins, OCxB, OCxD and OCxF, Polarity Control bit[1]
1 = Output pin polarity is active-low
0 = Output pin polarity is active-high

Note 1: These bits are implemented in MCCP modules only.

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REGISTER 14-3: CCPxCON3: CAPTURE/COMPARE/PWMx CONTROL 3 REGISTER (CONTINUED)

bit 19-18 **PSSACE<1:0>:** PWMx Output Pins, OCxA, OCxC and OCxE, Shutdown State Control bits
11 = Pins are driven active when a shutdown event occurs
10 = Pins are driven inactive when a shutdown event occurs
0x = Pins are in a high-impedance state when a shutdown event occurs

bit 17-16 **PSSBDF<1:0>:** PWMx Output Pins, OCxB, OCxD and OCxF, Shutdown State Control bits[1]
11 = Pins are driven active when a shutdown event occurs
10 = Pins are driven inactive when a shutdown event occurs
0x = Pins are in a high-impedance state when a shutdown event occurs

bit 15-6 **Unimplemented:** Read as '0'

bit 5-0 **DT<5:0>:** PWM Dead-Time Select bits[1]
111111 = Insert 63 dead-time delay periods between complementary output signals
111110 = Insert 62 dead-time delay periods between complementary output signals
. . .
000010 = Insert 2 dead-time delay periods between complementary output signals
000001 = Insert 1 dead-time delay period between complementary output signals
000000 = Dead-time logic is disabled

Note 1: These bits are implemented in MCCP modules only.

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REGISTER 14-4: CCPxSTAT: CAPTURE/COMPARE/PWMx STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	R-0	R-0	R-0	R-0	R-0
	—	—	—	PRLWIP	TMRHWIP	TMRLWIP	RBWIP	RAWIP
15:8	U-0	U-0	U-0	U-0	U-0	R/C-0	U-0	U-0
	—	—	—	—	—	ICGARM(1)	—	—
7:0	R-0	W1-0	W1-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0
	CCPTRIG	TRSET	TRCLR	ASEVT	SCEVT	ICDIS	ICOV	ICBNE

Legend:	C = Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-21 **Unimplemented:** Read as ‘0’

bit 20 **PRLWIP:** CCPxPRL Write in Progress Status bit
1 = An update to the CCPxPRL register with the buffered contents is in progress
0 = An update to the CCPxPRL register is not in progress

bit 19 **TMRHWIP:** CCPxTMRH Write in Progress Status bit
1 = An update to the CCPxTMRH register with the buffered contents is in progress
0 = An update to the CCPxTMRH register is not in progress

bit 18 **TMRLWIP:** CCPxTMRL Write in Progress Status bit
1 = An update to the CCPxTMRL register with the buffered contents is in progress
0 = An update to the CCPxTMRL register is not in progress

bit 17 **RBWIP:** CCPxRB Write in Progress Status bit
1 = An update to the CCPxRB register with the buffered contents is in progress
0 = An update to the CCPxRB register is not in progress

bit 16 **RAWIP:** CCPxRA Write in Progress Status bit
1 = An update to the CCPxRA register with the buffered contents is in progress
0 = An update to the CCPxRA register is not in progress

bit 15-11 **Unimplemented:** Read as ‘0’

bit 10 **ICGARM:** Input Capture Gate Arm bit(1)
A write of ‘1’ to this location will arm the input capture gating logic for a one-shot gate event when ICGSM<1:0> = 01 or 10. The bit location reads as ‘0’.

bit 9-8 **Unimplemented:** Read as ‘0’

bit 7 **CCPTRIG:** CCPx Trigger Status bit
1 = Timer has been triggered and is running (set by hardware or writing to TRSET)
0 = Timer has not been triggered and is held in Reset (cleared by writing to TRCLR)

bit 6 **TRSET:** CCPx Trigger Set Request bit
Write ‘1’ to this location to trigger the timer when TRIGEN = 1 (location always reads ‘0’).

bit 5 **TRCLR:** CCPx Trigger Clear Request bit
Write ‘1’ to this location to cancel the timer trigger when TRIGEN = 1 (location always reads ‘0’).

bit 4 **ASEVT:** CCPx Auto-Shutdown Event Status/Control bit
1 = A shutdown event is in progress; CCPx outputs are in the shutdown state
0 = CCPx outputs operate normally

Note 1: This is not a physical bit location and will always read as ‘0’. A write of ‘1’ will initiate the hardware event.

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REGISTER 14-4: CCPxSTAT: CAPTURE/COMPARE/PWMx STATUS REGISTER (CONTINUED)

bit 3 **SCEVT:** Single Edge Compare Event Status bit
1 = A single edge compare event has occurred
0 = A single edge compare event has not occurred

bit 2 **ICDIS:** Input Capture Disable bit
1 = Event on input capture pin does not generate a capture event
0 = Event on input capture pin will generate a capture event

bit 1 **ICOV:** Input Capture Buffer Overflow Status bit
1 = The input capture FIFO buffer has overflowed
0 = The input capture FIFO buffer has not overflowed

bit 0 **ICBNE:** Input Capture Buffer Status bit
1 = The input capture buffer has data available
0 = The input capture buffer is empty

Note 1: This is not a physical bit location and will always read as ‘0’. A write of ‘1’ will initiate the hardware event.

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NOTES:

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15.0 SERIAL PERIPHERAL INTERFACE (SPI) AND INTER-IC SOUND (I^2S)

Note: This data sheet summarizes the features of the PIC32MM0256GPM064 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 23. "Serial Peripheral Interface (SPI)"** (DS61106) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32). The information in this data sheet supersedes the information in the FRM.

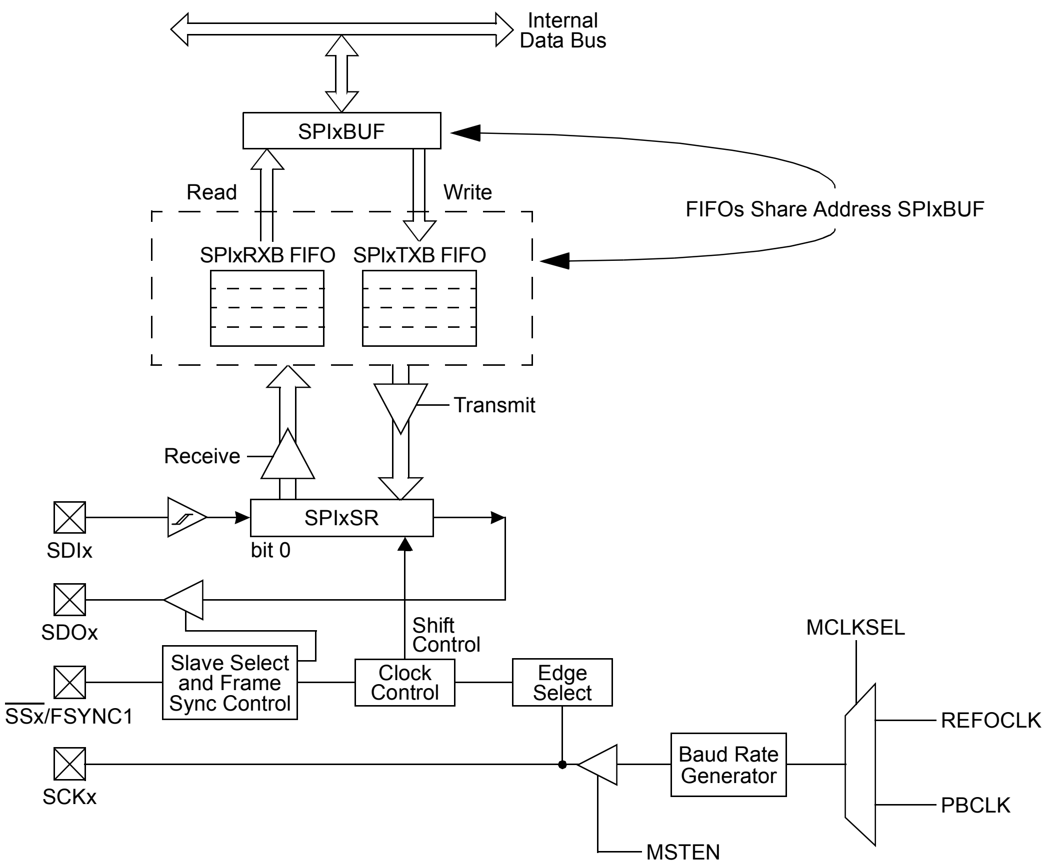
The SPI/I^2S module is a synchronous serial interface that is useful for communicating with external peripherals and other microcontroller devices, as well as digital audio devices. These peripheral devices may be serial EEPROMs, shift registers, display drivers, Analog-to-Digital Converters (ADC), etc.

The SPI/I^2S module is compatible with Motorola® SPI and SIOP interfaces.

Some of the key features of the SPI module are:

- Master and Slave modes Support
- Four Different Clock Formats
- Enhanced Framed SPI Protocol Support
- User-Configurable 8-Bit, 16-Bit and 32-Bit Data Width
- Separate SPI FIFO Buffers for Receive and Transmit:
  - FIFO buffers act as 4/8/16-level deep FIFOs based on 32/16/8-bit data width
- Programmable Interrupt Event on every 8-Bit, 16-Bit and 32-Bit Data Transfer
- Operation during Sleep and Idle modes
- Audio Codec Support:
  - I^2S protocol

FIGURE 15-1: SPI/I^2S MODULE BLOCK DIAGRAM



Note: Access the SPIxTXB and SPIxRXB FIFOs via the SPIxBUF register.

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15.1 SPI Control Registers

TABLE 15-1: SPI1, SPI2 AND SPI3 REGISTER MAP

Virtual Address (BF80_#)	Register Name[1]	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
8100	SPI1CON	31:16	FRMEN	FRMSYNC	FRMPOL	MSSEN	FRMSYPW	FRMCNT<2:0>			MCLKSEL	—	—	—	—	—	SPIFE	ENHBUF	0000
		15:0	ON	—	SIDL	DISSDO	MODE32	MODE16	SMP	CKE	SSEN	CKP	MSTEN	DISSDI	STXISEL<1:0>		SRXISEL<1:0>		0000
8110	SPI1STAT	31:16	—	—	—	RXBUFELM<4:0>					—	—	—	TXBUFELM<4:0>					0000
		15:0	—	—	—	FRMERR	SPIBUSY	—	—	SPITUR	SRMT	SPIROV	SPIRBE	—	SPITBE	—	SPITBF	SPIRBF	0008
8120	SPI1BUF	31:16	DATA<31:0>																0000
		15:0																	0000
8130	SPI1BRG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	BRG<12:0>													0000
8140	SPI1CON2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	SPISGNEXT	—	—	FRMERREN	SPIROVEN	SPITUREN	IGNROV	IGNTUR	AUDEN	—	—	—	AUDMONO	—	AUDMOD<1:0>		0000
8200	SPI2CON	31:16	FRMEN	FRMSYNC	FRMPOL	MSSEN	FRMSYPW	FRMCNT<2:0>			MCLKSEL	—	—	—	—	—	SPIFE	ENHBUF	0000
		15:0	ON	—	SIDL	DISSDO	MODE32	MODE16	SMP	CKE	SSEN	CKP	MSTEN	DISSDI	STXISEL<1:0>		SRXISEL<1:0>		0000
8210	SPI2STAT	31:16	—	—	—	RXBUFELM<4:0>					—	—	—	TXBUFELM<4:0>					0000
		15:0	—	—	—	FRMERR	SPIBUSY	—	—	SPITUR	SRMT	SPIROV	SPIRBE	—	SPITBE	—	SPITBF	SPIRBF	0008
8220	SPI2BUF	31:16	DATA<31:0>																0000
		15:0																	0000
8230	SPI2BRG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	BRG<12:0>													0000
8240	SPI2CON2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	SPISGNEXT	—	—	FRMERREN	SPIROVEN	SPITUREN	IGNROV	IGNTUR	AUDEN	—	—	—	AUDMONO	—	AUDMOD<1:0>		0000
8300	SPI3CON	31:16	FRMEN	FRMSYNC	FRMPOL	MSSEN	FRMSYPW	FRMCNT<2:0>			MCLKSEL	—	—	—	—	—	SPIFE	ENHBUF	0000
		15:0	ON	—	SIDL	DISSDO	MODE32	MODE16	SMP	CKE	SSEN	CKP	MSTEN	DISSDI	STXISEL<1:0>		SRXISEL<1:0>		0000
8310	SPI3STAT	31:16	—	—	—	RXBUFELM<4:0>					—	—	—	TXBUFELM<4:0>					0000
		15:0	—	—	—	FRMERR	SPIBUSY	—	—	SPITUR	SRMT	SPIROV	SPIRBE	—	SPITBE	—	SPITBF	SPIRBF	0008
8330	SPI3BUF	31:16	DATA<31:0>																0000
		15:0																	0000
8320	SPI3BRG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	BRG<12:0>													0000
8340	SPI3CON2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	SPISGNEXT	—	—	FRMERREN	SPIROVEN	SPITUREN	IGNROV	IGNTUR	AUDEN	—	—	—	AUDMONO	—	AUDMOD<1:0>		0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table, except SPIxBUF, have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively.

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REGISTER 15-1: SPIxCON: SPIx CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	FRMEN	FRMSYNC	FRMPOL	MSSEN	FRMSYPW	FRMCNT<2:0>		
23:16	R/W-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
	MCLKSEL(1)	—	—	—	—	—	SPIFE	ENHBUF(1)
15:8	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ON	—	SIDL	DISSDO(4)	MODE32	MODE16	SMP	CKE(2)
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	SSEN	CKP(3)	MSTEN	DISSDI(4)	STXISEL<1:0>		SRXISEL<1:0>	

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **FRMEN:** Framed SPI Support bit
1 = Framed SPI support is enabled ($\overline{SSx}$ pin is used as the FSYNC1 input/output)
0 = Framed SPI support is disabled

bit 30 **FRMSYNC:** Frame Sync Pulse Direction Control on $\overline{SSx}$ Pin bit (Framed SPI mode only)
1 = Frame sync pulse input (Slave mode)
0 = Frame sync pulse output (Master mode)

bit 29 **FRMPOL:** Frame Sync Polarity bit (Framed SPI mode only)
1 = Frame pulse is active-high
0 = Frame pulse is active-low

bit 28 **MSSEN:** Master Mode Slave Select Enable bit
1 = Slave select SPI support is enabled; the $\overline{SSx}$ pin is automatically driven during transmission in Master mode, polarity is determined by the FRMPOL bit
0 = Slave select SPI support is disabled

bit 27 **FRMSYPW:** Frame Sync Pulse-Width bit
1 = Frame sync pulse is one character wide
0 = Frame sync pulse is one clock wide

bit 26-24 **FRMCNT<2:0>:** Frame Sync Pulse Counter bits
Controls the number of data characters transmitted per pulse. This bit is only valid in Framed mode.
111 = Reserved
110 = Reserved
101 = Generates a frame sync pulse on every 32 data characters
100 = Generates a frame sync pulse on every 16 data characters
011 = Generates a frame sync pulse on every 8 data characters
010 = Generates a frame sync pulse on every 4 data characters
001 = Generates a frame sync pulse on every 2 data characters
000 = Generates a frame sync pulse on every data character

Note 1: These bits can only be written when the ON bit = 0. Refer to **Section 29.0 "Electrical Characteristics"** for maximum clock frequency requirements.
2: This bit is not used in the Framed SPI mode. The user should program this bit to '0' for the Framed SPI mode (FRMEN = 1).
3: When AUDEN = 1, the SPI/I^{2}S module functions as if the CKP bit is equal to '1', regardless of the actual value of the CKP bit.
4: These bits are present for legacy compatibility and are superseded by PPS functionality on these devices (see **Section 10.9 "Peripheral Pin Select (PPS)"** for more information).

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REGISTER 15-1: SPIxCON: SPIx CONTROL REGISTER (CONTINUED)

bit 23 **MCLKSEL:** Master Clock Enable bit[(1)]
1 = REFO1 is used by the Baud Rate Generator
0 = PBCLK is used by the Baud Rate Generator

bit 22-18 **Unimplemented:** Read as '0'

bit 17 **SPIFE:** Frame Sync Pulse Edge Select bit (Framed SPI mode only)
1 = Frame synchronization pulse coincides with the first bit clock
0 = Frame synchronization pulse precedes the first bit clock

bit 16 **ENHBUF:** Enhanced Buffer Enable bit[(1)]
1 = Enhanced Buffer mode is enabled
0 = Enhanced Buffer mode is disabled

bit 15 **ON:** SPIx Module On bit
1 = SPIx module is enabled
0 = SPIx module is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** SPIx Stop in Idle Mode bit
1 = Discontinues operation when CPU enters Idle mode
0 = Continues operation in Idle mode

bit 12 **DISSDO:** Disable SDOx Pin bit[(4)]
1 = SDOx pin is not used by the module; the pin is controlled by the associated PORTx register
0 = SDOx pin is controlled by the module

bit 11-10 **MODE<32,16>:** 32/16/8-Bit Communication Select bits

When AUDEN = 1:

MODE32	MODE16	Communication
1	1	24-bit data, 32-bit FIFO, 32-bit channel/64-bit frame
1	0	32-bit data, 32-bit FIFO, 32-bit channel/64-bit frame
0	1	16-bit data, 16-bit FIFO, 32-bit channel/64-bit frame
0	0	16-bit data, 16-bit FIFO, 16-bit channel/32-bit frame

When AUDEN = 0:

MODE32	MODE16	Communication
1	x	32-bit
0	1	16-bit
0	0	8-bit

bit 9 **SMP:** SPIx Data Input Sample Phase bit
Master mode (MSTEN = 1):
1 = Input data is sampled at end of data output time
0 = Input data is sampled at middle of data output time
Slave mode (MSTEN = 0):
SMP value is ignored when SPIx is used in Slave mode. The module always uses SMP = 0.

bit 8 **CKE:** SPIx Clock Edge Select bit[(2)]
1 = Serial output data changes on transition from active clock state to Idle clock state (see the CKP bit)
0 = Serial output data changes on transition from Idle clock state to active clock state (see the CKP bit)

Note 1: These bits can only be written when the ON bit = 0. Refer to **Section 29.0 "Electrical Characteristics"** for maximum clock frequency requirements.
2: This bit is not used in the Framed SPI mode. The user should program this bit to '0' for the Framed SPI mode (FRMEN = 1).
3: When AUDEN = 1, the SPI/I^{2}S module functions as if the CKP bit is equal to '1', regardless of the actual value of the CKP bit.
4: These bits are present for legacy compatibility and are superseded by PPS functionality on these devices (see **Section 10.9 "Peripheral Pin Select (PPS)"** for more information).

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REGISTER 15-1: SPIxCON: SPIx CONTROL REGISTER (CONTINUED)

bit 7 **SSEN:** Slave Select Enable (Slave mode) bit
1 = $\overline{\text{SSx}}$ pin is used for Slave mode
0 = $\overline{\text{SSx}}$ pin is not used for Slave mode, pin is controlled by port function

bit 6 **CKP:** Clock Polarity Select bit(3)
1 = Idle state for clock is a high level; active state is a low level
0 = Idle state for clock is a low level; active state is a high level

bit 5 **MSTEN:** Master Mode Enable bit
1 = Master mode
0 = Slave mode

bit 4 **DISSDI:** Disable SDIx bit(4)
1 = SDIx pin is not used by the SPIx module (pin is controlled by port function)
0 = SDIx pin is controlled by the SPIx module

bit 3-2 **STXISEL<1:0>:** SPIx Transmit Buffer Empty Interrupt Mode bits
11 = Interrupt is generated when the buffer is not full (has one or more empty elements)
10 = Interrupt is generated when the buffer is empty by one-half or more
01 = Interrupt is generated when the buffer is completely empty
00 = Interrupt is generated when the last transfer is shifted out of SPIxSR and transmit operations are complete

bit 1-0 **SRXISEL<1:0>:** SPIx Receive Buffer Full Interrupt Mode bits
11 = Interrupt is generated when the buffer is full
10 = Interrupt is generated when the buffer is full by one-half or more
01 = Interrupt is generated when the buffer is not empty
00 = Interrupt is generated when the last word in the receive buffer is read (i.e., buffer is empty)

Note 1: These bits can only be written when the ON bit = 0. Refer to **Section 29.0 "Electrical Characteristics"** for maximum clock frequency requirements.

2: This bit is not used in the Framed SPI mode. The user should program this bit to '0' for the Framed SPI mode (FRMEN = 1).

3: When AUDEN = 1, the SPI/I^{2}S module functions as if the CKP bit is equal to '1', regardless of the actual value of the CKP bit.

4: These bits are present for legacy compatibility and are superseded by PPS functionality on these devices (see **Section 10.9 "Peripheral Pin Select (PPS)"** for more information).

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REGISTER 15-2: SPIxCON2: SPIx CONTROL REGISTER 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	SPISGNEXT	—	—	FRMERREN	SPIROVEN	SPITUREN	IGNROV	IGNTUR
7:0	R/W-0	U-0	U-0	U-0	R/W-0	U-0	R/W-0	R/W-0
	AUDEN[1]	—	—	—	AUDMONO[1,2]	—	AUDMOD<1:0>[1,2]	

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **SPISGNEXT:** SPIx Sign-Extend Read Data from the RX FIFO bit
1 = Data from RX FIFO is sign-extended
0 = Data from RX FIFO is not sign-extended

bit 14-13 **Unimplemented:** Read as '0'

bit 12 **FRMERREN:** Enable Interrupt Events via FRMERR bit
1 = Frame error overflow generates error events
0 = Frame error does not generate error events

bit 11 **SPIROVEN:** Enable Interrupt Events via SPIROV bit
1 = Receive Overflow (ROV) generates error events
0 = Receive Overflow does not generate error events

bit 10 **SPITUREN:** Enable Interrupt Events via SPITUR bit
1 = Transmit Underrun (TUR) generates error events
0 = Transmit Underrun does not generate error events

bit 9 **IGNROV:** Ignore Receive Overflow (ROV) bit (for audio data transmissions)
1 = A ROV is not a critical error; during ROV, data in the FIFO is not overwritten by receive data
0 = A ROV is a critical error which stops SPIx operation

bit 8 **IGNTUR:** Ignore Transmit Underrun (TUR) bit (for audio data transmissions)
1 = A TUR is not a critical error and zeros are transmitted until the SPIxTXB is not empty
0 = A TUR is a critical error which stops SPIx operation

bit 7 **AUDEN:** Enable Audio Codec Support bit[1]
1 = Audio protocol is enabled
0 = Audio protocol is disabled

bit 6-4 **Unimplemented:** Read as '0'

bit 3 **AUDMONO:** Transmit Audio Data Format bit[1,2]
1 = Audio data is mono (each data word is transmitted on both left and right channels)
0 = Audio data is stereo

bit 2 **Unimplemented:** Read as '0'

bit 1-0 **AUDMOD<1:0>:** Audio Protocol Mode bits[1,2]
11 = PCM/DSP mode
10 = Right Justified mode
01 = Left Justified mode
00 = I^2S mode

Note 1: These bits can only be written when the ON bit = 0.
2: These bits are only valid for AUDEN = 1.

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REGISTER 15-3: SPIxSTAT: SPIx STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	R-0	R-0	R-0	R-0	R-0
	—	—	—	RXBUFELM<4:0>				
23:16	U-0	U-0	U-0	R-0	R-0	R-0	R-0	R-0
	—	—	—	TXBUFELM<4:0>				
15:8	U-0	U-0	U-0	R/C-0, HS	R-0	U-0	U-0	R-0
	—	—	—	FRMERR	SPIBUSY	—	—	SPITUR
7:0	R-0	R/W-0	R-0	U-0	R-1	U-0	R-0	R-0
	SRMT	SPIROV	SPIRBE	—	SPITBE	—	SPITBF	SPIRBF

Legend:	C = Clearable bit	HS = Hardware Settable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-29 **Unimplemented:** Read as ‘0’

bit 28-24 **RXBUFELM<4:0>:** Receive Buffer Element Count bits (valid only when ENHBUF = 1)

bit 23-21 **Unimplemented:** Read as ‘0’

bit 20-16 **TXBUFELM<4:0>:** Transmit Buffer Element Count bits (valid only when ENHBUF = 1)

bit 15-13 **Unimplemented:** Read as ‘0’

bit 12 **FRMERR:** SPIx Frame Error status bit
1 = Frame error detected
0 = No frame error detected
This bit is only valid when FRMEN = 1.

bit 11 **SPIBUSY:** SPIx Activity Status bit
1 = SPIx peripheral is currently busy with some transactions
0 = SPIx peripheral is currently Idle

bit 10-9 **Unimplemented:** Read as ‘0’

bit 8 **SPITUR:** Transmit Underrun (TUR) bit
1 = Transmit buffer has encountered an underrun condition
0 = Transmit buffer has no underrun condition
This bit is only valid in Framed Sync mode; the underrun condition must be cleared by disabling/re-enabling the module.

bit 7 **SRMT:** Shift Register Empty bit (valid only when ENHBUF = 1)
1 = When the SPIx Shift register is empty
0 = When the SPIx Shift register is not empty

bit 6 **SPIROV:** Receive Overflow (ROV) Flag bit
1 = A new data is completely received and discarded; the user software has not read the previous data in the SPIxBUF register
0 = No overflow has occurred
This bit is set in hardware; it can only be cleared (= 0) in software.

bit 5 **SPIRBE:** RX FIFO Empty bit (valid only when ENHBUF = 1)
1 = RX FIFO is empty (CPU Read Pointer (CRPTR) = SPI Write Pointer (SWPTR))
0 = RX FIFO is not empty (CRPTR ≠ SWPTR)

bit 4 **Unimplemented:** Read as ‘0’

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REGISTER 15-3: SPIxSTAT: SPIx STATUS REGISTER (CONTINUED)

bit 3 **SPITBE:** SPIx Transmit Buffer Empty Status bit
1 = Transmit buffer, SPIxTXB, is empty
0 = Transmit buffer, SPIxTXB, is not empty
Automatically set in hardware when SPIx transfers data from SPIxTXB to SPIxSR. Automatically cleared in hardware when SPIxBUF is written to, loading SPIxTXB.

bit 2 **Unimplemented:** Read as '0'

bit 1 **SPITBF:** SPIx Transmit Buffer Full Status bit
1 = Transmit has not yet started, SPIxTXB is full
0 = Transmit buffer is not full
Standard Buffer mode:
Automatically set in hardware when the core writes to the SPIxBUF location, loading SPIxTXB. Automatically cleared in hardware when the SPIx module transfers data from SPIxTXB to SPIxSR.
Enhanced Buffer mode:
Set when CPU Write Pointer (CWPTR) + 1 = SPI Read Pointer (SRPTR); cleared otherwise.

bit 0 **SPIRBF:** SPIx Receive Buffer Full Status bit
1 = Receive buffer, SPIxRXB, is full
0 = Receive buffer, SPIxRXB, is not full
Standard Buffer mode:
Automatically set in hardware when the SPIx module transfers data from SPIxSR to SPIxRXB. Automatically cleared in hardware when SPIxBUF is read from, reading SPIxRXB.
Enhanced Buffer mode:
Set when SWPTR + 1 = CRPTR; cleared otherwise.

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16.0 INTER-INTEGRATED CIRCUIT (I^2C)

> **Note:** This data sheet summarizes the features of the PIC32MM0256GPM064 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 24. "Inter-Integrated Circuit™ (I^2C™)"** (DS61116) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32). The information in this data sheet supersedes the information in the FRM.

The I^2C module provides complete hardware support for both Slave and Multi-Master modes of the I^2C serial communication standard.

Each I^2C module has a 2-pin interface:

- SCLx pin is clock
- SDAx pin is data

Each I^2C module offers the following key features:

- I^2C Interface Supporting Both Master and Slave Operation
- I^2C Slave mode Supports 7-Bit and 10-Bit Addressing
- I^2C Master mode Supports 7-Bit and 10-Bit Addressing
- I^2C Port allows Bidirectional Transfers between Master and Slaves
- Serial Clock Synchronization for the I^2C Port can be used as a Handshake Mechanism to Suspend and Resume Serial Transfer (SCLREL control)
- I^2C Supports Multi-Master Operation; Detects Bus Collision and Arbitrates Accordingly
- Provides Support for Address Bit Masking
- SMBus Support

Figure 16-1 illustrates the I^2C module block diagram.

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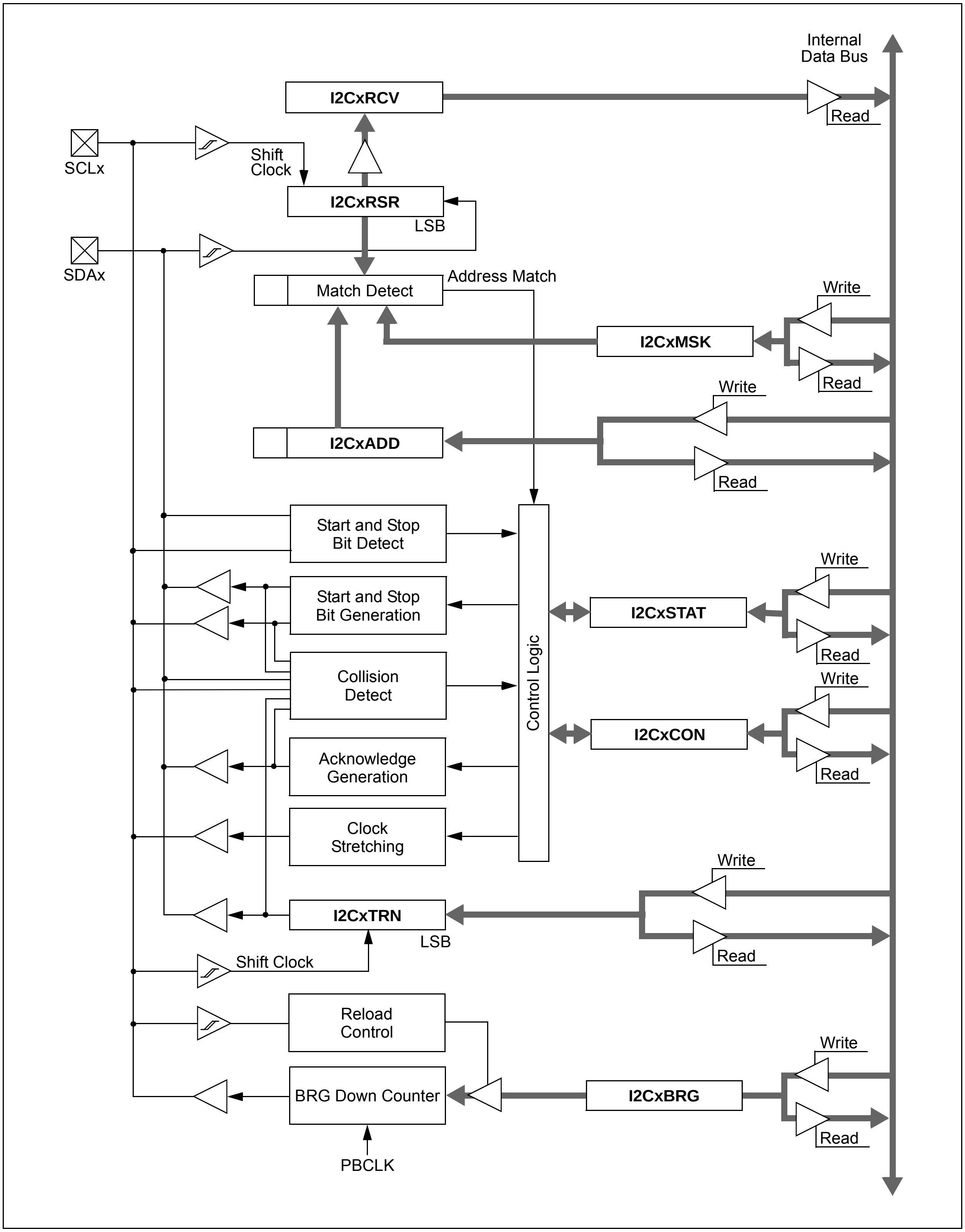
FIGURE 16-1: I2Cx BLOCK DIAGRAM



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16.1 I²C Control Registers

TABLE 16-1: I2C1, I2C2 AND I2C3 REGISTER MAP

Virtual Address (BF80_#)	Register Name(1)	Bit Range	Bits 31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
1500	I2C1CON	31:16	—	—	—	—	—	—	—	—	—	PCIE	SCIE	BOEN	SDAHT	SBCDE	r	r	0000
		15:0	ON	—	SIDL	SCLREL	STRICT	A10M	DISSLW	SMEN	GCEN	STREN	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	1000
1510	I2C1STAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ACKSTAT	TRSTAT	ACKTIM	—	—	BCL	GCSTAT	ADD10	IWCOL	I2COV	D/A	P	S	R/W	RBF	TBF	0000
1520	I2C1ADD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	I2C1 Address Register										0000
1530	I2C1MSK	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	I2C1 Address Mask Register										0000
1540	I2C1BRG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	Baud Rate Generator Register																0000
1550	I2C1TRN	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	I2C1 Transmit Register								0000
1560	I2C1RCV	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	I2C1 Receive Register								0000
1600	I2C2CON	31:16	—	—	—	—	—	—	—	—	—	PCIE	SCIE	BOEN	SDAHT	SBCDE	r	r	0000
		15:0	ON	—	SIDL	SCLREL	STRICT	A10M	DISSLW	SMEN	GCEN	STREN	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	1000
1610	I2C2STAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ACKSTAT	TRSTAT	ACKTIM	—	—	BCL	GCSTAT	ADD10	IWCOL	I2COV	D/A	P	S	R/W	RBF	TBF	0000
1620	I2C2ADD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	I2C2 Address Register										0000
1630	I2C2MSK	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	I2C2 Address Mask Register										0000
1640	I2C2BRG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	Baud Rate Generator Register																0000
1650	I2C2TRN	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	I2C2 Transmit Register								0000
1660	I2C2RCV	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	I2C2 Receive Register								0000

Legend: — = unimplemented, read as '0'; r = reserved bit. Reset values are shown in hexadecimal.

Note 1: All registers in this table, except I2CxRCV, have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively.

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TABLE 16-1: I2C1, I2C2 AND I2C3 REGISTER MAP (CONTINUED)

Virtual Address (BF80_#)	Register Name[1]	Bit Range	Bits 31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
1700	I2C3CON	31:16	—	—	—	—	—	—	—	—	—	PCIE	SCIE	BOEN	SDAHT	SBCDE	r	r	0000
		15:0	ON	—	SIDL	SCLREL	STRICT	A10M	DISSLW	SMEN	GCEN	STREN	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	1000
1710	I2C3STAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ACKSTAT	TRSTAT	ACKTIM	—	—	BCL	GCSTAT	ADD10	IWCOL	I2COV	D/A	P	S	R/W	RBF	TBF	0000
1720	I2C3ADD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	I2C2 Address Register										0000
1730	I2C3MSK	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	I2C2 Address Mask Register										0000
1740	I2C3BRG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	Baud Rate Generator Register																0000
1750	I2C3TRN	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	I2C2 Transmit Register								0000
1760	I2C3RCV	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	I2C2 Receive Register								0000

Legend: — = unimplemented, read as ‘0’; r = reserved bit. Reset values are shown in hexadecimal.

Note 1: All registers in this table, except I2CxRCV, have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively.

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REGISTER 16-1: I2CxCON: I2Cx CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	r-0	r-0
	—	PCIE	SCIE	BOEN	SDAHT	SBCDE	—	—
15:8	R/W-0	U-0	R/W-0	R/W-1, HC	R/W-0	R/W-0	R/W-0	R/W-0
	ON	—	SIDL	SCLREL	STRICT	A10M	DISSLW	SMEN
7:0	R/W-0	R/W-0	R/W-0	R/W-0, HC	R/W-0, HC	R/W-0, HC	R/W-0, HC	R/W-0, HC
	GCEN	STREN	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN

Legend:	r = Reserved bit	HC = Hardware Clearable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-23 **Unimplemented:** Read as ‘0’

bit 22 **PCIE:** Stop Condition Interrupt Enable bit (I²C Slave mode only)
1 = Enables interrupt on detection of Stop condition
0 = Stop detection interrupts are disabled

bit 21 **SCIE:** Start Condition Interrupt Enable bit (I²C Slave mode only)
1 = Enables interrupt on detection of Start or Restart conditions
0 = Start detection interrupts are disabled

bit 20 **BOEN:** Buffer Overwrite Enable bit (I²C Slave mode only)
1 = I2CxRCV is updated and an $\overline{\text{ACK}}$ is generated for a received address/data byte, ignoring the state of the I2COV bit (I2CxSTAT<6>) only if the RBF bit (I2CxSTAT<1>) = 0
0 = I2CxRCV is only updated when the I2COV bit (I2CxSTAT<6>) is clear

bit 19 **SDAHT:** SDAx Hold Time Selection bit
1 = Minimum of 300 ns hold time on SDAx after the falling edge of SCLx
0 = Minimum of 100 ns hold time on SDAx after the falling edge of SCLx

bit 18 **SBCDE:** Slave Mode Bus Collision Detect Enable bit (I²C Slave mode only)
1 = Enables slave bus collision interrupts
0 = Slave bus collision interrupts are disabled

bit 17-16 **Reserved:** Maintain as ‘0’

bit 15 **ON:** I2Cx Enable bit
1 = Enables the I2Cx module and configures the SDAx and SCLx pins as serial port pins
0 = Disables the I2Cx module; all I²C pins are controlled by port functions

bit 14 **Unimplemented:** Read as ‘0’

bit 13 **SIDL:** I2Cx Stop in Idle Mode bit
1 = Discontinues module operation when device enters Idle mode
0 = Continues module operation in Idle mode

bit 12 **SCLREL:** SCLx Release Control bit (when operating as I²C slave)
1 = Releases SCLx clock
0 = Holds SCLx clock low (clock stretch)

If STREN = 1:
Bit is R/W (i.e., software can write ‘0’ to initiate stretch and write ‘1’ to release clock). Hardware is clear at the beginning of slave transmission. Hardware is clear at the end of slave reception.

If STREN = 0:
Bit is R/S (i.e., software can only write ‘1’ to release clock). Hardware is clear at the beginning of slave transmission.

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REGISTER 16-1: I2CxCON: I2Cx CONTROL REGISTER (CONTINUED)

bit 11 **STRICT:** Strict I^{2}C Reserved Address Rule Enable bit
1 = Strict reserved addressing is enforced; device does not respond to reserved address space or generates addresses in reserved address space
0 = Strict I^{2}C reserved address rule is not enabled

bit 10 **A10M:** 10-Bit Slave Address bit
1 = I2CxADD is a 10-bit slave address
0 = I2CxADD is a 7-bit slave address

bit 9 **DISSLW:** Disable Slew Rate Control bit
1 = Slew rate control is disabled
0 = Slew rate control is enabled

bit 8 **SMEN:** SMBus Input Levels bit
1 = Enables I/O pin thresholds compliant with the SMBus specification
0 = Disables SMBus input thresholds

bit 7 **GCEN:** General Call Enable bit (when operating as I^{2}C slave)
1 = Enables interrupt when a general call address is received in the I2CxRSR (module is enabled for reception)
0 = General call address is disabled

bit 6 **STREN:** SCLx Clock Stretch Enable bit (when operating as I^{2}C slave)
Used in conjunction with the SCLREL bit.
1 = Enables software or receives clock stretching
0 = Disables software or receives clock stretching

bit 5 **ACKDT:** Acknowledge Data bit (when operating as I^{2}C master, applicable during master receive)
Value that is transmitted when the software initiates an Acknowledge sequence.
1 = Sends NACK during Acknowledge
0 = Sends ACK during Acknowledge

bit 4 **ACKEN:** Acknowledge Sequence Enable bit
(when operating as I^{2}C master, applicable during master receive)
1 = Initiates Acknowledge sequence on the SDAx and SCLx pins and transmits the ACKDT data bit; hardware is clear at the end of the master Acknowledge sequence
0 = Acknowledge sequence is not in progress

bit 3 **RCEN:** Receive Enable bit (when operating as I^{2}C master)
1 = Enables Receive mode for I^{2}C; hardware is clear at the end of the eighth bit of the master receive data byte
0 = Receive sequence is not in progress

bit 2 **PEN:** Stop Condition Enable bit (when operating as I^{2}C master)
1 = Initiates Stop condition on SDAx and SCLx pins; hardware is clear at the end of the master Stop sequence
0 = Stop condition is not in progress

bit 1 **RSEN:** Repeated Start Condition Enable bit (when operating as I^{2}C master)
1 = Initiates Repeated Start condition on SDAx and SCLx pins; hardware is clear at the end of the master Repeated Start sequence
0 = Repeated Start condition is not in progress

bit 0 **SEN:** Start Condition Enable bit (when operating as I^{2}C master)
1 = Initiates Start condition on SDAx and SCLx pins; hardware is clear at the end of the master Start sequence
0 = Start condition is not in progress

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REGISTER 16-2: I2CxSTAT: I2Cx STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R-0, HSC	R-0, HSC	R/C-0, HSC	U-0	U-0	R/C-0, HS	R-0, HSC	R-0, HSC
	ACKSTAT	TRSTAT	ACKTIM	—	—	BCL	GCSTAT	ADD10
7:0	R/C-0, HS	R/C-0, HS	R-0, HSC	R/C-0, HSC	R/C-0, HSC	R-0, HSC	R-0, HSC	R-0, HSC
	IWCOL	I2COV	D/A	P	S	R/W	RBF	TBF

Legend:	HS = Hardware Settable bit	HSC = Hardware Settable/Clearable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	C = Clearable bit

bit 31-16 **Unimplemented:** Read as ‘0’

bit 15 **ACKSTAT:** Acknowledge Status bit (when operating as I^{2}C master, applicable to master transmit operation)
1 = NACK received from slave
0 = ACK received from slave
Hardware is set or clear at the end of slave Acknowledge.

bit 14 **TRSTAT:** Transmit Status bit (when operating as I^{2}C master, applicable to master transmit operation)
1 = Master transmit is in progress (8 bits + ACK)
0 = Master transmit is not in progress
Hardware is set at the beginning of master transmission. Hardware is clear at the end of slave Acknowledge.

bit 13 **ACKTIM:** Acknowledge Time Status bit (valid in I^{2}C Slave mode only)
1 = I^{2}C bus is in an Acknowledge sequence, set on 8th falling edge of SCLx clock
0 = Not an Acknowledge sequence, cleared on 9th rising edge of SCLx clock

bit 12-11 **Unimplemented:** Read as ‘0’

bit 10 **BCL:** Master Bus Collision Detect bit
1 = A bus collision has been detected during a master operation
0 = No collision
Hardware is set at detection of a bus collision.

bit 9 **GCSTAT:** General Call Status bit
1 = General call address was received
0 = General call address was not received
Hardware is set when the address matches the general call address. Hardware is clear at Stop detection.

bit 8 **ADD10:** 10-Bit Address Status bit
1 = 10-bit address was matched
0 = 10-bit address was not matched
Hardware is set at match of the 2nd byte of matched 10-bit address. Hardware is clear at Stop detection.

bit 7 **IWCOL:** I2Cx Write Collision Detect bit
1 = An attempt to write to the I2CxTRN register failed because the I^{2}C module is busy
0 = No collision
Hardware is set at occurrence of a write to I2CxTRN while busy (cleared by software).

bit 6 **I2COV:** I2Cx Receive Overflow Flag bit
1 = A byte was received while the I2CxRCV register is still holding the previous byte
0 = No overflow
Hardware is set at attempt to transfer I2CxRSR to I2CxRCV (cleared by software).

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REGISTER 16-2: I2CxSTAT: I2Cx STATUS REGISTER (CONTINUED)

bit 5 **D/A:** Data/Address bit (when operating as I^2C slave)
1 = Indicates that the last byte received was data
0 = Indicates that the last byte received was a device address
Hardware is clear at a device address match. Hardware is set by reception of a slave byte.

bit 4 **P:** Stop bit
1 = Indicates that a Stop bit has been detected last
0 = Stop bit was not detected last
Hardware is set or clear when Start, Repeated Start or Stop is detected.

bit 3 **S:** Start bit
1 = Indicates that a Start (or Repeated Start) bit has been detected last
0 = Start bit was not detected last
Hardware is set or clear when Start, Repeated Start or Stop is detected.

bit 2 **R/W:** Read/Write Information bit (when operating as I^2C slave)
1 = Read – Indicates data transfer is output from slave
0 = Write – Indicates data transfer is input to slave
Hardware is set or clear after reception of an I^2C device address byte.

bit 1 **RBF:** Receive Buffer Full Status bit
1 = Receive is complete, I2CxRCV is full
0 = Receive is not complete, I2CxRCV is empty
Hardware is set when I2CxRCV is written with the received byte. Hardware is clear when software reads I2CxRCV.

bit 0 **TBF:** Transmit Buffer Full Status bit
1 = Transmit is in progress, I2CxTRN is full
0 = Transmit is complete, I2CxTRN is empty
Hardware is set when software writes to I2CxTRN. Hardware is clear at completion of the data transmission.

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17.0 UNIVERSAL ASYNCHRONOUS RECEIVER TRANSMITTER (UART)

Note:	This data sheet summarizes the features of the PIC32MM0256GPM064 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 21. "UART"** (DS61107) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32). The information in this data sheet supersedes the information in the FRM.

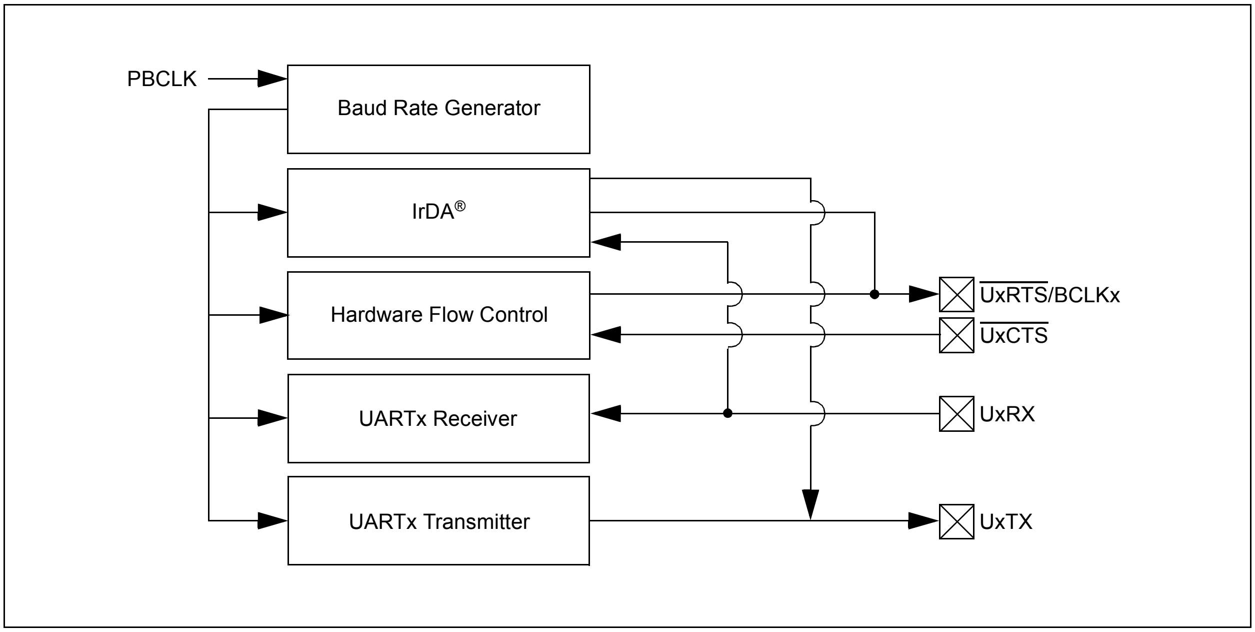
The UART module is one of the serial I/O modules available in the PIC32MM0256GPM064 family devices. The UART is a full-duplex, asynchronous communication channel that communicates with peripheral devices and personal computers through protocols, such as RS-232, RS-485, LIN/J2602 and IrDA®. The module also supports the hardware flow control option with the $\overline{\text{UxCTS}}$ and $\overline{\text{UxRTS}}$ pins, and also includes an IrDA® encoder and decoder.

The primary features of the UART module are:

- Full-Duplex, 8-Bit or 9-Bit Data Transmission
- Even, Odd or No Parity Options (for 8-bit data)
- One or Two Stop Bits
- Hardware Auto-Baud Feature
- Hardware Flow Control Option
- Fully Integrated Baud Rate Generator (BRG) with 16-Bit Prescaler
- Baud rates ranging from 47.4 bps to 6.25 Mbps at 25 MHz
- 8-Level Deep First-In-First-Out (FIFO) Transmit Data Buffer
- 8-Level Deep FIFO Receive Data Buffer
- Parity, Framing and Buffer Overrun Error Detection
- Support for Interrupt Only on Address Detect (9th bit = 1)
- Separate Transmit and Receive Interrupts
- Loopback mode for Diagnostic Support
- LIN/J2602 Protocol Support
- IrDA Encoder and Decoder with 16x Baud Clock Output for External IrDA Encoder/Decoder Support
- Supports Separate UART Baud Clock Input
- Ability to Continue to Run when a Receive Overflow Condition Exists
- Ability to Run and rEceive Data during Sleep mode

Figure 17-1 illustrates a simplified block diagram of the UART module.

FIGURE 17-1: UARTx SIMPLIFIED BLOCK DIAGRAM



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17.1 UART Control Registers

TABLE 17-1: UART1, UART2 AND UART3 REGISTER MAP

Virtual Address (BF80_#)	Register Name	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
1800	U1MODE[1]	31:16	—	—	—	—	—	—	—	—	SLPEN	ACTIVE	—	—	—	CLKSEL<1:0>		OVFDIS	0000
		15:0	ON	—	SIDL	IREN	RTSMD	—	UEN<1:0>		WAKE	LPBACK	ABAUD	RXINV	BRGH	PDSEL<1:0>		STSEL	0000
1810	U1STA[1]	31:16	UART1 MASK<7:0>								UART1 ADDR<7:0>								0000
		15:0	UTXISEL<1:0>		UTXINV	URXEN	UTXBRK	UTXEN	UTXBF	TRMT	URXISEL<1:0>		ADDEN	RIDLE	PERR	FERR	OERR	URXDA	0110
1820	U1TXREG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	TX8	UART1 Transmit Register								0000
1830	U1RXREG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	RX8	UART1 Receive Register								0000
1840	U1BRG[1]	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	Baud Rate Generator Prescaler																0000
1900	U2MODE[1]	31:16	—	—	—	—	—	—	—	—	SLPEN	ACTIVE	—	—	—	CLKSEL<1:0>		OVFDIS	0000
		15:0	ON	—	SIDL	IREN	RTSMD	—	UEN<1:0>		WAKE	LPBACK	ABAUD	RXINV	BRGH	PDSEL<1:0>		STSEL	0000
1910	U2STA[1]	31:16	UART2 MASK<7:0>								UART2 ADDR<7:0>								0000
		15:0	UTXISEL<1:0>		UTXINV	URXEN	UTXBRK	UTXEN	UTXBF	TRMT	URXISEL<1:0>		ADDEN	RIDLE	PERR	FERR	OERR	URXDA	0110
1920	U2TXREG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	TX8	UART2 Transmit Register								0000
1930	U2RXREG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	RX8	UART2 Receive Register								0000
1940	U2BRG[1]	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	Baud Rate Generator Prescaler																0000
2000	U3MODE[1]	31:16	—	—	—	—	—	—	—	—	SLPEN	ACTIVE	—	—	—	CLKSEL<1:0>		OVFDIS	0000
		15:0	ON	—	SIDL	IREN	RTSMD	—	UEN<1:0>		WAKE	LPBACK	ABAUD	RXINV	BRGH	PDSEL<1:0>		STSEL	0000
2010	U3STA[1]	31:16	UART2 MASK<7:0>								UART2 ADDR<7:0>								0000
		15:0	UTXISEL<1:0>		UTXINV	URXEN	UTXBRK	UTXEN	UTXBF	TRMT	URXISEL<1:0>		ADDEN	RIDLE	PERR	FERR	OERR	URXDA	0110
2020	U3TXREG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	TX8	UART2 Transmit Register								0000
2030	U3RXREG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	RX8	UART2 Receive Register								0000
2040	U3BRG[1]	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	Baud Rate Generator Prescaler																0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.
Note 1: These registers have corresponding CLR, SET and INV registers at their virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively.

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REGISTER 17-1: UxMODE: UARTx MODE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	R/W-0	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	SLPEN	ACTIVE	—	—	—	CLKSEL<1:0>		OVFDIS
15:8	R/W-0	U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0
	ON	—	SIDL	IREN	RTSMD	—	UEN<1:0>[1]	
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	WAKE	LPBACK	ABAUD	RXINV	BRGH	PDSEL<1:0>		STSEL

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-24 **Unimplemented:** Read as ‘0’

bit 23 **SLPEN:** UARTx Run During Sleep Enable bit
1 = UARTx clock runs during Sleep
0 = UARTx clock is turned off during Sleep

bit 22 **ACTIVE:** UARTx Running Status bit
1 = UARTx is active (UxMODE register shouldn’t be updated)
0 = UARTx is not active (UxMODE register can be updated)

bit 21-19 **Unimplemented:** Read as ‘0’

bit 18-17 **CLKSEL:** UARTx Clock Selection bits
11 = The UARTx clock is the Reference Output (REFO1) clock
10 = The UARTx clock is the FRC oscillator clock
01 = The UARTx clock is the SYSCLK
00 = The UARTx clock is the PBCLK

bit 16 **OVFDIS:** Run During Overflow Condition Mode bit
1 = When an Overflow Error (OERR) condition is detected, the shift register continues to run to remain synchronized
0 = When an Overflow Error (OERR) condition is detected, the shift register stops accepting new data (Legacy mode)

bit 15 **ON:** UARTx Enable bit
1 = UARTx is enabled; UARTx pins are controlled by UARTx, as defined by the UEN<1:0> and UTXEN control bits
0 = UARTx is disabled; all UARTx pins are controlled by the corresponding bits in the PORTx, TRISx and LATx registers, UARTx power consumption is minimal

bit 14 **Unimplemented:** Read as ‘0’

bit 13 **SIDL:** UARTx Stop in Idle Mode bit
1 = Discontinues operation when device enters Idle mode
0 = Continues operation in Idle mode

bit 12 **IREN:** IrDA® Encoder and Decoder Enable bit
1 = IrDA is enabled
0 = IrDA is disabled

Note 1: These bits are present for legacy compatibility and are superseded by PPS functionality on these devices (see **Section 10.9 “Peripheral Pin Select (PPS)”** for more information).

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REGISTER 17-1: UxMODE: UARTx MODE REGISTER (CONTINUED)

bit 11 **RTSMD:** Mode Selection for $\overline{\text{UxRTS}}$ Pin bit
1 = $\overline{\text{UxRTS}}$ pin is in Simplex mode
0 = $\overline{\text{UxRTS}}$ pin is in Flow Control mode

bit 10 **Unimplemented:** Read as '0'

bit 9-8 **UEN<1:0>:** UARTx Enable bits[(1)]
11 = UxTX, UxRX and UxBCLK pins are enabled and used; $\overline{\text{UxCTS}}$ pin is controlled by corresponding bits in the PORTx register
10 = UxTX, UxRX, $\overline{\text{UxCTS}}$ and $\overline{\text{UxRTS}}$ pins are enabled and used
01 = UxTX, UxRX and $\overline{\text{UxRTS}}$ pins are enabled and used; $\overline{\text{UxCTS}}$ pin is controlled by corresponding bits in the PORTx register
00 = UxTX and UxRX pins are enabled and used; $\overline{\text{UxCTS}}$ and $\overline{\text{UxRTS}}$/UxBCLK pins are controlled by corresponding bits in the PORTx register

bit 7 **WAKE:** Enable Wake-up on Start bit Detect During Sleep Mode bit
1 = Wake-up is enabled
0 = Wake-up is disabled

bit 6 **LPBACK:** UARTx Loopback Mode Select bit
1 = Loopback mode is enabled
0 = Loopback mode is disabled

bit 5 **ABAUD:** Auto-Baud Enable bit
1 = Enables baud rate measurement on the next character – requires reception of a Sync character (0x55); cleared by hardware upon completion
0 = Baud rate measurement is disabled or has completed

bit 4 **RXINV:** Receive Polarity Inversion bit
1 = UxRX Idle state is '0'
0 = UxRX Idle state is '1'

bit 3 **BRGH:** High Baud Rate Enable bit
1 = High-Speed mode – 4x baud clock is enabled
0 = Standard Speed mode – 16x baud clock is enabled

bit 2-1 **PDSEL<1:0>:** Parity and Data Selection bits
11 = 9-bit data, no parity
10 = 8-bit data, odd parity
01 = 8-bit data, even parity
00 = 8-bit data, no parity

bit 0 **STSEL:** Stop Selection bit
1 = 2 Stop bits
0 = 1 Stop bit

Note 1: These bits are present for legacy compatibility and are superseded by PPS functionality on these devices (see **Section 10.9 "Peripheral Pin Select (PPS)"** for more information).

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REGISTER 17-2: UxSTA: UARTx STATUS AND CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	MASK<7:0>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ADDR<7:0>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-0	R-1
	UTXISEL<1:0>		UTXINV	URXEN	UTXBRK	UTXEN	UTXBF	TRMT
7:0	R/W-0	R/W-0	R/W-0	R-1	R-0	R-0	R/W-0	R-0
	URXISEL<1:0>		ADDEN	RIDLE	PERR	FERR	OERR	URXDA

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-24 **MASK<7:0>:** UARTx Address Match Mask bits
Used to mask the ADDR<7:0> bits.
<u>For MASK<x>:</u>
1 = ADDR<x> is used to detect the address match
0 = ADDR<x> is not used to detect the address match

bit 23-16 **ADDR<7:0>:** UARTx Automatic Address Mask bits
When the ADDEN bit is ‘1’, this value defines the address character to use for automatic address detection.

bit 15-14 **UTXISEL<1:0>:** UARTx TX Interrupt Mode Selection bits
11 = Reserved, do not use
10 = Interrupt is generated and asserted while the transmit buffer is empty
01 = Interrupt is generated and asserted when all characters have been transmitted
00 = Interrupt is generated and asserted while the transmit buffer contains at least one empty space

bit 13 **UTXINV:** UARTx Transmit Polarity Inversion bit
<u>If IrDA mode is Disabled (i.e., IREN (UxMODE<12>) is ‘0’):</u>
1 = UxTX Idle state is ‘0’
0 = UxTX Idle state is ‘1’
<u>If IrDA mode is Enabled (i.e., IREN (UxMODE<12>) is ‘1’):</u>
1 = IrDA® encoded UxTX Idle state is ‘1’
0 = IrDA encoded UxTX Idle state is ‘0’

bit 12 **URXEN:** UARTx Receiver Enable bit
1 = UARTx receiver is enabled, UxRX pin is controlled by UARTx (if ON = 1)
0 = UARTx receiver is disabled, UxRX pin is ignored by the UARTx module

bit 11 **UTXBRK:** UARTx Transmit Break bit
1 = Sends Break on next transmission; Start bit, followed by twelve ‘0’ bits, followed by Stop bit, cleared by hardware upon completion
0 = Break transmission is disabled or has completed

bit 10 **UTXEN:** UARTx Transmit Enable bit
1 = UARTx transmitter is enabled, UxTX pin is controlled by UARTx (if ON = 1)
0 = UARTx transmitter is disabled, any pending transmission is aborted and the buffer is reset

bit 9 **UTXBF:** UARTx Transmit Buffer Full Status bit (read-only)
1 = Transmit buffer is full
0 = Transmit buffer is not full, at least one more character can be written

bit 8 **TRMT:** Transmit Shift Register (TSR) is Empty bit (read-only)
1 = Transmit Shift Register is empty and transmit buffer is empty (the last transmission has completed)
0 = Transmit Shift Register is not empty, a transmission is in progress or queued in the transmit buffer

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REGISTER 17-2: UxSTA: UARTx STATUS AND CONTROL REGISTER (CONTINUED)

bit 7-6 **URXISEL<1:0>:** UARTx Receive Interrupt Mode Selection bits
11 = Reserved
10 = Interrupt flag bit is asserted while receive buffer is 3/4 or more full
01 = Interrupt flag bit is asserted while receive buffer is 1/2 or more full
00 = Interrupt flag bit is asserted while receive buffer is not empty (i.e., has at least 1 data character)

bit 5 **ADDEN:** Address Character Detect bit (bit 8 of received data = 1)
1 = Address Detect mode is enabled; if 9-bit mode is not selected, this control bit has no effect
0 = Address Detect mode is disabled

bit 4 **RIDLE:** Receiver Idle bit (read-only)
1 = Receiver is Idle
0 = Data is being received

bit 3 **PERR:** Parity Error Status bit (read-only)
1 = Parity error has been detected for the current character
0 = Parity error has not been detected

bit 2 **FERR:** Framing Error Status bit (read-only)
1 = Framing error has been detected for the current character
0 = Framing error has not been detected

bit 1 **OERR:** Receive Buffer Overrun Error Status bit
This bit is set in hardware and can only be cleared (= 0) in software. Clearing a previously set OERR bit resets the receiver buffer and RSR to the empty state.
1 = Receive buffer has overflowed
0 = Receive buffer has not overflowed

bit 0 **URXDA:** UARTx Receive Buffer Data Available bit (read-only)
1 = Receive buffer has data, at least one more character can be read
0 = Receive buffer is empty

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18.0 USB ON-THE-GO (OTG)

> **Note 1:** This data sheet summarizes the features of the PIC32MM0256GPM064 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 27. "USB On-The-Go (OTG)"** (DS61126) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).
>
> **2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The Universal Serial Bus (USB) module contains analog and digital components to provide a USB 2.0 full-speed and low-speed embedded Host, full-speed Device or OTG implementation, with a minimum of external components. This module in Host mode is intended for use as an embedded host, and therefore, does not implement a UHCI or OHCI controller.

The USB module consists of the clock generator, the USB voltage comparators, the transceiver, the Serial Interface Engine (SIE), a dedicated USB DMA Controller, pull-up and pull-down resistors, and the register interface. A block diagram of the PIC32 USB OTG module is presented in Figure 18-1.

18.1 Reclaiming USB Pins When the USB Module is Operating

Select USB pins that are not used on all USB operating modes (USBID and VBUSON) can be reclaimed when the module is operating in a mode that does not require them. These pins can be reclaimed by clearing the appropriate device Configuration bit (refer to Register 26-1).

For example:

- USBID and VBUSON can be reclaimed in Device mode
- VBUSON can be reclaimed in Host mode if it is not used for the power VBUS control

18.2 Reclaiming USB Pins When the USB Module is Disabled

All USB signaling pins, D+, D-, VBUS, VBUSON and USBID, can be reclaimed and used for GPIO or other peripherals if available on the pin when the USB module is disabled. For proper operation of the RB10 and RB11 pins, the USB module must be disabled, but powered. Refer to **Section 18.1 "Reclaiming USB Pins When the USB Module is Operating"** for more information.

18.3 Introduction

The clock generator provides the 48 MHz clock required for USB full-speed and low-speed communication. The voltage comparators monitor the voltage on the VBUS pin to determine the state of the bus. The transceiver provides the analog translation between the USB bus and the digital logic. The SIE is a state machine that transfers data to and from the endpoint buffers, and generates the hardware protocol for data transfers. The dedicated USB DMA Controller transfers data between the data buffers in RAM and the SIE. The integrated pull-up and pull-down resistors eliminate the need for external signaling components. The register interface allows the CPU to configure and communicate with the module.

The USB module includes the following features:

- USB Full-Speed Support for Host and Device
- Low-Speed Support for Host and Device
- USB OTG Support
- Integrated Signaling Resistors
- Integrated Analog Comparators for VBUS Monitoring
- Integrated USB Transceiver
- Transaction Handshaking performed by Hardware
- Endpoint Buffering anywhere in System RAM
- Integrated DMA to access System RAM and Flash

> **Note:** The implementation and use of the USB specifications, as well as other third party specifications or technologies, may require licensing; including, but not limited to, USB Implementers Forum, Inc. (also referred to as USB-IF). The user is fully responsible for investigating and satisfying any applicable licensing obligations.

> **Note:** Adding any circuitry to the USB D+/D- pins, other than the connection to a USB connector, may degrade the USB signal quality and violate USB specifications.

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18.4 Powering the USB Transceiver

The V_{USB3V3} pin is used to power the USB transceiver. During USB operation, this provides the power for USB transceiver drivers. When the USB module is disabled, this pin can be used to bias the transceiver circuit to prevent additional current draw when using RB10 and/or RB11 as GPIOs.

Available options for V_{USB} power:

1. For USB operation, an external power source is required. For voltage compliant USB operation, the voltage applied to V_{USB3V3} must be in the range specified by Parameter USB313 in Table 29-38 regardless of the device operating voltage. If the device V_{DD} voltage meets these requirements, it can be used to power V_{USB3V3}.
2. For non-USB operation with RB11 and/or RB10 as GPIOs, the USB module must be disabled and power applied to V_{USB3V3} via V_{DD}.
3. For non-USB operation without using RB11 and/or RB10, the V_{USB3V3} pin should be connected to ground. This configuration has the lowest operating current.

Note:	To prevent additional current draw, V_{USB3V3} must either be powered or grounded.

18.4.1 OPERATION OF PORT PINS SHARED WITH THE USB TRANSCEIVER

The USB transceiver shares pins with GPIO port pins. The D+ pin is shared with RB11 and the D- pin is shared with RB10. When the USB module is enabled, the pins are controlled by the module as D+ and D-, and are not usable as GPIOs. When the module is disabled, the pins can be used as RB11 and RB10 GPIOs if the V_{USB3V3} pin is powered internally or externally. Refer to **Section 18.4 "Powering the USB Transceiver"** for more information.

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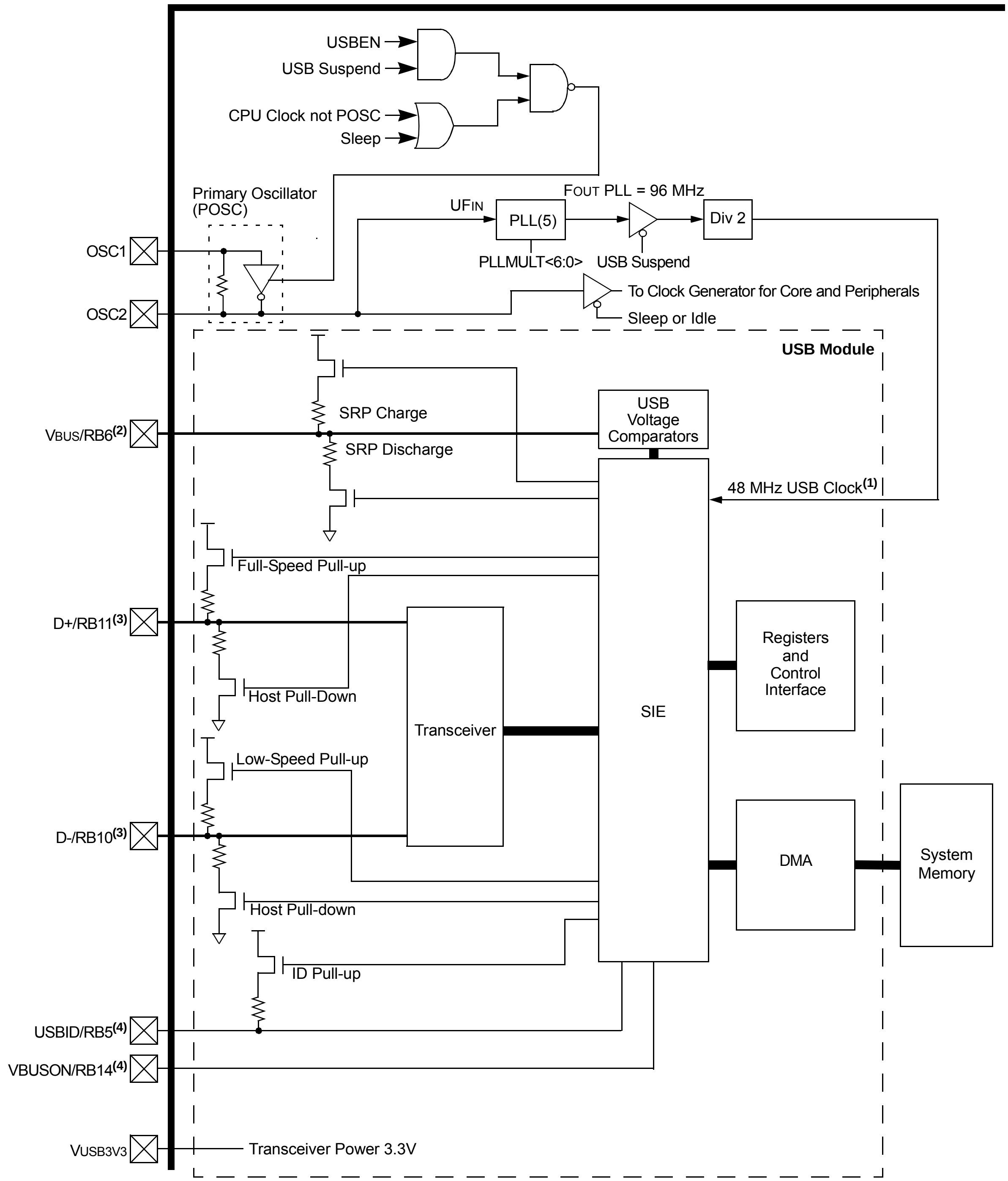
FIGURE 18-1: PIC32MM0256GPM064 FAMILY USB INTERFACE DIAGRAM



Note 1: A 48 MHz clock is required for proper USB operation.

2: This pin can be used as a GPIO when the USB module is disabled.

3: This pin can be used as a GPIO if the USB module is disabled and powered by an external source.

4: This pin is controlled by the USB module when the module is enabled in Host or OTG mode. If the module is disabled or enabled in a mode that does not require it, this pin can be reclaimed via a device Configuration bit (refer to Register 26-1).

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TABLE 18-1: USB OTG REGISTER MAP

Virtual Address (BF88_#)	Register Name[1]	Bit Range	Bits 31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
8440	U1OTGIR[2]	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	IDIF	T1MSECIF	LSTATEIF	ACTVIF	SESVDIF	SESENDIF	—	VBUSVDIF	0000
8450	U1OTGIE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	IDIE	T1MSECIE	LSTATEIE	ACTVIE	SESVDIE	SESENDIE	—	VBUSVDIE	0000
8460	U1OTGSTAT[3]	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	ID	—	LSTATE	—	SESVD	SESEND	—	VBUSVD	0000
8470	U1OTGCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	DPPULUP	DMPULUP	DPPULDWN	DMPULDWN	VBUSON	OTGEN	VBUSCHG	VBUSDIS	0000
8480	U1PWRC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	UACTPND[4]	—	—	USLPGRD	USBBUSY	—	USUSPEND	USBPWR	0000
8600	U1IR[2]	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	STALLIF	ATTACHIF	RESUMEIF	IDLEIF	TRNIF	SOFIF	UERRIF	URSTIF DETACHIF	0000 0000
8610	U1IE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	STALLIE	ATTACHIE	RESUMEIE	IDLEIE	TRNIE	SOFIE	UERRIE	URSTIE DETACHIE	0000 0000
8620	U1EIR[2]	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	BTSEF	BMXEF	DMAEF	BTOEF	DFN8EF	CRC16EF	CRC5EF EOFEF	PIDEF	0000 0000
8630	U1EIE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	BTSEE	BMXEE	DMAEE	BTOEE	DFN8EE	CRC16EE	CRC5EE EOFEE	PIDEE	0000 0000
8640	U1STAT[3]	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	ENDPT<3:0>[4]				DIR	PPBI	—	—	0000
8650	U1CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	JSTATE[4]	SE0[4]	PKTDIS TOKBUSY	USBRST	HOSTEN	RESUME	PPBRST	USBEN SOFEN	0000 0000
8660	U1ADDR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	LSPDEN	DEVADDR<6:0>							0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table (except as noted) have corresponding CLR, SET and INV registers at their virtual address, plus an offset of 0x4, 0x8 and 0xC respectively. See **Section 10.1 "CLR, SET and INV Registers"** for more information.

2: This register does not have associated SET and INV registers.

3: This register does not have associated CLR, SET and INV registers.

4: Reset value for these bits is undefined.

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TABLE 18-1: USB OTG REGISTER MAP (CONTINUED)

Virtual Address (BF88_#)	Register Name[1]	Bit Range	Bits 31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
8670	U1BDTP1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	BDTPTRL<7:1>							—	0000
8680	U1FRML[3]	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	FRML<7:0>								0000
8690	U1FRMH[3]	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	FRMH<2:0>			0000
86A0	U1TOK	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	PID<3:0>				EP<3:0>				0000
86B0	U1SOF	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	CNT<7:0>								0000
86C0	U1BDTP2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	BDTPTRH<7:0>								0000
86D0	U1BDTP3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	BDTPTRU<7:0>								0000
86E0	U1CNFG1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	UTEYE	UOEMON	—	USBSIDL	LSDEV	—	—	UASUSPND	0001
8700	U1EP0	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	LSPD	RETRYDIS	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
8710	U1EP1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
8720	U1EP2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
8730	U1EP3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
8740	U1EP4	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
8750	U1EP5	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
8760	U1EP6	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table (except as noted) have corresponding CLR, SET and INV registers at their virtual address, plus an offset of 0x4, 0x8 and 0xC respectively. See **Section 10.1 "CLR, SET and INV Registers"** for more information.

2: This register does not have associated SET and INV registers.

3: This register does not have associated CLR, SET and INV registers.

4: Reset value for these bits is undefined.

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TABLE 18-1: USB OTG REGISTER MAP (CONTINUED)

Virtual Address (BF88_#)	Register Name[1]	Bit Range	Bits 31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
8770	U1EP7	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
8780	U1EP8	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
8790	U1EP9	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
87A0	U1EP10	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
87B0	U1EP11	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
87C0	U1EP12	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
87D0	U1EP13	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
87E0	U1EP14	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
87F0	U1EP15	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table (except as noted) have corresponding CLR, SET and INV registers at their virtual address, plus an offset of 0x4, 0x8 and 0xC respectively. See **Section 10.1 "CLR, SET and INV Registers"** for more information.

2: This register does not have associated SET and INV registers.

3: This register does not have associated CLR, SET and INV registers.

4: Reset value for these bits is undefined.

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18.5 Control Registers

REGISTER 18-1: U1OTGIR: USB OTG INTERRUPT STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/WC-0, HS	R/WC-0, HS	R/WC-0, HS	R/WC-0, HS	R/WC-0, HS	R/WC-0, HS	U-0	R/WC-0, HS
	IDIF	T1MSECIF	LSTATEIF	ACTVIF	SESVDIF	SESENDIF	—	VBUSVDIF

Legend:	WC = Write ‘1’ to Clear bit	HS = Hardware Settable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as ‘0’

bit 7 **IDIF:** ID State Change Indicator bit
1 = Change in ID state is detected
0 = No change in ID state is detected

bit 6 **T1MSECIF:** 1 Millisecond Timer bit
1 = 1 millisecond timer has expired
0 = 1 millisecond timer has not expired

bit 5 **LSTATEIF:** Line State Stable Indicator bit
1 = USB line state has been stable for 1 ms, but different from last time
0 = USB line state has not been stable for 1 ms

bit 4 **ACTVIF:** Bus Activity Indicator bit
1 = Activity on the D+, D-, ID or VBUS pins has caused the device to wake-up
0 = Activity has not been detected

bit 3 **SESVDIF:** Session Valid Change Indicator bit
1 = VBUS voltage has dropped below the session end level
0 = VBUS voltage has not dropped below the session end level

bit 2 **SESENDIF:** B-Device VBUS Change Indicator bit
1 = Change on the session end input was detected
0 = No change on the session end input was detected

bit 1 **Unimplemented:** Read as ‘0’

bit 0 **VBUSVDIF:** A-Device VBUS Change Indicator bit
1 = Change on the session valid input was detected
0 = No change on the session valid input was detected

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REGISTER 18-2: U1OTGIE: USB OTG INTERRUPT ENABLE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0
	IDIE	T1MSECIE	LSTATEIE	ACTVIE	SESVDIE	SESENDIE	—	VBUSVDIE

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as ‘0’

bit 7 **IDIE:** ID Interrupt Enable bit
1 = ID interrupt is enabled
0 = ID interrupt is disabled

bit 6 **T1MSECIE:** 1 Millisecond Timer Interrupt Enable bit
1 = 1 millisecond timer interrupt is enabled
0 = 1 millisecond timer interrupt is disabled

bit 5 **LSTATEIE:** Line State Interrupt Enable bit
1 = Line state interrupt is enabled
0 = Line state interrupt is disabled

bit 4 **ACTVIE:** Bus Activity Interrupt Enable bit
1 = Activity interrupt is enabled
0 = Activity interrupt is disabled

bit 3 **SESVDIE:** Session Valid Interrupt Enable bit
1 = Session valid interrupt is enabled
0 = Session valid interrupt is disabled

bit 2 **SESENDIE:** B-Session End Interrupt Enable bit
1 = B-session end interrupt is enabled
0 = B-session end interrupt is disabled

bit 1 **Unimplemented:** Read as ‘0’

bit 0 **VBUSVDIE:** A-VBUS Valid Interrupt Enable bit
1 = A-VBUS valid interrupt is enabled
0 = A-VBUS valid interrupt is disabled

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REGISTER 18-3: U1OTGSTAT: USB OTG STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R-0	U-0	R-0	U-0	R-0	R-0	U-0	R-0
	ID	—	LSTATE	—	SESVD	SESEND	—	VBUSVD

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as ‘0’

bit 7 **ID:** ID Pin State Indicator bit
1 = No cable is attached or a “Type B” cable has been inserted into the USB receptacle
0 = A “Type A” OTG cable has been inserted into the USB receptacle

bit 6 **Unimplemented:** Read as ‘0’

bit 5 **LSTATE:** Line State Stable Indicator bit
1 = USB line state (SE0 (U1CON<6> and JSTATE (U1CON<7>) has been stable for the previous 1 ms
0 = USB line state (SE0 (U1CON<6> and JSTATE (U1CON<7>) has not been stable for the previous 1 ms

bit 4 **Unimplemented:** Read as ‘0’

bit 3 **SESVD:** Session Valid Indicator bit
1 = The VBUS voltage is above VA_SESS_VLD (as defined in the USB OTG Specification) on the A or B-device
0 = The VBUS voltage is below VA_SESS_VLD on the A or B-device

bit 2 **SESEND:** B-Device Session End Indicator bit
1 = The VBUS voltage is above VB_SESS_END (as defined in the USB OTG Specification) on the B-device
0 = The VBUS voltage is below VB_SESS_END on the B-device

bit 1 **Unimplemented:** Read as ‘0’

bit 0 **VBUSVD:** A-Device VBUS Valid Indicator bit
1 = The VBUS voltage is above VA_VBUS_VLD (as defined in the USB OTG Specification) on the A-device
0 = The VBUS voltage is below VA_VBUS_VLD on the A-device

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REGISTER 18-4: U1OTGCON: USB OTG CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DPPULUP	DMPULUP	DPPULDWN	DMPULDWN	VBUSON	OTGEN	VBUSCHG	VBUSDIS

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **DPPULUP:** D+ Pull-Up Enable bit
1 = D+ data line pull-up resistor is enabled
0 = D+ data line pull-up resistor is disabled

bit 6 **DMPULUP:** D- Pull-Up Enable bit
1 = D- data line pull-up resistor is enabled
0 = D- data line pull-up resistor is disabled

bit 5 **DPPULDWN:** D+ Pull-Down Enable bit
1 = D+ data line pull-down resistor is enabled
0 = D+ data line pull-down resistor is disabled

bit 4 **DMPULDWN:** D- Pull-Down Enable bit
1 = D- data line pull-down resistor is enabled
0 = D- data line pull-down resistor is disabled

bit 3 **VBUSON:** VBUS Power-on bit
1 = VBUS line is powered
0 = VBUS line is not powered

bit 2 **OTGEN:** OTG Functionality Enable bit
1 = DPPULUP, DMPULUP, DPPULDWN and DMPULDWN bits are under software control
0 = DPPULUP, DMPULUP, DPPULDWN and DMPULDWN bits are under USB hardware control

bit 1 **VBUSCHG:** VBUS Charge Enable bit
1 = VBUS line is charged through a pull-up resistor
0 = VBUS line is not charged through a resistor

bit 0 **VBUSDIS:** VBUS Discharge Enable bit
1 = VBUS line is discharged through a pull-down resistor
0 = VBUS line is not discharged through a resistor

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REGISTER 18-5: U1PWRC: USB POWER CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R-0	U-0	U-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0
	UACTPND	—	—	USLPGRD	USBBUSY(1)	—	USUSPEND	USBPWR(1)

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **UACTPND:** USB Activity Pending bit

1 = USB bus activity has been detected, but an interrupt is pending; it has not been generated yet
0 = An interrupt is not pending

bit 6-5 **Unimplemented:** Read as '0'

bit 4 **USLPGRD:** USB Sleep Entry Guard bit

1 = Sleep entry is blocked if USB bus activity is detected or if a notification is pending
0 = USB module does not block Sleep entry

bit 3 **USBBUSY:** USB Module Busy bit(1)

1 = USB module is active or disabled, but not ready to be enabled
0 = USB module is not active and is ready to be enabled

bit 2 **Unimplemented:** Read as '0'

bit 1 **USUSPEND:** USB Suspend Mode bit

1 = USB module is placed in Suspend mode
(The 48 MHz USB clock will be gated off. The transceiver is placed in a low-power state.)
0 = USB module operates normally

bit 0 **USBPWR:** USB Operation Enable bit(1)

1 = USB module is turned on
0 = USB module is disabled
(Outputs held inactive, device pins not used by USB, analog features are shut down to reduce power consumption.)

Note 1: When USBPWR = 0 and USBBUSY = 1, status from all other registers is invalid and writes to all USB module registers produce undefined results.

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REGISTER 18-6: U1IR: USB INTERRUPT REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/WC-0, HS	R/WC-0, HS	R/WC-0, HS	R/WC-0, HS	R/WC-0, HS	R/WC-0, HS	R-0	R/WC-0, HS
	STALLIF	ATTACHIF(1)	RESUMEIF(2)	IDLEIF	TRNIF(3)	SOFIF	UERRIF(4)	URSTIF(5) DETACHIF(6)

Legend:	WC = Write '1' to Clear bit	HS = Hardware Settable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **STALLIF:** Stall Handshake Interrupt bit
1 = In Host mode, a Stall handshake was received during the handshake phase of the transaction; in Device mode, a Stall handshake was transmitted during the handshake phase of the transaction
0 = Stall handshake has not been sent

bit 6 **ATTACHIF:** Peripheral Attach Interrupt bit(1)
1 = Peripheral attachment was detected by the USB module
0 = Peripheral attachment was not detected

bit 5 **RESUMEIF:** Resume Interrupt bit(2)
1 = K-State is observed on the D+ or D- pin for 2.5 μs
0 = K-State is not observed

bit 4 **IDLEIF:** Idle Detect Interrupt bit
1 = Idle condition detected (constant Idle state of 3 ms or more)
0 = No Idle condition detected

bit 3 **TRNIF:** Token Processing Complete Interrupt bit(3)
1 = Processing of current token is complete; a read of the U1STAT register will provide endpoint information
0 = Processing of current token not complete

bit 2 **SOFIF:** SOF Token Interrupt bit
1 = SOF token received by the peripheral or the SOF threshold reached by the host
0 = SOF token was not received nor threshold reached

bit 1 **UERRIF**: USB Error Condition Interrupt bit(4)
1 = Unmasked error condition has occurred
0 = Unmasked error condition has not occurred

Note 1: This bit is only valid if the HOSTEN bit is set (see Register 18-11), there is no activity on the USB for 2.5 μs and the current bus state is not SE0.
2: When not in Suspend mode, this interrupt should be disabled.
3: Clearing this bit will cause the STAT FIFO to advance.
4: Only error conditions enabled through the U1EIE register will set this bit.
5: Device mode.
6: Host mode.

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REGISTER 18-6: U1IR: USB INTERRUPT REGISTER (CONTINUED)

bit 0 **URSTIF:** USB Reset Interrupt bit (Device mode)[5]
1 = Valid USB Reset has occurred
0 = No USB Reset has occurred

DETACHIF: USB Detach Interrupt bit (Host mode)[6]
1 = Peripheral detachment was detected by the USB module
0 = Peripheral detachment was not detected

Note 1: This bit is only valid if the HOSTEN bit is set (see Register 18-11), there is no activity on the USB for 2.5 μs and the current bus state is not SE0.

2: When not in Suspend mode, this interrupt should be disabled.

3: Clearing this bit will cause the STAT FIFO to advance.

4: Only error conditions enabled through the U1EIE register will set this bit.

5: Device mode.

6: Host mode.

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REGISTER 18-7: U1IE: USB INTERRUPT ENABLE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	STALLIE	ATTACHIE	RESUMEIE	IDLEIE	TRNIE	SOFIE	UERRIE(1)	URSTIE(2) DETACHIE(3)

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as ‘0’

bit 7 **STALLIE:** Stall Handshake Interrupt Enable bit
1 = Stall interrupt is enabled
0 = Stall interrupt is disabled

bit 6 **ATTACHIE:** Attach Interrupt Enable bit
1 = Attach interrupt is enabled
0 = Attach interrupt is disabled

bit 5 **RESUMEIE:** Resume Interrupt Enable bit
1 = Resume interrupt is enabled
0 = Resume interrupt is disabled

bit 4 **IDLEIE:** Idle Detect Interrupt Enable bit
1 = Idle interrupt is enabled
0 = Idle interrupt is disabled

bit 3 **TRNIE:** Token Processing Complete Interrupt Enable bit
1 = TRNIF interrupt is enabled
0 = TRNIF interrupt is disabled

bit 2 **SOFIE:** SOF Token Interrupt Enable bit
1 = SOFIF interrupt is enabled
0 = SOFIF interrupt is disabled

bit 1 **UERRIE:** USB Error Interrupt Enable bit(1)
1 = USB error interrupt is enabled
0 = USB error interrupt is disabled

bit 0 **URSTIE:** USB Reset Interrupt Enable bit(2)
1 = URSTIF interrupt is enabled
0 = URSTIF interrupt is disabled

DETACHIE: USB Detach Interrupt Enable bit(3)
1 = DATTCHIF interrupt is enabled
0 = DATTCHIF interrupt is disabled

Note 1: For an interrupt to propagate USBIF, the UERRIE bit (U1IE<1>) must be set.
2: Device mode.
3: Host mode.

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REGISTER 18-8: U1EIR: USB ERROR INTERRUPT STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/WC-0, HS	R/WC-0, HS	R/WC-0, HS	R/WC-0, HS	R/WC-0, HS	R/WC-0, HS	R/WC-0, HS	R/WC-0, HS
	BTSEF	BMXEF	DMAEF(1)	BTOEF(2)	DFN8EF	CRC16EF	CRC5EF(4) EOFEF(3,5)	PIDEF

Legend:	WC = Write ‘1’ to Clear bit	HS = Hardware Settable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as ‘0’

bit 7 **BTSEF:** Bit Stuff Error Flag bit
1 = Packet rejected due to bit stuff error
0 = Packet accepted

bit 6 **BMXEF:** Bus Matrix Error Flag bit
1 = Invalid base address of the BDT or the address of an individual buffer pointed to by a BDT entry
0 = No address error

bit 5 **DMAEF:** DMA Error Flag bit(1)
1 = USB DMA error condition detected
0 = No DMA error

bit 4 **BTOEF:** Bus Turnaround Time-out Error Flag bit(2)
1 = Bus turnaround time-out has occurred
0 = No bus turnaround time-out has occurred

bit 3 **DFN8EF:** Data Field Size Error Flag bit
1 = Data field received is not an integral number of bytes
0 = Data field received is an integral number of bytes

bit 2 **CRC16EF:** CRC16 Failure Flag bit
1 = Data packet rejected due to CRC16 error
0 = Data packet accepted

Note 1: This type of error occurs when the module’s request for the DMA bus is not granted in time to service the module’s demand for memory, resulting in an overflow or underflow condition, and/or the allocated buffer size is not sufficient to store the received data packet causing it to be truncated.

2: This type of error occurs when more than 16-bit times of Idle from the previous End-of-Packet (EOP) has elapsed.

3: This type of error occurs when the module is transmitting or receiving data and the SOF counter has reached zero.

4: Device mode.

5: Host mode.

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REGISTER 18-8: U1EIR: USB ERROR INTERRUPT STATUS REGISTER (CONTINUED)

bit 1 **CRC5EF:** CRC5 Host Error Flag bit[4]

1 = Token packet rejected due to CRC5 error
0 = Token packet accepted

EOFEF: EOF Error Flag bit[3,5]

1 = EOF error condition detected
0 = No EOF error condition

bit 0 **PIDEF:** PID Check Failure Flag bit

1 = PID check failed
0 = PID check passed

Note 1: This type of error occurs when the module's request for the DMA bus is not granted in time to service the module's demand for memory, resulting in an overflow or underflow condition, and/or the allocated buffer size is not sufficient to store the received data packet causing it to be truncated.

2: This type of error occurs when more than 16-bit times of Idle from the previous End-of-Packet (EOP) has elapsed.

3: This type of error occurs when the module is transmitting or receiving data and the SOF counter has reached zero.

4: Device mode.

5: Host mode.

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REGISTER 18-9: U1EIE: USB ERROR INTERRUPT ENABLE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BTSEE	BMXEE	DMAEE	BTOEE	DFN8EE	CRC16EE	CRC5EE(1) / EOFEE(2)	PIDEE

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as ‘0’

bit 7 **BTSEE:** Bit Stuff Error Interrupt Enable bit
1 = BTSEF interrupt is enabled
0 = BTSEF interrupt is disabled

bit 6 **BMXEE:** Bus Matrix Error Interrupt Enable bit
1 = BMXEF interrupt is enabled
0 = BMXEF interrupt is disabled

bit 5 **DMAEE:** DMA Error Interrupt Enable bit
1 = DMAEF interrupt is enabled
0 = DMAEF interrupt is disabled

bit 4 **BTOEE:** Bus Turnaround Time-out Error Interrupt Enable bit
1 = BTOEF interrupt is enabled
0 = BTOEF interrupt is disabled

bit 3 **DFN8EE:** Data Field Size Error Interrupt Enable bit
1 = DFN8EF interrupt is enabled
0 = DFN8EF interrupt is disabled

bit 2 **CRC16EE:** CRC16 Failure Interrupt Enable bit
1 = CRC16EF interrupt is enabled
0 = CRC16EF interrupt is disabled

bit 1 **CRC5EE:** CRC5 Host Error Interrupt Enable bit(1)
1 = CRC5EF interrupt is enabled
0 = CRC5EF interrupt is disabled

EOFEE: EOF Error Interrupt Enable bit(2)
1 = EOF interrupt is enabled
0 = EOF interrupt is disabled

bit 0 **PIDEE:** PID Check Failure Interrupt Enable bit
1 = PIDEF interrupt is enabled
0 = PIDEF interrupt is disabled

Note 1: Device mode.
2: Host mode.

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REGISTER 18-10: U1STAT: USB STATUS REGISTER[(1)]

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R-x	R-x	R-x	R-x	R-x	R-x	U-0	U-0
	ENDPT<3:0>				DIR	PPBI	—	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as ‘0’

bit 7-4 **ENDPT<3:0>:** Encoded Number of Last Endpoint Activity bits
(Represents the number of the BDT, updated by the last USB transfer.)
`1111` = Endpoint 15
`1110` = Endpoint 14
•
•
•
`0001` = Endpoint 1
`0000` = Endpoint 0

bit 3 **DIR:** Last Buffer Descriptor Direction Indicator bit
`1` = Last transaction was a transmit transfer (TX)
`0` = Last transaction was a receive transfer (RX)

bit 2 **PPBI:** Ping-Pong Buffer Descriptor Pointer Indicator bit
`1` = Last transaction was to the Odd buffer descriptor bank
`0` = Last transaction was to the Even buffer descriptor bank

bit 1-0 **Unimplemented:** Read as ‘0’

Note 1: The U1STAT register is a window into a 4-byte FIFO maintained by the USB module. The U1STAT value is only valid when TRNIF (U1IR<3>) is active. Clearing the TRNIF bit advances the FIFO. The data in the register is invalid when TRNIF = `0`.

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REGISTER 18-11: U1CON: USB CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R-x	R-x	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	JSTATE	SE0	PKTDIS[(4)] TOKBUSY[(1,5)]	USBRST	HOSTEN[(2)]	RESUME[(3)]	PPBRST	USBEN[(4)] SOFEN[(5)]

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **JSTATE:** Live Differential Receiver JSTATE Flag bit
1 = JSTATE was detected on the USB
0 = JSTATE was not detected

bit 6 **SE0:** Live Single-Ended Zero Flag bit
1 = Single-ended zero was detected on the USB
0 = Single-ended zero was not detected

bit 5 **PKTDIS:** Packet Transfer Disable bit[(4)]
1 = Token and packet processing are disabled (set upon SETUP token received)
0 = Token and packet processing are enabled

TOKBUSY: Token Busy Indicator bit[(1,5)]
1 = Token is being executed by the USB module
0 = No token is being executed

bit 4 **USBRST:** Module Reset bit
1 = USB Reset is generated
0 = USB Reset is terminated

bit 3 **HOSTEN:** Host Mode Enable bit[(2)]
1 = USB host capability is enabled
0 = USB host capability is disabled

bit 2 **RESUME:** Resume Signaling Enable bit[(3)]
1 = Resume signaling is activated
0 = Resume signaling is disabled

Note 1: Software is required to check this bit before issuing another token command to the U1TOK register (see Register 18-15).
2: All host control logic is reset any time that the value of this bit is toggled.
3: Software must set RESUME for 10 ms in Device mode, or for 25 ms in Host mode, and then clear it to enable remote wake-up. In Host mode, the USB module will append a low-speed EOP to the Resume signaling when this bit is cleared.
4: Device mode.
5: Host mode.

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REGISTER 18-11: U1CON: USB CONTROL REGISTER (CONTINUED)

bit 1 **PPBRST:** Ping-Pong Buffers Reset bit

1 = Resets all Even/Odd Buffer Pointers to the Even buffer descriptor banks
0 = Even/Odd Buffer Pointers are not reset

bit 0 **USBEN:** USB Module Enable bit(4)

1 = USB module and supporting circuitry are enabled
0 = USB module and supporting circuitry are disabled

SOFEN: SOF Enable bit(5)

1 = SOF token is sent every 1 ms
0 = SOF token is disabled

Note 1: Software is required to check this bit before issuing another token command to the U1TOK register (see Register 18-15).

2: All host control logic is reset any time that the value of this bit is toggled.

3: Software must set RESUME for 10 ms in Device mode, or for 25 ms in Host mode, and then clear it to enable remote wake-up. In Host mode, the USB module will append a low-speed EOP to the Resume signaling when this bit is cleared.

4: Device mode.

5: Host mode.

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REGISTER 18-12: U1ADDR: USB ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	LSPDEN	DEVADDR<6:0>						

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as ‘0’

bit 7 **LSPDEN:** Low-Speed Enable Indicator bit
1 = Next token command to be executed at low speed
0 = Next token command to be executed at full speed

bit 6-0 **DEVADDR<6:0>:** 7-Bit USB Device Address bits

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REGISTER 18-13: U1FRML: USB FRAME NUMBER LOW REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	FRML<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as ‘0’

bit 7-0 **FRML<7:0>:** 11-Bit Frame Number Lower bits
These register bits are updated with the current frame number whenever a SOF token is received.

REGISTER 18-14: U1FRMH: USB FRAME NUMBER HIGH REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	R-0	R-0	R-0
	—	—	—	—	—	FRMH<2:0>		

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-3 **Unimplemented:** Read as ‘0’

bit 2-0 **FRMH<2:0>:** Upper 3 Bits of the Frame Numbers bits
These register bits are updated with the current frame number whenever a SOF token is received.

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REGISTER 18-15: U1TOK: USB TOKEN REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PID<3:0>(1)				EP<3:0>			

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as ‘0’

bit 7-4 **PID<3:0>:** Token Type Indicator bits(1)
- `1101` = SETUP (TX) token type transaction
- `1001` = IN (RX) token type transaction
- `0001` = OUT (TX) token type transaction

bit 3-0 **EP<3:0>:** Token Command Endpoint Address bits
The 4-bit value must specify a valid endpoint.

Note 1: All other values not listed are reserved and must not be used.

REGISTER 18-16: U1SOF: USB SOF THRESHOLD REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CNT<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as ‘0’

bit 7-0 **CNT<7:0>:** SOF Threshold Value bits
<u>Typical Values of the Threshold are:</u>
- `01001010` = 64-byte packet
- `00101010` = 32-byte packet
- `00011010` = 16-byte packet
- `00010010` = 8-byte packet

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REGISTER 18-17: U1BDTP1: USB BUFFER DESCRIPTOR TABLE PAGE 1 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0
	BDTPTRL<7:1>							—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as ‘0’

bit 7-1 **BDTPTRL<7:1>:** BDT Base Address bits

This 7-bit value provides Address bits 7 through 1 of the BDT base address, which defines the starting location of the BDT in system memory.

The 32-bit BDT base address is 512-byte aligned.

bit 0 **Unimplemented:** Read as ‘0’

REGISTER 18-18: U1BDTP2: USB BUFFER DESCRIPTOR TABLE PAGE 2 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BDTPTRH<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as ‘0’

bit 7-0 **BDTPTRH<7:0>:** BDT Base Address bits

This 8-bit value provides Address bits 7 through 0 of the BDT base address, which defines the starting location of the BDT in system memory.

The 32-bit BDT base address is 512-byte aligned.

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REGISTER 18-19: U1BDTP3: USB BUFFER DESCRIPTOR TABLE PAGE 3 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BDTPTRU<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as ‘0’

bit 7-0 **BDTPTRU<7:0>:** BDT Base Address bits

This 8-bit value provides Address bits 7 through 0 of the BDT base address, defines the starting location of the BDT in system memory.

The 32-bit BDT base address is 512-byte aligned.

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REGISTER 18-20: U1CNFG1: USB CONFIGURATION 1 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	U-0	U-0	R/W-0
	UTEYE	UOEMON	—	USBSIDL	LSDEV	—	—	UASUSPND

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as ‘0’

bit 7 **UTEYE:** USB Eye Pattern Test Enable bit
1 = Eye pattern test is enabled
0 = Eye pattern test is disabled

bit 6 **UOEMON:** USB $\overline{\text{OE}}$ Monitor Enable bit
1 = $\overline{\text{OE}}$ signal is active; it indicates intervals during which the D+/D- lines are driving
0 = $\overline{\text{OE}}$ signal is inactive

bit 5 **Unimplemented:** Read as ‘0’

bit 4 **USBSIDL:** USB Stop in Idle Mode bit
1 = Discontinues module operation when device enters Idle mode
0 = Continues module operation in Idle mode

bit 3 **LSDEV:** USB Low-Speed Device Enable bit
1 = USB macro operates in Low-Speed Device Only mode
0 = USB macro operates in OTG, Host or Fast Speed Device mode

bit 2-1 **Unimplemented:** Read as ‘0’

bit 0 **UASUSPND:** Automatic Suspend Enable bit
1 = USB module automatically suspends upon entry to Sleep mode; see the USUSPEND bit (U1PWRC<1>) in Register 18-5
0 = USB module does not automatically suspend upon entry to Sleep mode; software must use the USUSPEND bit (U1PWRC<1>) to suspend the module, including the USB 48 MHz clock

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REGISTER 18-21: U1EP0-U1EP15: USB ENDPOINT CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	LSPD	RETRYDIS	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **LSPD:** Low-Speed Direct Connection Enable bit (Host mode and U1EP0 only)
1 = Direct connection to a low-speed device is enabled
0 = Direct connection to a low-speed device is disabled; hub required with PRE_PID

bit 6 **RETRYDIS:** Retry Disable bit (Host mode and U1EP0 only)
1 = Retry NACK'd transactions are disabled
0 = Retry NACK'd transactions are enabled; retry done in hardware

bit 5 **Unimplemented:** Read as '0'

bit 4 **EPCONDIS:** Bidirectional Endpoint Control bit
If EPTXEN = 1 and EPRXEN = 1:
1 = Disables Endpoint n from control transfers; only TX and RX transfers are allowed
0 = Enables Endpoint n for control (SETUP) transfers; TX and RX transfers are also allowed
Otherwise, this bit is ignored.

bit 3 **EPRXEN:** Endpoint Receive Enable bit
1 = Endpoint n receive is enabled
0 = Endpoint n receive is disabled

bit 2 **EPTXEN:** Endpoint Transmit Enable bit
1 = Endpoint n transmit is enabled
0 = Endpoint n transmit is disabled

bit 1 **EPSTALL:** Endpoint Stall Status bit
1 = Endpoint n was stalled
0 = Endpoint n was not stalled

bit 0 **EPHSHK:** Endpoint Handshake Enable bit
1 = Endpoint handshake is enabled
0 = Endpoint handshake is disabled (typically used for isochronous endpoints)

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NOTES:

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19.0 REAL-TIME CLOCK AND CALENDAR (RTCC)

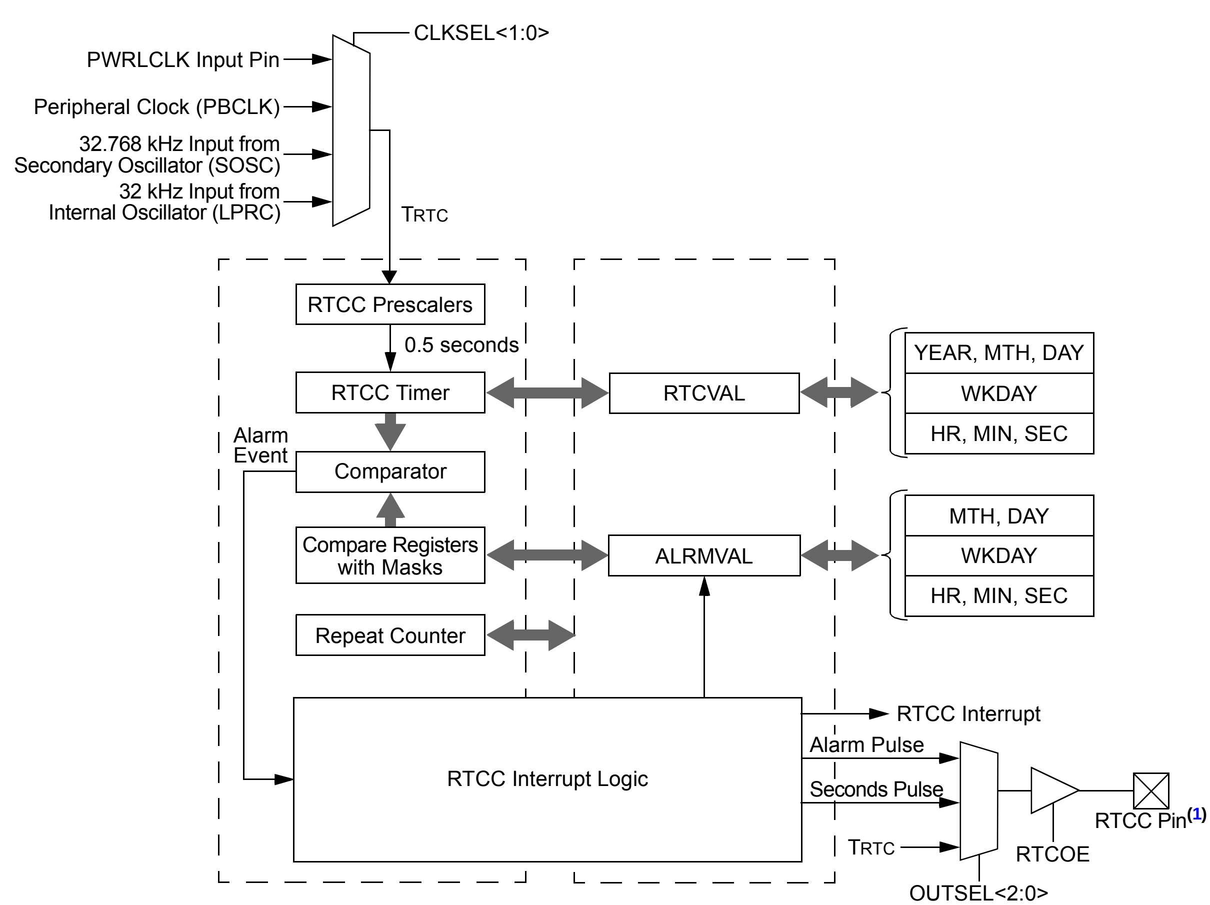
Note:	This data sheet summarizes the features of the PIC32MM0256GPM064 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 28. "RTCC with Timestamp"** (DS60001362) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32). The information in this data sheet supersedes the information in the FRM.

The RTCC module is intended for applications in which accurate time must be maintained for extended periods of time with minimal or no CPU intervention. Low-power optimization provides extended battery lifetime while keeping track of time.

Key features of the RTCC module are:

- Time: Hours, Minutes and Seconds
- 24-Hour Format (military time)
- Visibility of One-Half Second Period
- Provides Calendar: Weekday, Date, Month and Year
- Alarm Intervals are Configurable for Half of a Second, 1 Second, 10 Seconds, 1 Minute, 10 Minutes, 1 Hour, 1 Day, 1 Week, 1 Month and 1 Year
- Alarm Repeat with Decrementing Counter
- Alarm with Indefinite Repeat: Chime
- Year Range: 2000 to 2099
- Leap Year Correction
- BCD Format for Smaller Firmware Overhead
- Optimized for Long-Term Battery Operation
- Fractional Second Synchronization
- User Calibration of the Clock Crystal Frequency with Auto-Adjust
- Uses External 32.768 kHz Crystal, 32 kHz Internal Oscillator, PWRLCLK Input Pin or Peripheral Clock
- Alarm Pulse, Seconds Clock or Internal Clock Output on RTCC Pin

FIGURE 19-1: RTCC BLOCK DIAGRAM



Note 1: In Retention mode, the maximum peripheral output frequency to an I/O pin must be limited to 33 kHz or less.

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19.1 RTCC Control Registers

TABLE 19-1: RTCC REGISTER MAP

Virtual Address (BF80_#)	Register Name[1]	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
0000	RTCCON1	31:16	ALRMEN	CHIME	—	—	AMASK<3:0>				ALMRPT<7:0>								0000
		15:0	ON	—	—	—	WRLOCK	—	—	—	RTCOE	OUTSEL<2:0>			—	—	—	—	0000
0010	RTCCON2	31:16	DIV<15:0>																0000
		15:0	FDIV<4:0>					—	—	—	—	—	PS<1:0>		—	—	CLKSEL<1:0>		0000
0030	RTCSTAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	ALMEVT	—	—	SYNC	ALMSYNC	HALFSEC	0000
0040	RTCTIME	31:16	—	HRTEN<2:0>			HRONE<3:0>				—	MINTEN<2:0>			MINONE<3:0>				xxxx
		15:0	SECTEN<3:0>				SECONE<3:0>				—	—	—	—	—	—	—	—	xx00
0050	RTCDATE	31:16	YRTEN<3:0>				YRONE<3:0>				—	—	—	MTHTEN	MTHONE<3:0>				0000
		15:0	—	—	DAYTEN<1:0>		DAYONE<3:0>				—	—	—	—	—	WDAY<2:0>			0000
0060	ALMTIME	31:16	—	HRTEN<2:0>			HRONE<3:0>				—	MINTEN<2:0>			MINONE<3:0>				xxxx
		15:0	SECTEN<3:0>				SECONE<3:0>				—	—	—	—	—	—	—	—	xx00
0070	ALMDATE	31:16	—	—	—	—	—	—	—	—	—	—	—	MTHTEN	MTHONE<3:0>				0000
		15:0	—	—	DAYTEN<1:0>		DAYONE<3:0>				—	—	—	—	—	WDAY<2:0>			0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively.

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REGISTER 19-1: RTCCON1: RTCC CONTROL 1 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	ALRMEN	CHIME	—	—	AMASK<3:0>			
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ALMRPT<7:0>(1)							
15:8	R/W-0	U-0	U-0	U-0	R/W-0	U-0	U-0	U-0
	ON	—	—	—	WRLOCK	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0
	RTCOE	OUTSEL<2:0>			—	—	—	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31 **ALRMEN:** Alarm Enable bit
1 = Alarm is enabled
0 = Alarm is disabled

bit 30 **CHIME:** Chime Enable bit
1 = Chime is enabled; ALMRPT<7:0> bits are allowed to underflow from ‘00’ to ‘FF’
0 = Chime is disabled; ALMRPT<7:0> bits stop once they reach ‘00’

bit 29-28 **Unimplemented:** Read as ‘0’

bit 27-24 **AMASK<3:0>:** Alarm Mask Configuration bits
11xx = Reserved, do not use
101x = Reserved, do not use
1001 = Once a year (or once every 4 years when configured for February 29th)
1000 = Once a month
0111 = Once a week
0110 = Once a day
0101 = Every hour
0100 = Every 10 minutes
0011 = Every minute
0010 = Every 10 seconds
0001 = Every second
0000 = Every half-second

bit 23-16 **ALMRPT<7:0>:** Alarm Repeat Counter Value bits(1)
11111111 = Alarm will repeat 255 more times
11111110 = Alarm will repeat 254 more times
• • •
00000010 = Alarm will repeat 2 more times
00000001 = Alarm will repeat 1 more time
00000000 = Alarm will not repeat

bit 15 **ON:** RTCC Enable bit
1 = RTCC is enabled and counts from selected clock source
0 = RTCC is disabled

bit 14-12 **Unimplemented:** Read as ‘0’

Note 1: The counter decrements on any alarm event. The counter is prevented from rolling over from ‘00’ to ‘FF’ unless CHIME = 1.

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REGISTER 19-1: RTCCON1: RTCC CONTROL 1 REGISTER (CONTINUED)

bit 11 **WRLOCK:** RTCC Registers Write Lock bit
1 = Registers associated with accurate timekeeping are locked
0 = Registers associated with accurate timekeeping may be written to by user

bit 10-8 **Unimplemented:** Read as '0'

bit 7 **RTCOE:** RTCC Output Enable bit
1 = RTCC clock output is enabled; signal selected by OUTSEL<2:0> is presented on the RTCC pin
0 = RTCC clock output is disabled

bit 6-4 **OUTSEL<2:0>:** RTCC Signal Output Selection bits
111 = Reserved
• • •
011 = Reserved
010 = RTCC input clock source (user-defined divided output based on the combination of the RTCCON2 bits, DIV<15:0> and PS<1:0>)
001 = Seconds clock
000 = Alarm event

bit 3-0 **Unimplemented:** Read as '0'

Note 1: The counter decrements on any alarm event. The counter is prevented from rolling over from '00' to 'FF' unless CHIME = 1.

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REGISTER 19-2: RTCCON2: RTCC CONTROL 2 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DIV<15:8>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	DIV<7:0>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0
	FDIV<4:0>					—	—	—
7:0	U-0	U-0	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0
	—	—	PS<1:0>		—	—	CLKSEL<1:0>	

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-16 **DIV<15:0>:** Clock Divide bits
Sets the period of the clock divider counter for the seconds output.

bit 15-11 **FDIV<4:0>:** Fractional Clock Divide bits
11111 = Clock period increases by 31 RTCC input clock cycles every 16 seconds
11101 = Clock period increases by 30 RTCC input clock cycles every 16 seconds
• • •
00010 = Clock period increases by 2 RTCC input clock cycles every 16 seconds
00001 = Clock period increases by 1 RTCC input clock cycle every 16 seconds
00000 = No fractional clock division

bit 10-6 **Unimplemented:** Read as ‘0’

bit 5-4 **PS<1:0>:** Prescale Select bits
Sets the prescaler for the seconds output.
11 = 1:256
10 = 1:64
01 = 1:16
00 = 1:1

bit 3-2 **Unimplemented:** Read as ‘0’

bit 1-0 **CLKSEL<1:0>:** Clock Select bits
11 = Peripheral clock (FCY)
10 = PWRLCLK input pin
01 = LPRC
00 = SOSC

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REGISTER 19-3: RTCSTAT: RTCC STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	R-0, HS, HC	U-0	U-0	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC
	—	—	ALMEVT	—	—	SYNC	ALMSYNC	HALFSEC

Legend:	HC = Hardware Clearable bit	HS = Hardware Settable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-6 **Unimplemented:** Read as '0'

bit 5 **ALMEVT:** Alarm Event bit
1 = An alarm event has occurred
0 = An alarm event has not occurred

bit 4-3 **Unimplemented:** Read as '0'

bit 2 **SYNC:** Synchronization Status bit
1 = Time registers may change during software read
0 = Time registers may be read safely

bit 1 **ALMSYNC:** Alarm Synchronization Status bit
1 = Alarm registers (ALMTIME and ALMDATE) and RTCCON1 should not be modified; the ALRMEN and ALMRPT<7:0> bits may change during software read
0 = Alarm registers and Alarm Control registers may be modified safely

bit 0 **HALFSEC:** Half-Second Status bit
1 = Second half of 1-second period
0 = First half of 1-second period

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REGISTER 19-4: RTCTIME/ALMTIME: RTCC TIME/ALARM REGISTERS

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	HRTEN<2:0>			HRONE<3:0>			
23:16	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	MINTEN<2:0>			MINONE<3:0>			
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	SECTEN<3:0>				SECONE<3:0>			
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31 **Unimplemented:** Read as ‘0’

bit 30-28 **HRTEN<2:0>:** Binary Coded Decimal Value of Hours 10-Digit bits
Contains a value from 0 to 2.

bit 27-24 **HRONE<3:0>:** Binary Coded Decimal Value of Hours 1-Digit bits
Contains a value from 0 to 9.

bit 23 **Unimplemented:** Read as ‘0’

bit 22-20 **MINTEN<2:0>:** Binary Coded Decimal Value of Minutes 10-Digit bits
Contains a value from 0 to 5.

bit 19-16 **MINONE<3:0>:** Binary Coded Decimal Value of Minutes 1-Digit bits
Contains a value from 0 to 9.

bit 15-12 **SECTEN<2:0>:** Binary Coded Decimal Value of Seconds 10-Digit bits
Contains a value from 0 to 5.

bit 11-8 **SECONE<3:0>:** Binary Coded Decimal Value of Seconds 1-Digit bits
Contains a value from 0 to 9.

bit 7-0 **Unimplemented:** Read as ‘0’

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REGISTER 19-5: RTCDATE/ALMDATE: RTCC DATE/ALARM REGISTERS

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	MTHTEN	MTHONE<3:0>			
15:8	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	DAYTEN<1:0>		DAYONE<3:0>			
7:0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	—	WDAY<2:0>		

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-21 **Unimplemented:** Read as '0'

bit 20 **MTHTEN:** Binary Coded Decimal Value of Months 10-Digit bit
Contains a value from 0 to 1.

bit 19-16 **MTHONE<3:0>:** Binary Coded Decimal Value of Months 1-Digit bits
Contains a value from 0 to 9.

bit 15-14 **Unimplemented:** Read as '0'

bit 13-12 **DAYTEN<1:0>:** Binary Coded Decimal Value of Days 10-Digit bits
Contains a value from 0 to 3.

bit 11-8 **DAYONE<3:0>:** Binary Coded Decimal Value of Days 1-Digit bits
Contains a value from 0 to 9.

bit 7-3 **Unimplemented:** Read as '0'

bit 2-0 **WDAY<2:0>:** Binary Coded Decimal Value of Weekdays Digit bits
Contains a value from 0 to 6.

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20.0 12-BIT ADC CONVERTER WITH THRESHOLD DETECT

> **Note:** This data sheet summarizes the features of the PIC32MM0256GPM064 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 25. "12-Bit Analog-to-Digital Converter (ADC) with Threshold Detect"** (DS60001359) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32). The information in this data sheet supersedes the information in the FRM.

20.1 Introduction

The 12-bit ADC Converter with Threshold Detect includes the following features:

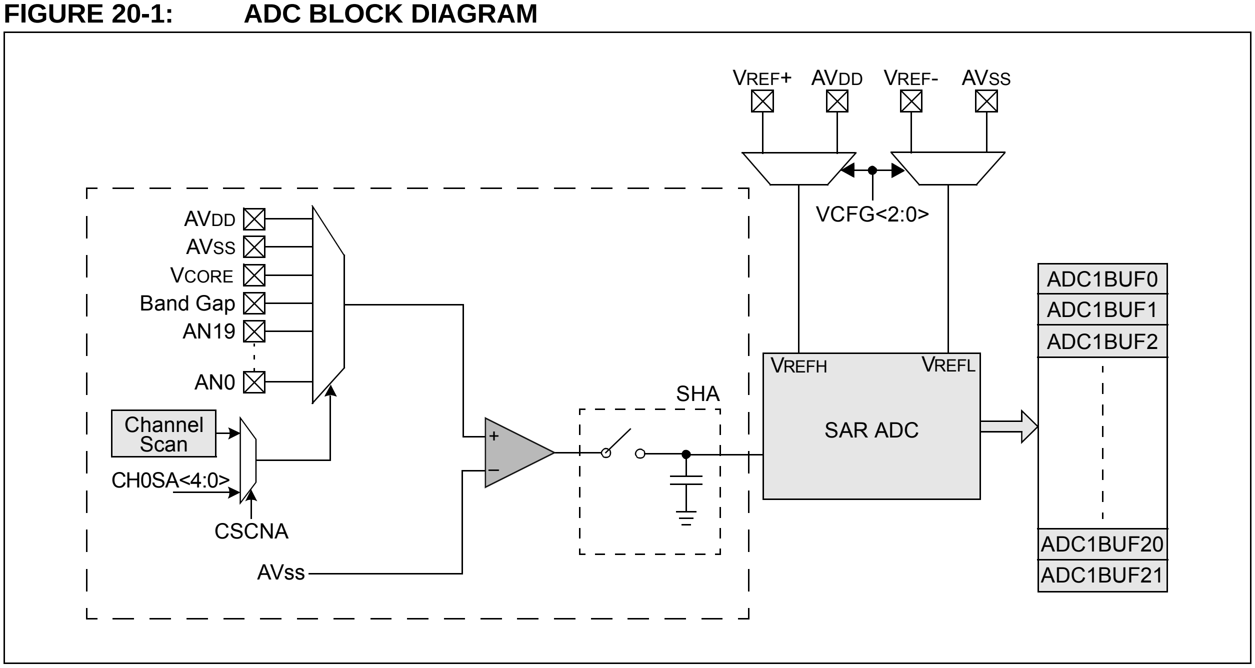
- Successive Approximation Register (SAR) Conversion
- Conversion Speeds of up to 300 ksps
- User-Selectable Resolution of 10 or 12 bits
- Up to 24 Analog Inputs (internal and external)
- External Voltage Reference Input Pins
- Unipolar Differential Sample-and-Hold Amplifier (SHA)
- Automated Threshold Scan and Compare Operation to Pre-Evaluate Conversion Results
- Selectable Conversion Trigger Source
- Fixed-Length Configurable Conversion Result Buffer
- Eight Options for Result Alignment and Encoding
- Configurable Interrupt Generation
- Operation during CPU Sleep and Idle modes

Figure 20-1 illustrates a block diagram of the 12-bit ADC. The 12-bit ADC has external analog inputs, AN0 through AN19, and 4 internal analog inputs connected to VDD, VSS, VCORE and band gap. In addition, there are two analog input pins for external voltage reference connections.

The analog inputs are connected through a multiplexer to the SHA. Unipolar differential conversions are possible on all inputs (see Figure 20-1).

The Automatic Input Scan mode sequentially converts multiple analog inputs. A special control register specifies which inputs will be included in the scanning sequence. The 12-bit ADC is connected to a 22-word result buffer. The 12-bit result is converted to one of eight output formats in either 32-bit or 16-bit word widths.

FIGURE 20-1: ADC BLOCK DIAGRAM



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20.2 Control Registers

The ADC module has the following Special Function Registers (SFRs):

- **AD1CON1: ADC Control Register 1**
- **AD1CON2: ADC Control Register 2**
- **AD1CON3: ADC Control Register 3**
- **AD1CON5: ADC Control Register 5**

  The AD1CON1, AD1CON2, AD1CON3 and AD1CON5 registers control the operation of the ADC module.
- **AD1CHS: ADC Input Select Register**

  The AD1CHS register selects the input pins to be connected to the SHA.
- **AD1CSS: ADC Input Scan Select Register**

  The AD1CSS register selects inputs to be sequentially scanned.
- **AD1CHIT: ADC Compare Hit Register**

  The AD1CHIT register indicates the channels meeting specified comparison requirements.

Table 20-1 provides a summary of all ADC related registers, including their addresses and formats. Corresponding registers appear after the summary, followed by a detailed description of each register. All unimplemented registers and/or bits within a register read as zero.

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TABLE 20-1: ADC REGISTER MAP

Virtual Address (BF80_#)	Register Name(2)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
2100	ADC1BUF0	31:16	ADC1BUF0<31:0>																0000
		15:0																	0000
2110	ADC1BUF1	31:16	ADC1BUF1<31:0>																0000
		15:0																	0000
2120	ADC1BUF2	31:16	ADC1BUF2<31:0>																0000
		15:0																	0000
2130	ADC1BUF3	31:16	ADC1BUF3<31:0>																0000
		15:0																	0000
2140	ADC1BUF4	31:16	ADC1BUF4<31:0>																0000
		15:0																	0000
2150	ADC1BUF5	31:16	ADC1BUF5<31:0>																0000
		15:0																	0000
2160	ADC1BUF6	31:16	ADC1BUF6<31:0>																0000
		15:0																	0000
2170	ADC1BUF7	31:16	ADC1BUF7<31:0>																0000
		15:0																	0000
2180	ADC1BUF8	31:16	ADC1BUF8<31:0>																0000
		15:0																	0000
2190	ADC1BUF9	31:16	ADC1BUF9<31:0>																0000
		15:0																	0000
21A0	ADC1BUF10	31:16	ADC1BUF10<31:0>																0000
		15:0																	0000
21B0	ADC1BUF11	31:16	ADC1BUF11<31:0>																0000
		15:0																	0000
21C0	ADC1BUF12	31:16	ADC1BUF12<31:0>																0000
		15:0																	0000
21D0	ADC1BUF13	31:16	ADC1BUF13<31:0>																0000
		15:0																	0000
21E0	ADC1BUF14	31:16	ADC1BUF14<31:0>																0000
		15:0																	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: The CSS<19:12> bits are not implemented in 28-pin devices. The CSS<19:15> bits are not implemented in 36-pin and 40-pin devices. The CSS<17:14> bits are not implemented in 48-pin devices.

2: All registers in this table have corresponding CLR, SET and INV registers at their virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively.

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TABLE 20-1: ADC REGISTER MAP (CONTINUED)

Virtual Address (BF80_#)	Register Name[2]	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
21F0	ADC1BUF15	31:16	ADC1BUF15<31:0>																0000
		15:0																	0000
2200	ADC1BUF16	31:16	ADC1BUF16<31:0>																0000
		15:0																	0000
2210	ADC1BUF17	31:16	ADC1BUF17<31:0>																0000
		15:0																	0000
2220	ADC1BUF18	31:16	ADC1BUF18<31:0>																0000
		15:0																	0000
2230	ADC1BUF19	31:16	ADC1BUF19<31:0>																0000
		15:0																	0000
2240	ADC1BUF20	31:16	ADC1BUF20<31:0>																0000
		15:0																	0000
2250	ADC1BUF21	31:16	ADC1BUF21<31:0>																0000
		15:0																	0000
2260	AD1CON1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON		SIDL	—	—	FORM<2:0>			SSRC<3:0>				MODE12	ASAM	SAMP	DONE	0000
2270	AD1CON2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	VCFG<2:0>			OFFCAL	BUFREGEN	CSCNA	—	—	BUFS	—	SMPI<3:0>				BUFM	—	0000
2280	AD1CON3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ADRC	EXTSAM	—	SAMC<4:0>					ADCS<7:0>								0000
2290	AD1CHS	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	CHONA<2:0>			CHOSA<4:0>					0000
22A0	AD1CSS	31:16	—	CSS<30:27>				—	—	—	—	—	—	—	CSS<19:16>				0000
		15:0	CSS<15:0>[1]																0000
22C0	AD1CON5	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ASEN	LPEN	—	BGREQ	—	—	ASINT<1:0>		—	—	—	—	WM<1:0>		CM<1:0>		0000
22D0	AD1CHIT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	CHH<19:16>				0000
		15:0	CHH<15:0>																0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: The CSS<19:12> bits are not implemented in 28-pin devices. The CSS<19:15> bits are not implemented in 36-pin and 40-pin devices. The CSS<17:14> bits are not implemented in 48-pin devices.

2: All registers in this table have corresponding CLR, SET and INV registers at their virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively.

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REGISTER 20-1: AD1CON1: ADC CONTROL REGISTER 1

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	ON	—	SIDL	—	—	FORM<2:0>		
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0, HSC	R/W-0, HSC
	SSRC<3:0>				MODE12	ASAM	SAMP[2]	DONE[1]

Legend:	HSC = Hardware Settable/Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** ADC Operating Mode bit
1 = ADC module is operating
0 = ADC is off

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** ADC Stop in Idle Mode bit
1 = Discontinues module operation when device enters Idle mode
0 = Continues module operation in Idle mode

bit 12-11 **Unimplemented:** Read as '0'

bit 10-8 **FORM<2:0>:** Data Output Format bits
For 12-Bit Operation (MODE12 bit = 1):
111 = Signed fractional 32-bit (DOUT = sddd dddd dddd 0000 0000 0000 0000)
110 = Fractional 32-bit (DOUT = dddd dddd dddd 0000 0000 0000 0000 0000)
101 = Signed integer 32-bit (DOUT = ssss ssss ssss ssss ssss sddd dddd dddd)
100 = Integer 32-bit (DOUT = 0000 0000 0000 0000 0000 dddd dddd dddd)
011 = Signed fractional 16-bit (DOUT = 0000 0000 0000 0000 sddd dddd dddd 0000)
010 = Fractional 16-bit (DOUT = 0000 0000 0000 0000 dddd dddd dddd 0000)
001 = Signed integer 16-bit (DOUT = 0000 0000 0000 0000 ssss sddd dddd dddd)
000 = Integer 16-bit (DOUT = 0000 0000 0000 0000 0000 dddd dddd dddd)
For 10-Bit Operation (MODE12 bit = 0):
111 = Signed fractional 32-bit (DOUT = sddd dddd dd00 0000 0000 0000 0000)
110 = Fractional 32-bit (DOUT = dddd dddd dd00 0000 0000 0000 0000 0000)
101 = Signed integer 32-bit (DOUT = ssss ssss ssss ssss ssss sssd dddd dddd)
100 = Integer 32-bit (DOUT = 0000 0000 0000 0000 0000 00dd dddd dddd)
011 = Signed fractional 16-bit (DOUT = 0000 0000 0000 0000 sddd dddd dd00 0000)
010 = Fractional 16-bit (DOUT = 0000 0000 0000 0000 dddd dddd dd00 0000)
001 = Signed integer 16-bit (DOUT = 0000 0000 0000 0000 ssss sssd dddd dddd)
000 = Integer 16-bit (DOUT = 0000 0000 0000 0000 0000 00dd dddd dddd)

Note 1: The DONE bit is not persistent in Automatic modes; it is cleared by hardware at the beginning of the next sample.

2: The SAMP bit is cleared and cannot be written if the ADC is disabled (ON bit = 0).

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REGISTER 20-1: AD1CON1: ADC CONTROL REGISTER 1 (CONTINUED)

bit 7-4 **SSRC<3:0>:** Conversion Trigger Source Select bits

1111 = CLC2 module event ends sampling and starts conversion
1110 = CLC1 module event ends sampling and starts conversion
1101 = SCCP6 module event ends sampling and starts conversion
1100 = SCCP5 module event ends sampling and starts conversion
1011 = SCCP4 module event ends sampling and starts conversion
1010 = MCCP3 module event ends sampling and starts conversion
1001 = MCCP2 module event ends sampling and starts conversion
1000 = MCCP1 module event ends sampling and starts conversion
0111 = Internal counter ends sampling and starts conversion (auto-convert)
0110 = Timer1 period match ends sampling and starts conversion (can trigger during Sleep mode)
0101 = Timer1 period match ends sampling and starts conversion (will not trigger during Sleep mode)
0100-0011 = Reserved
0010 = Timer3 period match ends sampling and starts conversion
0001 = Active transition on INT0 pin ends sampling and starts conversion
0000 = Clearing the SAMP bit ends sampling and starts conversion

bit 3 **MODE12:** 12-Bit Operation Mode bit

1 = 12-bit ADC operation
0 = 10-bit ADC operation

bit 2 **ASAM:** ADC Sample Auto-Start bit

1 = Sampling begins immediately after last conversion completes; SAMP bit is automatically set
0 = Sampling begins when SAMP bit is set

bit 1 **SAMP:** ADC Sample Enable bit(2)

1 = The ADC Sample-and-Hold Amplifier (SHA) is sampling
0 = The ADC SHA is holding
When ASAM = 0, writing '1' to this bit starts sampling. When SSRC<3:0 = 0000, writing '0' to this bit will end sampling and start conversion.

bit 0 **DONE:** ADC Conversion Status bit(1)

1 = Analog-to-Digital conversion is done
0 = Analog-to-Digital conversion is not done or has not started
Clearing this bit will not affect any operation in progress.

Note 1: The DONE bit is not persistent in Automatic modes; it is cleared by hardware at the beginning of the next sample.

2: The SAMP bit is cleared and cannot be written if the ADC is disabled (ON bit = 0).

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REGISTER 20-2: AD1CON2: ADC CONTROL REGISTER 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0
	VCFG<2:0>			OFFCAL	BUFREGEN	CSCNA	—	—
7:0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0
	BUFS	—	SMPI<3:0>				BUFM	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-13 **VCFG<2:0>:** Voltage Reference Configuration bits

	ADC VR+	ADC VR-
000	AVDD	AVSS
001	AVDD	External VREF- Pin
010	External VREF+ Pin	AVSS
011	External VREF+ Pin	External VREF- Pin
1xx	Unimplemented; do not use	

bit 12 **OFFCAL:** Input Offset Calibration Mode Select bit
1 = Enables Offset Calibration mode: The inputs of the SHA are connected to the negative reference
0 = Disables Offset Calibration mode: The inputs to the SHA are controlled by AD1CHS or AD1CSS

bit 11 **BUFREGEN:** ADC Buffer Register Enable bit
1 = Conversion result is loaded into the buffer location determined by the converted channel
0 = ADC result buffer is treated as a FIFO

bit 10 **CSCNA:** Scan Input Selections for CH0+ SHA Input for Input Multiplexer Setting bit
1 = Scans inputs
0 = Does not scan inputs

bit 9-8 **Unimplemented:** Read as '0'

bit 7 **BUFS:** Buffer Fill Status bit
Only valid when BUFM = 1 (ADC buffers split into 2 x 11-word buffers).
1 = ADC is currently filling Buffers 11-21, user should access data in 0-10
0 = ADC is currently filling Buffers 0-10, user should access data in 11-21

bit 6 **Unimplemented:** Read as '0'

bit 5-2 **SMPI<3:0>:** Sample/Convert Sequences Per Interrupt Selection bits
1111 = Interrupts at the completion of conversion for each 16^{th} sample/convert sequence
1110 = Interrupts at the completion of conversion for each 15^{th} sample/convert sequence
•
•
•
0001 = Interrupts at the completion of conversion for each 2^{nd} sample/convert sequence
0000 = Interrupts at the completion of conversion for each sample/convert sequence

bit 1 **BUFM:** ADC Result Buffer Mode Select bit
1 = Buffer configured as two 11-word buffers, ADC1BUF(0...10), ADC1BUF(11...21)
0 = Buffer configured as one 22-word buffer, ADC1BUF(0...21)

bit 0 **Unimplemented:** Read as '0'

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REGISTER 20-3: AD1CON3: ADC CONTROL REGISTER 3

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ADRC	EXTSAM	—	SAMC<4:0>				
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ADCS<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as ‘0’

bit 15 **ADRC:** ADC Conversion Clock Source (TSRC) bit
1 = Clock derived from the Fast RC (FRC) oscillator
0 = Clock derived from the Peripheral Bus Clock (PBCLK, 1:1 with SYSCLK)

bit 14 **EXTSAM:** Extended Sampling Time bit
1 = ADC is still sampling after SAMP bit = 0
0 = ADC stops sampling when SAMP bit = 0

bit 13 **Unimplemented:** Read as ‘0’

bit 12-8 **SAMC<4:0>:** Auto-Sample Time bits
11111 = 31 TAD
•
•
•
00001 = 1 TAD
00000 = 0 TAD (Not allowed)

bit 7-0 **ADCS<7:0>:** ADC Conversion Clock Select bits
11111111 = 2 • TSRC • ADCS<7:0> = 510 • TSRC = TAD
•
•
•
00000001 = 2 • TSRC • ADCS<7:0> = 2 • TSRC = TAD
00000000 = 1 • TSRC = TAD
Where TSRC is a period of clock selected by the ADRC bit (AD1CON3<15>).

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REGISTER 20-4: AD1CON5: ADC CONTROL REGISTER 5

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	U-0	R/W-0	U-0	U-0	R/W-0	R/W-0
	ASEN	LPEN	—	BGREQ	—	—	ASINT<1:0>[1]	
7:0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	WM<1:0>		CM<1:0>	

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as ‘0’

bit 15 **ASEN:** Auto-Scan Enable bit
1 = Auto-scan is enabled
0 = Auto-scan is disabled

bit 14 **LPEN:** Low-Power Enable bit
1 = Low power is enabled after scan
0 = Full power is enabled after scan

bit 13 **Unimplemented:** Read as ‘0’

bit 12 **BGREQ:** Band Gap Request bit
1 = Band gap is enabled when the ADC is enabled and active
0 = Band gap is not enabled by the ADC

bit 11-10 **Unimplemented:** Read as ‘0’

bit 9-8 **ASINT<1:0>:** Auto-Scan (Threshold Detect) Interrupt Mode bits[1]
11 = Interrupt after Threshold Detect sequence has completed and a valid compare has occurred
10 = Interrupt after valid compare has occurred
01 = Interrupt after Threshold Detect sequence has completed
00 = No interrupt

bit 7-4 **Unimplemented:** Read as ‘0’

bit 3-2 **WM<1:0>:** Write Mode bits
11 = Reserved
10 = Auto-compare only (conversion results are not saved, but interrupts are generated when a valid match occurs, as defined by the CM<1:0> and ASINT<1:0> bits)
01 = Convert and save (conversion results saved to locations as determined by register bits when a match occurs, as defined by the CM<1:0> bits)
00 = Legacy operation (conversion data saved to location determined by buffer register bits)

bit 1-0 **CM<1:0>:** Compare Mode bits
11 = Outside Window mode (valid match occurs if the conversion result is outside of the window defined by the corresponding buffer pair)
10 = Inside Window mode (valid match occurs if the conversion result is inside the window defined by the corresponding buffer pair)
01 = Greater Than mode (valid match occurs if the result is greater than value in the corresponding buffer register)
00 = Less Than mode (valid match occurs if the result is less than value in the corresponding buffer register)

Note 1: The ASINT<1:0> bits setting only takes effect when ASEN (AD1CON5<15>) = 1. Interrupt generation is governed by the SMPI<3:0> bits field.

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REGISTER 20-5: AD1CHS: ADC INPUT SELECT REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CH0NA<2:0>			CH0SA<4:0>				

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as ‘0’

bit 7-5 **CH0NA<2:0>:** Negative Input Select bits
111-001 = Reserved
000 = Negative input is AVSS

bit 4-0 **CH0SA<4:0>:** Positive Input Select bits
11111 = Reserved
11110 = Positive input is AVDD
11101 = Positive input is AVSS
11100 = Positive input is Band Gap Reference (VBG)
11011 = VDD core
10100-10110 = Reserved
10011 = Positive input is AN19(1)
10010 = Positive input is AN18(1)
10001 = Positive input is AN17(1)
10000 = Positive input is AN16(1)
01111 = Positive input is AN15(2)
01110 = Positive input is AN14(3)
01101 = Positive input is AN13(3)
01100 = Positive input is AN12(3)
01011 = Positive input is AN11
01010 = Positive input is AN10
01001 = Positive input is AN9
01000 = Positive input is AN8
00111 = Positive input is AN7
00110 = Positive input is AN6
00101 = Positive input is AN5
00100 = Positive input is AN4
00011 = Positive input is AN3
00010 = Positive input is AN2
00001 = Positive input is AN1
00000 = Positive input is AN0

Note 1: This option is not available in 28, 36, 40 or 48-pin packages.
2: This option is not available in 28, 36 or 40-pin packages.
3: This option is not available in 28-pin packages.

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REGISTER 20-6: AD1CSS: ADC INPUT SCAN SELECT REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0
	—	CSS<30:27>				—	—	—
23:16	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	CSS<19:16>(1,2,3)			
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CSS<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CSS<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31 **Unimplemented:** Read as ‘0’

bit 30-27 **CSS<30:27>:** ADC Input Pin Scan Selection bits
1 = Selects ANx for the input scan
0 = Skips ANx for the input scan

bit 26-20 **Unimplemented:** Read as ‘0’

bit 19-0 **CSS<19:0>:** ADC Input Pin Scan Selection bits(1,2,3)
1 = Selects ANx for the input scan
0 = Skips ANx for the input scan

Note 1: The CSS<19:12> bits are not implemented in 28-pin devices
2: The CSS<19:15> bits are not implemented in 36-pin and 40-pin devices
3: The CSS<17:14> bits are not implemented in 48-pin devices

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REGISTER 20-7: AD1CHIT: ADC COMPARE HIT REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	CHH<19:16>(1,2,3)			
15:8	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	CHH<13:8>					
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHH<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-20 **Unimplemented:** Read as ‘0’

bit 19-0 **CHH<21:16>:** ADC Compare Hit bits(1,2,3)

If CM<1:0> = 11:
1 = ADC Result Buffer n has been written with data or a match has occurred
0 = ADC Result Buffer n has not been written with data

For All Other Values of CM<1:0>:
1 = A match has occurred on ADC Result Channel n
0 = No match has occurred on ADC Result Channel n

Note 1: The CHH<19:12> bits are not implemented in 28-pin devices
2: The CHH<19:15> bits are not implemented in 36-pin and 40-pin devices
3: The CHH<17:14> bits are not implemented in 48-pin devices

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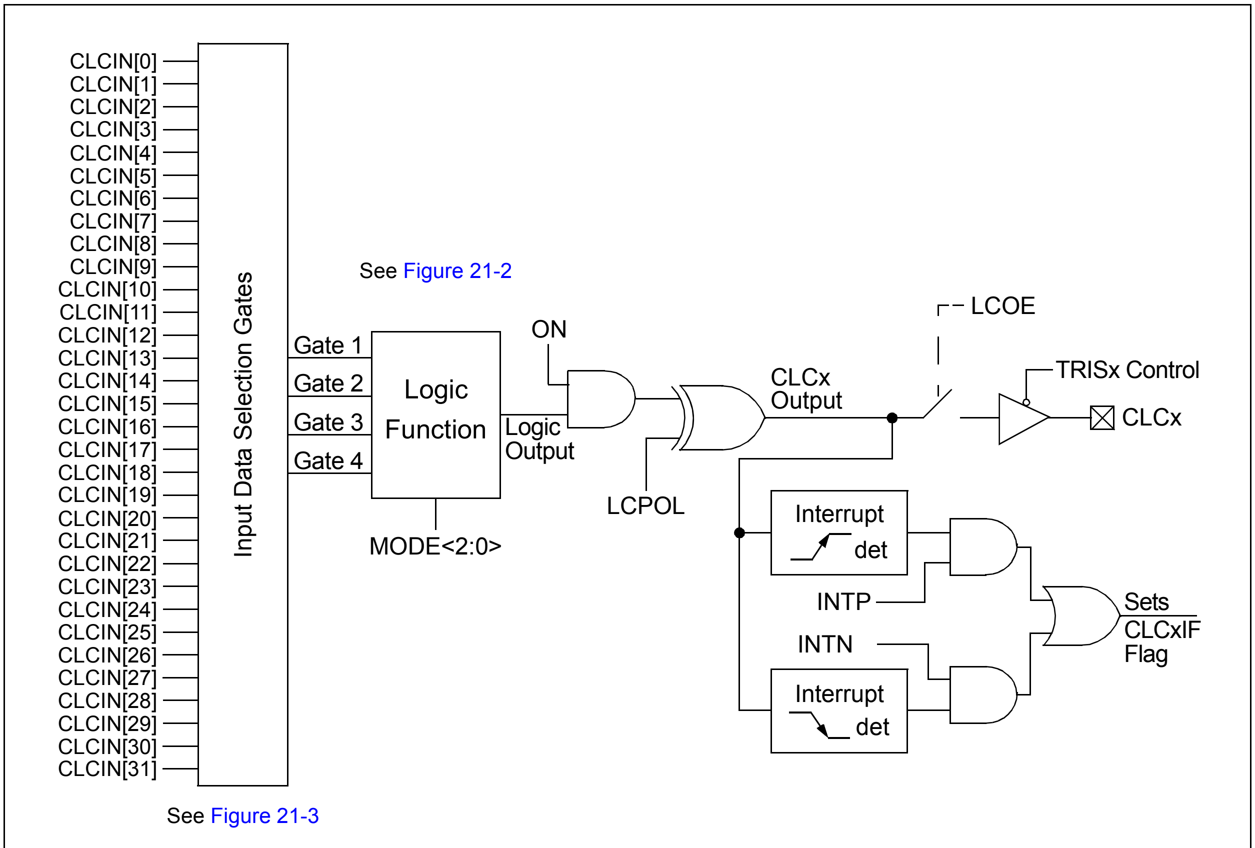
21.0 CONFIGURABLE LOGIC CELL (CLC)

Note: This data sheet summarizes the features of the PIC32MM0256GPM064 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 36. "Configurable Logic Cell"** (DS60001363) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32). The information in this data sheet supersedes the information in the FRM.

The Configurable Logic Cell (CLC) module allows the user to specify combinations of signals as inputs to a logic function and to use the logic output to control other peripherals or I/O pins. This provides greater flexibility and potential in embedded designs since the CLC module can operate outside the limitations of software execution, and supports a vast amount of output designs.

There are four input gates to the selected logic function. These four input gates select from a pool of up to 32 signals that are selected using four data source selection multiplexers. Figure 21-1 shows an overview of the module. Figure 21-3 shows the details of the data source multiplexers and logic input gate connections.

FIGURE 21-1: CLCx MODULE



Note: All register bits shown in this figure can be found in the CLCxCON register.

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FIGURE 21-2: CLCx LOGIC FUNCTION COMBINATORIAL OPTIONS

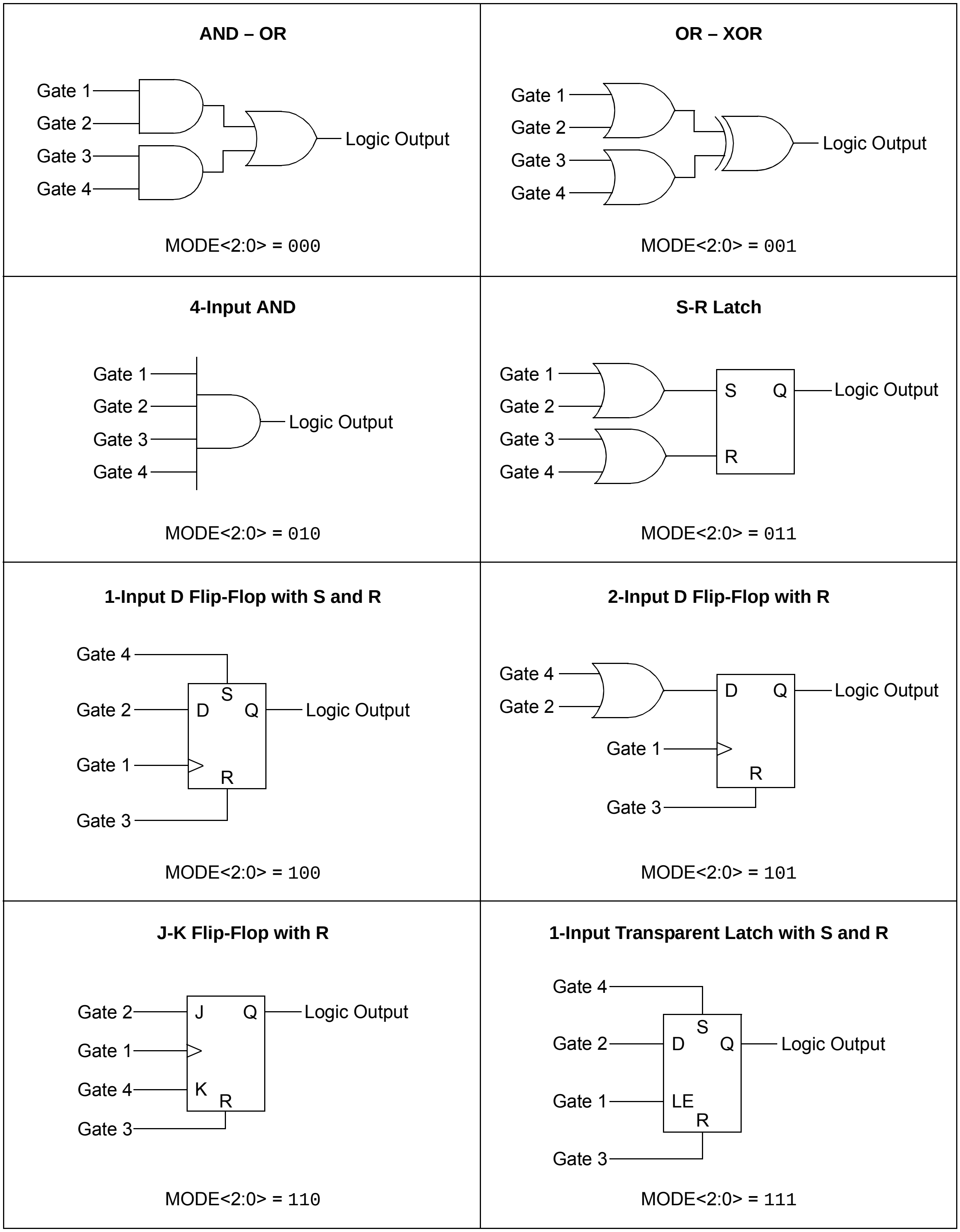

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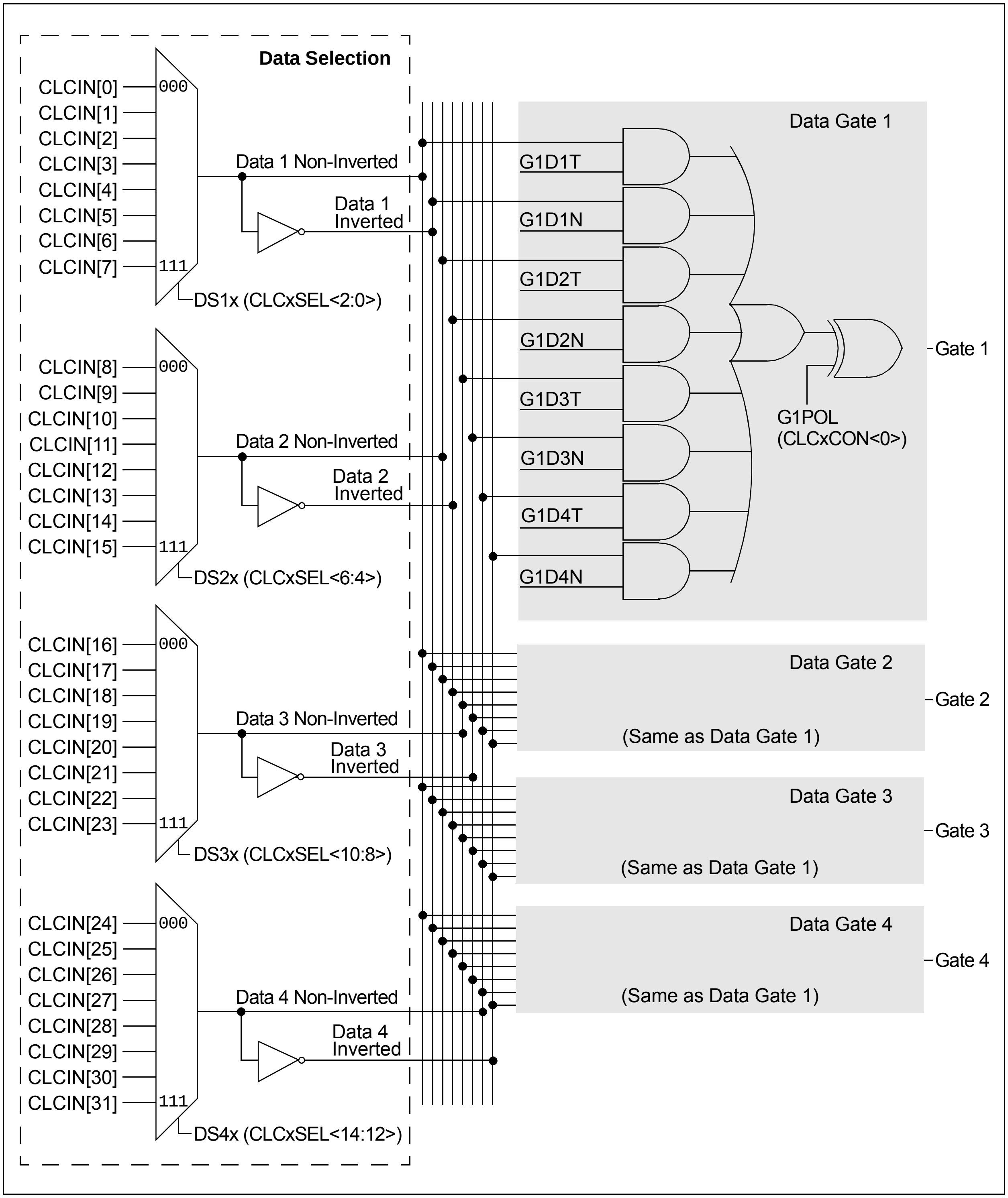
FIGURE 21-3: CLCx INPUT SOURCE SELECTION DIAGRAM



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21.1 Control Registers

The CLCx module is controlled by the following registers:

- CLCxCON
- CLCxSEL
- CLCxGLS

The CLCx Control register (CLCxCON) is used to enable the module and interrupts, control the output enable bit, select output polarity and select the logic function. The CLCx Control registers also allow the user to control the logic polarity of not only the cell output, but also some intermediate variables.

The CLCx Source Select register (CLCxSEL) allows the user to select up to 4 data input sources using the 4 data input selection multiplexers. Each multiplexer has a list of 8 data sources available.

The CLCx Gate Logic Select register (CLCxGLS) allows the user to select which outputs from each of the selection MUXes are used as inputs to the input gates of the logic cell. Each data source MUX outputs both a true and a negated version of its output. All of these 8 signals are enabled, ORed together by the logic cell input gates.

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TABLE 21-1: CLC1, CLC2 AND CLC3 REGISTER MAP

Virtual Address (BF80_#)	Register Name[1]	Bit Range	Bits 31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
2480	CLC1CON	32:16	—	—	—	—	—	—	—	—	—	—	—	—	G4POL	G3POL	G2POL	G1POL	0000
		15:0	ON	—	SIDL	—	INTP	INTN	—	—	LCOE	LCOUT	LCPOL	—	—	MODE<2:0>			0000
2490	CLC1SEL	32:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	DS4<2:0>			—	DS3<2:0>			—	DS2<2:0>			—	DS1<2:0>			0000
24A0	CLC1GLS	32:16	G4D4T	G4D4N	G4D3T	G4D3N	G4D2T	G4D2N	G4D1T	G4D1N	G3D4T	G3D4N	G3D3T	G3D3N	G3D2T	G3D2N	G3D1T	G3D1N	0000
		15:0	G2D4T	G2D4N	G2D3T	G2D3N	G2D2T	G2D2N	G2D1T	G2D1N	G1D4T	G1D4N	G1D3T	G1D3N	G1D2T	G1D2N	G1D1T	G1D1N	0000
2500	CLC2CON	32:16	—	—	—	—	—	—	—	—	—	—	—	—	G4POL	G3POL	G2POL	G1POL	0000
		15:0	ON	—	SIDL	—	INTP	INTN	—	—	LCOE	LCOUT	LCPOL	—	—	MODE<2:0>			0000
2510	CLC2SEL	32:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	DS4<2:0>			—	DS3<2:0>			—	DS2<2:0>			—	DS1<2:0>			0000
2520	CLC2GLS	32:16	G4D4T	G4D4N	G4D3T	G4D3N	G4D2T	G4D2N	G4D1T	G4D1N	G3D4T	G3D4N	G3D3T	G3D3N	G3D2T	G3D2N	G3D1T	G3D1N	0000
		15:0	G2D4T	G2D4N	G2D3T	G2D3N	G2D2T	G2D2N	G2D1T	G2D1N	G1D4T	G1D4N	G1D3T	G1D3N	G1D2T	G1D2N	G1D1T	G1D1N	0000
2580	CLC3CON	32:16	—	—	—	—	—	—	—	—	—	—	—	—	G4POL	G3POL	G2POL	G1POL	0000
		15:0	ON	—	SIDL	—	INTP	INTN	—	—	LCOE	LCOUT	LCPOL	—	—	MODE<2:0>			0000
2590	CLC3SEL	32:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	DS4<2:0>			—	DS3<2:0>			—	DS2<2:0>			—	DS1<2:0>			0000
25A0	CLC3GLS	32:16	G4D4T	G4D4N	G4D3T	G4D3N	G4D2T	G4D2N	G4D1T	G4D1N	G3D4T	G3D4N	G3D3T	G3D3N	G3D2T	G3D2N	G3D1T	G3D1N	0000
		15:0	G2D4T	G2D4N	G2D3T	G2D3N	G2D2T	G2D2N	G2D1T	G2D1N	G1D4T	G1D4N	G1D3T	G1D3N	G1D2T	G1D2N	G1D1T	G1D1N	0000
2600	CLC4CON	32:16	—	—	—	—	—	—	—	—	—	—	—	—	G4POL	G3POL	G2POL	G1POL	0000
		15:0	ON	—	SIDL	—	INTP	INTN	—	—	LCOE	LCOUT	LCPOL	—	—	MODE<2:0>			0000
2610	CLC4SEL	32:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	DS4<2:0>			—	DS3<2:0>			—	DS2<2:0>			—	DS1<2:0>			0000
2620	CLC4GLS	32:16	G4D4T	G4D4N	G4D3T	G4D3N	G4D2T	G4D2N	G4D1T	G4D1N	G3D4T	G3D4N	G3D3T	G3D3N	G3D2T	G3D2N	G3D1T	G3D1N	0000
		15:0	G2D4T	G2D4N	G2D3T	G2D3N	G2D2T	G2D2N	G2D1T	G2D1N	G1D4T	G1D4N	G1D3T	G1D3N	G1D2T	G1D2N	G1D1T	G1D1N	0000

Legend: — = unimplemented, read as ‘0’. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively.

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REGISTER 21-1: CLCxCON: CLCx CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	G4POL	G3POL	G2POL	G1POL
15:8	R/W-0	U-0	R/W-0	U-0	R/W-0	R/W-0	U-0	U-0
	ON	—	SIDL	—	INTP(1)	INTN(1)	—	—
7:0	R/W-0	R-0, HS, HC	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	LCOE	LCOUT	LCPOL	—	—	MODE<2:0>		

Legend:	HC = Hardware Clearable bit	HS = Hardware Settable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-20 **Unimplemented:** Read as ‘0’

bit 19 **G4POL:** Gate 4 Polarity Control bit
1 = The output of Channel 4 logic is inverted when applied to the logic cell
0 = The output of Channel 4 logic is not inverted

bit 18 **G3POL:** Gate 3 Polarity Control bit
1 = The output of Channel 3 logic is inverted when applied to the logic cell
0 = The output of Channel 3 logic is not inverted

bit 17 **G2POL:** Gate 2 Polarity Control bit
1 = The output of Channel 2 logic is inverted when applied to the logic cell
0 = The output of Channel 2 logic is not inverted

bit 16 **G1POL:** Gate 1 Polarity Control bit
1 = The output of Channel 1 logic is inverted when applied to the logic cell
0 = The output of Channel 1 logic is not inverted

bit 15 **ON:** CLCx Enable bit
1 = CLCx is enabled and mixing input signals
0 = CLCx is disabled and has logic zero outputs

bit 14 **Unimplemented:** Read as ‘0’

bit 13 **SIDL:** CLCx Stop in Idle Mode bit
1 = Discontinues module operation when device enters Idle mode
0 = Continues module operation in Idle mode

bit 12 **Unimplemented:** Read as ‘0’

bit 11 **INTP:** CLCx Positive Edge Interrupt Enable bit(1)
1 = Interrupt will be generated when a rising edge occurs on LCOUT
0 = Interrupt will not be generated

bit 10 **INTN:** CLCx Negative Edge Interrupt Enable bit(1)
1 = Interrupt will be generated when a falling edge occurs on LCOUT
0 = Interrupt will not be generated

bit 9-8 **Unimplemented:** Read as ‘0’

bit 7 **LCOE:** CLCx Port Enable bit
1 = CLCx port pin output is enabled
0 = CLCx port pin output is disabled

Note 1: The INTP and INTN bits should not be set at the same time for proper interrupt functionality.

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REGISTER 21-1: CLCxCON: CLCx CONTROL REGISTER (CONTINUED)

bit 6 **LCOUT:** CLCx Data Output Status bit
1 = CLCx output high
0 = CLCx output low

bit 5 **LCPOL:** CLCx Output Polarity Control bit
1 = The output of the module is inverted
0 = The output of the module is not inverted

bit 4-3 **Unimplemented:** Read as ‘0’

bit 2-0 **MODE<2:0>:** CLCx Mode bits
111 = Cell is a 1-input transparent latch with S and R
110 = Cell is a JK flip-flop with R
101 = Cell is a 2-input D flip-flop with R
100 = Cell is a 1-input D flip-flop with S and R
011 = Cell is an SR latch
010 = Cell is a 4-input AND
001 = Cell is an OR-XOR
000 = Cell is a AND-OR

Note 1: The INTP and INTN bits should not be set at the same time for proper interrupt functionality.

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REGISTER 21-2: CLCxSEL: CLCx INPUT MUX SELECT REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0
	—	DS4<2:0>			—	DS3<2:0>		
7:0	U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0
	—	DS2<2:0>			—	DS1<2:0>		

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-15 **Unimplemented:** Read as ‘0’

bit 14-12 **DS4<2:0>:** Data Selection MUX 4 Signal Selection bits

For CLC1:
111 = SCCP5 OCMP compare match event
110 = MCCP1 OCMP compare match event
101 = RTCC event
100 = CMP3 out
011 = SPI1 SDI1 in
010 = SCCP5 OCM5 output
001 = CLC2 out
000 = CLCINB I/O pin

For CLC2:
111 = SCCP5 OCMP compare match event
110 = MCCP1 OCMP compare match event
101 = RTCC event
100 = CMP3 out
011 = SPI2 SDI2 in
010 = SCCP5 OCM6 output
001 = CLC1 out
000 = CLCINB I/O pin

For CLC3:
111 = SCCP7 OCMP compare match event
110 = MCCP2 OCMP compare match event
101 = RTCC event
100 = CMP3 out
011 = SPI3 SDI3 in
010 = SCCP7 OCM7A output
001 = CLC4 out
000 = CLCINB I/O pin

For CLC4:
111 = SCCP7 OCMP compare match event
110 = MCCP3 OCMP compare match event
101 = RTCC event
100 = CMP3 out
011 = Reserved
010 = SCCP7 OCM3A output
001 = CLC3 out
000 = CLCINB I/O pin

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REGISTER 21-2: CLCxSEL: CLCx INPUT MUX SELECT REGISTER (CONTINUED)

bit 11 **Unimplemented:** Read as '0'

bit 10-8 **DS3<2:0>:** Data Selection MUX 3 Signal Selection bits

For CLC1:
111 = Unused
110 = MCCP1 OCMP compare match event
101 = DMA Channel 0 interrupt
100 = ADC end of conversion
011 = UART1 TX out
010 = CMP1 out
001 = CLC2 out
000 = CLCINB I/O pin

For CLC2:
111 = Unused
110 = MCCP1 OCMP compare match event
101 = DMA Channel 1 interrupt
100 = ADC end of conversion
011 = UART2 TX out
010 = CMP1 out
001 = CLC1 out
000 = CLCINB I/O pin

For CLC3:
111 = Reserved
110 = MCCP2 OCMP compare match event
101 = DMA Channel 0 interrupt
100 = ADC end of conversion
011 = UART3 TX out
010 = CMP1 out
001 = CLC4 out
000 = CLCINB I/O pin

For CLC4:
111 = Reserved
110 = MCCP3 OCMP compare match event
101 = DMA Channel 1 interrupt
100 = ADC end of conversion
011 = Reserved
010 = CMP1 out
001 = CLC3 out
000 = CLCINB I/O pin

bit 7 **Unimplemented:** Read as '0'

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REGISTER 21-2: CLCxSEL: CLCx INPUT MUX SELECT REGISTER (CONTINUED)

bit 6-4 **DS2<2:0>:** Data Selection MUX 2 Signal Selection bits

For CLC1:
111 = SCCP5 OCMP compare match event
110 = SCCP4 OCMP compare match event
101 = SCCP4 OCM4 output
100 = UART1 RX in
011 = SPI1 SDO1 out
010 = CMP2 out
001 = CLC1 out
000 = CLCINA I/O pin

For CLC2:
111 = SCCP5 OCMP compare match event
110 = SCCP4 OCMP compare match event
101 = SCCP4 OCM4 output
100 = UART2 RX in
011 = SPI2 SDO2 out
010 = CMP2 out
001 = CLC2 out
000 = CLCINA I/O pin

For CLC3:
111 = SCCP7 OCMP compare match event
110 = SCCP6 OCMP compare match event
101 = SCCP6 OCM6A output
100 = UART3 RX in
011 = SPI3 SDO3 out
010 = CMP2 out
001 = CLC3 out
000 = CLCINA I/O pin

For CLC4:
111 = SCCP7 OCMP compare match event
110 = SCCP6 OCMP compare match event
101 = SCCP6 OCM2A output
100 = Reserved
011 = Reserved
010 = CMP2 out
001 = CLC4 out
000 = CLCINA I/O pin

bit 3 **Unimplemented:** Read as '0'

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REGISTER 21-2: CLCxSEL: CLCx INPUT MUX SELECT REGISTER (CONTINUED)

bit 2-0 **DS1<2:0>:** Data Selection MUX 1 Signal Selection bits

For CLC1:
111 = SCCP5 OCMP compare match event
110 = MCCP1 OCMP compare match event
101 = RTCC event
100 = CMP3 out
011 = SPI1 SDI1 in
010 = SCCP5 OCM5 output
001 = CLC2 out
000 = CLCINB I/O pin

For CLC2:
111 = SCCP5 OCMP compare match event
110 = MCCP1 OCMP compare match event
101 = RTCC event
100 = CMP3 out
011 = SPI2 SDI2 in
010 = SCCP5 OCM6 output
001 = CLC1 out
000 = CLCINB I/O pin

For CLC3:
111 = SCCP7 OCMP compare match event
110 = MCCP2 OCMP compare match event
101 = RTCC event
100 = CMP3 out
011 = SPI3 SDI3 in
010 = SCCP7 OCM7A output
001 = CLC4 out
000 = CLCINB I/O pin

For CLC4:
111 = SCCP7 OCMP compare match event
110 = MCCP3 OCMP compare match event
101 = RTCC event
100 = CMP3 out
011 = Reserved
010 = SCCP7 OCM3A output
001 = CLC3 out
000 = CLCINB I/O pin

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REGISTER 21-3: CLCxGLS: CLCx GATE LOGIC INPUT SELECT REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	G4D4T	G4D4N	G4D3T	G4D3N	G4D2T	G4D2N	G4D1T	G4D1N
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	G3D4T	G3D4N	G3D3T	G3D3N	G3D2T	G3D2N	G3D1T	G3D1N
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	G2D4T	G2D4N	G2D3T	G2D3N	G2D2T	G2D2N	G2D1T	G2D1N
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	G1D4T	G1D4N	G1D3T	G1D3N	G1D2T	G1D2N	G1D1T	G1D1N

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **G4D4T:** Gate 4 Data Source 4 True Enable bit
1 = The Data Source 4 signal is enabled for Gate 4
0 = The Data Source 4 signal is disabled for Gate 4

bit 30 **G4D4N:** Gate 4 Data Source 4 Negated Enable bit
1 = The Data Source 4 inverted signal is enabled for Gate 4
0 = The Data Source 4 inverted signal is disabled for Gate 4

bit 29 **G4D3T:** Gate 4 Data Source 3 True Enable bit
1 = The Data Source 3 signal is enabled for Gate 4
0 = The Data Source 3 signal is disabled for Gate 4

bit 28 **G4D3N:** Gate 4 Data Source 3 Negated Enable bit
1 = The Data Source 3 inverted signal is enabled for Gate 4
0 = The Data Source 3 inverted signal is disabled for Gate 4

bit 27 **G4D2T:** Gate 4 Data Source 2 True Enable bit
1 = The Data Source 2 signal is enabled for Gate 4
0 = The Data Source 2 signal is disabled for Gate 4

bit 26 **G4D2N:** Gate 4 Data Source 2 Negated Enable bit
1 = The Data Source 2 inverted signal is enabled for Gate 4
0 = The Data Source 2 inverted signal is disabled for Gate 4

bit 25 **G4D1T:** Gate 4 Data Source 1 True Enable bit
1 = The Data Source 1 signal is enabled for Gate 4
0 = The Data Source 1 signal is disabled for Gate 4

bit 24 **G4D1N:** Gate 4 Data Source 1 Negated Enable bit
1 = The Data Source 1 inverted signal is enabled for Gate 4
0 = The Data Source 1 inverted signal is disabled for Gate 4

bit 23 **G3D4T:** Gate 3 Data Source 4 True Enable bit
1 = The Data Source 4 signal is enabled for Gate 3
0 = The Data Source 4 signal is disabled for Gate 3

bit 22 **G3D4N:** Gate 3 Data Source 4 Negated Enable bit
1 = The Data Source 4 inverted signal is enabled for Gate 3
0 = The Data Source 4 inverted signal is disabled for Gate 3

bit 21 **G3D3T:** Gate 3 Data Source 3 True Enable bit
1 = The Data Source 3 signal is enabled for Gate 3
0 = The Data Source 3 signal is disabled for Gate 3

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REGISTER 21-3: CLCxGLS: CLCx GATE LOGIC INPUT SELECT REGISTER (CONTINUED)

bit 20 **G3D3N:** Gate 3 Data Source 3 Negated Enable bit
1 = The Data Source 3 inverted signal is enabled for Gate 3
0 = The Data Source 3 inverted signal is disabled for Gate 3

bit 19 **G3D2T:** Gate 3 Data Source 2 True Enable bit
1 = The Data Source 2 signal is enabled for Gate 3
0 = The Data Source 2 signal is disabled for Gate 3

bit 18 **G3D2N:** Gate 3 Data Source 2 Negated Enable bit
1 = The Data Source 2 inverted signal is enabled for Gate 3
0 = The Data Source 2 inverted signal is disabled for Gate 3

bit 17 **G3D1T:** Gate 3 Data Source 1 True Enable bit
1 = The Data Source 1 signal is enabled for Gate 3
0 = The Data Source 1 signal is disabled for Gate 3

bit 16 **G3D1N:** Gate 3 Data Source 1 Negated Enable bit
1 = The Data Source 1 inverted signal is enabled for Gate 3
0 = The Data Source 1 inverted signal is disabled for Gate 3

bit 15 **G2D4T:** Gate 2 Data Source 4 True Enable bit
1 = The Data Source 4 signal is enabled for Gate 2
0 = The Data Source 4 signal is disabled for Gate 2

bit 14 **G2D4N:** Gate 2 Data Source 4 Negated Enable bit
1 = The Data Source 4 inverted signal is enabled for Gate 2
0 = The Data Source 4 inverted signal is disabled for Gate 2

bit 13 **G2D3T:** Gate 2 Data Source 3 True Enable bit
1 = The Data Source 3 signal is enabled for Gate 2
0 = The Data Source 3 signal is disabled for Gate 2

bit 12 **G2D3N:** Gate 2 Data Source 3 Negated Enable bit
1 = The Data Source 3 inverted signal is enabled for Gate 2
0 = The Data Source 3 inverted signal is disabled for Gate 2

bit 11 **G2D2T:** Gate 2 Data Source 2 True Enable bit
1 = The Data Source 2 signal is enabled for Gate 2
0 = The Data Source 2 signal is disabled for Gate 2

bit 10 **G2D2N:** Gate 2 Data Source 2 Negated Enable bit
1 = The Data Source 2 inverted signal is enabled for Gate 2
0 = The Data Source 2 inverted signal is disabled for Gate 2

bit 9 **G2D1T:** Gate 2 Data Source 1 True Enable bit
1 = The Data Source 1 signal is enabled for Gate 2
0 = The Data Source 1 signal is disabled for Gate 2

bit 8 **G2D1N:** Gate 2 Data Source 1 Negated Enable bit
1 = The Data Source 1 inverted signal is enabled for Gate 2
0 = The Data Source 1 inverted signal is disabled for Gate 2

bit 7 **G1D4T:** Gate 1 Data Source 4 True Enable bit
1 = The Data Source 4 signal is enabled for Gate 1
0 = The Data Source 4 signal is disabled for Gate 1

bit 6 **G1D4N:** Gate 1 Data Source 4 Negated Enable bit
1 = The Data Source 4 inverted signal is enabled for Gate 1
0 = The Data Source 4 inverted signal is disabled for Gate 1

bit 5 **G1D3T:** Gate 1 Data Source 3 True Enable bit
1 = The Data Source 3 signal is enabled for Gate 1
0 = The Data Source 3 signal is disabled for Gate 1

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REGISTER 21-3: CLCxGLS: CLCx GATE LOGIC INPUT SELECT REGISTER (CONTINUED)

bit 4	**G1D3N:** Gate 1 Data Source 3 Negated Enable bit 1 = The Data Source 3 inverted signal is enabled for Gate 1 0 = The Data Source 3 inverted signal is disabled for Gate 1
bit 3	**G1D2T:** Gate 1 Data Source 2 True Enable bit 1 = The Data Source 2 signal is enabled for Gate 1 0 = The Data Source 2 signal is disabled for Gate 1
bit 2	**G1D2N:** Gate 1 Data Source 2 Negated Enable bit 1 = The Data Source 2 inverted signal is enabled for Gate 1 0 = The Data Source 2 inverted signal is disabled for Gate 1
bit 1	**G1D1T:** Gate 1 Data Source 1 True Enable bit 1 = The Data Source 1 signal is enabled for Gate 1 0 = The Data Source 1 signal is disabled for Gate 1
bit 0	**G1D1N:** Gate 1 Data Source 1 Negated Enable bit 1 = The Data Source 1 inverted signal is enabled for Gate 1 0 = The Data Source 1 inverted signal is disabled for Gate 1

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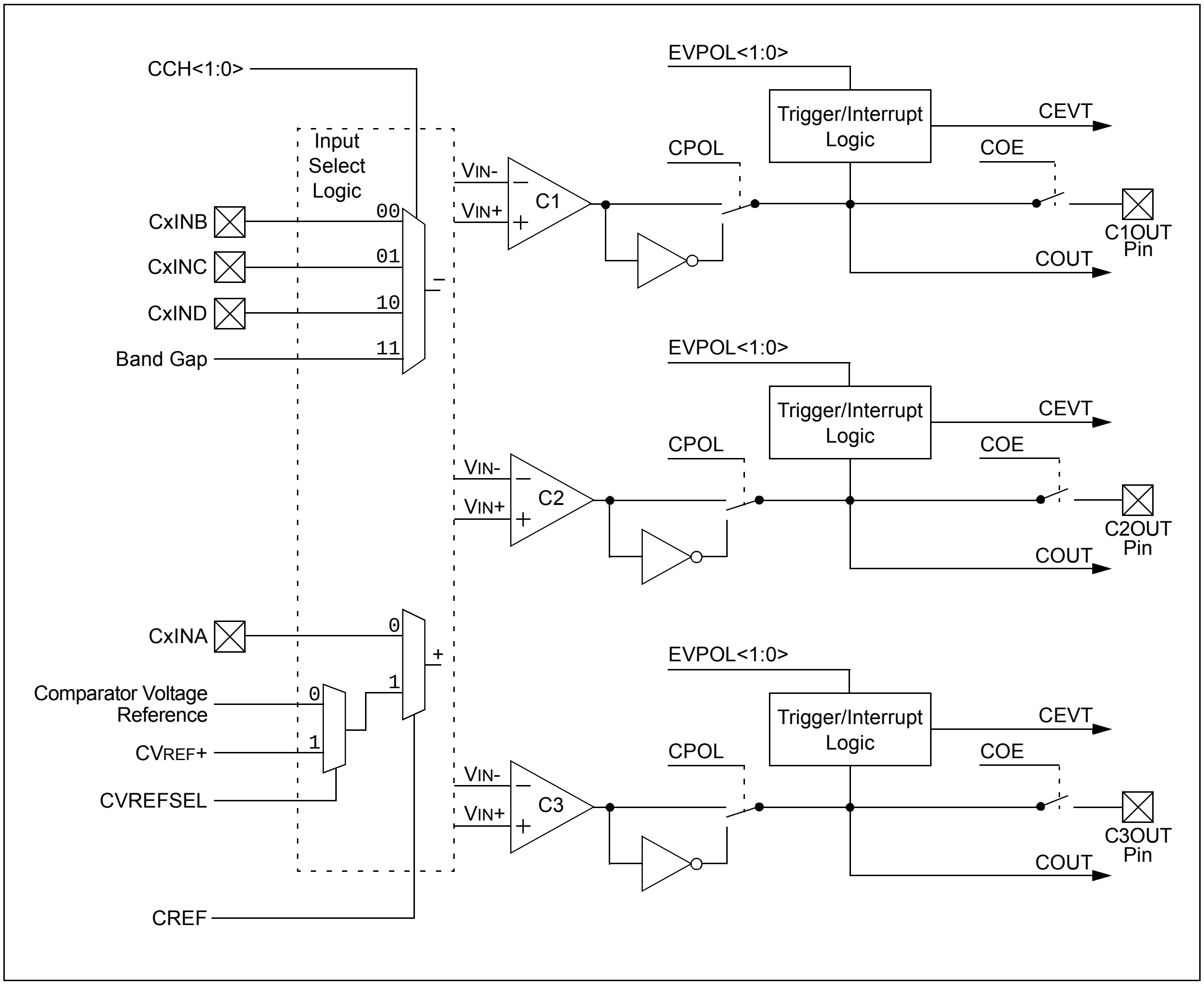
22.0 COMPARATOR

> **Note:** This data sheet summarizes the features of the PIC32MM0256GPM064 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 19. "Comparator"** (DS60001110) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32). The information in this data sheet supersedes the information in the FRM.

The comparator module provides three dual input comparators. The inputs to the comparator can be configured to use any one of five external analog inputs (CxINA, CxINB, CxINC, CxIND and CVREF+). The comparator outputs may be directly connected to the CxOUT pins. When the respective COE bit equals '1', the I/O pad logic makes the unsynchronized output of the comparator available on the pin.

A simplified block diagram of the module in shown in Figure 22-1. Each comparator has its own control register, CMxCON (Register 22-2), for enabling and configuring its operation. The output and event status of two comparators is provided in the CMSTAT register (Register 22-1).

FIGURE 22-1: THREE DUAL COMPARATOR MODULES BLOCK DIAGRAM



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22.1 Comparator Control Registers

TABLE 22-1: COMPARATORS 1, 2 AND 3 REGISTER MAP

Virtual Address (BF80_#)	Register Name[1]	Bit Range	Bits 31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
2300	CMSTAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	C3EVT	C2EVT	C1EVT	0000
		15:0	—	—	SIDL	—	—	—	—	CVREFSEL	—	—	—	—	—	C3OUT	C2OUT	C1OUT	0000
2310	CM1CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	COE	CPOL	—	—	—	CEVT	COUT	EVPOL<1:0>		—	CREF	—	—	CCH<1:0>		0000
2330	CM2CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	COE	CPOL	—	—	—	CEVT	COUT	EVPOL<1:0>		—	CREF	—	—	CCH<1:0>		0000
2350	CM3CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	COE	CPOL	—	—	—	CEVT	COUT	EVPOL<1:0>		—	CREF	—	—	CCH<1:0>		0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively.

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REGISTER 22-1: CMSTAT: COMPARATOR MODULE STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC
	—	—	—	—	—	C3EVT	C2EVT	C1EVT
15:8	U-0	U-0	R/W-0	U-0	U-0	U-0	U-0	R/W-0
	—	—	SIDL	—	—	—	—	CVREFSEL
7:0	U-0	U-0	U-0	U-0	U-0	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC
	—	—	—	—	—	C3OUT	C2OUT	C1OUT

Legend:	HC = Hardware Clearable bit	HS = Hardware Settable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-19 **Unimplemented:** Read as ‘0’

bit 18 **C3EVT:** Comparator 3 Event Status bit (read-only)
Shows the current event status of Comparator 3 (CM3CON<9>).

bit 17 **C2EVT:** Comparator 2 Event Status bit (read-only)
Shows the current event status of Comparator 2 (CM2CON<9>).

bit 16 **C1EVT:** Comparator 1 Event Status bit (read-only)
Shows the current event status of Comparator 1 (CM1CON<9>).

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13 **SIDL:** Comparator Stop in Idle Mode bit
1 = Discontinues operation of all comparators when device enters Idle mode
0 = Continues operation of all enabled comparators in Idle mode

bit 12-9 **Unimplemented:** Read as ‘0’

bit 8 **CVREFSEL:** Comparator Reference Voltage Select Enable bit
1 = External voltage reference from the CVREF+ pin is selected
0 = Internal band gap voltage reference is selected

bit 7-3 **Unimplemented:** Read as ‘0’

bit 2 **C3OUT:** Comparator 3 Output Status bit (read-only)
Shows the current output of Comparator 3 (CM3CON<8>).

bit 1 **C2OUT:** Comparator 2 Output Status bit (read-only)
Shows the current output of Comparator 2 (CM2CON<8>).

bit 0 **C1OUT:** Comparator 1 Output Status bit (read-only)
Shows the current output of Comparator 1 (CM1CON<8>).

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REGISTER 22-2: CMxCON: COMPARATOR x CONTROL REGISTERS (COMPARATORS 1, 2 AND 3)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	R-0, HS, HC	R-0, HS, HC
	ON	COE	CPOL	—	—	—	CEVT	COUT
7:0	R/W-0	R/W-0	U-0	R/W-0	U-0	U-0	R/W-0	R/W-0
	EVPOL<1:0>		—	CREF	—	—	CCH<1:0>	

Legend:	HC = Hardware Clearable bit	HS = Hardware Settable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Comparator Enable bit
1 = Comparator is enabled
0 = Comparator is disabled

bit 14 **COE:** Comparator Output Enable bit
1 = Comparator output is present on the CxOUT pin
0 = Comparator output is internal only

bit 13 **CPOL:** Comparator Output Polarity Select bit
1 = Comparator output is inverted
0 = Comparator output is not inverted

bit 12-10 **Unimplemented:** Read as '0'

bit 9 **CEVT:** Comparator Event bit
1 = Comparator event that is defined by EVPOL<1:0> has occurred; subsequent triggers and interrupts are disabled until the bit is cleared
0 = Comparator event has not occurred

bit 8 **COUT:** Comparator Output bit
When CPOL = 0:
1 = VIN+ > VIN-
0 = VIN+ < VIN-
When CPOL = 1:
1 = VIN+ < VIN-
0 = VIN+ > VIN-

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REGISTER 22-2: CMxCON: COMPARATOR x CONTROL REGISTERS (COMPARATORS 1, 2 AND 3) (CONTINUED)

bit 7-6 **EVPOL<1:0>:** Trigger/Event/Interrupt Polarity Select bits
11 = Trigger/event/interrupt is generated on any change of the comparator output (while CEVT = 0)
10 = Trigger/event/interrupt is generated on transition of the comparator output:
If CPOL = 0 (non-inverted polarity):
High-to-low transition only.
If CPOL = 1 (inverted polarity):
Low-to-high transition only.
01 = Trigger/event/interrupt is generated on transition of the comparator output:
If CPOL = 0 (non-inverted polarity):
Low-to-high transition only.
If CPOL = 1 (inverted polarity):
High-to-low transition only.
00 = Trigger/event/interrupt generation is disabled

bit 5 **Unimplemented:** Read as ‘0’

bit 4 **CREF:** Comparator Reference Select bit (non-inverting input)
1 = Non-inverting input connects to the internal reference defined by the CVREFSEL bit in CMSTAT register
0 = Non-inverting input connects to the CxINA pin

bit 3-2 **Unimplemented:** Read as ‘0’

bit 1-0 **CCH<1:0>:** Comparator Channel Select bits
11 = Inverting input of the comparator connects to the band gap reference voltage
10 = Inverting input of the comparator connects to the CxIND pin
01 = Inverting input of the comparator connects to the CxINC pin
00 = Inverting input of the comparator connects to the CxINB pin

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23.0 VOLTAGE REFERENCE (CVREF)

> **Note:** This data sheet summarizes the features of the PIC32MM0256GPM064 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 20. "Comparator Voltage Reference"** (DS61109) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32). The information in this data sheet supersedes the information in the FRM.

The CVREF module is a 32-TAP DAC that provides a selectable reference voltage. Although its primary purpose is to provide a reference for the analog comparators, it may also be used independently from them.

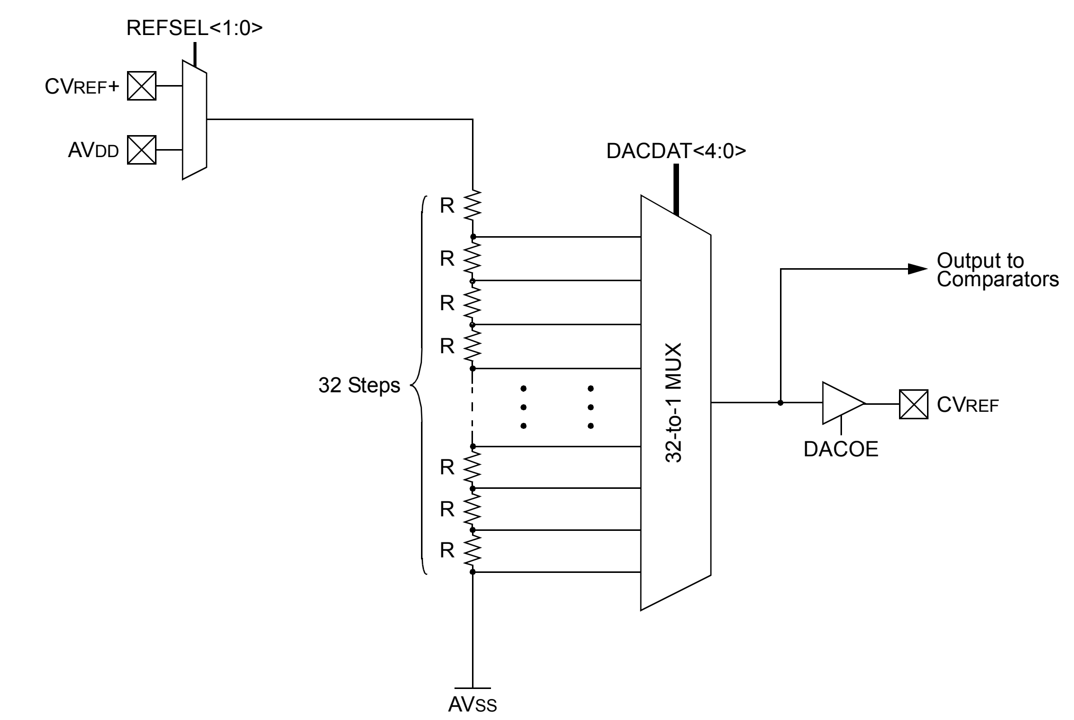
The module's supply reference can be provided from either the device VDD/VSS or an external voltage reference pin. The CVREF output is available for the comparators and for pin output.

The voltage reference has the following features:

- 32 Output Levels are Available
- Internally Connected to Comparators to Conserve Device Pins
- Output can be Connected to a Pin

A block diagram of the CVREF module is illustrated in Figure 23-1.

FIGURE 23-1: VOLTAGE REFERENCE BLOCK DIAGRAM



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23.1 Voltage Reference Control Registers

TABLE 23-1: VOLTAGE REFERENCE REGISTER MAP

Virtual Address (BF80_#)	Register Name[1]	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
2380	DAC1CON	31:16	—	—	—	—	—	—	—	—	—	—	—	DACDAT<4:0>					0000
		15:0	ON	—	—	—	—	—	—	DACOE	—	—	—	—	—	—	REFSEL<1:0>		0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: The register in this table has corresponding CLR, SET and INV registers at its virtual address, plus offsets of 0x4, 0x8 and 0xC, respectively.

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REGISTER 23-1: DAC1CON: VOLTAGE REFERENCE CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	DACDAT<4:0>				
15:8	R/W-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
	ON	—	—	—	—	—	—	DACOE
7:0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
	—	—	—	—	—	—	REFSEL<1:0>	

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-21 **Unimplemented:** Read as ‘0’

bit 20-16 **DACDAT<4:0>:** Voltage Reference Selection bits

11111 = (DACDAT<4:0> * CVREF+/32) or (DACDAT<4:0> * AVDD/32) volts depending on the REFSEL<1:0> bits
•
•
•
00000 = 0.0 volts

bit 15 **ON:** Voltage Reference Enable bit

1 = Voltage reference is enabled
0 = Voltage reference is disabled

bit 14-9 **Unimplemented:** Read as ‘0’

bit 8 **DACOE:** Voltage Reference Output Enable bit

1 = Voltage level is output on the CVREF pin
0 = Voltage level is disconnected from the CVREF pin

bit 7-2 **Unimplemented:** Read as ‘0’

bit 1-0 **REFSEL<1:0>:** Voltage Reference Source Select bits

11 = Reference voltage is AVDD
10 = No reference is selected – output is AVSS
01 = Reference voltage is the CVREF+ input pin voltage
00 = No reference is selected – output is AVSS

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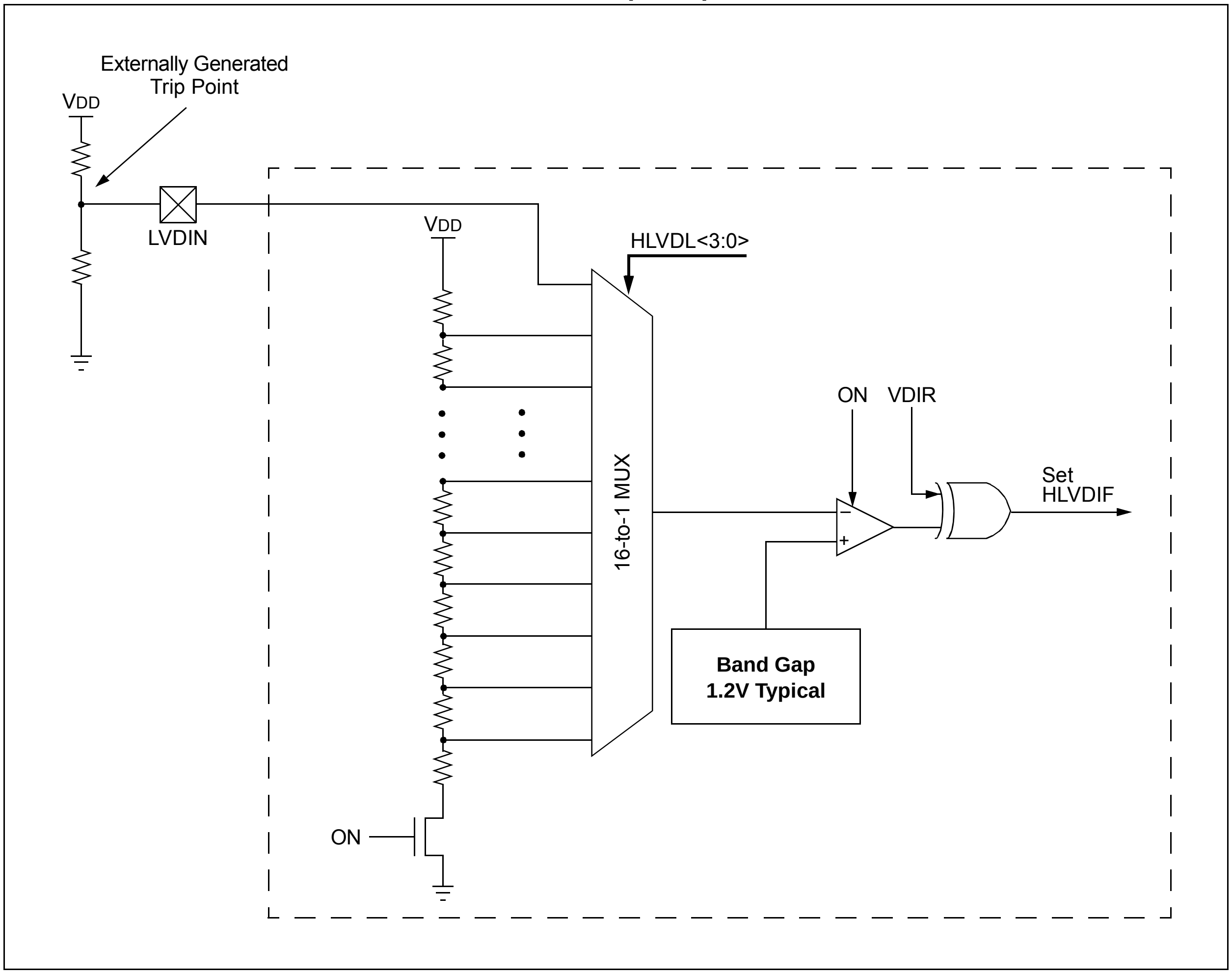
24.0 HIGH/LOW-VOLTAGE DETECT (HLVD)

The High/Low-Voltage Detect (HLVD) module is a programmable circuit that allows the user to specify both the device voltage trip point and the direction of change.

An interrupt flag is set if the device experiences an excursion past the trip point in the direction of change. If the interrupt is enabled, the program execution will branch to the interrupt vector address and the software can then respond to the interrupt.

The HLVD Control register (see Register 24-1) completely controls the operation of the HLVD module. This allows the circuitry to be "turned off" by the user under software control, which minimizes the current consumption for the device.

FIGURE 24-1: HIGH/LOW-VOLTAGE DETECT (HLVD) MODULE BLOCK DIAGRAM



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24.1 High/Low-Voltage Detect Registers

TABLE 24-1: HIGH/LOW-VOLTAGE DETECT REGISTER MAP

Virtual Address (BF80_#)	Register Name[1]	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
2920	HLVDCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	VDIR	BGVST	IRVST	HLEVT	—	—	—	—	HLVDL<3:0>				0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: The register in this table has corresponding CLR, SET and INV registers at its virtual address, plus offsets of 0x4, 0x8 and 0xC, respectively.

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REGISTER 24-1: HLVDCON: HIGH/LOW-VOLTAGE DETECT CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	
15:8	R/W-0	U-0	R/W-0	U-0	R/W-0	R-0, HS, HC	R-0, HS, HC	R-0, HS, HC
	ON	—	SIDL	—	VDIR	BGVST	IRVST	HLEVT
7:0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	HLVDL<3:0>			

Legend:	HC = Hardware Clearable bit	HS = Hardware Settable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as ‘0’

bit 15 **ON:** HLVD Power Enable bit
1 = HLVD is enabled
0 = HLVD is disabled

bit 14 **Unimplemented:** Read as ‘0’

bit 13 **SIDL:** HLVD Stop in Idle Mode bit
1 = Discontinues module operation when device enters Idle mode
0 = Continues module operation in Idle mode

bit 12 **Unimplemented:** Read as ‘0’

bit 11 **VDIR:** Voltage Change Direction Select bit
1 = Event occurs when voltage equals or exceeds trip point (HLVDL<3:0>)
0 = Event occurs when voltage equals or falls below trip point (HLVDL<3:0>)

bit 10 **BGVST:** Band Gap Voltage Stable Flag bit
1 = Indicates that the band gap voltage is stable
0 = Indicates that the band gap voltage is unstable

bit 9 **IRVST:** Internal Reference Voltage Stable Flag bit
1 = Internal reference voltage is stable; the High-Voltage Detect logic generates the interrupt flag at the specified voltage range
0 = Internal reference voltage is unstable; the High-Voltage Detect logic will not generate the interrupt flag at the specified voltage range and the HLVD interrupt should not be enabled

bit 8 **HLEVT:** High/Low-Voltage Detection Event Status bit
1 = Indicates HLVD event is active
0 = Indicates HLVD event is not active

bit 7-4 **Unimplemented:** Read as ‘0’

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REGISTER 24-1: HLVDCON: HIGH/LOW-VOLTAGE DETECT CONTROL REGISTER (CONTINUED)

bit 3-0 **HLVDL<3:0>:** High/Low-Voltage Detection Limit bits

1111 = External analog input is used (input comes from the LVDIN pin and compared with 1.2V band gap)
1110 = V_{DD} trip point is between 2.00V and 2.22V
1101 = V_{DD} trip point is between 2.08V and 2.33V
1100 = V_{DD} trip point is between 2.15V and 2.44V
1011 = V_{DD} trip point is between 2.25V and 2.55V
1010 = V_{DD} trip point is between 2.35V and 2.69V
1001 = V_{DD} trip point is between 2.45V and 2.80V
1000 = V_{DD} trip point is between 2.65V and 2.98V
0111 = V_{DD} trip point is between 2.75V and 3.09V
0110 = V_{DD} trip point is between 2.95V and 3.30V
0101 = V_{DD} trip point is between 3.25V and 3.63V
0100-0000 = Reserved; do not use.

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25.0 POWER-SAVING FEATURES

Note:	This data sheet summarizes the features of the PIC32MM0256GPM064 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 10. "Power-Saving Modes"** (DS60001130) in the *"PIC32 Family "Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32). The information in this data sheet supersedes the information in the FRM.

This section describes the power-saving features for the PIC32MM0256GPM064 family devices. These devices offer various methods and modes that allow the application to balance power consumption with device performance. In all of the methods and modes described in this section, power saving is controlled by software. The peripherals and CPU can be halted or disabled to reduce power consumption.

25.1 Sleep Mode

In Sleep mode, the CPU and most peripherals are halted and the associated clocks are disabled. Some peripherals can continue to operate in Sleep mode and can be used to wake the device from Sleep. See the individual peripheral module sections for descriptions of behavior in Sleep. The device enters Sleep mode when the SLPEN bit (OSCCON<4>) is set and a `WAIT` instruction is executed.

Sleep mode includes the following characteristics:

- There can be a Wake-up Delay based on the Oscillator Selection
- The Fail-Safe Clock Monitor (FSCM) does not Operate During Sleep mode
- The BOR Circuit remains Operative during Sleep mode
- The WDT, if Enabled, is not automatically Cleared prior to Entering Sleep mode
- Some Peripherals can Continue to Operate at Limited Functionality in Sleep mode; these Peripherals include I/O Pins that Detect a Change in the Input Signal, WDT, ADC, UART and Peripherals that use an External Clock Input or the Internal LPRC Oscillator (e.g., RTCC and Timer1)
- I/O Pins Continue to Sink or Source Current in the Same Manner as they do when the Device is not in Sleep

The processor will exit, or "wake-up", from Sleep on one of the following events:

- On any interrupt from an enabled source that is operating in Sleep. The interrupt priority must be greater than the current CPU priority.
- On any form of device Reset.
- On a WDT time-out.

If the interrupt priority is lower than or equal to the current priority, the CPU will remain halted, but the Peripheral Bus Clock (PBCLK) will start running and the device will enter into Idle mode. To set or clear the SLPEN bit, an unlock sequence must be executed. Refer to **Section 26.4 "System Registers Write Protection"** for details.

25.2 Standby Sleep Mode

Standby Sleep mode places the voltage regulator in Standby mode. This mode draws less power than Sleep mode but has a longer wake-up time. Standby Sleep mode is entered by setting the VREGS bit (PWRCON<0>) prior to entering Sleep by executing a `WAIT` instruction. All peripherals that can operate in Sleep mode can operate in Standby Sleep mode.

25.3 Retention Sleep Mode

Retention Sleep uses a separate voltage regulator to provide the lowest power Sleep mode. This mode has a longer wake-up time than Sleep or Standby Sleep. This mode is entered by clearing the RETVR Configuration bit (FPOR<2>) and setting the RETEN bit (PWRCON<1>), prior to entering Sleep mode, and executing a `WAIT` instruction.

Only select peripherals, such as Timer1, WDT, RTCC and REFO, can operate in Retention Sleep mode.

Note:	In Retention mode, the maximum peripheral output frequency to an I/O pin must be less than 33 kHz.

Note:	When $\overline{\text{MCLR}}$ is used to wake the device from Retention Sleep, a POR Reset will occur.

25.4 Idle Mode

In Idle mode, the CPU is halted; however, all clocks are still enabled. This allows peripherals to continue to operate. Peripherals can be individually configured to halt when entering Idle by setting their respective SIDL bit. Latency, when exiting Idle mode, is very low due to the CPU oscillator source remaining active.

The device enters Idle mode when the SLPEN bit (OSCCON<4>) is clear and a `WAIT` instruction is executed.

The processor will wake or exit from Idle mode on the following events:

- On any interrupt event for which the interrupt source is enabled. The priority of the interrupt event must be greater than the current priority of the CPU. If the priority of the interrupt event is lower than or equal to the current priority of the CPU, the CPU will remain halted and the device will remain in Idle mode.
- On any form of device Reset.
- On a WDT time-out interrupt.

To set or clear the SLPEN bit, an unlock sequence must be executed. Refer to **Section 26.4 "System Registers Write Protection"** for details.

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25.5 Peripheral Module Disable

The Peripheral Module Disable (PMD) registers provide a method to disable a peripheral module by stopping all clock sources supplied to that module. When a peripheral is disabled using the appropriate PMD control bit, the peripheral is in a minimum power consumption state. The control and status registers associated with the peripheral are also disabled, so writes to those registers do not take effect and read values are invalid.

To disable a peripheral, the associated PMDx bit must be set to ‘1’. To enable a peripheral, the associated PMDx bit must be cleared (default).

To prevent accidental configuration changes under normal operation, writes to the PMDx registers are not allowed. Attempted writes appear to execute normally, but the contents of the registers remain unchanged. To change these registers, they must be unlocked in hardware. The register lock is controlled by the PMDLOCK bit in the PMDCON register (PMDCON<11>). Setting PMDLOCK prevents writes to the control registers; clearing PMDLOCK allows writes. To set or clear PMDLOCK, an unlock sequence must be executed. Refer to **Section 26.4 “System Registers Write Protection”** for details.

Table 25-1 lists the module disable bits locations for all modules.

TABLE 25-1: PERIPHERAL MODULE DISABLE BITS AND LOCATIONS

Peripheral	PMDx Bit Name	Register Name and Bit Location
Analog-to-Digital Converter (ADC)	ADCMD	PMD1<0>
Voltage Reference (VR)	VREFMD	PMD1<12>
High/Low-Voltage Detect (HLVD)	HLVDMD	PMD1<20>
Comparator 1 (CMP1)	CMP1MD	PMD2<0>
Comparator 2 (CMP2)	CMP2MD	PMD2<1>
Comparator 3 (CMP3)	CMP3MD	PMD2<2>
Configurable Logic Cell 1 (CLC1)	CLC1MD	PMD2<24>
Configurable Logic Cell 2 (CLC2)	CLC2MD	PMD2<25>
Configurable Logic Cell 3 (CLC3)	CLC3MD	PMD2<26>
Configurable Logic Cell 4 (CLC4)	CLC4MD	PMD2<27>
Multiple Outputs Capture/Compare/PWM/ Timer1 (MCCP1)	CCP1MD	PMD3<8>
Multiple Outputs Capture/Compare/PWM/ Timer2 (MCCP2)	CCP2MD	PMD3<9>
Multiple Outputs Capture/Compare/PWM/ Timer3 (MCCP3)	CCP3MD	PMD3<10>
Single Output Capture/Compare/PWM/ Timer4 (SCCP4)	CCP4MD	PMD3<11>
Single Output Capture/Compare/PWM/ Timer5 (SCCP5)	CCP5MD	PMD3<12>
Single Output Capture/Compare/PWM/ Timer6 (SCCP6)	CCP6MD	PMD3<13>
Single Output Capture/Compare/PWM/ Timer7 (SCCP7)	CCP7MD	PMD3<14>
Single Output Capture/Compare/PWM/ Timer8 (SCCP8)	CCP8MD	PMD3<15>
Single Output Capture/Compare/PWM/ Timer9 (SCCP9)	CCP9MD	PMD3<16>
Timer1 (TMR1)	T1MD	PMD4<0>
Timer2 (TMR2)	T2MD	PMD4<1>
Timer3 (TMR3)	T3MD	PMD4<2>
Universal Asynchronous Receiver Transmitter 1 (UART1)	U1MD	PMD5<0>

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TABLE 25-1: PERIPHERAL MODULE DISABLE BITS AND LOCATIONS (CONTINUED)

Peripheral	PMDx Bit Name	Register Name and Bit Location
Universal Asynchronous Receiver Transmitter 2 (UART2)	U2MD	PMD5<1>
Universal Asynchronous Receiver Transmitter 3 (UART3)	U3MD	PMD5<2>
Serial Peripheral Interface 1 (SPI1)	SPI1MD	PMD5<8>
Serial Peripheral Interface 2 (SPI2)	SPI2MD	PMD5<9>
Serial Peripheral Interface 3 (SPI3)	SPI3MD	PMD5<10>
Inter-Integrated Circuit Interface 1 (I2C1)	I2C1MD	PMD5<16>
Inter-Integrated Circuit Interface 2 (I2C2)	I2C2MD	PMD5<17>
Inter-Integrated Circuit Interface 3 (I2C3)	I2C3MD	PMD5<18>
Universal Serial Bus (USB)	USBMD	PMD5<24>
Real-Time Clock and Calendar (RTCC)	RTCCMD	PMD6<0>
Reference Clock Output (REFO1)	REFOMD	PMD6<8>
Direct Memory Access (DMA)	DMAMD	PMD7<4>

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TABLE 25-2: PERIPHERAL MODULE DISABLE REGISTERS MAP

Virtual Address (BF80_#)	Register Name[1]	Bit Range	Bits 31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
35B0	PMDCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FFFF
		15:0	—	—	—	—	PMDLOCK	—	—	—	—	—	—	—	—	—	—	—	F7FF
35C0	PMD1	31:16	—	—	—	—	—	—	—	—	—	—	—	HLVDMD	—	—	—	—	FFEF
		15:0	—	—	—	VREFMD	—	—	—	—	—	—	—	—	—	—	—	ADCMD	EFFE
35D0	PMD2	31:16	—	—	—	—	CLC4MD	CLC3MD	CLC2MD	CLC1MD	—	—	—	—	—	—	—	—	F0FF
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	CMP3MD	CMP2MD	CMP1MD	FFF8
35E0	PMD3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CCP9MD	FFFE
		15:0	CCP8MD	CCP7MD	CCP6MD	CCP5MD	CCP4MD	CCP3MD	CCP2MD	CCP1MD	—	—	—	—	—	—	—	—	00FF
35F0	PMD4	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FFFF
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	T3MD	T2MD	T1MD	FFF8
3600	PMD5	31:16	—	—	—	—	—	—	—	USBMD	—	—	—	—	—	I2C3MD	I2C2MD	I2C1MD	FEF8
		15:0	—	—	—	—	—	SPI3MD	SPI2MD	SPI1MD	—	—	—	—	—	U3MD	U2MD	U1MD	F8F8
3610	PMD6	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FEFF
		15:0	—	—	—	—	—	—	—	REFOMD	—	—	—	—	—	—	—	RTCCMD	FEFE
3620	PMD7	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FFFF
		15:0	—	—	—	—	—	—	—	—	—	—	—	DMAMD	—	—	—	—	FFEF

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively.

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25.6 On-Chip Voltage Regulator Low-Power Modes

The main on-chip regulator always consumes a small incremental amount of current over IDD/IPD, including when the device is in Sleep mode, even though the core digital logic does not require power. To provide additional savings in applications where power resources are critical, the regulator can be made to enter Standby mode on its own whenever the device goes into Sleep mode. This feature is controlled by the VREGS bit (PWRCON<0>). Clearing the VREGS bit enables Standby mode.

Note 1: The SYSKEY register is used to unlock the PWRCON register.

When in Sleep mode, PIC32MM0256GPM064 family devices may use a separate low-power, low-voltage/retention regulator to power critical circuits. This regulator, which operates at 1.2V nominal, maintains power to data RAM, WDT, Timer1 and the RTCC, while all other core digital logic is powered down. The low-voltage/retention regulator is only available when Sleep mode is invoked. It is controlled by the RETVR Configuration bit (FPOR<2>) and in firmware by the RETEN bit (PWRCON<1>). RETVR must be programmed to zero (= `0`) and the RETEN bit must be set (= `1`) for the regulator to be enabled. When the retention regulator is enabled, the main regulator is off and does not consume power.

Note 1: When using the low-voltage/retention regulator, VREGS (PWRCON<0>) must be set to '`1`'.

The main voltage regulator takes approximately 10 µS to generate output. During this time, designated as TVREG, code execution is disabled. TVREG is applied every time the device resumes operation after standby (VREGS bit = `0`) or retention (RETEN bit = `1`, RETVR bit = `0`) modes. The TVREG specification is listed in Table 29-12.

25.7 Low-Power Brown-out Reset

The PIC32MM0256GPM064 family devices have a second low-power Brown-out Reset circuit with a reduced trip point precision. This low-power BOR circuit can be activated when the main BOR is disabled. It can be done by programming the LPBOREN Configuration bit (FPOR<3>) to one.

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NOTES:

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26.0 SPECIAL FEATURES

> **Note:** This data sheet summarizes the features of the PIC32MM0256GPM064 family of devices. However, it is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 33. "Programming and Diagnostics"** (DS61129) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32). The information in this data sheet supersedes the information in the FRM.

26.1 Configuration Bits

PIC32MM0256GPM064 family devices contain a Boot Flash Memory (BFM) with an associated configuration space. All Configuration Words are listed in Table 26-3 and Table 26-4, and Register 26-1 through Register 26-6 describe the configuration options.

26.2 Code Execution from RAM

PIC32MM0256GPM064 family devices allow executing the code from RAM. The starting boundary of this special RAM space can be adjusted using the EXECADDR<7:0> bits in the CFGCON register with a 1-Kbyte step. Writing a non-zero value to these bits will move the boundary, effectively reducing the total amount of program memory space in RAM. Refer to Table 26-5 and Register 26-7 for more information.

26.3 Device ID

The Device ID identifies the device used. The ID can be read from the DEVID register. The Device IDs for the PIC32MM0256GPM064 family devices are listed in Table 26-1. Also refer to Table 26-5 and Register 26-8 for more information.

TABLE 26-1: DEVICE IDs FOR PIC32MM0256GPM064 FAMILY DEVICES

Device	DEVID
PIC32MM0064GPM028	0x07708053
PIC32MM0128GPM028	0x07710053
PIC32MM0256GPM028	0x07718053
PIC32MM0064GPM036	0x0770A053
PIC32MM0128GPM036	0x07712053
PIC32MM0256GPM036	0x0771A053
PIC32MM0064GPM048	0x0772C053
PIC32MM0128GPM048	0x07734053
PIC32MM0256GPM048	0x0773C053
PIC32MM0064GPM064	0x0770E053
PIC32MM0128GPM064	0x07716053
PIC32MM0256GPM064	0x0771E053

26.4 System Registers Write Protection

The critical registers in the PIC32MM0256GPM064 family devices are protected (locked) to prevent an accidental write. If the registers are locked, a special two-step unlock sequence is required to modify the content of these registers (refer to Example 26-1). Once an unlock sequence is performed, the registers remain unlocked until they are relocked by writing an invalid key value.

A system unlock sequence is invalidated by writes to addresses other than SYSKEY. To prevent this, DMA transfers and interrupts should be disabled or the unlock sequence can be performed until a read of SYSKEY indicates a successful unlock (refer to Example 26-2).

To unlock the registers, the following steps should be done:

1. Disable interrupts and DMA transfers prior to the system unlock sequence.
2. Write a non-key value (such as 0x00000000) to the SYSKEY register to perform a lock.
3. Execute the system unlock sequence by writing the key values of 0xAA996655 and 0x556699AA to the SYSKEY register, in two back-to-back assembly or 'C' instructions.
4. Write the new value to the required register.
5. Write a non-key value (such as 0x00000000) to the SYSKEY register to perform a lock.
6. Re-enable interrupts and DMA transfers.

EXAMPLE 26-1: SYSTEM UNLOCK

```
SYSKEY = 0;             // force lock
SYSKEY = AA996655;      // unlock sequence
SYSKEY = 556699AA;      // lock sequence
// user code to modify register contents
SYSKEY = 0;             // relock
```

EXAMPLE 26-2: SYSTEM UNLOCK WITH DMA AND INTERRUPTS ENABLED

```
While (SYSKEY == 0) // repeat unlock sequence
                       until unlock succeeds
{
SYSKEY = 0;          // force lock
SYSKEY = AA996655;   // unlock sequence
SYSKEY = 556699AA;   // lock sequence
}

// user code to modify register contents
SYSKEY = 0;          // relock
```


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The registers that require this unlocking sequence are listed in the Table 26-2.

TABLE 26-2: SYSTEM LOCKED REGISTERS

Register Name	Register Description	Peripheral
OSCCON	Oscillator Control	Oscillator
SPLLCON	System PLL Control	Oscillator
OSCTUN	FRC Tuning	Oscillator
PMDCON	Peripheral Module Disable Control	PMD
RSWRST	Software Reset	Reset
RPCON	Peripheral Pin Select Configuration	I/O Ports
PWRCON	Sleep Power Control	System
RTCCON1	RTCC Control	RTCC

The SYSKEY register read value indicates the status. A value of '0' indicates that the system registers are locked. A value of '1' indicates that the system registers are unlocked. For more information about the SYSKEY register refer to Table 26-5 and Register 26-9.

26.5 Band Gap Voltage Reference

PIC32MM0256GPM064 family devices have a precision voltage reference band gap circuit used by many modules. The analog buffers are implemented between the band gap circuit and these modules. The buffers are automatically enabled by the hardware if some part of the device needs the band gap reference. The stabilization time is required when the buffer is switched on. The software can enable these buffers in advance to allow the band gap voltage to stabilize before the module uses it. The ANGFG register contains bits to enable the band gap buffers for the comparators (VBGCMP bit) and ADC (VBGADC bit). Refer to Table 26-6 and Register 26-10 for more information.

26.6 Programming and Diagnostics

PIC32MM0256GPM064 family devices provide a complete range of programming and diagnostic features:

- Simplified field programmability using two-wire In-Circuit Serial Programming™ (ICSP™) interfaces
- Debugging using ICSP
- Programming and debugging capabilities using the EJTAG extension of JTAG
- JTAG boundary scan testing for device and board diagnostics

26.7 Unique Device Identifier (UDID)

PIC32MM0256GPM064 family devices are individually encoded during final manufacturing with a Unique Device Identifier or UDID. The UDID cannot be erased by a bulk erase command or any other user accessible means. This feature allows for manufacturing traceability of Microchip Technology devices in applications where this is a requirement. It may also be used by the application manufacturer for any number of things that may require unique identification, such as:

- Tracking the device
- Unique serial number
- Unique security key

The UDID comprises five 32-bit program words. When taken together, these fields form a unique 160-bit identifier.

The UDID is stored in five read-only locations, located from 0xBFC41840 to 0xBFC41850 in the device configuration space. Table 26-7 lists the addresses of the Identifier Words.

26.8 Reserved Registers

PIC32MM0256GPM064 family devices have 3 reserved registers, located at 0xBF800400, 0xBF800480 and 0xBF802280. The application code must not modify these reserved locations. Table 26-8 lists the addresses of these reserved registers.

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26.9 Configuration Word Registers

TABLE 26-3: CONFIGURATION WORDS SUMMARY

Virtual Address (BFC0_#)	Register Name	Bit Range	Bits 31\15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0
17C0	RESERVED	31:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
		15:0	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
17C4	FDEVOPT	31:16	USERID<15:0>															
		15:0	FVBUSIO	FUSBIDIO	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	ALTI2C	SOSCHP	r-1	r-1	r-1
17C8	FICD	31:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
		15:0	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	ICS<1:0>		JTAGEN	r-1	r-1
17CC	FPOR	31:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
		15:0	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	LPBOREN	RETVR	BOREN<1:0>	
17D0	FWDT	31:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
		15:0	FWDTEN	RCLKSEL<1:0>		RWDTPS<4:0>					WINDIS	FWDTWINSZ<1:0>		SWDTPS<4:0>				
17D4	FOSCSEL	31:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
		15:0	FCKSM<1:0>		r-1	SOSCSEL	r-1	OSCIOFNC	POSCMOD<1:0>		IESO	SOSCEN	r-1	PLLSRC	r-1	FNOSC<2:0>		
17D8	FSEC	31:16	CP	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
		15:0	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
17DC	RESERVED	31:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
		15:0	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
17E0	RESERVED	31:16	r-0	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
		15:0	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
17E4	RESERVED	31:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
		15:0	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1

Legend: r-0 = Reserved bit, must be programmed as '0'; r-1 = Reserved bit, must be programmed as '1'.

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TABLE 26-4: ALTERNATE CONFIGURATION WORDS SUMMARY

Virtual Address (BFC0_#)	Register Name	Bit Range	Bits 31\15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0
1740	RESERVED	31:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
		15:0	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
1744	AFDEVOPT	31:16	USERID<15:0>															
		15:0	FVBUSIO	FUSBIDIO	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	ALTI2C	SOSCHP	r-1	r-1	r-1
1748	AFICD	31:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
		15:0	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	ICS<1:0>		JTAGEN	r-1	r-1
174C	AFPOR	31:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
		15:0	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	LPBOREN	RETVR	BOREN<1:0>	
1750	AFWDT	31:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
		15:0	FWDTEN	RCLKSEL<1:0>		RWDTPS<4:0>					WINDIS	FWDTWINSZ<1:0>		SWDTPS<4:0>				
1754	AFOSCSEL	31:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
		15:0	FCKSM<1:0>		r-1	SOSCSEL	r-1	OSCIOFNC	POSCMOD<1:0>		IESO	SOSCEN	r-1	PLLSRC	r-1	FNOSC<2:0>		
1758	AFSEC	31:16	CP	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
		15:0	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
175C	RESERVED	31:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
		15:0	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
1760	RESERVED	31:16	r-0	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
		15:0	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
1764	RESERVED	31:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
		15:0	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1

Legend: r-0 = Reserved bit, must be programmed as '0'; r-1 = Reserved bit, must be programmed as '1'.

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REGISTER 26-1: FDEVOPT/AFDEVOPT: DEVICE OPTIONS CONFIGURATION REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/P	R/P	R/P	R/P	R/P	R/P	R/P	R/P
	USERID<15:8>							
23:16	R/P	R/P	R/P	R/P	R/P	R/P	R/P	R/P
	USERID<7:0>							
15:8	R/P	R/P	r-1	r-1	r-1	r-1	r-1	r-1
	FVBUSIO	FUSBIDIO	—	—	—	—	—	—
7:0	r-1	r-1	r-1	R/P	R/P	r-1	r-1	r-1
	—	—	—	ALTI2C	SOSCHP	—	—	—

Legend:	r = Reserved bit	P = Programmable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-16 **USERID<15:0>:** User ID bits (2 bytes which can programmed to any value)

bit 15 **FVBUSIO:** USB VBUS_ON Selection bit
1 = VBUSON pin is controlled by the USB module
0 = VBUSON pin is controlled by the port function

bit 14 **FUSBIDIO:** USB USBID Selection bit
1 = USBID pin is controlled by the USB module
0 = USBID pin is controlled by the port function

bit 13-5 **Reserved:** Program as ‘1’

bit 4 **ALTI2C:** Alternate I2C1 Location Select bit
1 = SDA1 and SCL1 are on pins, RB8 and RB9
0 = SDA1 and SCL1 are moved to alternate I^2C locations, RB5 and RC9

bit 3 **SOSCHP:** Secondary Oscillator (SOSC) High-Power Enable bit
1 = SOSC operates in normal power mode
0 = SOSC operates in High-Power mode

bit 2-0 **Reserved:** Program as ‘1’

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REGISTER 26-2: FICD/AFICD: ICD/DEBUG CONFIGURATION REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
	—	—	—	—	—	—	—	—
23:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
	—	—	—	—	—	—	—	—
15:8	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
	—	—	—	—	—	—	—	—
7:0	r-1	r-1	r-1	R/P	R/P	R/P	r-1	r-1
	—	—	—	ICS<1:0>		JTAGEN	—	—

Legend:	r = Reserved bit	P = Programmable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-5 **Reserved:** Program as ‘1’

bit 4-3 **ICS<1:0>:** ICE/ICD Communication Channel Selection bits
- 11 = Communicates on PGEC1/PGED1
- 10 = Communicates on PGEC2/PGED2
- 01 = Communicates on PGEC3/PGED3
- 00 = Not connected

bit 2 **JTAGEN:** JTAG Enable bit
- 1 = JTAG is enabled
- 0 = JTAG is disabled

bit 1-0 **Reserved:** Program as ‘1’

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REGISTER 26-3: FPOR/AFPOR: POWER-UP SETTINGS CONFIGURATION REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
	—	—	—	—	—	—	—	—
23:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
	—	—	—	—	—	—	—	—
15:8	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
	—	—	—	—	—	—	—	—
7:0	r-1	r-1	r-1	r-1	R/P	R/P	R/P	R/P
	—	—	—	—	LPBOREN	RETVR	BOREN<1:0>	

Legend:	r = Reserved bit	P = Programmable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-4 **Reserved:** Program as ‘1’

bit 3 **LPBOREN:** Low-Power BOR Enable bit
1 = Low-Power BOR is enabled when main BOR is disabled
0 = Low-Power BOR is disabled

bit 2 **RETVR:** Retention Voltage Regulator Enable bit
1 = Retention regulator is disabled
0 = Retention regulator is enabled and controlled by the RETEN bit during Sleep

bit 1-0 **BOREN<1:0>:** Brown-out Reset Enable bits
11 = Brown-out Reset is enabled in hardware; SBOREN bit is disabled
10 = Brown-out Reset is enabled only while device is active and disabled in Sleep; SBOREN bit is disabled
01 = Brown-out Reset is controlled with the SBOREN bit setting
00 = Brown-out Reset is disabled in hardware; SBOREN bit is disabled

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REGISTER 26-4: FWDT/AFWDT: WATCHDOG TIMER CONFIGURATION REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
	—	—	—	—	—	—	—	—
23:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
	—	—	—	—	—	—	—	—
15:8	R/P	R/P	R/P	R/P	R/P	R/P	R/P	R/P
	FWDTEN	RCLKSEL<1:0>		RWDTPS<4:0>				
7:0	R/P	R/P	R/P	R/P	R/P	R/P	R/P	R/P
	WINDIS	FWDTWINSZ<1:0>		SWDTPS<4:0>				

Legend:	r = Reserved bit	P = Programmable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-16 **Reserved:** Program as ‘1’

bit 15 **FWDTEN:** Watchdog Timer Enable bit
1 = WDT is enabled
0 = WDT is disabled

bit 14-13 **RCLKSEL<1:0>:** Run Mode Watchdog Timer Clock Source Selection bits
11 = Clock source is the LPRC oscillator (same as for Sleep mode)
10 = Clock source is the FRC oscillator
01 = Reserved
00 = Clock source is the system clock

bit 12-8 **RWDTPS<4:0>:** Run Mode Watchdog Timer Postscale Select bits
From 10100 to 11111 = 1:1048576.
10011 = 1:524288
10010 = 1:262144
10001 = 1:131072
10000 = 1:65536
01111 = 1:32768
01110 = 1:16384
01101 = 1:8192
01100 = 1:4096
01011 = 1:2048
01010 = 1:1024
01001 = 1:512
01000 = 1:256
00111 = 1:128
00110 = 1:64
00101 = 1:32
00100 = 1:16
00011 = 1:8
00010 = 1:4
00001 = 1:2
00000 = 1:1

bit 7 **WINDIS:** Windowed Watchdog Timer Disable bit
1 = Windowed mode is disabled
0 = Windowed mode is enabled

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REGISTER 26-4: FWDT/AFWDT: WATCHDOG TIMER CONFIGURATION REGISTER (CONTINUED)

bit 6-5 **FWDTWINSZ<1:0>:** Watchdog Timer Window Size bits

11 = Watchdog Timer window size is 25%
10 = Watchdog Timer window size is 37.5%
01 = Watchdog Timer window size is 50%
00 = Watchdog Timer window size is 75%

bit 4-0 **SWDTPS<4:0>:** Sleep Mode Watchdog Timer Postscale Select bits

From 10100 to 11111 = 1:1048576.
10011 = 1:524288
10010 = 1:262144
10001 = 1:131072
10000 = 1:65536
01111 = 1:32768
01110 = 1:16384
01101 = 1:8192
01100 = 1:4096
01011 = 1:2048
01010 = 1:1024
01001 = 1:512
01000 = 1:256
00111 = 1:128
00110 = 1:64
00101 = 1:32
00100 = 1:16
00011 = 1:8
00010 = 1:4
00001 = 1:2
00000 = 1:1

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REGISTER 26-5: FOSCSEL/AFOSCSEL: OSCILLATOR SELECTION CONFIGURATION REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
	—	—	—	—	—	—	—	—
23:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
	—	—	—	—	—	—	—	—
15:8	R/P	R/P	r-1	R/P	r-1	R/P	R/P	R/P
	FCKSM<1:0>		—	SOSCSEL	—	OSCIOFNC	POSCMOD<1:0>	
7:0	R/P	R/P	r-1	R/P	r-1	R/P	R/P	R/P
	IESO	SOSCEN	—	PLLSRC	—	FNOSC<2:0>		

Legend:	r = Reserved bit	P = Programmable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Reserved:** Program as '1'

bit 15-14 **FCKSM<1:0>:** Clock Switching and Fail-Safe Clock Monitor Enable bits
11 = Clock switching is enabled; Fail-Safe Clock Monitor is enabled
10 = Clock switching is disabled; Fail-Safe Clock Monitor is enabled
01 = Clock switching is enabled; Fail-Safe Clock Monitor is disabled
00 = Clock switching is disabled; Fail-Safe Clock Monitor is disabled

bit 13 **Reserved:** Program as '1'

bit 12 **SOSCSEL:** Secondary Oscillator (SOSC) External Clock Enable bit
1 = Crystal is used (RA4 and RB4 pins are controlled by the SOSC)
0 = External clock connected to the SOSCO pin is used (RA4 and RB4 pins are controlled by I/O PORTx registers)

bit 11 **Reserved:** Program as '1'

bit 10 **OSCIOFNC:** System Clock on CLKO Pin Enable bit
1 = CLKO/OSC2 pin operates as normal I/O
0 = System clock is connected to the CLKO/OSC2 pin

bit 9-8 **POSCMOD<1:0>:** Primary Oscillator (POSC) Mode Selection bits
11 = Primary Oscillator is disabled
10 = HS Oscillator mode is selected
01 = XT Oscillator mode is selected
00 = External Clock (EC) mode is selected

bit 7 **IESO:** Two-Speed Start-up Enable bit
1 = Two-Speed Start-up is enabled
0 = Two-Speed Start-up is disabled

bit 6 **SOSCEN:** Secondary Oscillator (SOSC) Enable bit
1 = Secondary Oscillator enable
0 = Secondary Oscillator disable

bit 5 **Reserved:** Program as '1'

bit 4 **PLLSRC:** System PLL Input Clock Selection bit
1 = FRC oscillator is selected as the PLL reference input on a device Reset
0 = Primary Oscillator (POSC) is selected as the PLL reference input on a device Reset

bit 3 **Reserved:** Program as '1'

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REGISTER 26-5: FOSCSEL/AFOSCSEL: OSCILLATOR SELECTION CONFIGURATION REGISTER (CONTINUED)

bit 2-0 **FNOSC<2:0>:** Oscillator Selection bits
110 and 111 = Reserved (selects Fast RC (FRC) Oscillator with Divide-by-N)
101 = Low-Power RC Oscillator (LPRC)
100 = Secondary Oscillator (SOSC)
011 = Reserved
010 = Primary Oscillator (XT, HS, EC)
001 = Primary or FRC Oscillator with PLL
000 = Fast RC Oscillator (FRC) with Divide-by-N

REGISTER 26-6: FSEC/AFSEC: CODE-PROTECT CONFIGURATION REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/P	r-1	r-1	r-1	r-1	r-1	r-1	r-1
	CP	—	—	—	—	—	—	—
23:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
	—	—	—	—	—	—	—	—
15:8	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
	—	—	—	—	—	—	—	—
7:0	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
	—	—	—	—	—	—	—	—

Legend:	r = Reserved bit	P = Programmable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31 **CP:** Code Protection Enable bit
1 = Code protection is disabled
0 = Code protection is enabled

bit 30-0 **Reserved:** Program as ‘1’

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TABLE 26-5: RAM CONFIGURATION, DEVICE ID AND SYSTEM LOCK REGISTERS MAP

Virtual Address (BF80_#)	Register Name	Bit Range	Bits 31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets(1)
3640	CFGCON	31:16	—	—	—	—	BMXERRDIS	—	BMXARB<1:0>		EXECADDR<7:0>								0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	JTAGEN	—	r	r	0003
3660	DEVID	31:16	VER<3:0>				DEVID<27:16>												xxxx
		15:0	DEVID<15:0>																xxxx
3670	SYSKEY	31:16	SYSKEY<31:16>																0000
		15:0	SYSKEY<15:0>																0001

Legend: x = unknown value on Reset; r = reserved bit; — = unimplemented, read as ‘0’. Reset values are shown in hexadecimal.

Note 1: Reset values are dependent on the device variant.

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REGISTER 26-7: CFGCON: CONFIGURATION CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	R/W-0	U-0	R/W-0	R/W-0
	—	—	—	—	BMXERRDIS	—	BMXARB<1:0>	
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	EXECADDR<7:0>							
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	R/W-P	U-0	r-1	r-1
	—	—	—	—	JTAGEN	—	—	—

Legend:	r = Reserved bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-28 **Unimplemented:** Read as '0'

bit 27 **BMXERRDIS:** Bus Matrix (BMX) Exception Error Disable bit
1 = Disables BMX error exception generation[1]
0 = Enables BMX error exception generation

bit 26 **Unimplemented:** Read as '0'

bit 25-24 **BMXARB<1:0>:** Bus Matrix Arbitration Mode Select bits
11 = Reserved
10 = Mode 2 – Round Robin
01 = Mode 1 – Fixed with CPU as the lowest priority
00 = Mode 0 – Fixed with CPU as the highest priority

bit 23-16 **EXECADDR<7:0>:** RAM Program Space Start Address bits
11111111 = RAM program space starts at the 255-Kbyte boundary (from 0xA003FC00)
•
•
•
00000010 = RAM program space starts at 2-Kbyte boundary (from 0xA0000800)
00000001 = RAM program space starts at 1-Kbyte boundary (from 0xA0000400)
00000000 = All data RAM is allocated to program space (from 0xA0000000)

bit 15-4 **Unimplemented:** Read as '0'

bit 3 **JTAGEN:** JTAG Enable bit
1 = Enables 4-wire JTAG
0 = Disables 4-wire JTAG

bit 2 **Unimplemented:** Read as '0'

bit 1-0 **Reserved:** Maintain as '1'

Note 1: An exception is not generated when an unimplemented address is accessed. The returned value on a read operation of unimplemented memory is 0x00000000.

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REGISTER 26-8: DEVID: DEVICE ID REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
	VER<3:0>[1]				ID<27:24>[1]			
23:16	R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
	ID<23:16>[1]							
15:8	R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
	ID<15:8>[1]							
7:0	R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
	ID<7:0>[1]							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-28 **VER<3:0>:** Revision Identifier bits[1]

bit 27-0 **DEVID<27:0>:** Device ID bits[1]

Note 1: Reset values are dependent on the device variant.

REGISTER 26-9: SYSKEY: SYSTEM UNLOCK REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0
	SYSKEY<31:24>							
23:16	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0
	SYSKEY<23:16>							
15:8	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0
	SYSKEY<15:8>							
7:0	W-0	W-0	W-0	W-0	W-0	W-0	W-0	R/W-1
	SYSKEY<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-0 **SYSKEY<31:0>:** Unlock and Lock Key bits

A write of 0xAA996655, followed by a write of 0x556699AA to SYSKEY, is required to unlock select system registers. Refer to Example 26-1.

Bit 0 Indicates System Lock Status:
`1` = The system is unlocked
`0` = The system is locked

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TABLE 26-6: BAND GAP REGISTER MAP

Virtual Address (BF80_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
2300	ANCFG[1]	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	VBGADC	VBGCMP	—	0000

Legend: — = unimplemented, read as ‘0’. Reset values are shown in hexadecimal.

Note 1: This register has corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively.

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REGISTER 26-10: ANCFG: BAND GAP CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	R/W-0, HS, HC	R/W-0, HS, HC	U-0
	—	—	—	—	—	VBGADC	VBGCMP	—

Legend:	HC = Hardware Clearable bit	HS = Hardware Settable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-3 **Unimplemented:** Read as ‘0’

bit 2 **VBGADC:** ADC Band Gap Enable bit
1 = ADC band gap is enabled
0 = ADC band gap is disabled

bit 1 **VBGCMP:** Comparator Band Gap Enable bit
1 = Comparator band gap is enabled
0 = Comparator band gap is disabled

bit 0 **Unimplemented:** Read as ‘0’

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TABLE 26-7: UNIQUE DEVICE IDENTIFIER (UDID) REGISTER MAP

Virtual Address (BF84_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
1840	UDID1	31:16	UDID Word 1<31:0>																xxxx
		15:0																	xxxx
1844	UDID2	31:16	UDID Word 2<31:0>																xxxx
		15:0																	xxxx
1848	UDID3	31:16	UDID Word 3<31:0>																xxxx
		15:0																	xxxx
184C	UDID4	31:16	UDID Word 4<31:0>																xxxx
		15:0																	xxxx
1850	UDID5	31:16	UDID Word 5<31:0>																xxxx
		15:0																	xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 26-8: RESERVED REGISTERS MAP

Virtual Address (BF80_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
2900	RESERVED1	31:16	Reserved Register 1<31:0>																0000
		15:0																	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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NOTES:

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27.0 INSTRUCTION SET

The PIC32MM0256GPM064 family instruction set complies with the MIPS® Release 3 instruction set architecture. Only microMIPS32™ instructions are supported. The PIC32MM0256GPM064 family does not have the following features:

- Core extend instructions
- Coprocessor 1 instructions
- Coprocessor 2 instructions

Note:	Refer to the *"MIPS® Architecture for Programmers Volume II-B: The microMIPS32™ Instruction Set"* at www.imgtec.com for more information.

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NOTES:

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28.0 DEVELOPMENT SUPPORT

The PIC® microcontrollers (MCU) and dsPIC® digital signal controllers (DSC) are supported with a full range of software and hardware development tools:

- Integrated Development Environment
  - MPLAB® X IDE Software
- Compilers/Assemblers/Linkers
  - MPLAB XC Compiler
  - MPASM™ Assembler
  - MPLINK™ Object Linker/ MPLIB™ Object Librarian
  - MPLAB Assembler/Linker/Librarian for Various Device Families
- Simulators
  - MPLAB X SIM Software Simulator
- Emulators
  - MPLAB REAL ICE™ In-Circuit Emulator
- In-Circuit Debuggers/Programmers
  - MPLAB ICD 3
  - PICkit™ 3
- Device Programmers
  - MPLAB PM3 Device Programmer
- Low-Cost Demonstration/Development Boards, Evaluation Kits and Starter Kits
- Third-party development tools

28.1 MPLAB X Integrated Development Environment Software

The MPLAB X IDE is a single, unified graphical user interface for Microchip and third-party software, and hardware development tool that runs on Windows®, Linux and Mac OS® X. Based on the NetBeans IDE, MPLAB X IDE is an entirely new IDE with a host of free software components and plug-ins for high-performance application development and debugging. Moving between tools and upgrading from software simulators to hardware debugging and programming tools is simple with the seamless user interface.

With complete project management, visual call graphs, a configurable watch window and a feature-rich editor that includes code completion and context menus, MPLAB X IDE is flexible and friendly enough for new users. With the ability to support multiple tools on multiple projects with simultaneous debugging, MPLAB X IDE is also suitable for the needs of experienced users.

Feature-Rich Editor:

- Color syntax highlighting
- Smart code completion makes suggestions and provides hints as you type
- Automatic code formatting based on user-defined rules
- Live parsing

User-Friendly, Customizable Interface:

- Fully customizable interface: toolbars, toolbar buttons, windows, window placement, etc.
- Call graph window

Project-Based Workspaces:

- Multiple projects
- Multiple tools
- Multiple configurations
- Simultaneous debugging sessions

File History and Bug Tracking:

- Local file history feature
- Built-in support for Bugzilla issue tracker

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28.2 MPLAB XC Compilers

The MPLAB XC Compilers are complete ANSI C compilers for all of Microchip's 8, 16 and 32-bit MCU and DSC devices. These compilers provide powerful integration capabilities, superior code optimization and ease of use. MPLAB XC Compilers run on Windows, Linux or MAC OS X.

For easy source level debugging, the compilers provide debug information that is optimized to the MPLAB X IDE.

The free MPLAB XC Compiler editions support all devices and commands, with no time or memory restrictions, and offer sufficient code optimization for most applications.

MPLAB XC Compilers include an assembler, linker and utilities. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. MPLAB XC Compiler uses the assembler to produce its object file. Notable features of the assembler include:

- Support for the entire device instruction set
- Support for fixed-point and floating-point data
- Command-line interface
- Rich directive set
- Flexible macro language
- MPLAB X IDE compatibility

28.3 MPASM Assembler

The MPASM Assembler is a full-featured, universal macro assembler for PIC10/12/16/18 MCUs.

The MPASM Assembler generates relocatable object files for the MPLINK Object Linker, Intel® standard HEX files, MAP files to detail memory usage and symbol reference, absolute LST files that contain source lines and generated machine code, and COFF files for debugging.

The MPASM Assembler features include:

- Integration into MPLAB X IDE projects
- User-defined macros to streamline assembly code
- Conditional assembly for multipurpose source files
- Directives that allow complete control over the assembly process

28.4 MPLINK Object Linker/ MPLIB Object Librarian

The MPLINK Object Linker combines relocatable objects created by the MPASM Assembler. It can link relocatable objects from precompiled libraries, using directives from a linker script.

The MPLIB Object Librarian manages the creation and modification of library files of precompiled code. When a routine from a library is called from a source file, only the modules that contain that routine will be linked in with the application. This allows large libraries to be used efficiently in many different applications.

The object linker/library features include:

- Efficient linking of single libraries instead of many smaller files
- Enhanced code maintainability by grouping related modules together
- Flexible creation of libraries with easy module listing, replacement, deletion and extraction

28.5 MPLAB Assembler, Linker and Librarian for Various Device Families

MPLAB Assembler produces relocatable machine code from symbolic assembly language for PIC24, PIC32 and dsPIC DSC devices. MPLAB XC Compiler uses the assembler to produce its object file. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. Notable features of the assembler include:

- Support for the entire device instruction set
- Support for fixed-point and floating-point data
- Command-line interface
- Rich directive set
- Flexible macro language
- MPLAB X IDE compatibility

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28.6 MPLAB X SIM Software Simulator

The MPLAB X SIM Software Simulator allows code development in a PC-hosted environment by simulating the PIC MCUs and dsPIC DSCs on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a comprehensive stimulus controller. Registers can be logged to files for further run-time analysis. The trace buffer and logic analyzer display extend the power of the simulator to record and track program execution, actions on I/O, most peripherals and internal registers.

The MPLAB X SIM Software Simulator fully supports symbolic debugging using the MPLAB XC Compilers, and the MPASM and MPLAB Assemblers. The software simulator offers the flexibility to develop and debug code outside of the hardware laboratory environment, making it an excellent, economical software development tool.

28.7 MPLAB REAL ICE In-Circuit Emulator System

The MPLAB REAL ICE In-Circuit Emulator System is Microchip's next generation high-speed emulator for Microchip Flash DSC and MCU devices. It debugs and programs all 8, 16 and 32-bit MCU, and DSC devices with the easy-to-use, powerful graphical user interface of the MPLAB X IDE.

The emulator is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with either a connector compatible with in-circuit debugger systems (RJ-11) or with the new high-speed, noise tolerant, Low-Voltage Differential Signal (LVDS) interconnection (CAT5).

The emulator is field upgradable through future firmware downloads in MPLAB X IDE. MPLAB REAL ICE offers significant advantages over competitive emulators including full-speed emulation, run-time variable watches, trace analysis, complex breakpoints, logic probes, a ruggedized probe interface and long (up to three meters) interconnection cables.

28.8 MPLAB ICD 3 In-Circuit Debugger System

The MPLAB ICD 3 In-Circuit Debugger System is Microchip's most cost-effective, high-speed hardware debugger/programmer for Microchip Flash DSC and MCU devices. It debugs and programs PIC Flash microcontrollers and dsPIC DSCs with the powerful, yet easy-to-use graphical user interface of the MPLAB IDE.

The MPLAB ICD 3 In-Circuit Debugger probe is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with a connector compatible with the MPLAB ICD 2 or MPLAB REAL ICE systems (RJ-11). MPLAB ICD 3 supports all MPLAB ICD 2 headers.

28.9 PICkit 3 In-Circuit Debugger/ Programmer

The MPLAB PICkit 3 allows debugging and programming of PIC and dsPIC Flash microcontrollers at a most affordable price point using the powerful graphical user interface of the MPLAB IDE. The MPLAB PICkit 3 is connected to the design engineer's PC using a full-speed USB interface and can be connected to the target via a Microchip debug (RJ-11) connector (compatible with MPLAB ICD 3 and MPLAB REAL ICE). The connector uses two device I/O pins and the Reset line to implement in-circuit debugging and In-Circuit Serial Programming™ (ICSP™).

28.10 MPLAB PM3 Device Programmer

The MPLAB PM3 Device Programmer is a universal, CE compliant device programmer with programmable voltage verification at VDDMIN and VDDMAX for maximum reliability. It features a large LCD display (128 x 64) for menus and error messages, and a modular, detachable socket assembly to support various package types. The ICSP cable assembly is included as a standard item. In Stand-Alone mode, the MPLAB PM3 Device Programmer can read, verify and program PIC devices without a PC connection. It can also set code protection in this mode. The MPLAB PM3 connects to the host PC via an RS-232 or USB cable. The MPLAB PM3 has high-speed communications and optimized algorithms for quick programming of large memory devices, and incorporates an MMC card for file storage and data applications.

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28.11 Demonstration/Development Boards, Evaluation Kits and Starter Kits

A wide variety of demonstration, development and evaluation boards for various PIC MCUs and dsPIC DSCs allows quick application development on fully functional systems. Most boards include prototyping areas for adding custom circuitry and provide application firmware and source code for examination and modification.

The boards support a variety of features, including LEDs, temperature sensors, switches, speakers, RS-232 interfaces, LCD displays, potentiometers and additional EEPROM memory.

The demonstration and development boards can be used in teaching environments, for prototyping custom circuits and for learning about various microcontroller applications.

In addition to the PICDEM™ and dsPICDEM™ demonstration/development board series of circuits, Microchip has a line of evaluation kits and demonstration software for analog filter design, KEELOQ® security ICs, CAN, IrDA®, PowerSmart battery management, SEEVAL® evaluation system, Sigma-Delta ADC, flow rate sensing, plus many more.

Also available are starter kits that contain everything needed to experience the specified device. This usually includes a single application and debug capability, all on one board.

Check the Microchip web page (www.microchip.com) for the complete list of demonstration, development and evaluation kits.

28.12 Third-Party Development Tools

Microchip also offers a great collection of tools from third-party vendors. These tools are carefully selected to offer good value and unique functionality.

- Device Programmers and Gang Programmers from companies, such as SoftLog and CCS
- Software Tools from companies, such as Gimpel and Trace Systems
- Protocol Analyzers from companies, such as Saleae and Total Phase
- Demonstration Boards from companies, such as MikroElektronika, Digilent® and Olimex
- Embedded Ethernet Solutions from companies, such as EZ Web Lynx, WIZnet and IPLogika®

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29.0 ELECTRICAL CHARACTERISTICS

This section provides an overview of the PIC32MM0256GPM064 family electrical characteristics. Additional information will be provided in future revisions of this document as it becomes available.

Absolute maximum ratings for the PIC32MM0256GPM064 family are listed below. Exposure to these maximum rating conditions for extended periods may affect device reliability. Functional operation of the device at these, or any other conditions above the parameters indicated in the operation listings of this specification, is not implied.

Absolute Maximum Ratings[†]

Ambient temperature under bias .... -40°C to +105°C
Storage temperature .... -65°C to +150°C
Voltage on V_{DD} with respect to V_{SS} .... -0.3V to +4.0V
Voltage on any general purpose digital or analog pin (not 5.5V tolerant) with respect to V_{SS} .... -0.3V to (V_{DD} + 0.3V)
Voltage on any general purpose digital or analog pin (5.5V tolerant) with respect to V_{SS}:

- When V_{DD} = 0V: .... -0.3V to +4.0V
- When $V_{DD} \geq$ 2.0V: .... -0.3V to +6.0V

Voltage on AV_{DD} with respect to V_{DD} .... (V_{DD} – 0.3V) to (lesser of: 4.0V or (V_{DD} + 0.3V))
Voltage on AV_{SS} with respect to V_{SS} .... -0.3V to +0.3V
Maximum current out of V_{SS} pin .... 100 mA
Maximum current into V_{DD} pin[(1)] .... 300 mA
Maximum output current sunk by I/O pin .... 11 mA
Maximum output current sourced by I/O pin .... 16 mA
Maximum output current sunk by I/O pin with increased current drive strength (RA3, RA8, RA10, RB8, RB9, RB13, RB15, RC9, RC13 and RD0) .... 17 mA
Maximum output current sourced by I/O pin with increased current drive strength (RA3, RA8, RA10, RB8, RB9, RB13, RB15, RC9, RC13 and RD0) .... 24 mA
Maximum current sunk by all ports .... 300 mA
Maximum current sourced by all ports[(1)] .... 300 mA

Note 1: Maximum allowable current is a function of device maximum power dissipation (see Table 29-1).

† **NOTICE:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

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29.1 DC Characteristics

FIGURE 29-1: PIC32MM0256GPM064 FAMILY VOLTAGE-FREQUENCY GRAPH

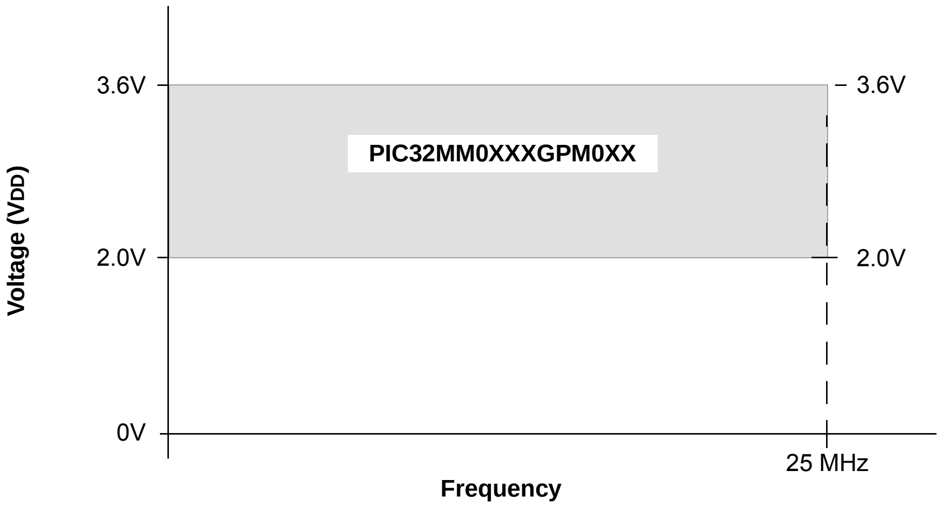

TABLE 29-1: THERMAL OPERATING CONDITIONS

Rating	Symbol	Min	Typ	Max	Unit
PIC32MM0XXXGPM0XX:					
Operating Junction Temperature Range	T_J	-40	—	+125	°C
Operating Ambient Temperature Range	T_A	-40	—	+85	°C
Power Dissipation: Internal Chip Power Dissipation: $P_{INT} = V_{DD} \times (I_{DD} - \Sigma I_{OH})$ I/O Pin Power Dissipation: $P_{I/O} = \Sigma (\{V_{DD} - V_{OH}\} \times I_{OH}) + \Sigma (V_{OL} \times I_{OL})$	P_D	$P_{INT} + P_{I/O}$			W
Maximum Allowed Power Dissipation	P_{DMAX}	$(T_J - T_A)/\theta_{JA}$			W

TABLE 29-2: PACKAGE THERMAL RESISTANCE[(1)]

Package	Symbol	Typ	Unit
28-Pin SSOP	θ_{JA}	71.0	°C/W
28-Pin QFN	θ_{JA}	69.7	°C/W
28-Pin UQFN	θ_{JA}	26	°C/W
36-Pin VQFN	θ_{JA}	30.0	°C/W
40-Pin UQFN	θ_{JA}	41	°C/W
48-Pin UQFN	θ_{JA}	24.5	°C/W
48-Pin TQFP	θ_{JA}	51	°C/W
64-Pin QFN	θ_{JA}	29.4	°C/W
64-Pin TQFP	θ_{JA}	44.5	°C/W

Note 1: Junction to ambient thermal resistance; Theta-JA (θ_{JA}) numbers are achieved by package simulations.

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TABLE 29-3: OPERATING VOLTAGE SPECIFICATIONS

DC CHARACTERISTICS			Operating Conditions: 2.0V < VDD < 3.6V, -40°C < TA < +85°C (unless otherwise stated)				
Param No.	Symbol	Characteristic	Min	Typ	Max	Units	Conditions
DC10	VDD	**Supply Voltage**	2.0	—	3.6	V	
DC16	VPOR[1]	**VDD Start Voltage** to Ensure Internal Power-on Reset Signal	VSS	—	100	mV	
DC17A	SVDD[1]	**Recommended VDD Rise Rate** to Ensure Internal Power-on Reset Signal	0.05	—	—	V/ms	0-3.3V in 66 ms, 0-2.0V in 40 ms
DC17B	VBOR	**Brown-out Reset Voltage** on VDD Transition, High-to-Low	2.0	—	2.083	V	

Note 1: If the VPOR or SVDD parameters are not met, or the application experiences slow power-down VDD ramp rates, it is recommended to enable and use BOR.

TABLE 29-4: OPERATING CURRENT (IDD)[2]

DC CHARACTERISTICS						
Parameter No.	Typical[1]	Max	Units	Operating Temperature	VDD	Conditions
DC19	.72	.96	mA	-40°C to +85°C	2.0V	FSYS = 1 MHz
	—	.96	mA	-40°C to +85°C	3.3V	
DC23	2.5	3.7	mA	-40°C to +85°C	2.0V	FSYS = 8 MHz
	2.5	3.7	mA	-40°C to +85°C	3.3V	
DC24	7.9	10.2	mA	-40°C to +85°C	2.0V	FSYS = 25 MHz
	7.9	10.2	mA	-40°C to +85°C	3.3V	
DC25	.4	.8	μA	-40°C to +85°C	2.0V	LPRC, FSYS = 32 kHz
	.4	.8	μA	-40°C to +85°C	3.3V	

Note 1: Typical parameters are for design guidance only and are not tested.

2: IDD is primarily a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption. The test conditions for all IDD measurements are as follows:

- Oscillator is configured in EC mode with PLL, OSC1 is driven with external square wave from rail-to-rail (EC Clock Overshoot/Undershoot < 250 mV required)
- CLKO is configured as an I/O input pin in the Configuration Word
- All I/O pins are configured as outputs and driving low
- $\overline{\text{MCLR}}$ = VDD; WDT and FSCM are disabled
- CPU, SRAM, program memory and data memory are operational
- No peripheral modules are operating or being clocked (defined PMDx bits are all ones)
- CPU executing:

```
while(1)
 {
 NOP();
 }
```

3: JTAG is disabled

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TABLE 29-5: IDLE CURRENT (I_{IDLE})(2)

DC CHARACTERISTICS						
Parameter No.	Typical(1)	Max	Units	Operating Temperature	VDD	Conditions
DC40	.69	.8	µA	-40°C to +85°C	2.0V	FSYS = 1 MHz
	.69	.8	µA	-40°C to +85°C	3.3V	
DC41	.98	1.7	mA	-40°C to +85°C	2.0V	FSYS = 8 MHz
	.98	1.7	mA	-40°C to +85°C	3.3V	
DC42	2.9	3.7	mA	-40°C to +85°C	2.0V	FSYS = 25 MHz
	2.9	3.7	mA	-40°C to +85°C	3.3V	
DC44	.36	.7	µA	-40°C to +85°C	2.0V	FSYS = 32 kHz
	.36	.7	µA	-40°C to +85°C	3.3V	

Note 1: Parameters are for design guidance only and are not tested.

2: Base IIDLE current is measured with the core in Idle, the clock on and all modules turned off. OSC1 driven with external square wave from rail-to-rail (EC Clock Overshoot/Undershoot < 250 mV required). Peripheral Module Disable SFR registers are zeroed. All I/O pins are configured as inputs and pulled to VSS.

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TABLE 29-6: POWER-DOWN CURRENT (I_{PD})[2]

DC CHARACTERISTICS						
Parameter No.	**Typical[1]**	**Max**	**Units**	**Operating Temperature**	**V_{DD}**	**Conditions**
DC60	130	255	µA	-40°C	2.0V	Sleep with active main Voltage Regulator (VREGS (PWRCON<0>) bit = 1, RETEN (PWRCON<1>) bit = 0)
	130	255	µA	+25°C		
	145	265	µA	+85°C		
	130	255	µA	-40°C	3.3V	
	130	265	µA	+25°C		
	145	275	µA	+85°C		
DC61	3.5	12	µA	-40°C	2.0V	Sleep with main Voltage Regulator in Standby mode (VREGS (PWRCON<0>) bit = 0, RETEN (PWRCON<1>) bit = 0)
	4.5	22	µA	+25°C		
	15	35	µA	+85°C		
	4	17	µA	-40°C	3.3V	
	5	30	µA	+25°C		
	18	38	µA	+85°C		
DC62	4.3	—	µA	-40°C	2.0V	Sleep with enabled Retention Voltage Regulator (RETEN (PWRCON<1>) bit = 1, RETVR (FPOR<2>) bit = 0)
	5	—	µA	+25°C		
	10	—	µA	+85°C		
	5	—	µA	-40°C	3.3V	
	5.6	—	µA	+25°C		
	12	—	µA	+85°C		
DC63	.3	—	µA	-40°C	2.0V	Sleep with enabled Retention Voltage Regulator (VREGS (PWRCON<0>) bit = 0, RETEN (PWRCON<1>) bit = 1, RETVR (FPOR<2>) bit = 0)
	.4	—	µA	+25°C		
	3.5	—	µA	+85°C		
	0.35	—	µA	-40°C	3.3V	
	0.45	—	µA	+25°C		
	4.5	—	µA	+85°C		

Note 1: Parameters are for design guidance only and are not tested.

2: Base IPD is measured with:

- Oscillator is configured in FRC mode without PLL (FNOSC<2:0> (FOSCSEL<2:0>) = 000)
- OSC1 pin is driven with external square wave from rail-to-rail (EC Clock Overshoot/Undershoot < 250 mV required)
- OSC2 is configured as an I/O in Configuration Words (OSCIOFNC (FOSCSEL<10>) = 1)
- FSCM is disabled (FCKSM<1:0> (FOSCSEL<15:14>) = 00)
- Secondary Oscillator circuits are disabled (SOSCEN (FOSCSEL<6>) = 0 and SOSCSEL (FOSCSEL<12>) = 0)
- Main and low-power BOR circuits are disabled (BOREN<1:0> (FPOR<1:0>) = 00 and LPBOREN (FPOR<3>) = 0)
- Watchdog Timer is disabled (FWDTEN (FWDT<15>) = 0)
- All I/O pins (excepting OSC1) are configured as outputs and driven low
- No peripheral modules are operating or being clocked (defined PMDx bits are all ones)

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TABLE 29-7: Δ CURRENT[2]

DC CHARACTERISTICS						
Parameter No.	**Typical[1]**	**Max**	**Units**	**Operating Temperature**	**VDD**	**Conditions**
Incremental Current Brown-out Reset (ΔBOR)						
DC71	3	—	μA	-40°C to +85°C	2.0V	ΔBOR
	4	—	μA	-40°C to +85°C	3.3V	
Incremental Current Watchdog Timer (ΔWDT)						
DC72	0.22	—	μA	-40°C to +85°C	2.0V	ΔWDT (with LPRC)
	0.3	—	μA	-40°C to +85°C	3.3V	
Incremental Current High/Low-Voltage Detect (ΔHLVD)						
DC73	2.1	—	μA	-40°C to +85°C	2.0V	ΔHLVD
	2.4	—	μA	-40°C to +85°C	3.3V	
Incremental Current Real-Time Clock and Calendar (ΔRTCC)						
DC74	1.1	—	μA	-40°C to +85°C	2.0V	ΔRTCC (with SOSC)
	1.2	—	μA	-40°C to +85°C	3.3V	
DC75	0.35	—	μA	-40°C to +85°C	2.0V	ΔRTCC (with LPRC)
	0.45	—	μA	-40°C to +85°C	3.3V	
Incremental Current ADC (ΔADC)						
DC76	450	—	μA	-40°C to +85°C	2.0V	ΔADC (with Timer1 and ADC internal oscillator enabled)
	475	—	μA	-40°C to +85°C	3.3V	
Incremental Current Fast RC Oscillator (ΔFRC)						
DC78	—	—	μA	-40°C to +85°C	2.0V	ΔFRC
	—	—	μA	-40°C to +85°C	3.3V	
Incremental Current PLL (ΔPLL)						
DC79	1200	—	μA	-40°C to +85°C	2.0V	ΔPLL (24 MHz)
	1340	—	μA	-40°C to +85°C	3.3V	
DC79a	1460	—	μA	-40°C to +85°C	2.0V	ΔPLL (48 MHz)
	1600	—	μA	-40°C to +85°C	3.3V	
Incremental Current Voltage Reference CVREF (ΔVREF)						
DC80	30	—	μA	-40°C to +85°C	2.0V	ΔVREF
	35	—	μA	-40°C to +85°C	3.3V	

Note 1: Data in the "Typical" column is for design guidance only and is not tested.

2: The Δ current is the additional current consumed when the module is enabled. This current should be added to the base IPD current.

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TABLE 29-8: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C				
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
	VIL	**Input Low Voltage(3)**					
DI10		I/O Pins with ST Buffer	VSS	—	0.2 VDD	V	
DI15		$\overline{\text{MCLR}}$	VSS	—	0.2 VDD	V	
DI16		OSC1 (XT mode)	VSS	—	0.2 VDD	V	
DI17		OSC1 (HS mode)	VSS	—	0.2 VDD	V	
	VIH	**Input High Voltage(3)**					
DI20		I/O Pins with ST Buffer: Without 5V Tolerance With 5V Tolerance	 0.8 VDD 0.8 VDD	 — —	 VDD 5.5	 V V	
DI25		$\overline{\text{MCLR}}$	0.8 VDD	—	VDD	V	
DI26		OSCI (XT mode)	0.7 VDD	—	VDD	V	
DI27		OSCI (HS mode)	0.7 VDD	—	VDD	V	
DI30	ICNPU	**CNPUx Pull-up Current**	150	350	450	µA	VDD = 3.3V, VPIN = VSS
DI30A	ICNPD	**CNPDx Pull-Down Current**	230	300	500	µA	VDD = 3.3V, VPIN = VDD
	IIL	**Input Leakage Current(2)**					
DI50		I/O Pins – 5V Tolerant	—	—	1	µA	VSS ≤ VPIN ≤ VDD, pin at high-impedance
DI51		I/O Pins – Not 5V Tolerant	—	—	1	µA	VSS ≤ VPIN ≤ VDD, pin at high-impedance
DI55		$\overline{\text{MCLR}}$	—	—	1	µA	VSS ≤ VPIN ≤ VDD
DI56		OSC1/CLKI	—	—	1	µA	VSS ≤ VPIN ≤ VDD, XT and HS modes

Note 1: Data in the “Typ” column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: Negative current is defined as current sourced by the pin.

3: Refer to Table 1-1 for I/O pin buffer types.

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TABLE 29-9: DC CHARACTERISTICS: I/O PIN INPUT INJECTION CURRENT SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C				
Param No.	Symbol	Characteristics	Min.	Typical[1]	Max.	Units	Conditions
DI60a	I_{ICL}	**Input Low Injection Current**	0	—	-5[2,5]	mA	This parameter applies to all pins. Maximum I_{ICH} current for this exception is 0 mA.
DI60b	I_{ICH}	**Input High Injection Current**	0	—	+5[3,4,5]	mA	This parameter applies to all pins, with the exception of all 5V tolerant pins and SOSCI. Maximum I_{ICH} current for these exceptions is 0 mA.
DI60c	$\sum I_{ICT}$	**Total Input Injection Current (sum of all I/O and control pins)**	-20[6]	—	+20[6]	mA	Absolute instantaneous sum of all ± input injection currents from all I/O pins: $(\mid I_{ICL} + \mid I_{ICH} \mid) \leq \sum I_{ICT}$

Note 1: Data in the “Typical” column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: V_{IL} Source < (V_{SS} – 0.3). Characterized but not tested.

3: V_{IH} Source > (V_{DD} + 0.3) for non-5V tolerant pins only.

4: Digital 5V tolerant pins do not have an internal high side diode to V_{DD}, and therefore, cannot tolerate any “positive” input injection current.

5: Injection currents > | 0 | can affect the ADC results by approximately 4 to 6 counts (i.e., V_{IH} Source > (V_{DD} + 0.3) or V_{IL} Source < (V_{SS} – 0.3)).

6: Any number and/or combination of I/O pins, not excluded under I_{ICL} or I_{ICH} conditions, are permitted provided the “absolute instantaneous” sum of the input injection currents from all pins do not exceed the specified limit. If **Note 2**, I_{ICL} = (((V_{SS} – 0.3) – V_{IL} Source)/R_S). If **Note 3**, I_{ICH} = (((I_{ICH} Source – (V_{DD} + 0.3))/R_S). R_S = Resistance between input source voltage and device pin. If (V_{SS} – 0.3) ≤ V_{SOURCE} ≤ (V_{DD} + 0.3), Injection Current = 0.

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TABLE 29-10: DC CHARACTERISTICS: I/O PIN OUTPUT SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C				
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
	VOL	**Output Low Voltage**					
DO10		I/O Ports	—	—	.4	V	IOL = 6.6 mA, VDD = 3.6V
			—	—	.21	V	IOL = 5.0 mA, VDD = 2V
DO16		OSC2/CLKO	—	—	.16	V	IOL = 6.6 mA, VDD = 3.6V
			—	—	.12	V	IOL = 5.0 mA, VDD = 2V
	VOH	**Output High Voltage**					
DO20		I/O Ports	3.25	—	—	V	IOH = -6.0 mA, VDD = 3.6V
			1.4	—	—	V	IOH = -3.0 mA, VDD = 2V
DO26		OSC2/CLKO	3.3	—	—	V	IOH = -6.0 mA, VDD = 3.6V
			1.55	—	—	V	IOH = -1.0 mA, VDD = 2V

Note 1: Data in the “Typ” column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

TABLE 29-11: DC CHARACTERISTICS: PROGRAM MEMORY

DC CHARACTERISTICS			Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C				
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
		Program Flash Memory					
D130	EP	Cell Endurance	10000	20000	—	E/W	
D131	VPR	VDD for Read	2.0	—	3.6	V	
D132B		VDD for Self-Timed Write	2.0	—	3.6	V	
D133A	TIW	Self-Timed Double-Word Write Cycle Time	61.4	62.5	63.6	µs	8 bytes, data is not all ‘1’s
		Self-Timed Row Write Cycle Time	1.41	1.44	1.47	ms	512 bytes, data is not all ‘1’s; SYSCLK > 2 MHz
D133B	TIE	Self-Timed Page Erase Time	4.18	4.26	4.33	ms	2048 bytes
D134	TRETD	Characteristic Retention	20	—	—	Year	If no other specifications are violated
D136	TCE	Self-Timed Chip Erase Time	16.6	16.9	17.3	ms	

Note 1: Data in the “Typ” column is at 3.3V, +25°C unless otherwise stated.

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TABLE 29-12: INTERNAL VOLTAGE REGULATOR SPECIFICATIONS

Operating Conditions: -40°C < T_A < +85°C (unless otherwise stated)							
Param No.	**Symbol**	**Characteristics**	**Min**	**Typ**	**Max**	**Units**	**Comments**
DVR10	V_{BG}	Internal Band Gap Reference	—	1.2	—	V	
DVR20	V_{RGOUT}	Regulator Output Voltage	—	1.8	—	V	V_{DD} > 1.9V
DVR21	C_{EFC}	External Filter Capacitor Value	4.7	10	—	µF	Series Resistance < 3Ω recommended; < 5Ω required
DVR30	V_{LVR}	Low-Voltage Regulator Output Voltage	0.9	—	1.2	V	RETEN = 1, RETVR (FPOR<2>) = 0

TABLE 29-13: HIGH/LOW-VOLTAGE DETECT CHARACTERISTICS

Operating Conditions: -40°C < T_A < +85°C (unless otherwise stated)								
Param No.	**Symbol**	**Characteristic**		**Min**	**Typ**	**Max**	**Units**	**Conditions**
DC18	V_{HLVD}	HLVD Voltage on V_{DD} Transition	HLVDL<3:0> = 0101	3.25	—	3.63	V	
			HLVDL<3:0> = 0110	2.95	—	3.30	V	
			HLVDL<3:0> = 0111	2.75	—	3.09	V	
			HLVDL<3:0> = 1000	2.65	—	2.98	V	
			HLVDL<3:0> = 1001	2.45	—	2.80	V	
			HLVDL<3:0> = 1010	2.35	—	2.69	V	
			HLVDL<3:0> = 1011	2.25	—	2.55	V	
			HLVDL<3:0> = 1100	2.15	—	2.44	V	
			HLVDL<3:0> = 1101	2.08	—	2.33	V	
			HLVDL<3:0> = 1110	2.00	—	2.22	V	
DC101	V_{THL}	HLVD Voltage on LVDIN Pin Transition	HLVDL<3:0> = 1111	—	1.2	—	V	

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TABLE 29-14: COMPARATOR DC SPECIFICATIONS

Operating Conditions: 2.0V < VDD < 3.6V, -40°C < TA < +85°C (unless otherwise stated)							
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ**	**Max**	**Units**	**Comments**
D300	VIOFF	Input Offset Voltage	-20	—	+20	mV	(Note 1)
D301	VICM	Input Common-Mode Voltage	VSS – 0.3V	—	VDD + 0.3V	V	(Note 1)
D307	TRESP	Response Time	—	150	—	ns	(Note 2)

Note 1: Parameters are characterized but not tested.

2: Measured with one input at VDD/2 and the other transitioning from VSS to VDD, 40 mV step, 15 mV overdrive.

TABLE 29-15: VOLTAGE REFERENCE DC SPECIFICATIONS

Operating Conditions: 2.0V < VDD < 3.6V, -40°C < TA < +85°C (unless otherwise stated)							
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ**	**Max**	**Units**	**Comments**
VRD310	TSET	Settling Time	—	—	10	µs	(Note 1)
VRD311	VRAA	Absolute Accuracy	-1	—	1	LSb	
VRD312	VRUR	Unit Resistor Value (R)	—	4.5	—	kΩ	

Note 1: Measures the interval while DACDAT<4:0> transitions from ‘11111’ to ‘00000’.

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29.2 AC Characteristics and Timing Parameters

The information contained in this section defines the PIC32MM0256GPM064 family AC characteristics and timing parameters.

TABLE 29-16: TEMPERATURE AND VOLTAGE SPECIFICATIONS – AC

AC CHARACTERISTICS	**Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated)** Operating temperature -40°C ≤ T_A ≤ +85°C Operating voltage V_{DD} range as described in **Section 29.1 "DC Characteristics"**.

FIGURE 29-2: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS

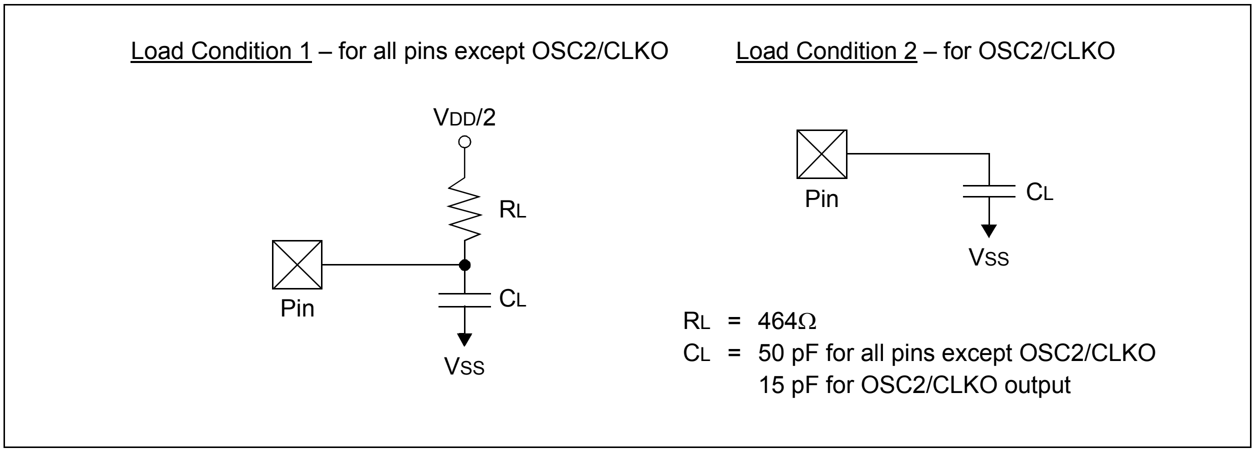

TABLE 29-17: CAPACITIVE LOADING CONDITIONS ON OUTPUT PINS

Param No.	Symbol	Characteristic	Min	Typ[(1)]	Max	Units	Conditions
DO50	C_{OSCO}	OSC2/CLKO Pin	—	—	TBD	pF	In XT and HS modes when external clock is used to drive OSC1/CLKI
DO56	C_{IO}	All I/O Pins and OSC2	—	—	TBD	pF	EC mode
DO58	C_B	SCLx, SDAx	—	—	TBD	pF	In I^2C mode

Legend: TBD = To Be Determined

Note 1: Data in the "Typ" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

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FIGURE 29-3: EXTERNAL CLOCK TIMING

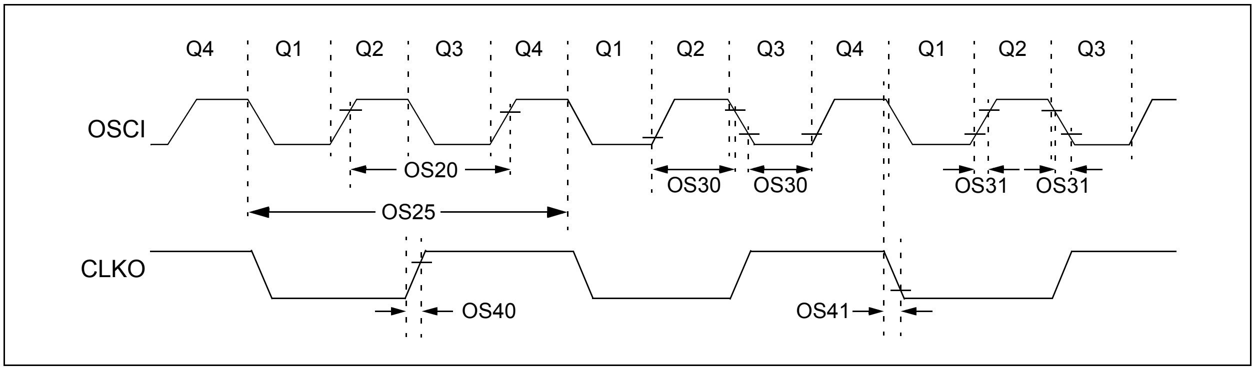

TABLE 29-18: EXTERNAL CLOCK TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param No.	Symbol	Characteristic	Min	Typ(1)	Max	Units	Conditions
OS10	FOSC	External CLKI Frequency	DC 2	— —	32 48	MHz MHz	EC ECPLL(2)
		Oscillator Frequency	3.5 3.5 10 10 31	— — — — —	10 10 32 24 50	MHz MHz MHz MHz kHz	XT XTPLL HS HSPLL SOSC
OS20	TOSC	TOSC = 1/FOSC	—	—	—	—	See Parameter OS10 for FOSC value
OS25	TCY	Instruction Cycle Time	40	—	DC	ns	
OS30	TosL, TosH	External Clock in (OSC1) High or Low Time	0.45 x TOSC	—	—	ns	EC
OS31	TosR, TosF	External Clock in (OSC1) Rise or Fall Time	—	—	TBD	ns	EC
OS40	TckR	CLKO Rise Time(3)	—	15	30	ns	
OS41	TckF	CLKO Fall Time(3)	—	15	30	ns	

Legend: TBD = To Be Determined

Note 1: Data in the "Typ" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: Represents input to the system clock prescaler. PLL dividers and postscalers must still be configured so that the system clock frequency does not exceed the maximum frequency, as shown in Figure 29-1.

3: Measurements are taken in EC mode. The CLKO signal is measured on the OSC2 pin.

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TABLE 29-19: PLL CLOCK TIMING SPECIFICATIONS

AC CHARACTERISTICS			Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param No.	Symbol	Characteristic	Min	Typ	Max	Units	Conditions
OS50	FPLLI	PLL Input Frequency Range(1)	2	—	24	MHz	
OS54	FPLLO	PLL Output Frequency Range(1)	16	—	96	MHz	
OS52	TLOCK	PLL Start-up Time (Lock Time)	—	—	24	μs	
OS53	DCLK	CLKO Stability (Jitter)	-0.12	—	0.12	%	

Note 1: These parameters are characterized but not tested in manufacturing.

TABLE 29-20: INTERNAL RC ACCURACY

AC CHARACTERISTICS		Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param No.	Characteristic	Min	Typ	Max	Units	Conditions
F20	FRC Accuracy @ 8 MHz	-1.5	—	1.5	%	2.0V ≤ VDD ≤ 3.6V, -40°C ≤ TA ≤ +85°C(1)
F21	LPRC @ 32 kHz	-20	—	20	%	VCAP Output Voltage = 1.8V
F22	FRC Tune Step-Size (in OSCTUN register)	—	.05	—	%/bit	

Note 1: To achieve this accuracy, physical stress applied to the microcontroller package (ex., by flexing the PCB) must be kept to a minimum.

TABLE 29-21: RC OSCILLATOR START-UP TIME

AC CHARACTERISTICS			Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param No.	Symbol	Characteristic	Min	Typ	Max	Units	Conditions
FR0	TFRC	FRC Oscillator Start-up Time	—	—	2	μs	
FR1	TLPRC	Low-Power RC Oscillator Start-up Time	—	—	70	μs	

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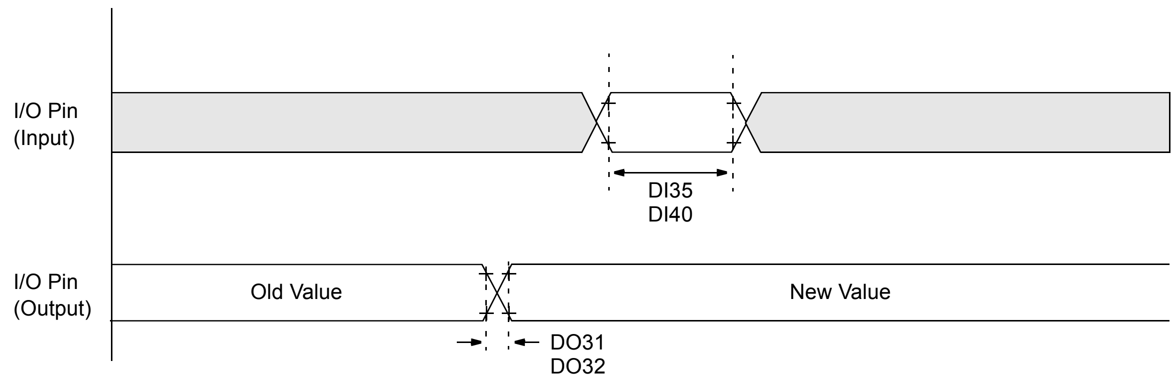
FIGURE 29-4: CLKO AND I/O TIMING CHARACTERISTICS



Note: Refer to Figure 29-2 for load conditions.

TABLE 29-22: CLKO AND I/O TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param No.	Symbol	Characteristic	Min	Typ[1]	Max	Units	Conditions
DO31	TIOR	Port Output Rise Time	—	10	25	ns	
DO32	TIOF	Port Output Fall Time	—	10	25	ns	
DI35	TINP	INTx Pin High or Low Time (input)	1	—	—	TCY	
DI40	TRBP	CNx High or Low Time (input)	1	—	—	TCY	

Note 1: Data in the “Typ” column is at 3.3V, +25°C unless otherwise stated.

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TABLE 29-23: RESET AND BROWN-OUT RESET REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param No.	Symbol	Characteristic	Min	Typ[1]	Max	Units	Conditions
SY10	TMCL	$\overline{\text{MCLR}}$ Pulse Width (Low)	2	—	—	µs	
SY13	TIOZ	I/O High-Impedance from $\overline{\text{MCLR}}$ Low or Watchdog Timer Reset	—	1	—	µs	Device running or in Idle
SY25	TBOR	Brown-out Reset Pulse Width	1	—	—	µs	VDD ≤ VBOR
SY45	TRST	Internal State Reset Time	—	25	—	µs	
SY71	TPM	Program Memory Wake-up Time	—	22	—	µs	Sleep wake-up with VREGS = 0
			—	3.8	—	µs	Sleep wake-up with VREGS = 1
SY72	TLVR	Low-Voltage Regulator Wake-up Time	—	163	—	µs	Sleep wake-up with VREGS = 0
			—	23	—	µs	Sleep wake-up with VREGS = 1

Note 1: Parameters are for design guidance and are not tested.

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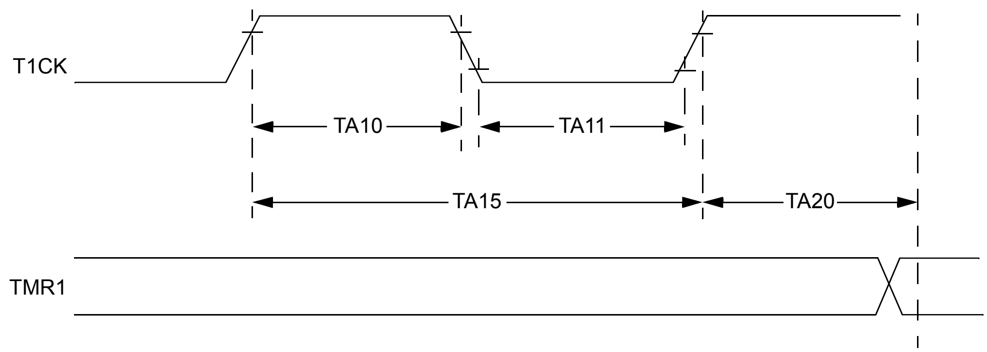
FIGURE 29-5: TIMER1 EXTERNAL CLOCK TIMING CHARACTERISTICS



Note: Refer to Figure 29-2 for load conditions.

TABLE 29-24: TIMER1 EXTERNAL CLOCK TIMING REQUIREMENTS

AC CHARACTERISTICS				Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C				
Param No.	**Symbol**	**Characteristics(1)**		**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
TA10	TTXH	T1CK High Time	Synchronous, with Prescaler	[(12.5 ns or 1 TPBCLK)/N] + 20 ns	—	—	ns	Must also meet Parameter TA15(2)
			Asynchronous, with Prescaler	10	—	—	ns	
TA11	TTXL	T1CK Low Time	Synchronous, with Prescaler	[(12.5 ns or 1 TPBCLK)/N] + 20 ns	—	—	ns	Must also meet Parameter TA15(2)
			Asynchronous, with Prescaler	10	—	—	ns	
TA15	TTXP	T1CK Input Period	Synchronous, with Prescaler	[(Greater of 20 ns or 2 TPBCLK)/N] + 30 ns	—	—	ns	VDD > 2.0V(2)
				[(Greater of 20 ns or 2 TPBCLK)/N] + 50 ns	—	—	ns	VDD < 2.0V(2)
			Asynchronous, with Prescaler	20	—	—	ns	VDD > 2.0V
				50	—	—	ns	VDD < 2.0V
TA20	TCKEXTMRL	Delay from External T1CK Clock Edge to Timer Increment		—		1	TPBCLK	

Note 1: This parameter is characterized but not tested in manufacturing.
2: N = Prescale Value (1, 8, 64, 256).

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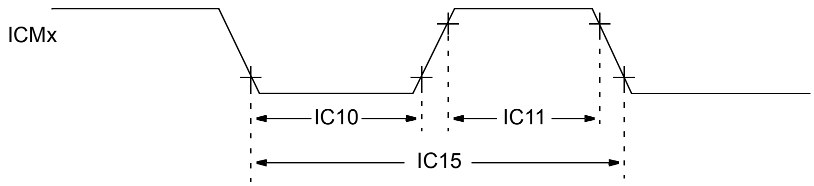
FIGURE 29-6: MCCP AND SCCP INPUT CAPTURE MODE TIMING CHARACTERISTICS



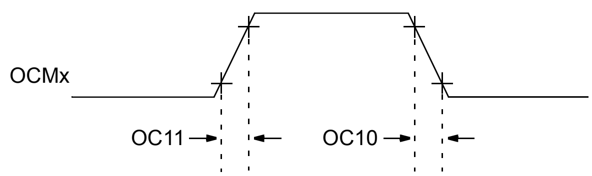
Note: Refer to Figure 29-2 for load conditions.

TABLE 29-25: MCCP AND SCCP INPUT CAPTURE MODE TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C			
Param No.	**Symbol**	**Characteristics(1)**	**Min.**	**Max.**	**Units**	**Conditions**
IC10	TCCL	ICMx Input Low Time	[(12.5 ns or 1 TPBCLK)/N] + 25 ns	—	ns	Must also meet Parameter IC15
IC11	TCCH	ICMx Input High Time	[(12.5 ns or 1 TPBCLK)/N] + 25 ns	—	ns	Must also meet Parameter IC15
IC15	TCCP	ICMx Input Period	[(25 ns or 2 TPBCLK)/N] + 50 ns	—	ns	

Note 1: These parameters are characterized but not tested in manufacturing.

FIGURE 29-7: MCCP AND SCCP OUTPUT COMPARE MODE TIMING CHARACTERISTICS



Note: Refer to Figure 29-2 for load conditions.

TABLE 29-26: MCCP AND SCCP OUTPUT COMPARE MODE TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C				
Param No.	**Symbol**	**Characteristics(1)**	**Min.**	**Typical**	**Max.**	**Units**	**Conditions**
OC10	TCCF	OCMx Output Fall Time	—	—	—	ns	See Parameter DO32
OC11	TCCR	OCMx Output Rise Time	—	—	—	ns	See Parameter DO31

Note 1: These parameters are characterized but not tested in manufacturing.

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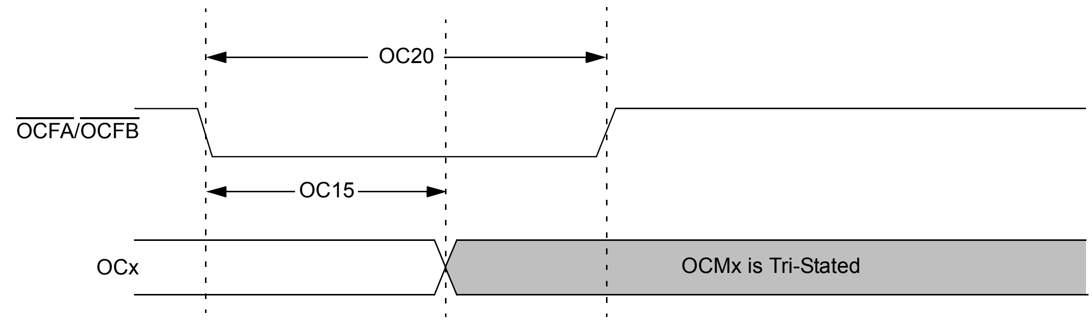
FIGURE 29-8: MCCP AND SCCP PWM MODE TIMING CHARACTERISTICS



Note: Refer to Figure 29-2 for load conditions.

TABLE 29-27: MCCP AND SCCP PWM MODE TIMING REQUIREMENTS

AC CHARACTERISTICS			**Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C				
Param No.	**Symbol**	**Characteristics[1]**	**Min**	**Typical**	**Max**	**Units**	**Conditions**
OC15	TFD	Fault Input to PWM I/O Change	—	—	50	ns	
OC20	TFLT	Fault Input Pulse Width	10	—	—	ns	

Note 1: These parameters are characterized but not tested in manufacturing.

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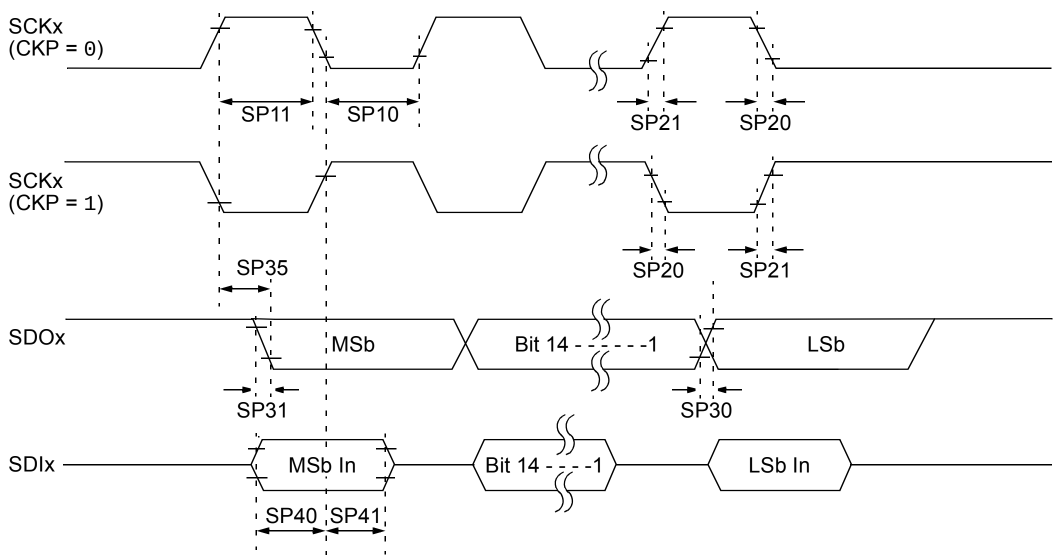
FIGURE 29-9: SPIx MODULE MASTER MODE (CKE = 0) TIMING CHARACTERISTICS



Note: Refer to Figure 29-2 for load conditions.

TABLE 29-28: SPIx MASTER MODE (CKE = 0) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.0V to 3.6V(unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C				
Param No.	**Symbol**	**Characteristics[1]**	**Min.**	**Typical[2]**	**Max.**	**Units**	**Conditions**
SP10	TSCL	SCKx Output Low Time[3]	TSCK/2	—	—	ns	
SP11	TSCH	SCKx Output High Time[3]	TSCK/2	—	—	ns	
SP20	TSCF	SCKx Output Fall Time[4]	—	—	—	ns	See Parameter DO32
SP21	TSCR	SCKx Output Rise Time[4]	—	—	—	ns	See Parameter DO31
SP30	TDOF	SDOx Data Output Fall Time[4]	—	—	—	ns	See Parameter DO32
SP31	TDOR	SDOx Data Output Rise Time[4]	—	—	—	ns	See Parameter DO31
SP35	TSCH2DOV, TSCL2DOV	SDOx Data Output Valid after SCKx Edge	—	—	7	ns	VDD > 2.0V
			—	—	10	ns	VDD < 2.0V
SP40	TDIV2SCH, TDIV2SCL	Setup Time of SDIx Data Input to SCKx Edge	5	—	—	ns	
SP41	TSCH2DIL, TSCL2DIL	Hold Time of SDIx Data Input to SCKx Edge	5	—	—	ns	

Note 1: These parameters are characterized but not tested in manufacturing.

2: Data in the "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

3: The minimum clock period for SCKx is 40 ns. Therefore, the clock generated in Master mode must not violate this specification.

4: Assumes 10 pF load on all SPIx pins.

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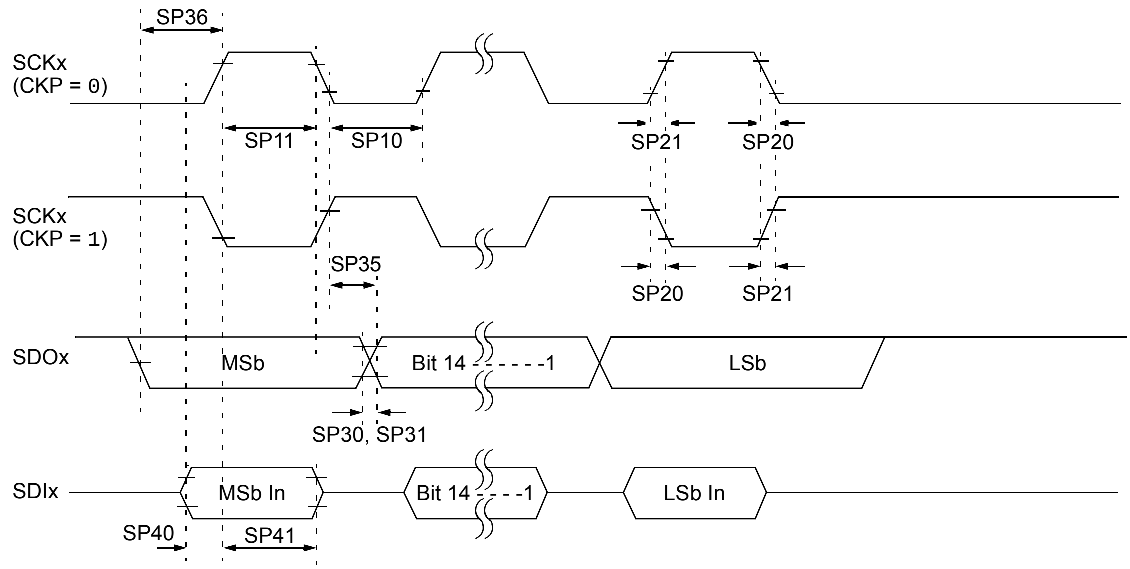
FIGURE 29-10: SPIx MODULE MASTER MODE (CKE = 1) TIMING CHARACTERISTICS



Note: Refer to Figure 29-2 for load conditions.

TABLE 29-29: SPIx MODULE MASTER MODE (CKE = 1) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C				
Param No.	Symbol	Characteristics(1)	Min.	Typ.(2)	Max.	Units	Conditions
SP10	TscL	SCKx Output Low Time(3)	Tsck/2	—	—	ns	
SP11	TscH	SCKx Output High Time(3)	Tsck/2	—	—	ns	
SP20	TscF	SCKx Output Fall Time(4)	—	—	—	ns	See Parameter DO32
SP21	TscR	SCKx Output Rise Time(4)	—	—	—	ns	See Parameter DO31
SP30	TdoF	SDOx Data Output Fall Time(4)	—	—	—	ns	See Parameter DO32
SP31	TdoR	SDOx Data Output Rise Time(4)	—	—	—	ns	See Parameter DO31
SP35	TscH2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	—	—	7	ns	VDD > 2.0V
			—	—	10	ns	VDD < 2.0V
SP36	TdoV2sc, TdoV2scL	SDOx Data Output Setup to First SCKx Edge	7	—	—	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	7	—	—	ns	VDD > 2.0V
			10	—	—	ns	VDD < 2.0V
SP41	TscH2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	7	—	—	ns	VDD > 2.0V
			10	—	—	ns	VDD < 2.0V

Note 1: These parameters are characterized but not tested in manufacturing.

2: Data in the “Typ.” column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

3: The minimum clock period for SCKx is 40 ns. Therefore, the clock generated in Master mode must not violate this specification.

4: Assumes 10 pF load on all SPIx pins.

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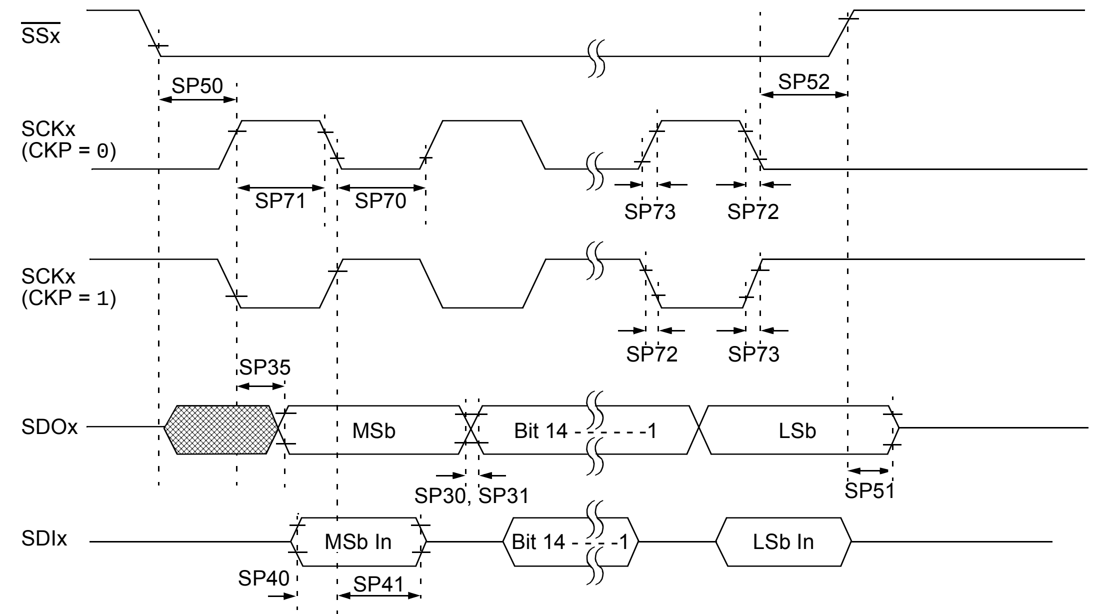
FIGURE 29-11: SPIx MODULE SLAVE MODE (CKE = 0) TIMING CHARACTERISTICS



Note: Refer to Figure 29-2 for load conditions.

TABLE 29-30: SPIx MODULE SLAVE MODE (CKE = 0) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C				
Param No.	Symbol	Characteristics[1]	Min.	Typ.[2]	Max.	Units	Conditions
SP70	TscL	SCKx Input Low Time[3]	Tsck/2	—	—	ns	
SP71	TscH	SCKx Input High Time[3]	Tsck/2	—	—	ns	
SP72	TscF	SCKx Input Fall Time	—	—	—	ns	See Parameter DO32
SP73	TscR	SCKx Input Rise Time	—	—	—	ns	See Parameter DO31
SP30	TdoF	SDOx Data Output Fall Time[4]	—	—	—	ns	See Parameter DO32
SP31	TdoR	SDOx Data Output Rise Time[4]	—	—	—	ns	See Parameter DO31
SP35	TscH2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	—	—	7	ns	VDD > 2.0V
			—	—	10	ns	VDD < 2.0V
SP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	5	—	—	ns	
SP41	TscH2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	5	—	—	ns	
SP50	TssL2scH, TssL2scL	SSx ↓ to SCKx ↑ or SCKx Input	88	—	—	ns	
SP51	TssH2doZ	SSx ↑ to SDOx Output High-Impedance[4]	2.5	—	12	ns	
SP52	TscH2ssH TscL2ssH	SSx after SCKx Edge	10	—	—	ns	

Note 1: These parameters are characterized but not tested in manufacturing.

2: Data in "Typ." column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

3: The minimum clock period for SCKx is 40 ns.

4: Assumes 10 pF load on all SPIx pins.

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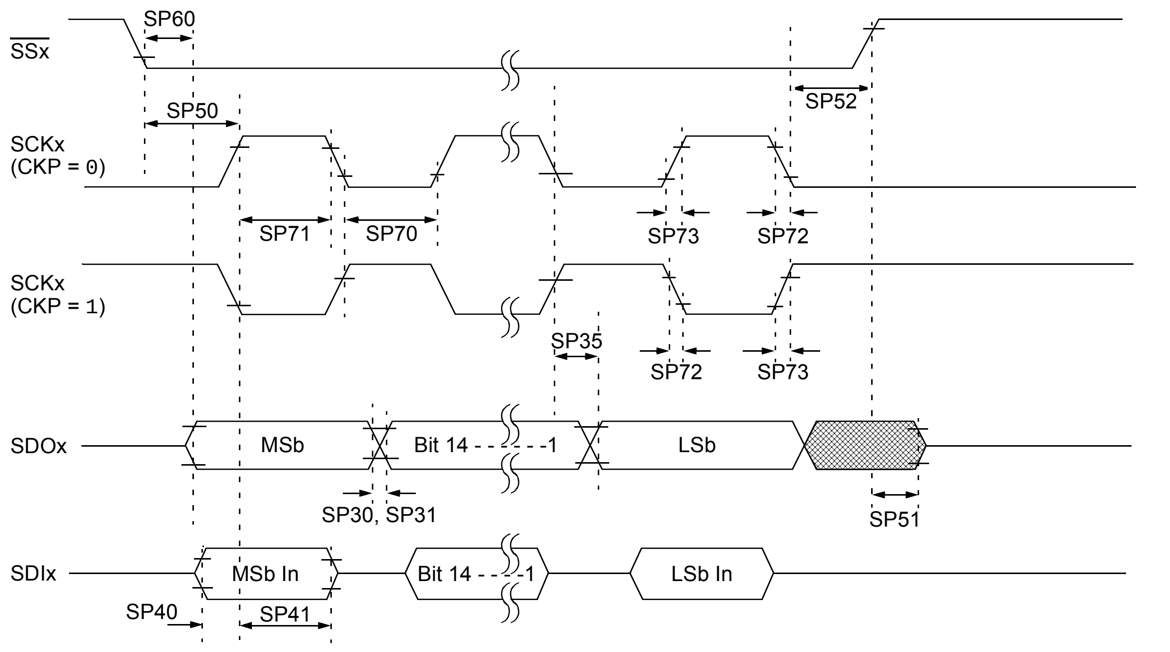
FIGURE 29-12: SPIx MODULE SLAVE MODE (CKE = 1) TIMING CHARACTERISTICS



Note: Refer to Figure 29-2 for load conditions.

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TABLE 29-31: SPIx MODULE SLAVE MODE (CKE = 1) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C				
Param No.	Symbol	Characteristics[1]	Min.	Typical[2]	Max.	Units	Conditions
SP70	TscL	SCKx Input Low Time[3]	Tsck/2	—	—	ns	
SP71	TscH	SCKx Input High Time[3]	Tsck/2	—	—	ns	
SP72	TscF	SCKx Input Fall Time	—	—	10	ns	
SP73	TscR	SCKx Input Rise Time	—	—	10	ns	
SP30	TdoF	SDOx Data Output Fall Time[4]	—	—	—	ns	See Parameter DO32
SP31	TdoR	SDOx Data Output Rise Time[4]	—	—	—	ns	See Parameter DO31
SP35	TscH2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	—	—	10	ns	VDD > 2.0V
			—	—	15	ns	VDD < 2.0V
SP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	0	—	—	ns	
SP41	TscH2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	7	—	—	ns	
SP50	TssL2scH, TssL2scL	$\overline{SSx}$ ↓ to SCKx ↓ or SCKx ↑ Input	88	—	—	ns	
SP51	TssH2doZ	$\overline{SSx}$ ↑ to SDOx Output High-Impedance[4]	2.5	—	12	ns	
SP52	TscH2ssH TscL2ssH	$\overline{SSx}$ ↑ after SCKx Edge	10	—	—	ns	
SP60	TssL2doV	SDOx Data Output Valid after $\overline{SSx}$ Edge	—	—	12.5	ns	

Note 1: These parameters are characterized but not tested in manufacturing.

2: Data in the "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

3: The minimum clock period for SCKx is 40 ns.

4: Assumes 10 pF load on all SPIx pins.

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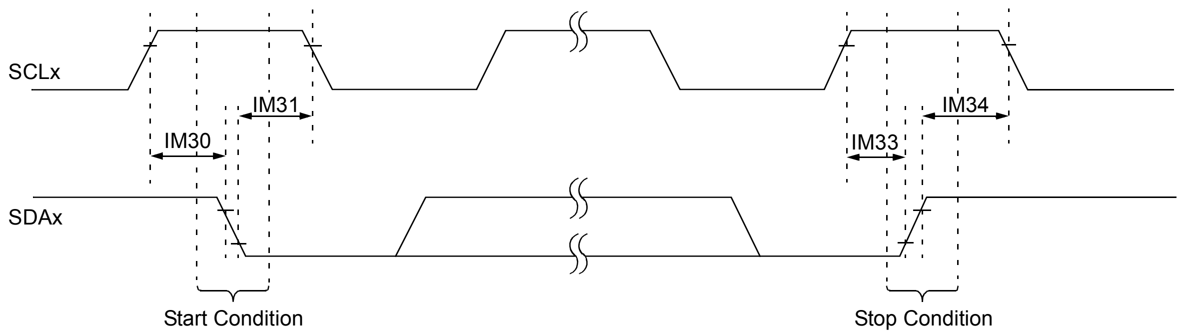
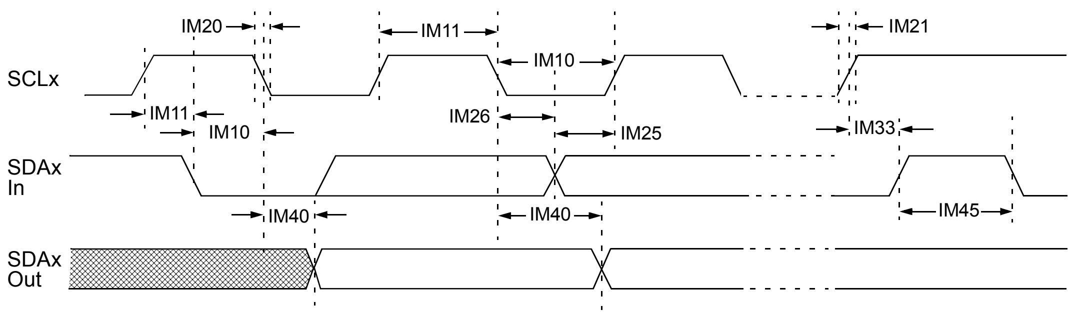
FIGURE 29-13: I2Cx BUS START/STOP BITS TIMING CHARACTERISTICS (MASTER MODE)



Note: Refer to Figure 29-2 for load conditions.

FIGURE 29-14: I2Cx BUS DATA TIMING CHARACTERISTICS (MASTER MODE)



Note: Refer to Figure 29-2 for load conditions.

TABLE 29-32: I2Cx BUS DATA TIMING REQUIREMENTS (MASTER MODE)

AC CHARACTERISTICS				Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C			
Param No.	**Sym**	**Characteristics**		**Min.(1)**	**Max.**	**Units**	**Conditions**
IM10	TLO:SCL	Clock Low Time	100 kHz mode	TSYSCLK * (BRG + 2)	—	µs	
			400 kHz mode	TSYSCLK * (BRG + 2)	—	µs	
			1 MHz mode(2)	TSYSCLK * (BRG + 2)	—	µs	
IM11	THI:SCL	Clock High Time	100 kHz mode	TSYSCLK * (BRG + 2)	—	µs	
			400 kHz mode	TSYSCLK * (BRG + 2)	—	µs	
			1 MHz mode(2)	TSYSCLK * (BRG + 2)	—	µs	
IM20	TF:SCL	SDAx and SCLx Fall Time	100 kHz mode	—	300	ns	CB is specified to be from 10 to 400 pF
			400 kHz mode	20 + 0.1 CB	300	ns	
			1 MHz mode(2)	—	100	ns	
IM21	TR:SCL	SDAx and SCLx Rise Time	100 kHz mode	—	1000	ns	CB is specified to be from 10 to 400 pF
			400 kHz mode	20 + 0.1 CB	300	ns	
			1 MHz mode(2)	—	300	ns	

Note 1: BRG is the value of the I^{2}C Baud Rate Generator.
2: Maximum Pin Capacitance = 10 pF for all I2Cx pins (for 1 MHz mode only).
3: The typical value for this parameter is 104 ns.

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TABLE 29-32: I2Cx BUS DATA TIMING REQUIREMENTS (MASTER MODE) (CONTINUED)

AC CHARACTERISTICS				Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C			
Param No.	Sym	Characteristics		Min.(1)	Max.	Units	Conditions
IM25	TSU:DAT	Data Input Setup Time	100 kHz mode	250	—	ns	
			400 kHz mode	100	—	ns	
			1 MHz mode(2)	100	—	ns	
IM26	THD:DAT	Data Input Hold Time	100 kHz mode	0	—	µs	
			400 kHz mode	0	0.9	µs	
			1 MHz mode(2)	0	0.3	µs	
IM30	TSU:STA	Start Condition Setup Time	100 kHz mode	TPBCLK * (BRG + 2)	—	µs	Only relevant for Repeated Start condition
			400 kHz mode	TPBCLK * (BRG + 2)	—	µs	
			1 MHz mode(2)	TPBCLK * (BRG + 2)	—	µs	
IM31	THD:STA	Start Condition Hold Time	100 kHz mode	TPBCLK * (BRG + 2)	—	µs	After this period, the first clock pulse is generated
			400 kHz mode	TPBCLK * (BRG + 2)	—	µs	
			1 MHz mode(2)	TPBCLK * (BRG + 2)	—	µs	
IM33	TSU:STO	Stop Condition Setup Time	100 kHz mode	TPBCLK * (BRG + 2)	—	µs	
			400 kHz mode	TPBCLK * (BRG + 2)	—	µs	
			1 MHz mode(2)	TPBCLK * (BRG + 2)	—	µs	
IM34	THD:STO	Stop Condition Hold Time	100 kHz mode	TPBCLK * (BRG + 2)	—	ns	
			400 kHz mode	TPBCLK * (BRG + 2)	—	ns	
			1 MHz mode(2)	TPBCLK * (BRG + 2)	—	ns	
IM40	TAA:SCL	Output Valid from Clock	100 kHz mode	—	3500	ns	
			400 kHz mode	—	1000	ns	
			1 MHz mode(2)	—	350	ns	
IM45	TBF:SDA	Bus Free Time	100 kHz mode	4.7	—	µs	The amount of time the bus must be free before a new transmission can start
			400 kHz mode	1.3	—	µs	
			1 MHz mode(2)	0.5	—	µs	
IM50	CB	Bus Capacitive Loading		—	—	pF	See Parameter DO58
IM51	TPGD	Pulse Gobbler Delay		52	312	ns	(Note 3)

Note 1: BRG is the value of the I^{2}C Baud Rate Generator.
2: Maximum Pin Capacitance = 10 pF for all I2Cx pins (for 1 MHz mode only).
3: The typical value for this parameter is 104 ns.

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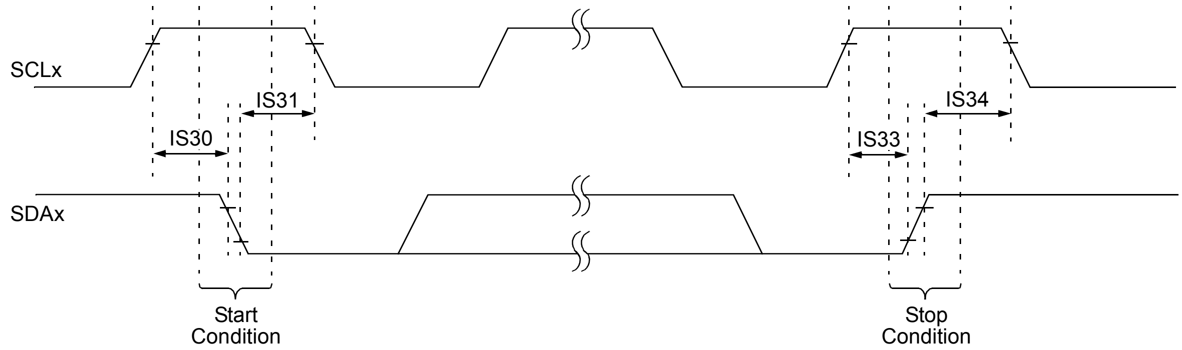
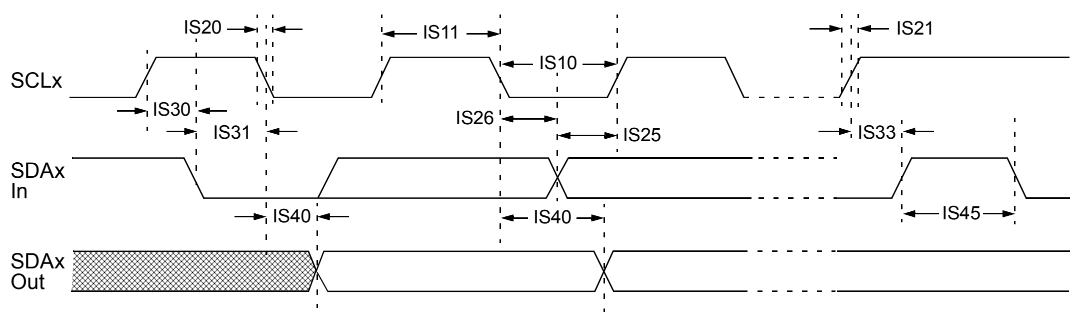
FIGURE 29-15: I2Cx BUS START/STOP BITS TIMING CHARACTERISTICS (SLAVE MODE)



Note: Refer to Figure 29-2 for load conditions.

FIGURE 29-16: I2Cx BUS DATA TIMING CHARACTERISTICS (SLAVE MODE)



Note: Refer to Figure 29-2 for load conditions.

TABLE 29-33: I2Cx BUS DATA TIMING REQUIREMENTS (SLAVE MODE)

AC CHARACTERISTICS				Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C			
Param No.	Sym	Characteristics		Min.	Max.	Units	Conditions
IS10	TLO:SCL	Clock Low Time	100 kHz mode	4.7	—	µs	PBCLK must operate at a minimum of 800 kHz
			400 kHz mode	1.3	—	µs	PBCLK must operate at a minimum of 3.2 MHz
			1 MHz mode(1)	0.5	—	µs	
IS11	THI:SCL	Clock High Time	100 kHz mode	4.0	—	µs	PBCLK must operate at a minimum of 800 kHz
			400 kHz mode	0.6	—	µs	PBCLK must operate at a minimum of 3.2 MHz
			1 MHz mode(1)	0.5	—	µs	
IS20	TF:SCL	SDAx and SCLx Fall Time	100 kHz mode	—	300	ns	CB is specified to be from 10 to 400 pF
			400 kHz mode	20 + 0.1 CB	300	ns	
			1 MHz mode(1)	—	100	ns	

Note 1: Maximum Pin Capacitance = 10 pF for all I2Cx pins (for 1 MHz mode only).

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TABLE 29-33: I2Cx BUS DATA TIMING REQUIREMENTS (SLAVE MODE) (CONTINUED)

AC CHARACTERISTICS				Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C			
Param No.	Sym	Characteristics		Min.	Max.	Units	Conditions
IS21	TR:SCL	SDAx and SCLx Rise Time	100 kHz mode	—	1000	ns	CB is specified to be from 10 to 400 pF
			400 kHz mode	20 + 0.1 CB	300	ns	
			1 MHz mode(1)	—	300	ns	
IS25	TSU:DAT	Data Input Setup Time	100 kHz mode	250	—	ns	
			400 kHz mode	100	—	ns	
			1 MHz mode(1)	100	—	ns	
IS26	THD:DAT	Data Input Hold Time	100 kHz mode	0	—	ns	
			400 kHz mode	0	0.9	μs	
			1 MHz mode(1)	0	0.3	μs	
IS30	TSU:STA	Start Condition Setup Time	100 kHz mode	4700	—	ns	Only relevant for Repeated Start condition
			400 kHz mode	600	—	ns	
			1 MHz mode(1)	250	—	ns	
IS31	THD:STA	Start Condition Hold Time	100 kHz mode	4000	—	ns	After this period, the first clock pulse is generated
			400 kHz mode	600	—	ns	
			1 MHz mode(1)	250	—	ns	
IS33	TSU:STO	Stop Condition Setup Time	100 kHz mode	4000	—	ns	
			400 kHz mode	600	—	ns	
			1 MHz mode(1)	600	—	ns	
IS34	THD:STO	Stop Condition Hold Time	100 kHz mode	4000	—	ns	
			400 kHz mode	600	—	ns	
			1 MHz mode(1)	250	—	ns	
IS40	TAA:SCL	Output Valid from Clock	100 kHz mode	0	3500	ns	
			400 kHz mode	0	1000	ns	
			1 MHz mode(1)	0	350	ns	
IS45	TBF:SDA	Bus Free Time	100 kHz mode	4.7	—	μs	The amount of time the bus must be free before a new transmission can start
			400 kHz mode	1.3	—	μs	
			1 MHz mode(1)	0.5	—	μs	
IS50	CB	Bus Capacitive Loading		—	—	pF	See Parameter DO58

Note 1: Maximum Pin Capacitance = 10 pF for all I2Cx pins (for 1 MHz mode only).

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TABLE 29-34: ADC MODULE INPUTS SPECIFICATIONS

Operating Conditions: 2.0V ≤ VDD ≤ 3.6V, -40°C ≤ TA ≤ +85°C (unless otherwise stated)					
Param No.	**Symbol**	**Characteristic**	**Min**	**Max**	**Units**
Reference Inputs					
AD05	VREFH	Reference Voltage High	AVSS + 1.7	AVDD	V
AD06	VREFL	Reference Voltage Low	AVSS	AVDD – 1.7	V
AD07	VREF	Absolute Reference Voltage	AVSS – 0.3	AVDD + 0.3	V
Analog Inputs					
AD10	VINH-VINL	Full-Scale Input Span	VREFL	VREFH	V
AD11	VIN	Absolute Input Voltage	AVSS – 0.3	AVDD + 0.3	V
AD12	VINL	Absolute VINL Input Voltage	AVSS – 0.3	AVDD + 0.3	V
AD17	RIN	Recommended Impedance of Analog Voltage Source	—	2.5K	Ω

TABLE 29-35: ADC ACCURACY AND CONVERSION TIMING REQUIREMENTS FOR 12-BIT MODE(1)

Operating Conditions: VDD = 3.3V, AVSS = VREFL = 0V, AVDD = VREFH = 3.3V, -40°C ≤ TA ≤ +85°C						
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ(2)**	**Max**	**Units**
ADC Accuracy						
AD20B	Nr	Resolution	—	12	—	bits
AD21B	INL	Integral Nonlinearity	—	±2.5	±3.5	LSb
AD22B	DNL	Differential Nonlinearity	—	±0.75	+1.75/-0.95	LSb
AD23B	GERR	Gain Error	–	+2	+3	LSb
AD24B	EOFF	Offset Error	—	+1	+2	LSb
Clock Parameters						
AD50B	TAD	ADC Clock Period	280	—	—	ns
AD61B	tPSS	Sample Start Delay from Setting Sample bit (SAMP)	2	—	3	TAD
Conversion Rate						
AD55B	tCONV	Conversion Time	—	14	—	TAD
AD56B	FCNV	Throughput Rate	—	—	200	ksps

Note 1: Measurements are taken with the external VREF+ and VREF- used as the ADC voltage reference.

2: Data in the “Typ” column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

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TABLE 29-36: ADC ACCURACY AND CONVERSION TIMING REQUIREMENTS FOR 10-BIT MODE[1]

Operating Conditions: V_{DD} = 3.3V, AV_{SS} = V_{REFL} = 0V, AV_{DD} = V_{REFH} = 3.3V, -40°C ≤ T_A ≤ +85°C						
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ[2]**	**Max**	**Units**
ADC Accuracy						
AD20A	Nr	Resolution	—	10	—	bits
AD21A	INL	Integral Nonlinearity	—	±0.5	—	LSb
AD22A	DNL	Differential Nonlinearity	—	±0.5	—	LSb
AD23A	G_{ERR}	Gain Error	—	+0.75	—	LSb
AD24A	E_{OFF}	Offset Error	—	+0.25	—	LSb
Clock Parameters						
AD50A	T_{AD}	ADC Clock Period	200	—	—	ns
AD61A	t_{PSS}	Sample Start Delay from Setting Sample bit (SAMP)	2	—	3	T_{AD}
Conversion Rate						
AD55A	t_{CONV}	Conversion Time	—	12	—	T_{AD}
AD56A	F_{CNV}	Throughput Rate	—	—	300	ksps

Note 1: Measurements are taken with the external V_{REF}+ and V_{REF}- used as the ADC voltage reference.

2: Data in the “Typ” column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

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FIGURE 29-17: EJTAG TIMING CHARACTERISTICS

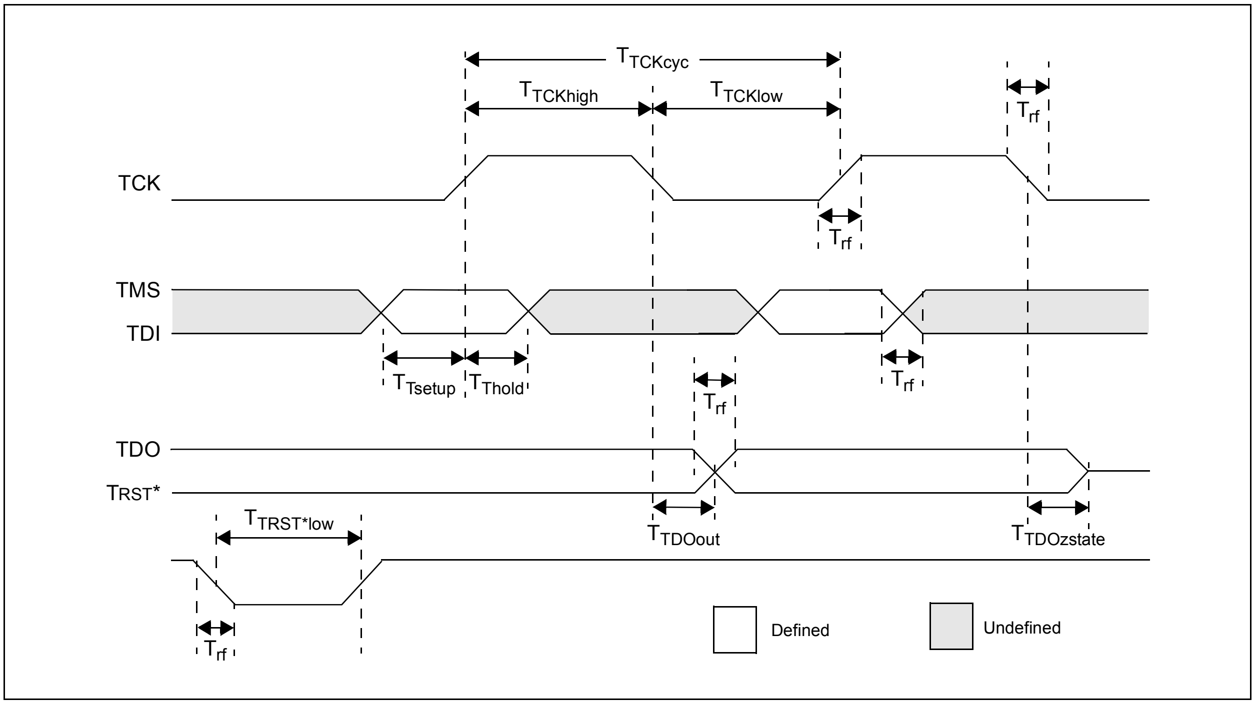

TABLE 29-37: EJTAG TIMING REQUIREMENTS

AC CHARACTERISTICS			**Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C			
Param No.	**Symbol**	**Description[1]**	**Min.**	**Max.**	**Units**	**Conditions**
EJ1	TTCKCYC	TCK Cycle Time	25	—	ns	
EJ2	TTCKHIGH	TCK High Time	10	—	ns	
EJ3	TTCKLOW	TCK Low Time	10	—	ns	
EJ4	TTSETUP	TAP Signals Setup Time before Rising TCK	5	—	ns	
EJ5	TTHOLD	TAP Signals Hold Time after Rising TCK	3	—	ns	
EJ6	TTDOOUT	TDO Output Delay Time from Falling TCK	—	5	ns	
EJ7	TTDOZSTATE	TDO 3-State Delay Time from Falling TCK	—	5	ns	
EJ8	TTRSTLOW	TRST Low Time	25	—	ns	
EJ9	TRF	TAP Signals Rise/Fall Time, All Input and Output	—	—	ns	

Note 1: These parameters are characterized but not tested in manufacturing.

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TABLE 29-38: USB OTG ELECTRICAL SPECIFICATIONS

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ T_A ≤ +85°C for Industrial				
Param. No.	**Symbol**	**Characteristics[1]**	**Min.**	**Typical**	**Max.**	**Units**	**Conditions**
USB313	V_{USB3V3}	USB Voltage	3.0	—	3.6	V	Voltage on V_{USB3V3} must be in this range for proper USB operation
USB315	V_{ILUSB}	Input Low Voltage for USB Buffer	—	—	0.8	V	
USB316	V_{IHUSB}	Input High Voltage for USB Buffer	2.0	—	—	V	
USB318	V_{DIFS}	Differential Input Sensitivity	—	—	0.2	V	The difference between D+ and D- must exceed this value while VCM is met
USB319	VCM	Differential Common-Mode Range	0.8	—	2.5	V	
USB320	Z_{OUT}	Driver Output Impedance	28.0	—	44.0	Ω	
USB321	V_{OL}	Voltage Output Low	0.0	—	0.3	V	14.25 kΩ load connected to 3.6V
USB322	V_{OH}	Voltage Output High	2.8	—	3.6	V	14.25 kΩ load connected to ground

Note 1: These parameters are characterized but not tested in manufacturing.

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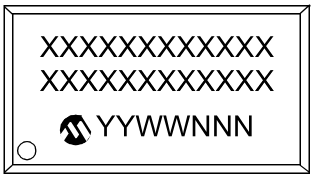
30.0 PACKAGING INFORMATION

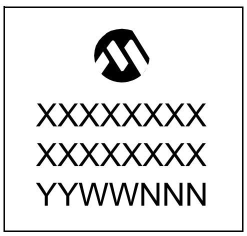
30.1 Package Marking Information

28-Lead SSOP (5.30 mm)



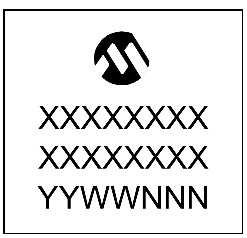
Example

28-Lead QFN (6x6 mm)



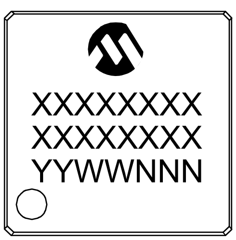
Example

28-Lead UQFN (4x4x0.6 mm)



Example

36-Lead VQFN (6x6x1.0 mm)



Example

Legend:	XX...X	Customer-specific information
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	*	All packages are Pb-free

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

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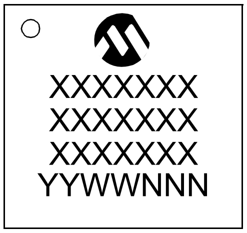
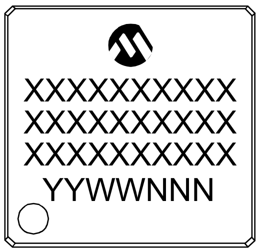
30.1 Package Marking Information (Continued)

40-Lead UQFN (5x5x0.5 mm)



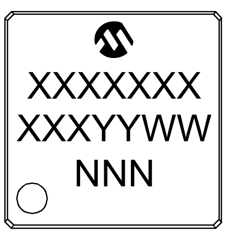
Example

48-Lead UQFN (6x6 mm)

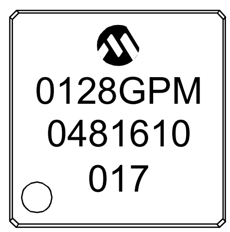


Example

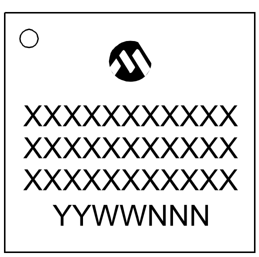
48-Lead TQFP (7x7x1.0 mm)



Example

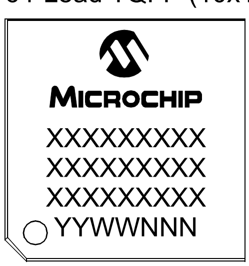


64-Lead QFN (9x9x0.9 mm)

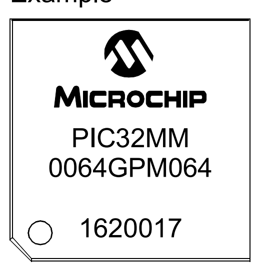


Example

64-Lead TQFP (10x10x1 mm)



Example



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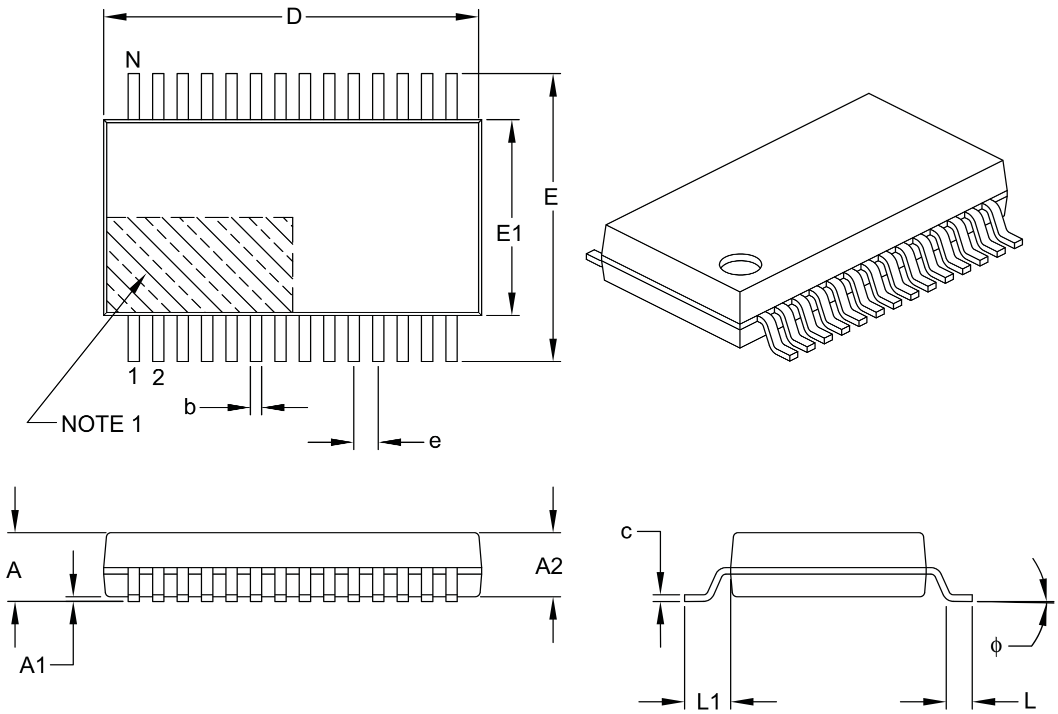
30.2 Package Details

The following sections give the technical details of the packages.

28-Lead Plastic Shrink Small Outline (SS) – 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		28	
Pitch	e		0.65 BSC	
Overall Height	A	–	–	2.00
Molded Package Thickness	A2	1.65	1.75	1.85
Standoff	A1	0.05	–	–
Overall Width	E	7.40	7.80	8.20
Molded Package Width	E1	5.00	5.30	5.60
Overall Length	D	9.90	10.20	10.50
Foot Length	L	0.55	0.75	0.95
Footprint	L1		1.25 REF	
Lead Thickness	c	0.09	–	0.25
Foot Angle	ϕ	0°	4°	8°
Lead Width	b	0.22	–	0.38

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.20 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-073B

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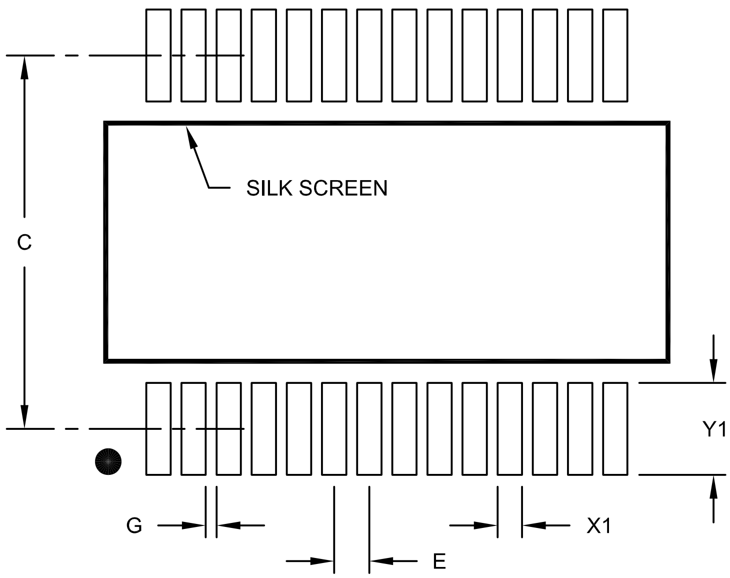
28-Lead Plastic Shrink Small Outline (SS) - 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Contact Pad Spacing	C		7.20	
Contact Pad Width (X28)	X1			0.45
Contact Pad Length (X28)	Y1			1.75
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2073A

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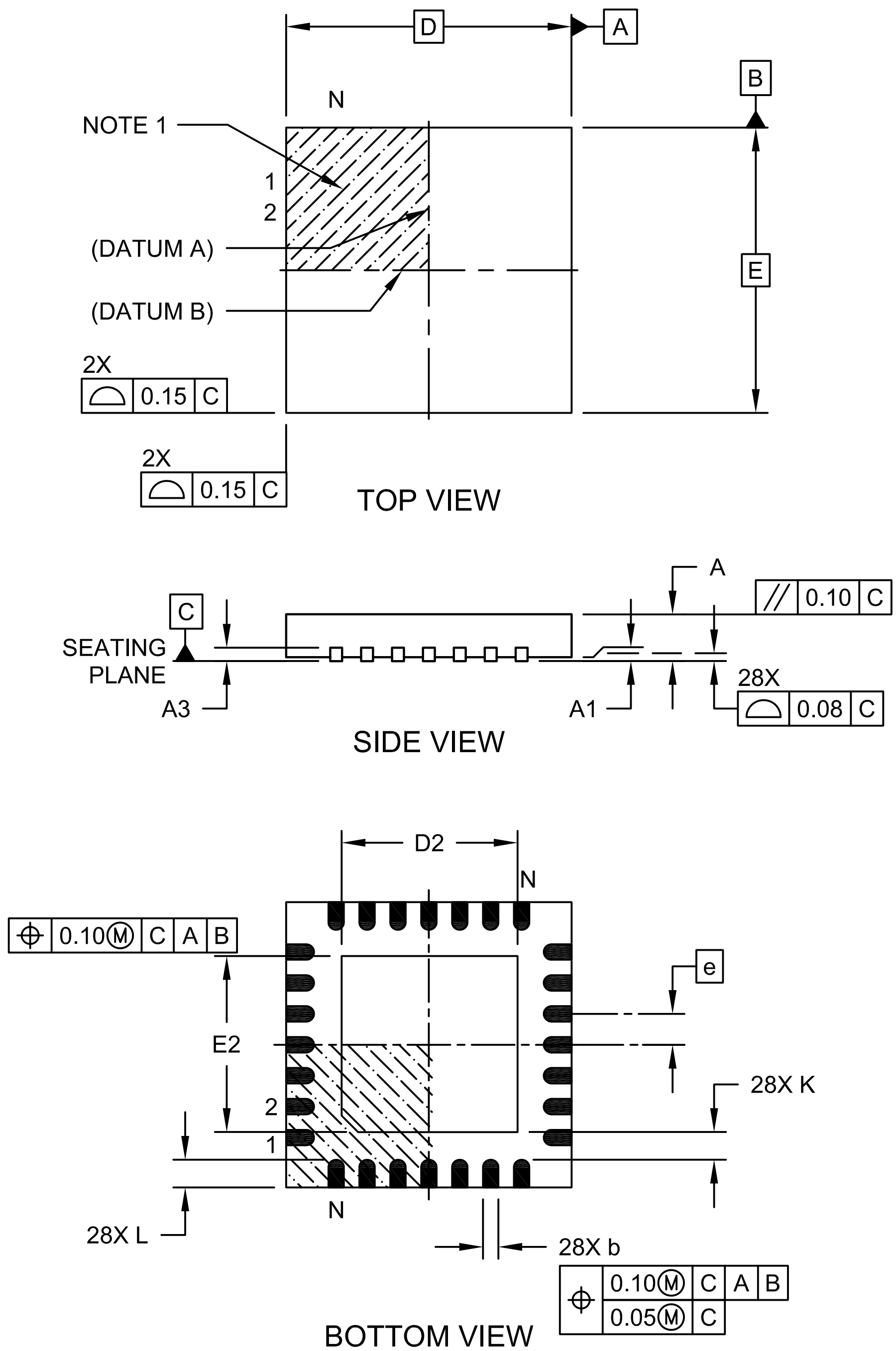
28-Lead Plastic Quad Flat, No Lead Package (ML) - 6x6 mm Body [QFN] With 0.55 mm Terminal Length

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-105C Sheet 1 of 2

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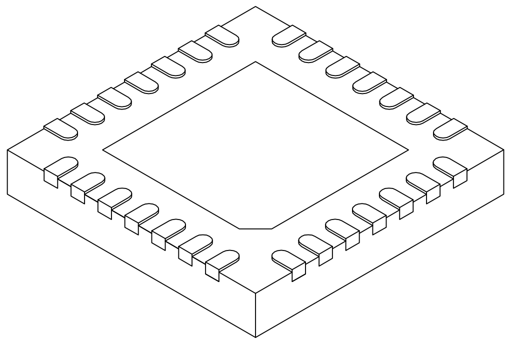
28-Lead Plastic Quad Flat, No Lead Package (ML) - 6x6 mm Body [QFN] With 0.55 mm Terminal Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units	MILLIMETERS		
Dimension	Limits	MIN	NOM	MAX
Number of Pins	N		28	
Pitch	e		0.65 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.20 REF	
Overall Width	E		6.00 BSC	
Exposed Pad Width	E2	3.65	3.70	4.20
Overall Length	D		6.00 BSC	
Exposed Pad Length	D2	3.65	3.70	4.20
Terminal Width	b	0.23	0.30	0.35
Terminal Length	L	0.50	0.55	0.70
Terminal-to-Exposed Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-105C Sheet 2 of 2

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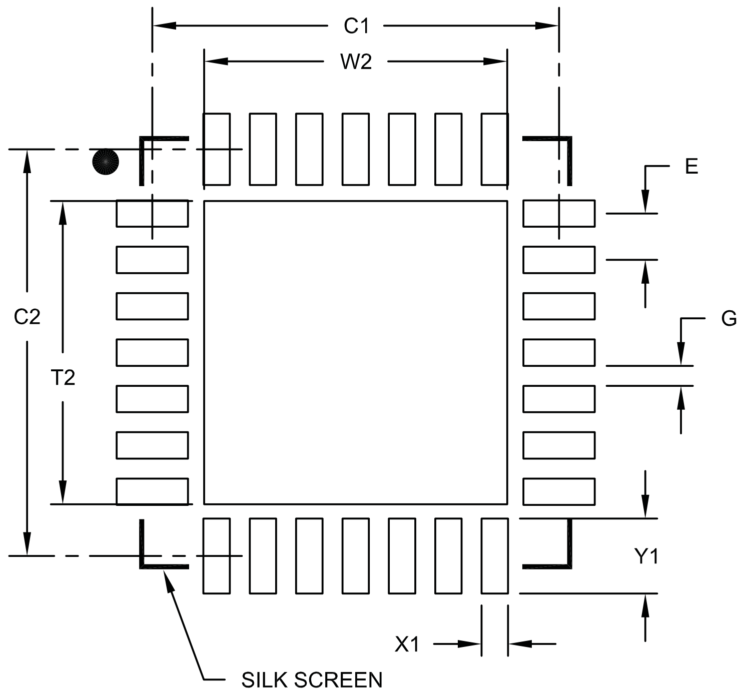
28-Lead Plastic Quad Flat, No Lead Package (ML) – 6x6 mm Body [QFN] with 0.55 mm Contact Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Optional Center Pad Width	W2			4.25
Optional Center Pad Length	T2			4.25
Contact Pad Spacing	C1		5.70	
Contact Pad Spacing	C2		5.70	
Contact Pad Width (X28)	X1			0.37
Contact Pad Length (X28)	Y1			1.00
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2105A

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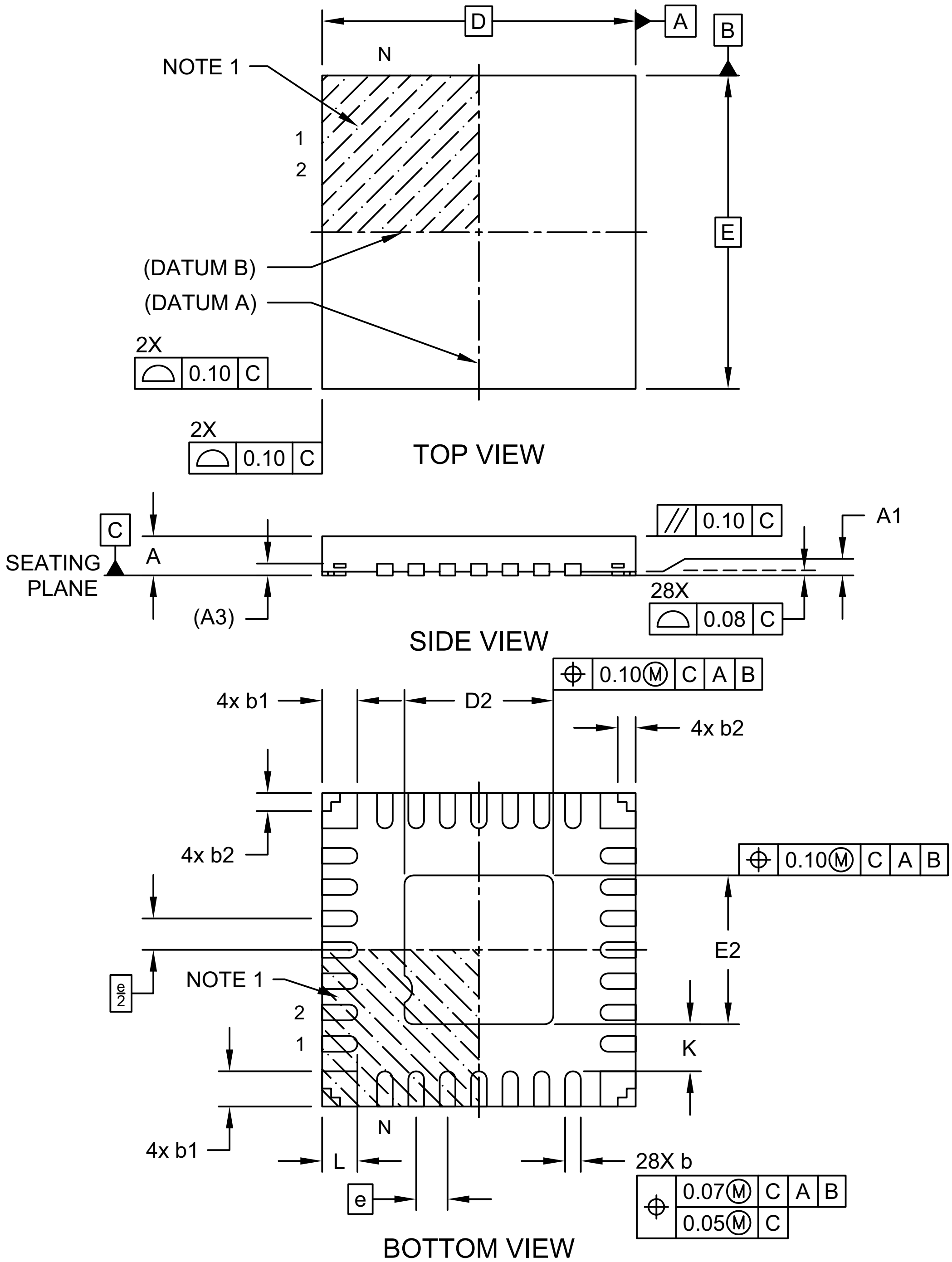
28-Lead Ultra Thin Plastic Quad Flat, No Lead Package (M6) - 4x4x0.6 mm Body [UQFN] With Corner Anchors

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-333-M6 Rev B Sheet 1 of 2

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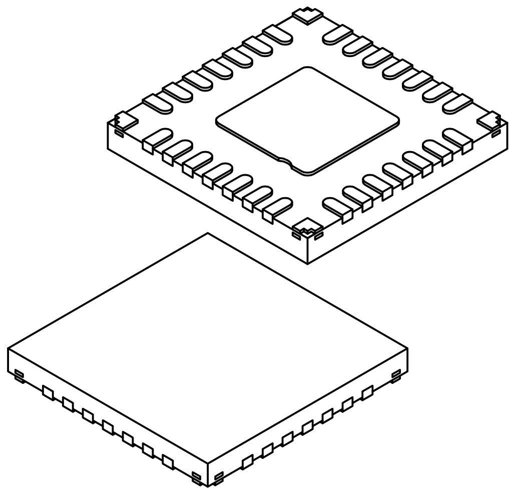
28-Lead Ultra Thin Plastic Quad Flat, No Lead Package (M6) - 4x4x0.6 mm Body [UQFN] With Corner Anchors

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		28	
Pitch	e		0.40 BSC	
Overall Height	A	-	-	0.60
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.152 REF	
Overall Width	E		4.00 BSC	
Exposed Pad Width	E2	1.80	1.90	2.00
Overall Length	D		4.00 BSC	
Exposed Pad Length	D2	1.80	1.90	2.00
Terminal Width	b	0.15	0.20	0.25
Corner Anchor Pad	b1	0.40	0.45	0.50
Corner Pad, Metal Free Zone	b2	0.18	0.23	0.28
Terminal Length	L	0.30	0.45	0.50
Terminal-to-Exposed-Pad	K	-	0.60	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

    BSC: Basic Dimension. Theoretically exact value shown without tolerances.

    REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-333-M6 Rev A Sheet 2 of 2

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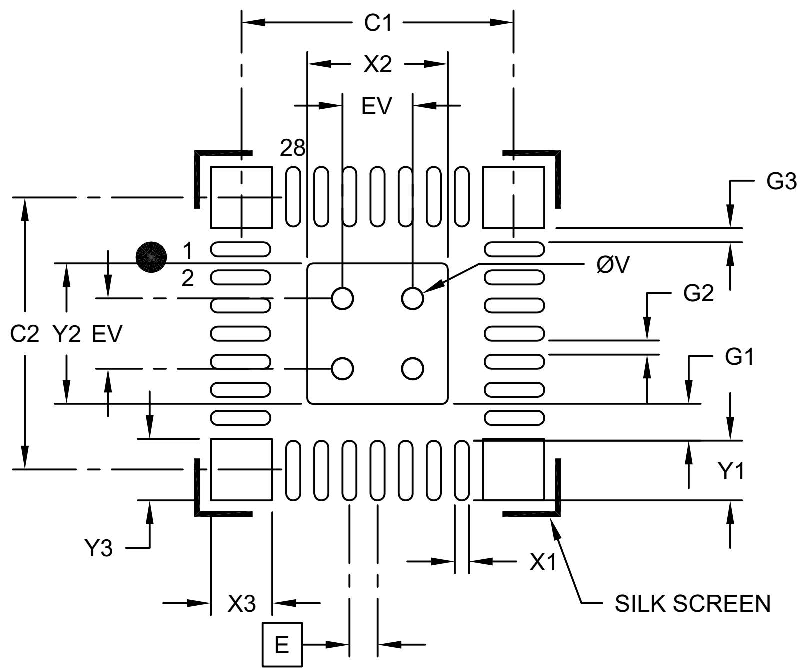
28-Lead Ultra Thin Plastic Quad Flat, No Lead Package (M6) - 4x4x0.6 mm Body [UQFN] With Corner Anchors

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

	Units	MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX
Contact Pitch	E		0.40 BSC	
Center Pad Width	X2			2.00
Center Pad Length	Y2			2.00
Contact Pad Spacing	C1		3.90	
Contact Pad Spacing	C2		3.90	
Contact Pad Width (X28)	X1			0.20
Contact Pad Length (X28)	Y1			0.85
Contact Pad to Center Pad (X28)	G1		0.52	
Contact Pad to Pad (X24)	G2	0.20		
Contact Pad to Corner Pad (X8)	G3	0.20		
Corner Anchor Width (X4)	X3			0.78
Corner Anchor Length (X4)	Y3			0.78
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2333-M6 Rev B

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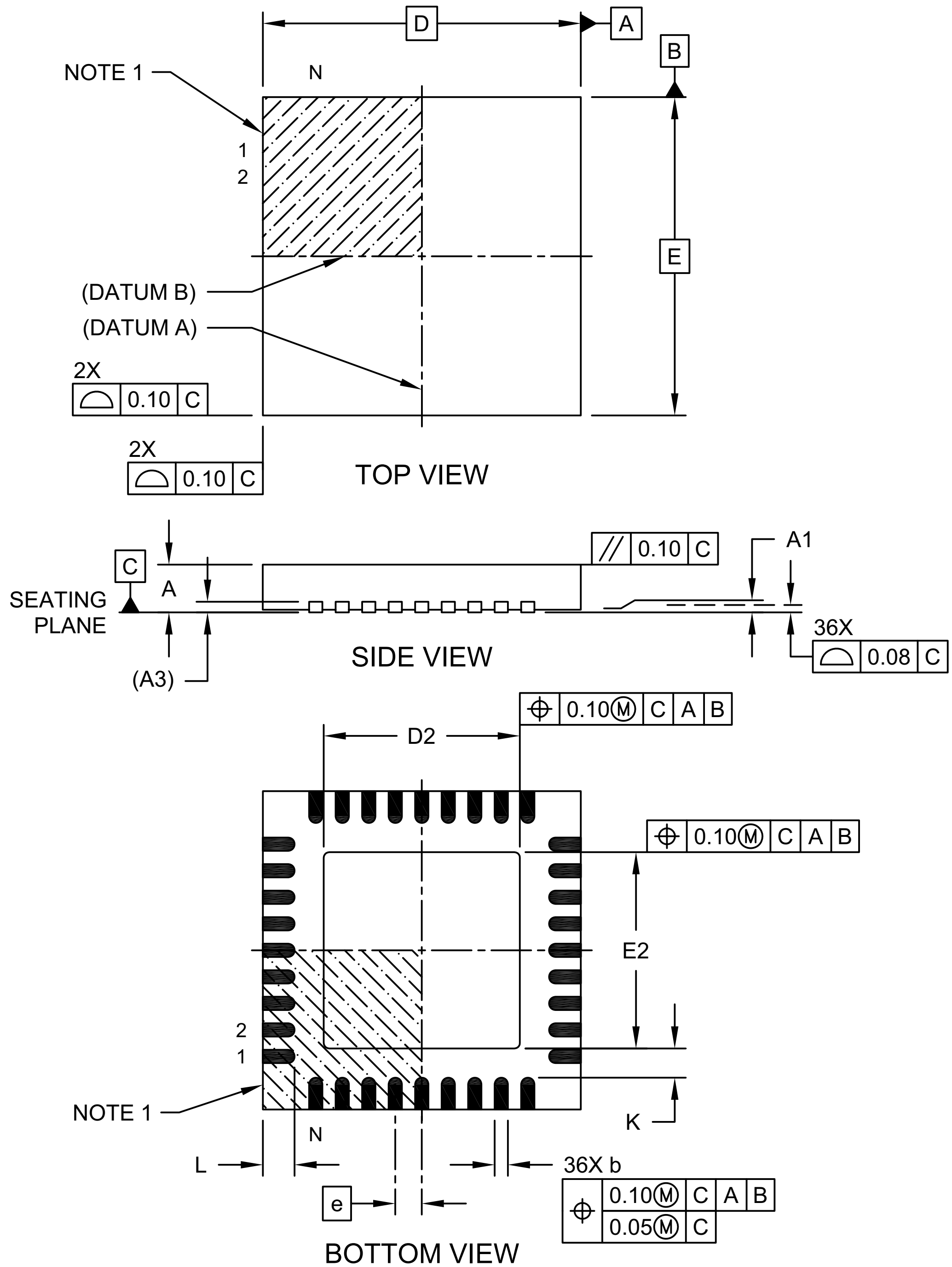
36-Terminal Very Thin Plastic Quad Flatpack No-Lead (M2) - 6x6x1.0mm Body [VQFN] SMSC Legacy "Sawn Quad Flatpack No-Lead [SQFN]"

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-272B-M2 Sheet 1 of 2

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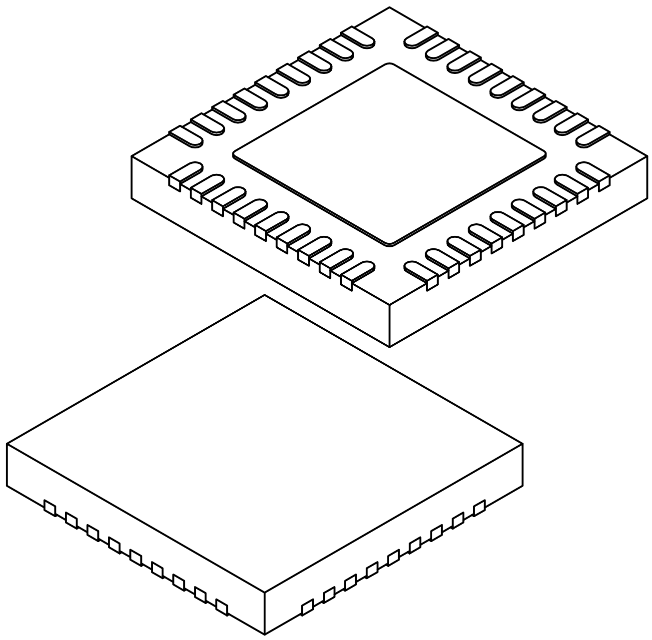
36-Terminal Very Thin Plastic Quad Flatpack No-Lead (M2) - 6x6x1.0mm Body [VQFN] SMSC Legacy "Sawn Quad Flatpack No-Lead [SQFN]"

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units	MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX
Number of Terminals	N		36	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.20 REF	
Overall Width	E		6.00 BSC	
Exposed Pad Width	E2	3.60	3.70	3.80
Overall Length	D		6.00 BSC	
Exposed Pad Length	D2	3.60	3.70	3.80
Terminal Width	b	0.18	0.25	0.30
Terminal Length	L	0.50	0.60	0.75
Terminal-to-Exposed-Pad	K	0.45	0.55	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-272B-M2 Sheet 2 of 2

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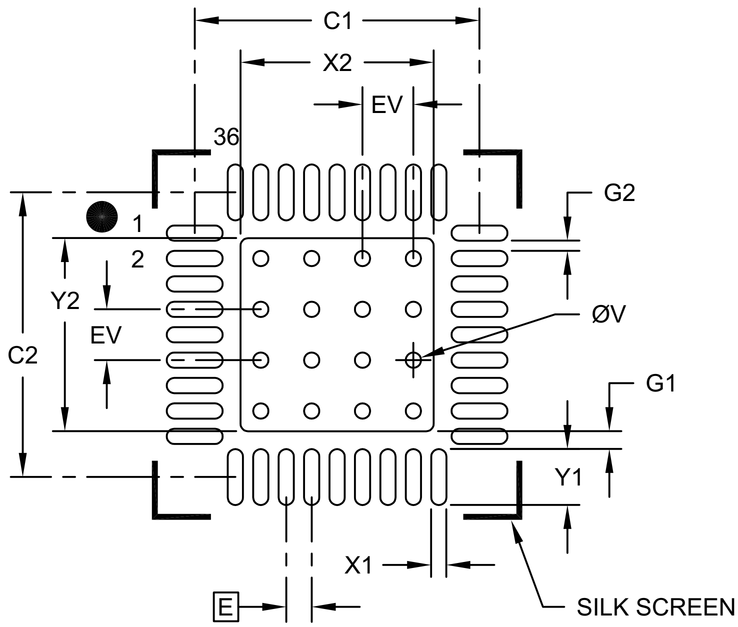
36-Terminal Very Thin Plastic Quad Flatpack No-Lead (M2) - 6x6x0.9 mm Body [VQFN] SMSC Legacy "Sawn Quad Flatpack No-Lead [SQFN]"

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

	Units	MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	X2			3.80
Optional Center Pad Length	Y2			3.80
Contact Pad Spacing	C1		5.60	
Contact Pad Spacing	C2		5.60	
Contact Pad Width (X36)	X1			0.30
Contact Pad Length (X36)	Y1			1.10
Contact Pad to Center Pad (X36)	G1	0.35		
Space Between Contact Pads (X32)	G2	0.20		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2272B-M2

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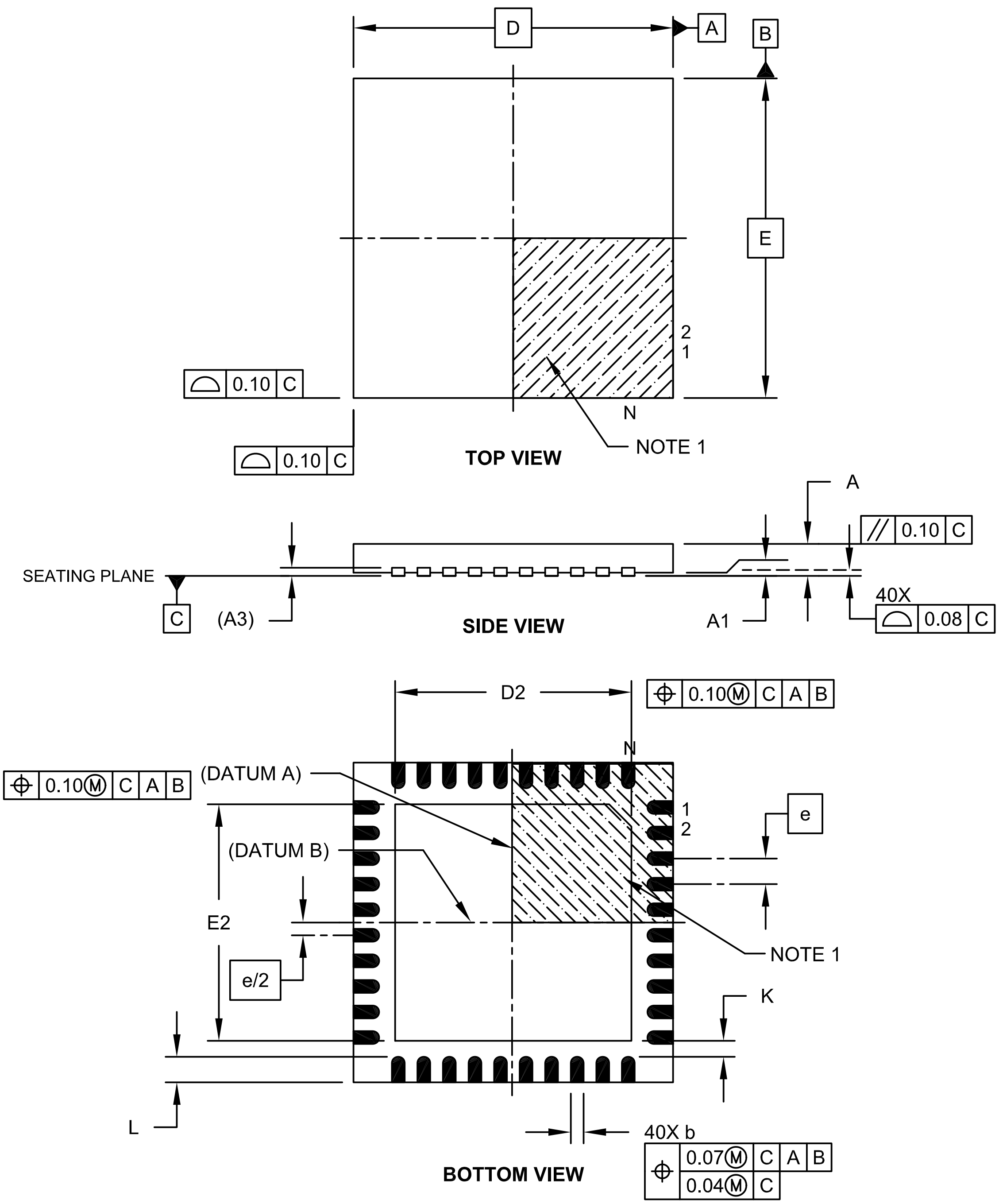
40-Lead Ultra Thin Plastic Quad Flat, No Lead Package (MV) – 5x5x0.5 mm Body [UQFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-156A Sheet 1 of 2

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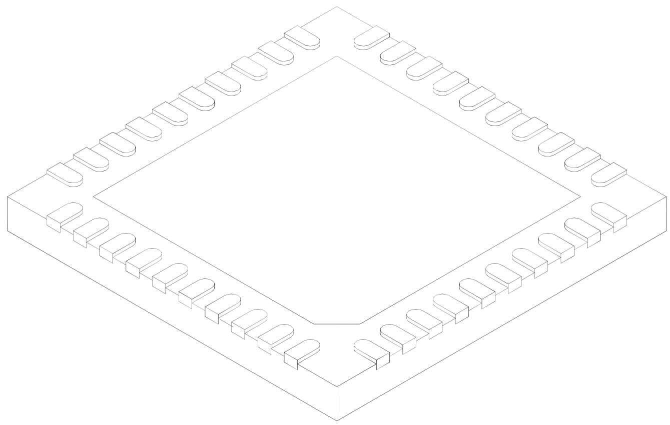
40-Lead Ultra Thin Plastic Quad Flat, No Lead Package (MV) – 5x5x0.5 mm Body [UQFN]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		40	
Pitch	e		0.40 BSC	
Overall Height	A	0.45	0.50	0.55
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.127 REF	
Overall Width	E		5.00 BSC	
Exposed Pad Width	E2	3.60	3.70	3.80
Overall Length	D		5.00 BSC	
Exposed Pad Length	D2	3.60	3.70	3.80
Contact Width	b	0.15	0.20	0.25
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-156A Sheet 2 of 2

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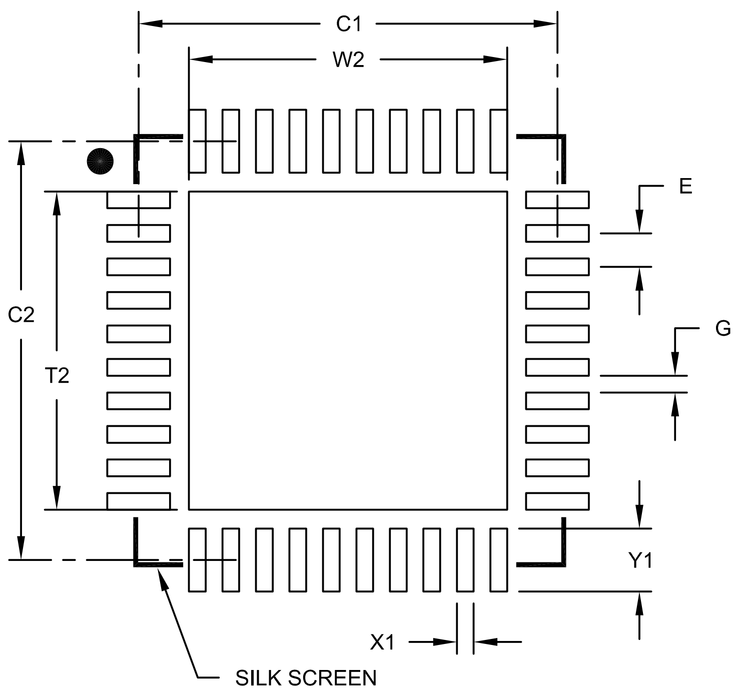
40-Lead Plastic Ultra Thin Quad Flat, No Lead Package (MV) - 5x5 mm Body [UQFN]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

	Units	MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.40 BSC		
Optional Center Pad Width	W2			3.80
Optional Center Pad Length	T2			3.80
Contact Pad Spacing	C1		5.00	
Contact Pad Spacing	C2		5.00	
Contact Pad Width (X40)	X1			0.20
Contact Pad Length (X40)	Y1			0.75
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2156B

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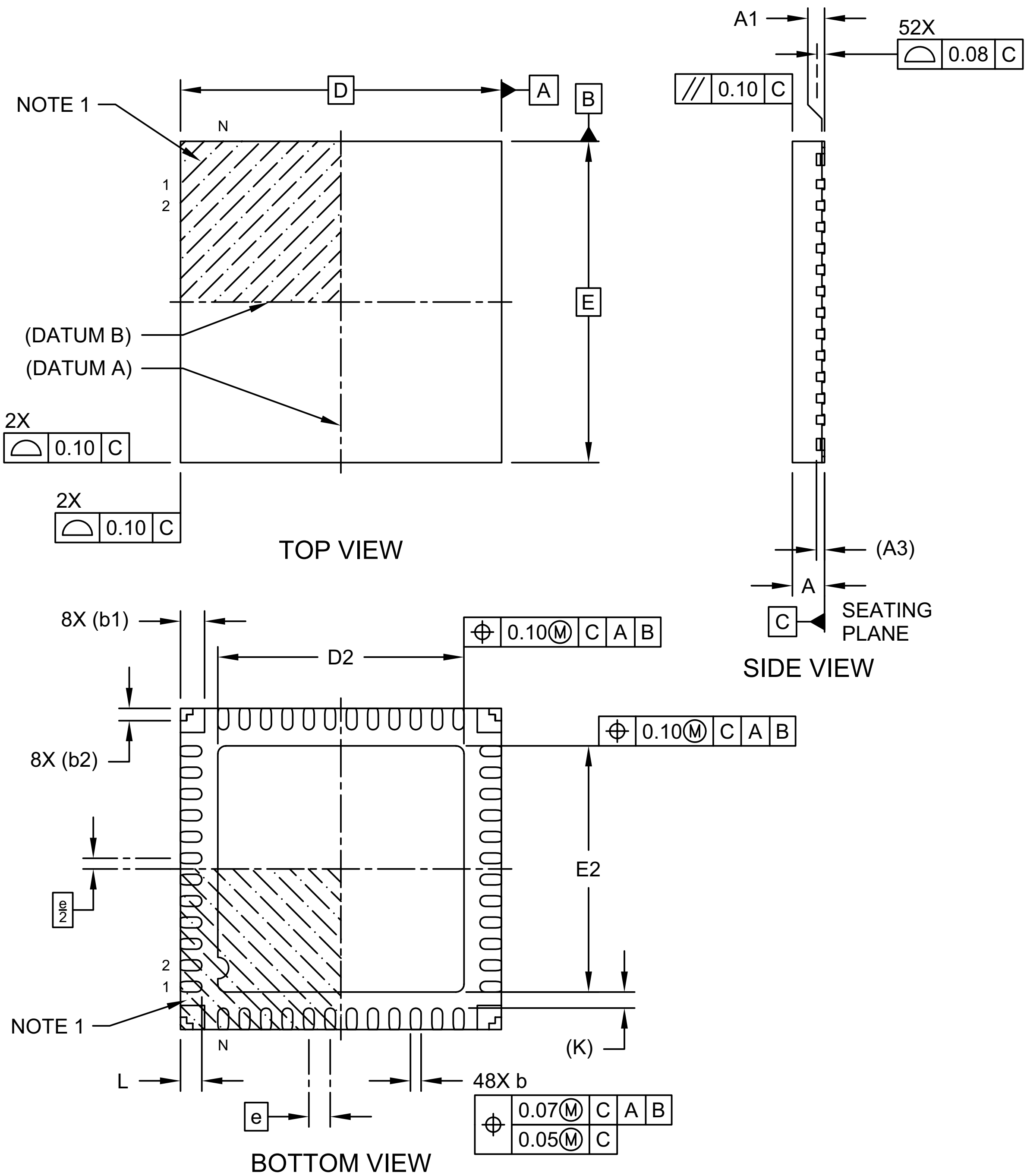
48-Lead Ultra Thin Plastic Quad Flat, No Lead Package (M4) - 6x6 mm Body [UQFN] With Corner Anchors and 4.6x4.6 mm Exposed Pad

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-442A-M4 Sheet 1 of 2

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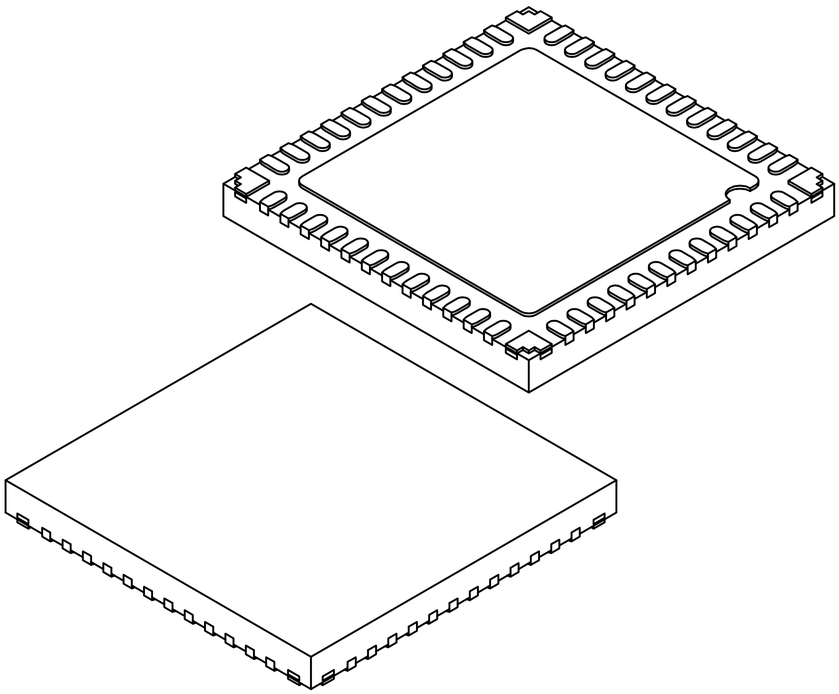
48-Lead Ultra Thin Plastic Quad Flat, No Lead Package (M4) - 6x6 mm Body [UQFN] With Corner Anchors and 4.6x4.6 mm Exposed Pad

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		48	
Pitch	e		0.40 BSC	
Overall Height	A	0.50	0.55	0.60
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.15 REF	
Overall Length	D		6.00 BSC	
Exposed Pad Length	D2	4.50	4.60	4.70
Overall Width	E		6.00 BSC	
Exposed Pad Width	E2	4.50	4.60	4.70
Terminal Width	b	0.15	0.20	0.25
Corner Anchor Pad	b1		0.45 REF	
Corner Anchor Pad, Metal-free Zone	b2		0.23 REF	
Terminal Length	L	0.35	0.40	0.45
Terminal-to-Exposed-Pad	K		0.30 REF	

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-442A-M4 Sheet 2 of 2

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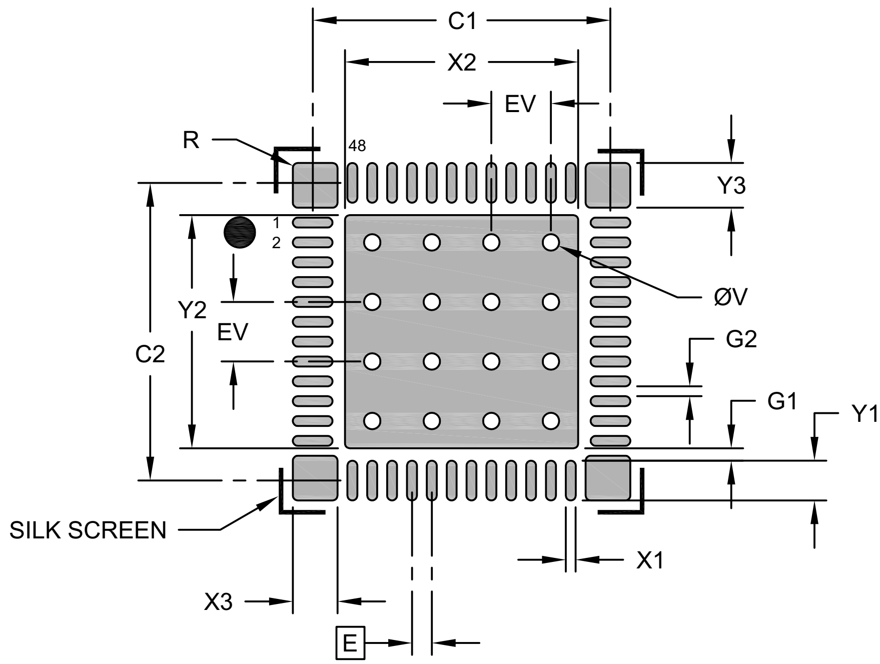
48-Lead Ultra Thin Plastic Quad Flat, No Lead Package (M4) - 6x6 mm Body [UQFN] With Corner Anchors and 4.6x4.6 mm Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.40 BSC	
Center Pad Width	X2			4.70
Center Pad Length	Y2			4.70
Contact Pad Spacing	C1		6.00	
Contact Pad Spacing	C2		6.00	
Contact Pad Width (X48)	X1			0.20
Contact Pad Length (X48)	Y1			0.80
Corner Anchor Pad Width (X4)	X3			0.90
Corner Anchor Pad Length (X4)	Y3			0.90
Pad Corner Radius (X 20)	R			0.10
Contact Pad to Center Pad (X48)	G1	0.25		
Contact Pad to Contact Pad	G2	0.20		
Thermal Via Diameter	V		0.33	
Thermal Via Pitch	EV		1.20	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2442A-M4

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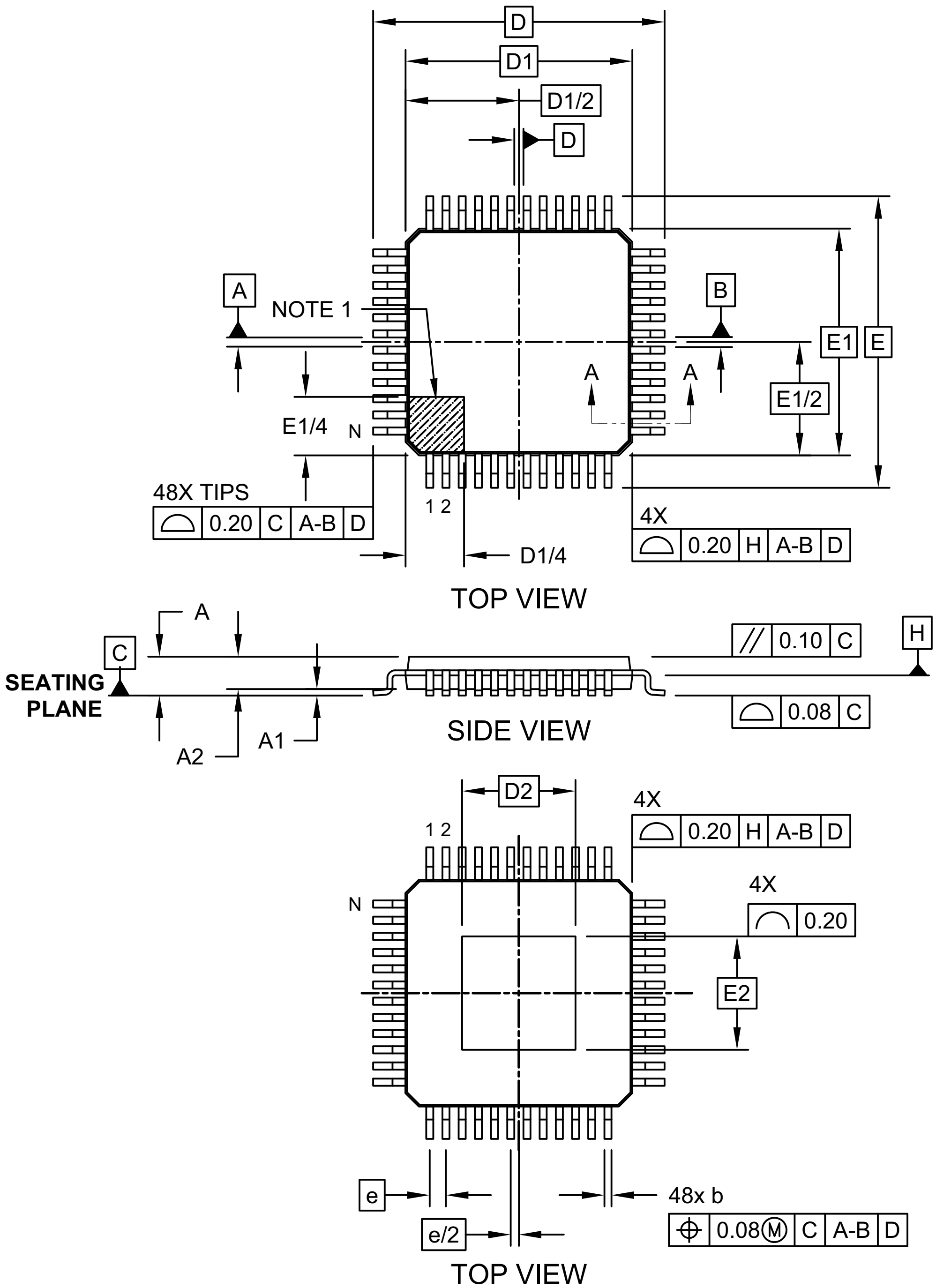
48-Lead Thin Quad Flatpack (PT) - 7x7x1.0 mm Body [TQFP] With Exposed Pad

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-183A Sheet 1 of 2

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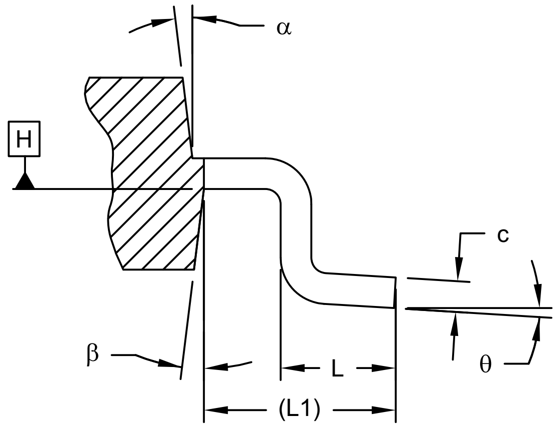
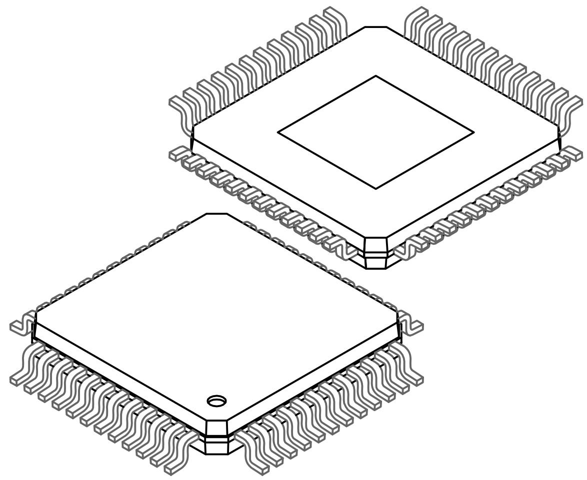
48-Lead Thin Quad Flatpack (PT) - 7x7x1.0 mm Body [TQFP] With Exposed Pad

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



SECTION A-A



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Leads	N		48	
Lead Pitch	e		0.50 BSC	
Overall Height	A	-	-	1.20
Standoff	A1	0.05	-	0.15
Molded Package Thickness	A2	0.95	1.00	1.05
Foot Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Foot Angle	φ	0°	3.5°	7°
Overall Width	E		9.00 BSC	
Overall Length	D		9.00 BSC	
Molded Package Width	E1		7.00 BSC	
Molded Package Length	D1		7.00 BSC	
Exposed Pad Width	E2		3.50 BSC	
Exposed Pad Length	D2		3.50 BSC	
Lead Thickness	c	0.09	-	0.16
Lead Width	b	0.17	0.22	0.27
Mold Draft Angle Top	α	11°	12°	13°
Mold Draft Angle Bottom	β	11°	12°	13°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Chamfers at corners are optional; size may vary.
3. Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-183A Sheet 2 of 2

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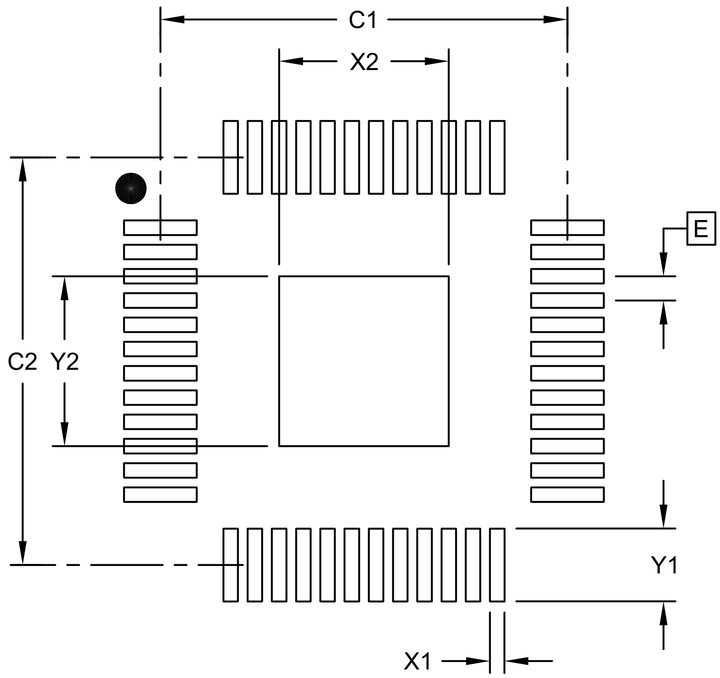
48-Lead Thin Quad Flatpack (PT) - 7x7x1.0 mm Body [TQFP] With Thermal Tab

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.50 BSC		
Optional Center Tab Width	X2		3.50	
Optional Center Tab Length	Y2		3.50	
Contact Pad Spacing	C1		8.40	
Contact Pad Spacing	C2		8.40	
Contact Pad Width (X48)	X1			0.30
Contact Pad Length (X48)	Y1			1.50

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2183A

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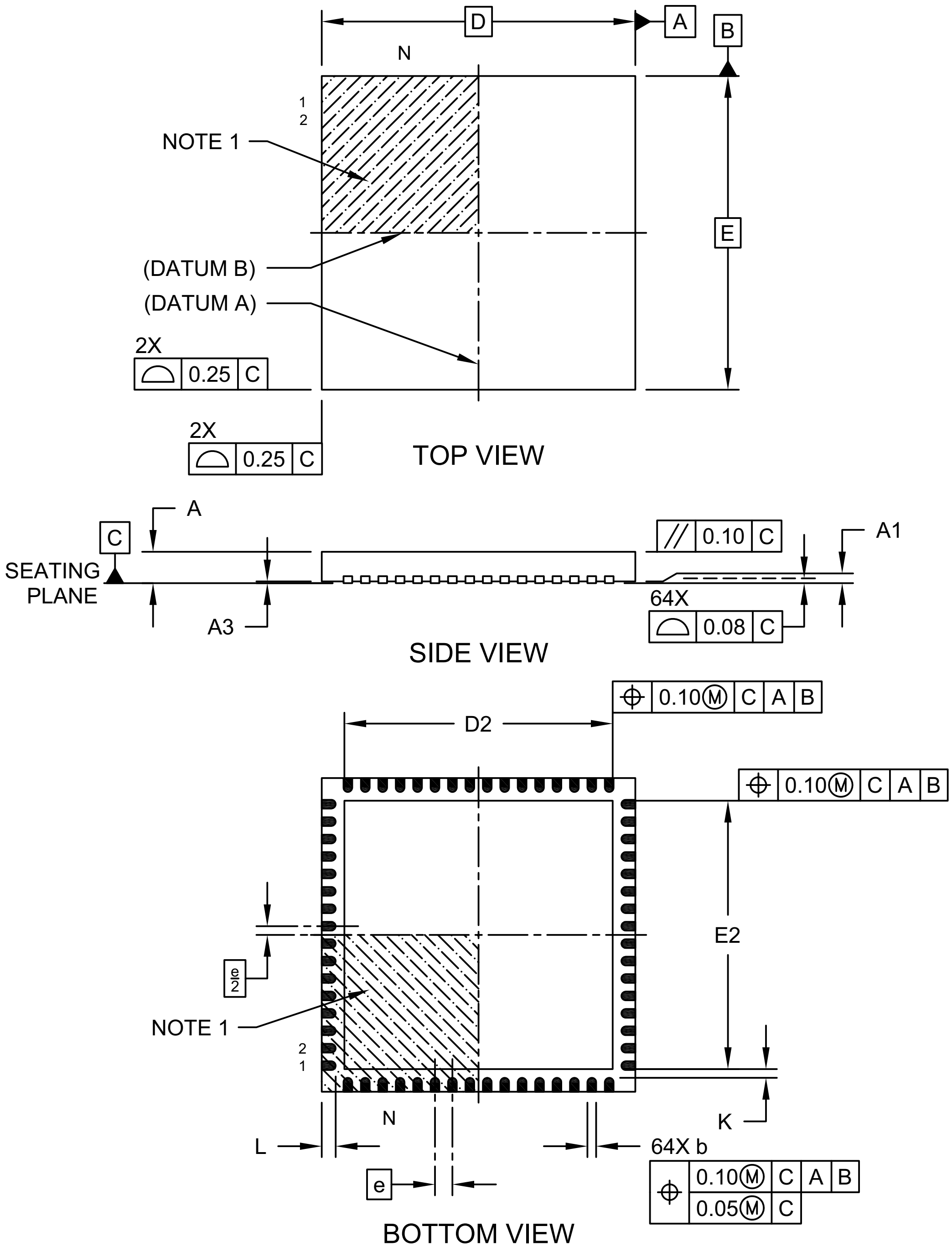
64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body [QFN]
With 7.70 x 7.70 Exposed Pad [QFN]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-213B Sheet 1 of 2

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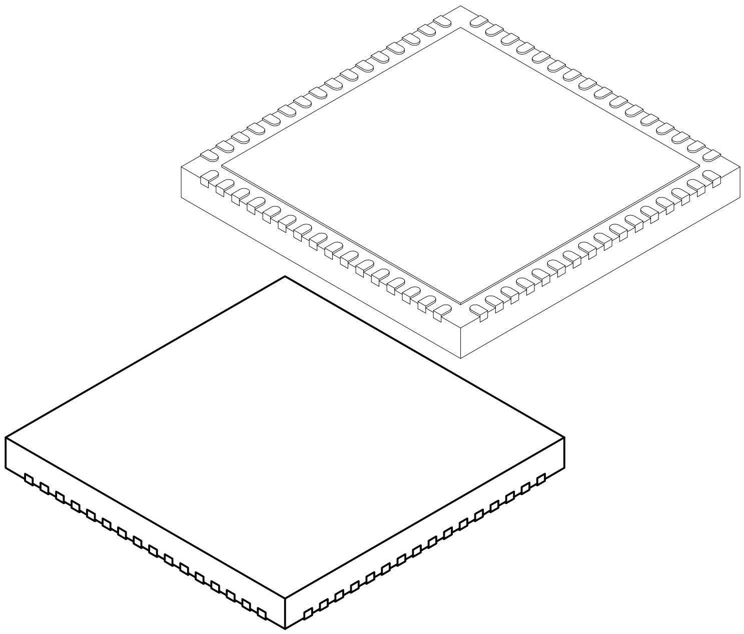
64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body [QFN] With 7.70 x 7.70 Exposed Pad [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		64	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.85	0.90
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Width	E		9.00 BSC	
Exposed Pad Width	E2	7.60	7.70	7.80
Overall Length	D		9.00 BSC	
Exposed Pad Length	D2	7.60	7.70	7.80
Contact Width	b	0.20	0.25	0.30
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	-	-

Notes:
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

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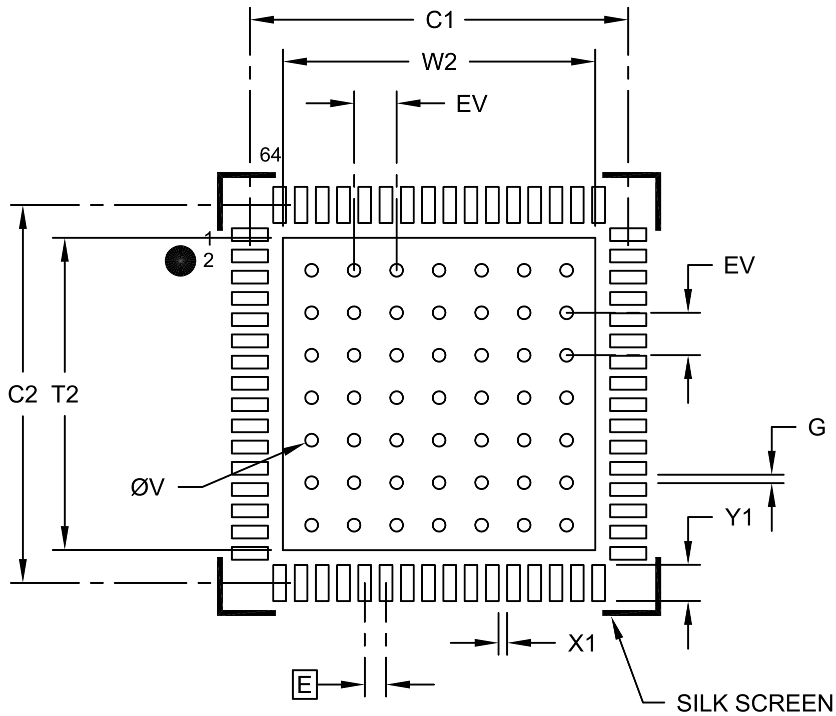
64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body [QFN]
With 0.40 mm Contact Length and 7.70x7.70mm Exposed Pad

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

	Units	MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	W2			7.50
Optional Center Pad Length	T2			7.50
Contact Pad Spacing	C1		8.90	
Contact Pad Spacing	C2		8.90	
Contact Pad Width (X20)	X1			0.30
Contact Pad Length (X20)	Y1			0.90
Contact Pad to Center Pad (X20)	G	0.20		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

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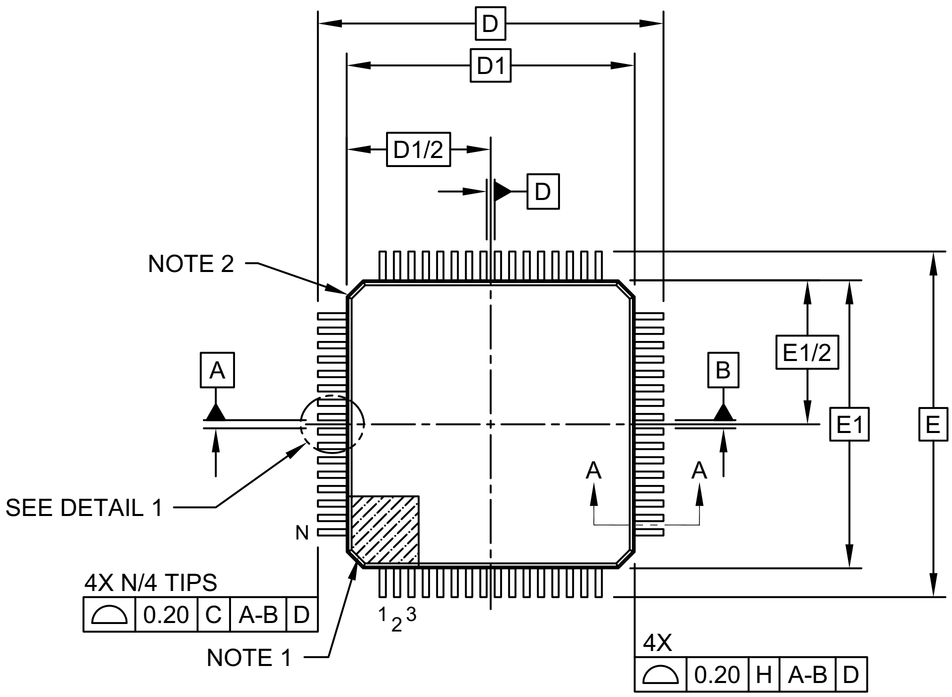
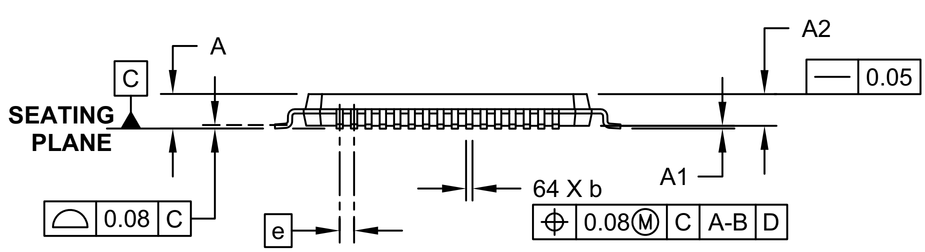
64-Lead Plastic Thin Quad Flatpack (PT)-10x10x1 mm Body, 2.00 mm Footprint [TQFP]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW

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64-Lead Plastic Thin Quad Flatpack (PT)-10x10x1 mm Body, 2.00 mm Footprint [TQFP]

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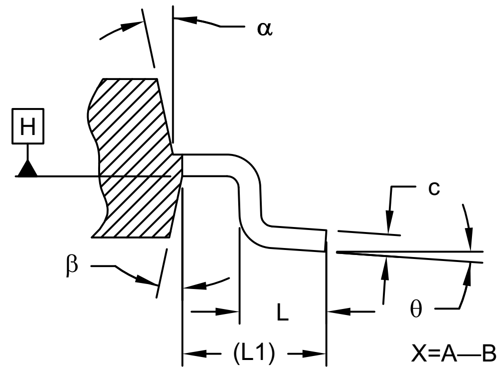
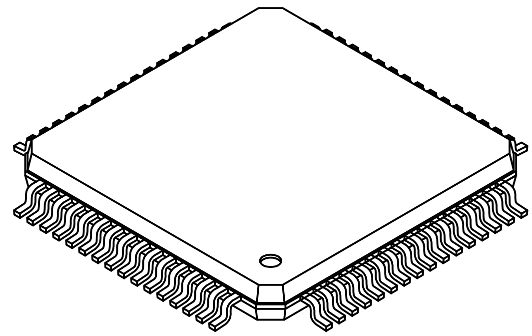
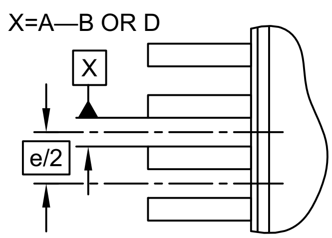


SECTION A-A





DETAIL 1

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Leads	N		64	
Lead Pitch	e		0.50 BSC	
Overall Height	A	-	-	1.20
Molded Package Thickness	A2	0.95	1.00	1.05
Standoff	A1	0.05	-	0.15
Foot Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Foot Angle	φ	0°	3.5°	7°
Overall Width	E		12.00 BSC	
Overall Length	D		12.00 BSC	
Molded Package Width	E1		10.00 BSC	
Molded Package Length	D1		10.00 BSC	
Lead Thickness	c	0.09	-	0.20
Lead Width	b	0.17	0.22	0.27
Mold Draft Angle Top	α	11°	12°	13°
Mold Draft Angle Bottom	β	11°	12°	13°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Chamfers at corners are optional; size may vary.
3. Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-085C Sheet 2 of 2

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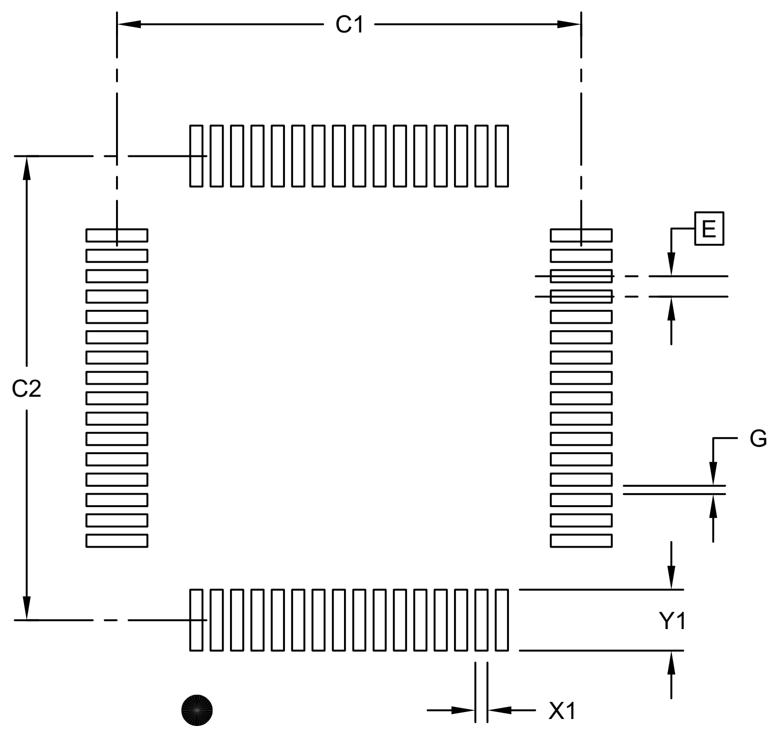
64-Lead Plastic Thin Quad Flatpack (PT)-10x10x1 mm Body, 2.00 mm Footprint [TQFP]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.50 BSC		
Contact Pad Spacing	C1		11.40	
Contact Pad Spacing	C2		11.40	
Contact Pad Width (X28)	X1			0.30
Contact Pad Length (X28)	Y1			1.50
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

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APPENDIX A: REVISION HISTORY

Revision A (January 2016)

This is the initial version of the document.

Revision B (March 2017)

This revision incorporates the following updates:

- Sections:
  - Updated the **"Low-Power Modes"**, **"Peripheral Features"**, **"Microcontroller Features"** and **"Analog Features"** sections.
  - Changed program row size to 128 32-bit words in **Section 5.0 "Flash Program Memory"**.
  - Updated **Section 4.2 "Bus Matrix (BMX)"**, **Section 8.0 "Direct Memory Access (DMA) Controller"**, **Section 9.0 "Oscillator Configuration"**, **Section 9.2 "Clock Switching Operation"**, **Section 9.3 "FRC Active Clock Tuning"**, **Section 10.1 "CLR, SET and INV Registers"**, **Section 10.5 "I/O Port Write/Read Timing"**, **Section 10.6 "GPIO Port Merging"**, **Section 20.1 "Introduction"**, **Section 26.5 "Band Gap Voltage Reference"** and **Section 26.7 "Unique Device Identifier (UDID)"**.
  - Added the 36-Lead VQFN (M2) and 48-Lead UQFN (M4) packaging diagrams to **Section 30.0 "Packaging Information"**.
- Tables:
  - Updated Table 1-1, Table 7-2, Table 7-3, Table 9-1, Table 10-5, Table 10-6, Table 10-7, Table 10-8, Table 20-1, Table 26-3, Table 26-4, Table 26-6, Table 26-8, Table 29-2, Table 29-3, Table 29-4, Table 29-5, Table 29-6, Table 29-7, Table 29-8, Table 29-11, Table 29-14, Table 29-20 and Table 29-21.
  - Replaced Table 29-34 with Table 29-34, Table 29-35 and Table 29-36.
  - Removed previously numbered Table 29-35.
- Examples:
  - Updated Example 9-1.
- Figures:
  - Updated Figure 1-1, Figure 8-1, Figure 9-1, Figure 9-2 and Figure 22-1.
  - Added Figure 9-2.
- Registers:
  - Updated Register 6-4, Register 9-1, Register 9-2, Register 9-3, Register 9-5, Register 14-1, Register 19-1, Register 19-2, Register 26-1,Register 26-5 and Register 26-10.
  - Removed Register 9-7.

Revision C (May 2017)

This revision incorporates the following updates:

- Sections:
  - Updated the **"Peripheral Features"** section.
  - Updated **Section 2.3 "Master Clear (MCLR) Pin"** and **Section 25.3 "Retention Sleep Mode"**.
- Tables:
  - Updated Table 29-4, Table 29-5, Table 29-6 and Table 29-7.
- Registers:
  - Updated Register 13-1.

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To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PIC32 MM XXXX GP M XXX T - XXX

- **Microchip Brand** — PIC32
- **Architecture** — MM
- **Flash Memory Size** — XXXX
- **Family** — GP
- **Key Feature Set** — M
- **Pin Count** — XXX
- **Tape and Reel Flag (if applicable)** — T
- **Pattern** — XXX

Architecture	MM	= MIPS32® microAptiv™ UC CPU Core
Flash Memory Size	0064 = 64 Kbytes 0128 = 128 Kbytes 0256 = 256 Kbytes	
Family	GP	= General Purpose Family
Key Feature	M	= Up to 25 MHz operating frequency with basic peripheral set of 3 UARTs, 3 SPIs, 3 I^2C modules and USB
Pin Count	028 036 048 064	= 28-pin = 36/40-pin = 48-pin = 64-pin
Pattern	Three-digit QTP, SQTP, Code or Special Requirements (blank otherwise) ES	 = Engineering Sample

Example:

PIC32MM0064GPM028-I/MV:
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