

MCP2517FD

External CAN FD Controller with SPI Interface

Features

<u>General</u>

- External CAN FD Controller with SPI Interface
- · Arbitration Bit Rate up to 1 Mbps
- · Data Bit Rate up to 8 Mbps
- · CAN FD Controller modes
 - Mixed CAN 2.0B and CAN FD mode
 CAN 2.0B mode
- Conforms to ISO 11898-1:2015

Message FIFOs

- 31 FIFOs, configurable as transmit or receive FIFOs
- One Transmit Queue (TXQ)
- · Transmit Event FIFO (TEF) with 32 bit time stamp

Message Transmission

- Message transmission prioritization:
 - Based on priority bit field, and/or
 - Message with lowest ID gets transmitted first using the Transmit Queue (TXQ)
- Programmable automatic retransmission attempts: unlimited, 3 attempts or disabled

Message Reception

- 32 Flexible Filter and Mask Objects
- Each object can be configured to filter either:
- Standard ID + first 18 data bits, or
- Extended ID
- 32-bit Time Stamp

Special Features

- VDD: 2.7 to 5.5V
- Active current: max. 20 mA at 5.5 V, 40 MHz CAN clock
- Sleep current: 10 µA, typical
- · Message objects are located in RAM: 2 KB
- Up to 3 configurable interrupt pins
- Bus Health Diagnostics and Error counters
- Transceiver standby control
- Start of frame pin for indicating the beginning of messages on the bus
- Temperature ranges:
- High (H): -40°C to +150°C

Oscillator Options

- 40, 20 or 4 MHz crystal, or ceramic resonator; or external clock input
- Clock output with prescaler

SPI Interface

- Up to 20 MHz SPI clock speed
- · Supports SPI modes 0,0 and 1,1
- Registers and bit fields are arranged in a way to enable efficient access via SPI

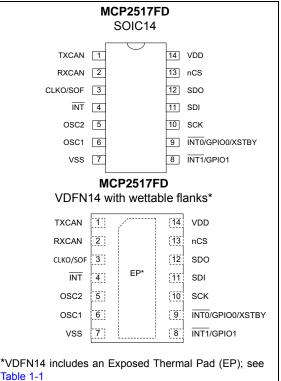
Safety Critical Systems

- SPI commands with CRC to detect noise on SPI interface
- Error Correction Code (ECC) protected RAM

Additional Features

- GPIO pins: INT0 and INT1 can be configured as general purpose I/O
- Open drain outputs: TXCAN, INT, INTO, and INT1 pins can be configured as push/pull or open drain outputs

Package Types



1.0 DEVICE OVERVIEW

The MCP2517FD is a cost-effective and small-footprint CAN FD controller that can be easily added to a microcontroller with an available SPI interface. Therefore, a CAN FD channel can be easily added to a microcontroller that is either lacking a CAN FD peripheral, or that doesn't have enough CAN FD channels.

The MCP2517FD supports both, CAN frames in the Classical format (CAN2.0B) and CAN Flexible Data Rate (CAN FD) format, as specified in ISO 11898-1:2015.

1.1 Block Diagram

Figure 1.1 shows the block diagram of the MCP2517FD. The MCP2517FD contains the following main blocks:

- The CAN FD Controller module implements the CAN FD protocol and contains the FIFOs, and Filters.
- The SPI interface is used to control the device by accessing SFRs and RAM.
- The RAM controller arbitrates the RAM accesses between the SPI and CAN FD Controller module.
- The Message RAM is used to store the data of the Message Objects.
- · The oscillator generates the CAN clock.
- The Internal LDO and POR circuit.
- The I/O control.

Note 1: This data sheet summarizes the features of the MCP2517FD. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the related section of the "MCP25xxFD Family Reference Manual".

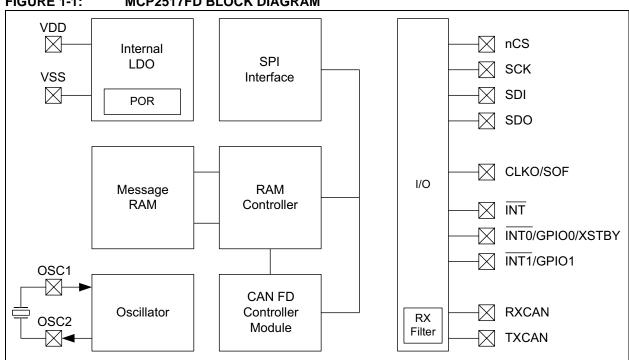


FIGURE 1-1: MCP2517FD BLOCK DIAGRAM

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1.2 Pin Out Description

Table 1-1 describes the functions of the pins.

TABLE 1-1: MCP2517FD STANDARD PINOUT VERSION

Pin Name	SOIC	VDFN	Pin Type	Description
TXCAN	1	1	0	Transmit output to CAN FD transceiver
RXCAN	2	2	I	Receive input from CAN FD transceiver
CLKO/SOF	3	3	0	Clock output/Start of Frame output
INT	4	4	0	Interrupt output (active low)
OSC2	5	5	0	External oscillator output
OSC1	6	6	I	External oscillator input
VSS	7	7	Р	Ground
INT1/GPIO1	8	8	I/O	RX Interrupt output (active low)/GPIO
INT0/GPIO0/ XSTBY	9	9	I/O	TX Interrupt output (active low)/GPIO/ Transceiver Standby output
SCK	10	10	I	SPI clock input
SDI	11	11	I	SPI data input
SDO	12	12	0	SPI data output
nCS	13	13	I	SPI chip select input
VDD	14	14	Р	Positive Supply
EP	-	15	Р	Exposed Pad; connect to VSS

Legend: P = Power, I = Input, O = Output

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1.3 Typical Application

Figure 1-2 shows an example of a typical application of the MCP2517FD. In this example, the microcontroller operates at 3.3V.

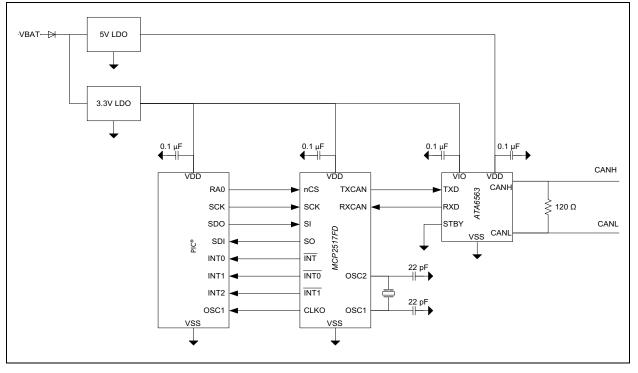
The MCP2517FD interfaces directly with microcontrollers operating at 2.7V to 5.5V. In addition, the MCP2517FD connects directly to high-speed CAN FD transceivers. There are no external level shifters required when connecting VDD of the MCP2517FD and the microcontroller to VIO of the transceiver. The VDD of the CAN FD transceiver is connected to 5V.

The SPI interface is used to configure and control the CAN FD controller.

The MCP2517FD signals interrupts to the microcontroller using INT, INTO and INT1. Interrupts need to be cleared by the microcontroller through SPI.

The CLKO pin provides the clock to the microcontroller.

FIGURE 1-2: MCP2517FD INTERFACING WITH A 3.3V MICROCONTROLLER



2.0 CAN FD CONTROLLER MODULE

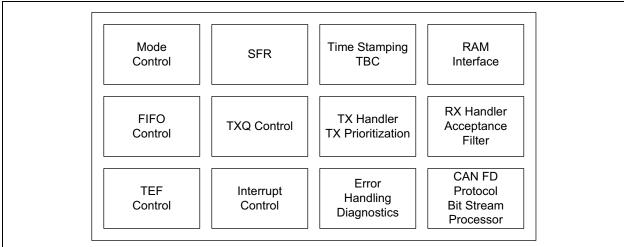
Figure 2-1 shows the main blocks of the CAN FD Controller module:

- The CAN FD Controller module has multiple modes:
 - Configuration
 - Normal CAN FD
 - Normal CAN 2.0
 - Sleep
 - Listen Only
 - Restricted Operation
 - Internal and External Loop back modes
- The CAN FD Bit Stream Processor (BSP) implements the Medium Access Control of the CAN FD protocol described in ISO 11898-1:2015. It serializes and de-serializes the bit stream, encodes and decodes the CAN FD frames, manages the medium access, acknowledges frames, and detects and signals errors.
- The TX Handler prioritizes the messages that are requested for transmission by the Transmit FIFOs. It uses the RAM Interface to fetch the transmit data from RAM and provides it to the BSP for transmission.
- The BSP provides received messages to the RX Handler. The RX Handler uses the Acceptance Filter to filter out messages that shall be stored into Receive FIFOs. It uses the RAM Interface to store received data into RAM.

- Each FIFO can be configured either as a Transmit or Receive FIFO. The FIFO Control keeps track of the FIFO Head and Tail, and calculates the User Address. For a TX FIFO, the User Address points to the address in RAM where the data for the next transmit message shall be stored. For a RX FIFO, the User Address points to the address in RAM where the data of the next receive message shall be read. The User notifies the FIFO that a message was written to or read from RAM by incrementing the Head/Tail of the FIFO.
- The Transmit Queue (TXQ) is a special transmit FIFO that transmits the messages based on the ID of the messages stored in the queue.
- The Transmit Event FIFO (TEF) stores the message IDs of the transmitted messages.
- A free-running Time Base Counter is used to time stamp received messages. Messages in the TEF can also be time stamped.
- The CAN FD Controller module generates interrupts when new messages are received or when messages were transmitted successfully.
- The Special Function Registers (SFR) are used to control and to read the status of the CAN FD Controller module.

Note 1: This data sheet summarizes the features of the CAN FD Controller module. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the related section of the "MCP25xxFD Family Reference Manual".

FIGURE 2-1: CAN FD CONTROLLER MODULE BLOCK DIAGRAM



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MCP2517FD

NOTES:

3.0 MEMORY ORGANIZATION

Figure 3-1 illustrates the main sections of the memory and its address ranges:

- MCP2517FD Special Function Registers (SFR)
- CAN FD Controller Module SFR
- Message Memory (RAM)

The SFR are 32 bit wide. The LSB is located at the lower address, e.g., the LSB of C1CON is located at address 0x000, while its MSB is located at address 0x003.

Table 3-1 lists the MCP2517FD specific registers. The first column contains the address of the SFR.

Table 3-2 lists the registers of the CAN FD Controller Module. The first column contains the address of the SFR.

FIGURE 3-1: MEMORY MAP

MSB Address	→ 32 bit	LSB Address
0x003	MSB LSB	0x000
	CAN FD Controller Module SFR (752 BYTE)	
0x2EF		0x2EC
0x2F3	Unimplemented (272 BYTE)	0x2F0
0x3FF 0x403		0x3FC 0x400
	RAM (2 KBYTE)	
0xBFF 0xC03		0xBFC 0xC00
0xDFF	(512 BYTE)	0xDFC
0xE03 0xE13	MCP2517FD SFR (20 BYTE)	0xE00
0xE13 0xE17	Reserved (492 BYTE)	0xE10 0xE14
0xFFF		0xFFC

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Address	Name		Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0		
E03	OSC	31:24				—	—	—	—	_		
E02		23:16	_	_	_	_	_	_	_			
E01		15:8	_	_	_	SCLKRDY	_	OSCRDY	—	PLLRDY		
E00 ⁽¹⁾		7:0		CLKOD	IV<1:0>	SCLKDIV	_	OSCDIS	—	PLLEN		
	IOCON	31:24	_	INTOD	SOF	TXCANOD	—	—	PM1	PM0		
		23:16	_	_	_	_	_	_	GPI01	GPIO0		
		15:8	_	_	_	—	_	_	LAT1	LAT0		
E04		7:0		XSTBYEN	-	_	_	_	TRIS1	TRIS0		
	CRC	31:24	_	_	_	_	_	_	FERRIE	CRCERRIE		
		23:16				—	_	_	FERRIF	CRCERRIF		
		15:8		CRC<15:8>								
E08		7:0				CRC	<7:0>					
	ECCCON	31:24	_			—			—			
		23:16	_	_	_	—	—	—	_	_		
		15:8	_				PARITY<6:0>					
E0C		7:0		-	_	_	_	DEDIE	SECIE	ECCEN		
	ECCSTAT	31:24	_	_	_	_		ERRADD)R<11:8>			
		23:16				ERRADI	DR<7:0>					
		15:8	_	—	—	—	_	_	—	_		
E10		7:0		-	_	_	_	DEDIF	SECIF	_		

TABLE 3-1: MCP2517FD REGISTER SUMMARY

Note 1: The lower order byte of the 32-bit register resides at the low-order address.

Addr.	Name		Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0			
03	C1CON	31:24		TXBWS	6<3:0>		ABAT		REQOP<2:0>				
02		23:16		OPMOD<2:0>	-	TXQEN	STEF	SERR2LOM	ESIGM	RTXAT			
01		15:8	_	—	_	BRSDIS	BUSY	WFT	<1:0>	WAKFIL			
00 ^[1]		7:0	_	PXEDIS	ISOCRCEN			DNCNT<4:0>					
	C1NBTCFG	31:24				BRP<	7:0>						
		23:16				TSEG1	<7:0>						
		15:8	—				TSEG2<6:0>						
04		7:0	—				SJW<6:0>						
	C1DBTCFG	31:24			BRP<7:0>								
		23:16	_	—	_		TSEG1<4:0>						
		15:8	_	—	_	_		TSEG	2<3:0>				
08		7:0		—	_	_		SJW	<3:0>				
	C1TDC	31:24	_	—	_	_	_	_	EDGFLTEN	SID11EN			
		23:16	_	_	—	—	—	_	TDCMO	D<1:0>			
		15:8	_				TDCO<6:0>						
0C		7:0	—	—			TDCV	/<5:0>					
	C1TBC	31:24 TBC<31:24>											
		23:16				TBC<2							
		15:8				TBC<	15:8>						
10		7:0			-	TBC<	7:0>	-					
	C1TSCON	31:24	—		—	—	—	—	—	—			
		23:16	_	_	_	_	_	TSRES	TSEOF	TBCEN			
		15:8	_	—	—	—	—	—	TBCPR	E<9:8>			
14		7:0	TBCPRE<7:0>										
	C1VEC	31:24	- RXCODE<6:0>										
		23:16				1	XCODE<6:0>						
		15:8	_	—	—			FILHIT<4:0>					
18		7:0					ICODE<6:0>						
	C1INT	31:24	IVMIE	WAKIE	CERRIE	SERRIE	RXOVIE	TXATIE	SPICRCIE	ECCIE			
		23:16		—	_	TEFIE	MODIE	TBCIE	RXIE	TXIE			
		15:8	IVMIF	WAKIF	CERRIF	SERRIF	RXOVIF	TXATIF	SPICRCIF	ECCIF			
1C		7:0		_	_	TEFIF	MODIF	TBCIF	RXIF	TXIF			
	C1RXIF	31:24				RFIF<3							
		23:16				RFIF<2							
20		15:8				RFIF<	15:8>						
20		7:0				RFIF<7:1>	4.045						
20	C1TXIF 31:24 TFIF<31:24>												
						TFIF<2							
		23:16											
24		15:8											
24		15:8 7:0				TFIF<	7:0>						
24	C1RXOVIF	15:8 7:0 31:24				TFIF< RFOVIF	:7:0> <31:24>						
24	C1RXOVIF	15:8 7:0 31:24 23:16				TFIF< RFOVIF RFOVIF	<pre>:7:0> <31:24> <23:16></pre>						
	C1RXOVIF	15:8 7:0 31:24 23:16 15:8				TFIF< RFOVIF RFOVIF RFOVIF	<pre>:7:0> <31:24> <23:16></pre>						
24 28		15:8 7:0 31:24 23:16 15:8 7:0				TFIF< RFOVIF RFOVIF RFOVIF RFOVIF<7:1>	7:0> <31:24> <23:16> <15:8>						
	C1RXOVIF	15:8 7:0 31:24 23:16 15:8 7:0 31:24				TFIF< RFOVIF RFOVIF RFOVIF RFOVIF<7:1> TFATIF<	7:0> <31:24> <23:16> <15:8> :31:24>			_			
		15:8 7:0 31:24 23:16 15:8 7:0				TFIF< RFOVIF RFOVIF RFOVIF RFOVIF<7:1>	7:0> <31:24> <23:16> <15:8> :31:24> :23:16>						

TABLE 3-2:	CAN FD CONTROLLER MODULE REGISTER SUMMARY

Note 1: The lower order byte of the 32-bit register resides at the low-order address.

Addr.	Name		Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0								
	C1TXREQ	31:24				TXREQ	<31:24>											
		23:16				TXREQ<	23:16>											
		15:8				TXREQ	<15:8>											
30		7:0	TXREQ<7:0>															
	C1TREC	31:24	_		_	_	_	_		_								
		23:16	—	_	TXBO	TXBP	RXBP	TXWARN	RXWARN	EWARN								
		15:8				TEC<	7:0>											
34		7:0		REC<7:0>														
	C1BDIAG0	31:24				DTERRC	NT<7:0>											
		23:16				DRERRC	NT<7:0>											
		15:8				NTERRC	NT<7:0>											
38		7:0				NRERRC	NT<7:0>											
	C1BDIAG1	31:24	DLCMM	ESI	DCRCERR	DSTUFERR	DFORMERR		DBIT1ERR	DBIT0ERR								
		23:16	TXBOERR	—	NCRCERR	NSTUFERR	NFORMERR	NACKERR	NBIT1ERR	NBIT0ERR								
		15:8		EFMSGCNT<15:8>														
3C		7:0				EFMSGC	NT<7:0>											
	C1TEFCON	31:24	—		—			FSIZE<4:0>	i	i								
		23:16	_		—	—	_	—	—	—								
		15:8	_	_	—	_	—	FRESET	—	UINC								
40		7:0	—	_	TEFTSEN	—	TEFOVIE	TEFFIE	TEFHIE	TEFNEIE								
	C1TEFSTA	31:24	—		_	_	_		—	—								
		23:16	_	_	_	_	_	_	_	_								
		15:8	_	_	_	_	_	_		_								
44		7:0	—	_	_	_	TEFOVIF	TEFFIF	TEFHIF	TEFNEIF								
	C1TEFUA	31:24				TEFUA<												
		23:16	TEFUA<23:16>															
		15:8	TEFUA<15:8>															
48		7:0				TEFUA												
	Reserved ⁽²⁾	31:24				Reserved												
		23:16				Reserved												
		15:8				Reserved												
4C		7:0				Reserve	d<7:0>											
	C1TXQCON	31:24		PLSIZE<2:0>				FSIZE<4:0>										
		23:16	_	TXAT	<1:0>			TXPRI<4:0>	TVD50									
		15:8	-		—	-	—	FRESET	TXREQ	UINC								
50		7:0	TXEN		—	TXATIE	—	TXQEIE	—	TXQNIE								
	C1TXQSTA	31:24	—		—	—	—		—	—								
		23:16	—		—	—	—		—	—								
F 4		15:8	— 		-	TVATIC		TXQCI<4:0>		TVONIE								
54	0473/0111	7:0	TXABT	TXLARB	TXERR	TXATIF		TXQEIF	—	TXQNIF								
	C1TXQUA																	
		23:16				TXQUA												
		15:8				TXQUA												
58		7:0				TXQUA	:0			7:0 TXQUA<7:0>								

TABLE 3-2: CAN FD CONTROLLER MODULE REGISTER SUMMARY (CONTINUED)

Note 1: The lower order byte of the 32-bit register resides at the low-order address.

Addr.	Name		Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
	C1FIFOCON1	31:24		PLSIZE<2:0>				FSIZE<4:0>		
		23:16	—	TXAT	<1:0>			TXPRI<4:0>		
		15:8	—	_	—	—	_	FRESET	TXREQ	UINC
5C		7:0	TXEN	RTREN	RXTSEN	TXATIE	RXOVIE	TFERFFIE	TFHRFHIE	TFNRFNIE
	C1FIFOSTA1	31:24	—	—	_	_	_	_	_	_
		23:16		—	—	—	-	_	—	_
		15:8	_	—	—			FIFOCI<4:0>		
60		7:0	TXABT	TXLARB	TXERR	TXATIF	RXOVIF	TFERFFIF	TFHRFHIF	TFNRFNI
	C1FIFOUA1	31:24				FIFOUA<	<31:24>			
	23:16 FIFOUA<23:16>									
		15:8				FIFOUA	<15:8>			
64		7:0				FIFOUA	<7:0>			
68	C1FIFOCON2	31:0				same as C1I	FIFOCON1			
6C	C1FIFOSTA2	31:0				same as C1	FIFOSTA1			
70	C1FIFOUA2	31:0				same as C1	IFIFOUA1			
74	C1FIFOCON3	31:0				same as C1I				
78	C1FIFOSTA3	31:0				same as C1				
7C	C1FIFOUA3	31:0				same as C1				
80	C1FIFOCON4	31:0				same as C1				
84	C1FIFOSTA4	31:0				same as C1				
88	C1FIFOUA4	31:0				same as C1				
8C	C1FIFOCON5	31:0				same as C1I				
90	C1FIFOCON5	31:0				same as C1				
90		31:0				same as C1				
94	C1FIFOUA5									
	C1FIFOCON6	31:0				same as C1				
9C	C1FIFOSTA6	31:0				same as C1				
A0	C1FIFOUA6	31:0				same as C1				
A4	C1FIFOCON7	31:0				same as C1				
A8	C1FIFOSTA7	31:0				same as C1				
AC	C1FIFOUA7	31:0				same as C1				
B0	C1FIFOCON8	31:0				same as C1				
B4	C1FIFOSTA8	31:0				same as C1				
B8	C1FIFOUA8	31:0				same as C1				
BC	C1FIFOCON9	31:0	<u> </u>			same as C1				
C0	C1FIFOSTA9	31:0				same as C1				
C4	C1FIFOUA9	31:0	<u> </u>			same as C1				
C8	C1FIFOCON10					same as C1				
CC	C1FIFOSTA10	31:0				same as C1				
D0	C1FIFOUA10	31:0	<u> </u>			same as C1				
D4	C1FIFOCON11	31:0	ļ			same as C1				
D8	C1FIFOSTA11	31:0				same as C1				
DC	C1FIFOUA11	31:0				same as C1				
E0	C1FIFOCON12	31:0				same as C1	FIFOCON1			
E4	C1FIFOSTA12	31:0				same as C1	FIFOSTA1			
E8	C1FIFOUA12	31:0				same as C1				
EC	C1FIFOCON13	31:0				same as C1	FIFOCON1			
F0	C1FIFOSTA13	31:0				same as C1	FIFOSTA1			
F4	C1FIFOUA13	31:0				same as C1	IFIFOUA1			
F8	C1FIFOCON14	31:0				same as C1	FIFOCON1			
FC	C1FIFOSTA14	31:0				same as C1	FIFOSTA1			
100	C1FIFOUA14	31:0				same as C1	IFIFOUA1			

Note 1: The lower order byte of the 32-bit register resides at the low-order address.

104 C1FIF0CON15 31.0 same as C1FIF0CON1 108 C1FIF0ZIA15 31.0 same as C1FIF0CON1 110 C1FIF0ZIA15 31.0 same as C1FIF0CON1 111 C1FIF0ZIA15 31.0 same as C1FIF0ZIA1 112 C1FIF0ZIA16 31.0 same as C1FIF0ZIA1 113 C1FIF0ZIA15 31.0 same as C1FIF0ZIA1 114 C1FIF0ZIA15 31.0 same as C1FIF0ZIA1 112 C1FIF0ZIA17 31.0 same as C1FIF0ZIA1 112 C1FIF0ZIA15 31.0 same as C1FIF0ZIA1 112 C1FIF0ZIA15 31.0 same as C1FIF0ZIA1 113 C1FIF0ZIA12 31.0 same as C1FIF0ZIA1 114 C1FIF0ZIA25 31.0 same as C1FIF0ZIA1	TABL	BLE 3-2: CAN FD CONTROLLER MODULE REGISTER SUMMARY (CONTINUED)												
198 CIFIFOSTAIS 310 same as CIFIFOUAT 10C CIFIFOUATS 310 same as CIFIFOUAT 11C CIFIFOCONIC 310 same as CIFIFOCONI 111C CIFIFOUATS 310 same as CIFIFOCONI 112C CIFIFOSTAT 310 same as CIFIFOCONI 112C CIFIFOSTAT 310 same as CIFIFOCONI 122 CIFIFOSTAT 310 same as CIFIFOCONI 122 CIFIFOSTAT 310 same as CIFIFOCONI 122 CIFIFOCONI 310 same as CIFIFOCONI 133 CIFIFOSTAT 310 same as CIFIFOCONI 134 CIFIFOSTAT 310 same as CIFIFOCONI 135 CIFIFOSTAT 310 same as CIFIFOCONI 136 CIFIFOSTAT 310 same as CIFIFOCONI 137 CIFIFOSTAT 310 same as CIFIFOCONI 138 CIFIFOSTAT 310 same as CIFIFOCONI 144 CIFIFOCON2 310 same as CIFIFOCONI 144 <td< th=""><th>Addr.</th><th>Name</th><th></th><th></th><th></th><th></th><th></th><th></th><th></th><th></th><th>Bit 24/16/8/0</th></td<>	Addr.	Name									Bit 24/16/8/0			
100 CIFIFOUA15 310 same as CIFIFOUA1 110 CIFIFORMA 31.0 same as CIFIFOUA1 111 CIFIFOUA16 31.0 same as CIFIFOUA1 112 CIFIFOUA16 31.0 same as CIFIFOUA1 116 CIFIFOUA17 31.0 same as CIFIFOUA1 112 CIFIFOUA17 31.0 same as CIFIFOUA1 112 CIFIFOUA17 31.0 same as CIFIFOUA1 112 CIFIFOUA18 31.0 same as CIFIFOUA1 112 CIFIFOUA18 31.0 same as CIFIFOUA1 113 CIFIFOUA18 31.0 same as CIFIFOUA1 113 CIFIFOUA18 31.0 same as CIFIFOUA1 114 CIFIFOUA20 31.0 same as CIFIFOUA1 114 CIFIFOUA20 31.0 same as CIFIFOUA1 114 CIFIFOUA20 31.0 same as CIFIFOUA1 114 CIFIFOUA21 31.0 same as CIFIFOUA1 114 CIFIFOUA21 31.0 same as CIFIFOUA1 115 CIFI	104	C1FIFOCON15	31:0				same as C1	FIFOCON1						
110 CTFFOCONIE 310 same as CTFFOCONI 114 CTFFOCATIE 31.0 same as CTFFOCONI 116 CTFFOCATIE 31.0 same as CTFFOCONI 117 CTFFOCATIE 31.0 same as CTFFOCONI 118 CTFFOCATIE 31.0 same as CTFFOCONI 110 CTFFOCATIE 31.0 same as CTFFOCONI 118 CTFFOCATIE 31.0 same as CTFFOCONI 118 CTFFOCATIE 31.0 same as CTFFOCONI 118 CTFFOCATIE 31.0 same as CTFFOCONI 119 CTFFOCATIE 31.0 same as CTFFOCONI 114 CTF	108	C1FIFOSTA15	31:0				same as C1	FIFOSTA1						
118 CIFIFOSTAIE 310 same as CIFIFOUAT 118 CIFIFOUATE 310 same as CIFIFOUAT 110 CIFIFOCONT7 310 same as CIFIFOUAT 120 CIFIFOUATT 310 same as CIFIFOUAT 121 CIFIFOUATT 310 same as CIFIFOUAT 122 CIFIFOUATE 310 same as CIFIFOUAT 123 CIFIFOUATE 310 same as CIFIFOUAT 124 CIFIFOUATE 310 same as CIFIFOUAT 125 CIFIFOUATE 310 same as CIFIFOUAT 132 CIFIFOUATE 310 same as CIFIFOUAT 133 CIFIFOUATE 310 same as CIFIFOUAT 144 CIFIFOUATE 310 same as CIFIFOUAT 145 CIFIFOUATE 310 same as CIFIFOUAT 146 CIFIFOUATE 310 same as CIFIFOUAT 146 CIFIFOUATE 310 same as CIFIFOUAT 146 CIFIFOUATE 310 same as CIFIFOUAT 145 CIFIFOUATE	10C	C1FIFOUA15	31:0				same as C	1FIFOUA1						
118 CIFFOUNT 310 same as CIFFOUNT 110 CIFFOCONIT 310 same as CIFFOUNT 124 CIFFOUNT 310 same as CIFFOUNT 128 CIFFOUNT 310 same as CIFFOUNT 129 CIFFOUNT 310 same as CIFFOUNT 120 CIFFOUNT 310 same as CIFFOUNT 121 CIFFOUNT 310 same as CIFFOUNT 122 CIFFOUNT 310 same as CIFFOUNT 130 CIFFOUNT 310 same as CIFFOUNT 131 CIFFOUNT 310 same as CIFFOUNT 132 CIFFOUNT 310 same as CIFFOUNT 134 CIFFOUNT 310 same as CIFFOUNT 144 CIFFOUNT 310 same as CIFFOUNT 145 CIFFOUNT 310 same as CIFFOUNT 146 CIFFOUNT 310 same as CIFFOUNT 146 CIFFOUNT 310 same as CIFFOUNT 150 CIFFOCONZ 310 same as CIFFOUNT	110	C1FIFOCON16	31:0		same as C1FIFOCON1									
11C C1FIFOSCN17 31.0 same as C1FIFOSCN1 120 C1FIFOSTAT 31.0 same as C1FIFOCN1 121 C1FIFOCN18 31.0 same as C1FIFOCN1 122 C1FIFOCN18 31.0 same as C1FIFOCN1 123 C1FIFOCN18 31.0 same as C1FIFOCN1 124 C1FIFOCN19 31.0 same as C1FIFOCN1 134 C1FIFOCN19 31.0 same as C1FIFOCN1 135 C1FIFOCN19 31.0 same as C1FIFOCN1 136 C1FIFOCN12 31.0 same as C1FIFOCN1 136 C1FIFOCN201 31.0 same as C1FIFOCN1 146 C1FIFOCN21 31.0 same as C1FIFOCN1 146 C1FIFOCN21 31.0 same as C1FIFOCN1 156 C1FIFOCN22 31.0 same as C1FIFOCN1 156 <td< td=""><td>114</td><td>C1FIFOSTA16</td><td>31:0</td><td></td><td colspan="10">same as C1FIFOSTA1</td></td<>	114	C1FIFOSTA16	31:0		same as C1FIFOSTA1									
120 C1FIFOSTA17 310 same as C1FIFOUA1 124 C1FIFOUA17 310 same as C1FIFOCON1 125 C1FIFOCON18 310 same as C1FIFOCON1 126 C1FIFOCON19 310 same as C1FIFOCON1 130 C1FIFOCON19 310 same as C1FIFOCON1 131 C1FIFOCON19 310 same as C1FIFOCON1 132 C1FIFOCON19 310 same as C1FIFOCON1 133 C1FIFOCON20 310 same as C1FIFOCON1 136 C1FIFOCON20 310 same as C1FIFOCON1 140 C1FIFOCON20 310 same as C1FIFOCON1 144 C1FIFOCON21 310 same as C1FIFOCON1 150 C1FIFOCON21 310 same as C1FIFOCON1 151 C1FIFOCON22 310 same as C1FIFOCON1 152 C1FIFOCON23 310 same as C1FIFOCON1 154 C1FIFOCON23 310 same as C1FIFOCON1 156 C1FIFOCON23 310 same as C1FIFOCON1 156	118	C1FIFOUA16	31:0				same as C	1FIFOUA1						
124 CIFIFOUA17 310 same as CIFIFOCON1 126 CIFIFOCON18 310 same as CIFIFOSTA1 130 CIFIFOCON19 310 same as CIFIFOSTA1 131 CIFIFOCON19 310 same as CIFIFOSTA1 132 CIFIFOCON19 310 same as CIFIFOCON1 133 CIFIFOCON19 310 same as CIFIFOCON1 134 CIFIFOCON20 310 same as CIFIFOCON1 140 CIFIFOCON20 310 same as CIFIFOCON1 140 CIFIFOCON21 310 same as CIFIFOCON1 144 CIFIFOCON21 310 same as CIFIFOCON1 150 CIFIFOCON21 310 same as CIFIFOCON1 150 CIFIFOCON22 310 same as CIFIFOCON1 150 CIFIFOCON23 310 same as CIFIFOCON1 150 CIFIFOCON23 310 same as CIFIFOCON1 150 CIFIFOCON23 310 same as CIFIFOCON1 151 CIFIFOCON23 310 same as CIFIFOCON1 156	11C	C1FIFOCON17	31:0				same as C1	FIFOCON1						
128 CIFIFOCON18 31.0 same as CIFIFOCON1 120 CIFIFOSTA1 31.0 same as CIFIFOUA1 134 CIFIFOQA18 31.0 same as CIFIFOUA1 134 CIFIFOQA18 31.0 same as CIFIFOUA1 136 CIFIFOQA19 31.0 same as CIFIFOUA1 136 CIFIFOQA19 31.0 same as CIFIFOUA1 140 CIFIFOQA19 31.0 same as CIFIFOUA1 144 CIFIFOUA19 31.0 same as CIFIFOUA1 144 CIFIFOUA20 31.0 same as CIFIFOUA1 146 CIFIFOUA21 31.0 same as CIFIFOUA1 156 CIFIFOUA21 31.0 same as CIFIFOUA1 156 CIFIFOUA21 31.0 same as CIFIFOUA1 156 CIFIFOUA23 31.0 same as CIFIFOUA1 156	120	C1FIFOSTA17	31:0				same as C1	FIFOSTA1						
12C C1FIFOSTA18 310 same as C1FIFOSTA1 130 C1FIFOQA18 31.0 same as C1FIFOCON1 134 C1FIFOQA19 31.0 same as C1FIFOCON1 138 C1FIFOSTA19 31.0 same as C1FIFOCON1 138 C1FIFOCON2 31.0 same as C1FIFOCON1 136 C1FIFOCON2 31.0 same as C1FIFOCON1 137 C1FIFOSTA2 31.0 same as C1FIFOCON1 144 C1FIFOCON2 31.0 same as C1FIFOCON1 144 C1FIFOCON21 31.0 same as C1FIFOCON1 150 C1FIFOCN22 31.0 same as C1FIFOCON1 150 C1FIFOCN22 31.0 same as C1FIFOCON1 150 C1FIFOCN22 31.0 same as C1FIFOCN1 150 C1FIFOCN23 31.0 same as C1FIFOCN1 151 C1FIFOCN23 31.0 same as C1FIFOCN1 152 C1FIFOCN23 31.0 same as C1FIFOCN1 156 C1FIFOCN23 31.0 same as C1FIFOCN1 156	124	C1FIFOUA17	31:0				same as C	1FIFOUA1						
130 C1FIFOUA18 31:0 same as C1FIFOUA1 134 C1FIFOCON19 31:0 same as C1FIFOSTA1 136 C1FIFOCAN19 31:0 same as C1FIFOSTA1 136 C1FIFOCAN29 31:0 same as C1FIFOSTA1 136 C1FIFOCAN29 31:0 same as C1FIFOSTA1 141 C1FIFOSTA20 31:0 same as C1FIFOSTA1 142 C1FIFOSTA21 31:0 same as C1FIFOSTA1 144 C1FIFOSTA21 31:0 same as C1FIFOSTA1 145 C1FIFOSTA21 31:0 same as C1FIFOSTA1 154 C1FIFOSTA22 31:0 same as C1FIFOSTA1 156 C1FIFOSTA22 31:0 same as C1FIFOSTA1 156 C1FIFOSTA23 31:0 same as C1FIFOSTA1 156 C1FIFOSTA23 31:0 same as C1FIFOSTA1 156 C1FIFOSTA23 31:0 same as C1FIFOSTA1 157 C1FIFOSTA23 31:0 same as C1FIFOSTA1 158 C1FIFOSTA23 31:0 same as C1FIFOSTA1	128	C1FIFOCON18	31:0				same as C1	FIFOCON1						
134 C1FIFOCON19 31.0 same as C1FIFOCON1 138 C1FIFOQIA19 31.0 same as C1FIFOQIA1 140 C1FIFOQIA19 31.0 same as C1FIFOQIA1 140 C1FIFOQIA20 31.0 same as C1FIFOQIA1 144 C1FIFOQIA20 31.0 same as C1FIFOQIA1 144 C1FIFOQIA20 31.0 same as C1FIFOQIA1 144 C1FIFOQIA21 31.0 same as C1FIFOQIA1 146 C1FIFOQIA21 31.0 same as C1FIFOQIA1 156 C1FIFOQIA21 31.0 same as C1FIFOQIA1 156 C1FIFOQIA21 31.0 same as C1FIFOQIA1 156 C1FIFOQIA22 31.0 same as C1FIFOQIA1 156 C1FIFOQIA22 31.0 same as C1FIFOQIA1 157 C1FIFOQIA23 31.0 same as C1FIFOQIA1 168 C1FIFOQIA23 31.0 same as C1FIFOQIA1 176 C1FIFOQIA23 31.0 same as C1FIFOQIA1 177 C1FIFOQIA23 31.0 same as C1FIFOQIA1	12C	C1FIFOSTA18	31:0				same as C1	FIFOSTA1						
138 CIFIFOSTA19 31.0 same as CIFIFOCA11 130 CIFIFOCAP01 31.0 same as CIFIFOCAN1 141 CIFIFOCAP02 31.0 same as CIFIFOCAN1 144 CIFIFOCAP02 31.0 same as CIFIFOCAN1 144 CIFIFOCAP12 31.0 same as CIFIFOCAN1 146 CIFIFOCAP12 31.0 same as CIFIFOCAN1 150 CIFIFOCAP12 31.0 same as CIFIFOCAN1 150 CIFIFOCAP12 31.0 same as CIFIFOCAN1 151 CIFIFOCAP22 31.0 same as CIFIFOCAN1 152 CIFIFOCAP22 31.0 same as CIFIFOCAN1 156 CIFIFOCAP23 31.0 same as CIFIFOCAN1 160 CIFIFOCAP23 31.0 same as CIFIFOCAN1 161 CIFIFOCAP23 31.0 same as CIFIFOCAN1 162 CIFIFOCAP23 31.0 same as CIFIFOCAN1 174 CIFIFOCAP23 31.0 same as CIFIFOCAN1 177 CIFIFOCAP24 31.0 same as CIFIFOCAN1	130	C1FIFOUA18	31:0				same as C	1FIFOUA1						
13C C1FIFOUA19 31.0 same as C1FIFOLA1 140 C1FIFOTA20 31.0 same as C1FIFOSTA1 144 C1FIFOTA20 31.0 same as C1FIFOSTA1 144 C1FIFOTA20 31.0 same as C1FIFOSTA1 145 C1FIFOUA21 31.0 same as C1FIFOUA1 150 C1FIFOUA21 31.0 same as C1FIFOUA1 151 C1FIFOUA21 31.0 same as C1FIFOUA1 152 C1FIFOUA22 31.0 same as C1FIFOUA1 155 C1FIFOUA22 31.0 same as C1FIFOUA1 156 C1FIFOUA23 31.0 same as C1FIFOUA1 156 C1FIFOUA23 31.0 same as C1FIFOUA1 168 C1FIFOUA23 31.0 same as C1FIFOUA1 168 C1FIFOUA23 31.0 same as C1FIFOUA1 170 C1FIFOUA23 31.0 same as C1FIFOUA1 171 C1FIFOUA23 31.0 same as C1FIFOUA1 172 C1FIFOUA23 31.0 same as C1FIFOUA1 174 <td< td=""><td>134</td><td>C1FIFOCON19</td><td>31:0</td><td></td><td></td><td></td><td>same as C1</td><td>FIFOCON1</td><td></td><td></td><td></td></td<>	134	C1FIFOCON19	31:0				same as C1	FIFOCON1						
140 CIFIFOCON20 31.0 same as CIFIFOCON1 144 CIFIFOCON20 31.0 same as CIFIFOCON1 148 CIFIFOCON21 31.0 same as CIFIFOCON1 140 CIFIFOCON21 31.0 same as CIFIFOCON1 150 CIFIFOCON21 31.0 same as CIFIFOCON1 154 CIFIFOCON22 31.0 same as CIFIFOCON1 155 CIFIFOCON22 31.0 same as CIFIFOCON1 156 CIFIFOCON22 31.0 same as CIFIFOCON1 156 CIFIFOCON22 31.0 same as CIFIFOCON1 156 CIFIFOCON22 31.0 same as CIFIFOCON1 166 CIFIFOSTA23 31.0 same as CIFIFOCON1 167 CIFIFOCON23 31.0 same as CIFIFOCON1 170 CIFIFOCON24 31.0 same as CIFIFOCON1 171 CIFIFOCON25 31.0 same as CIFIFOCON1 172 CIFIFOCON26 31.0 same as CIFIFOCON1 174 CIFIFOCON26 31.0 same as CIFIFOCON1	138	C1FIFOSTA19	31:0				same as C1	FIFOSTA1						
144 C1FIFOSTA20 31:0 same as C1FIFOUA1 148 C1FIFOUA20 31:0 same as C1FIFOUA1 140 C1FIFOCON21 31:0 same as C1FIFOUA1 141 C1FIFOSTA21 31:0 same as C1FIFOUA1 150 C1FIFOSTA21 31:0 same as C1FIFOUA1 154 C1FIFOCON22 31:0 same as C1FIFOCON1 155 C1FIFOCON23 31:0 same as C1FIFOCON1 156 C1FIFOCON23 31:0 same as C1FIFOSTA1 156 C1FIFOCON23 31:0 same as C1FIFOSTA1 166 C1FIFOCON23 31:0 same as C1FIFOSTA1 168 C1FIFOSTA24 31:0 same as C1FIFOSTA1 168 C1FIFOSTA23 31:0 same as C1FIFOSTA1 170 C1FIFOSTA24 31:0 same as C1FIFOSTA1 171 C1FIFOSTA24 31:0 same as C1FIFOSTA1 172 C1FIFOSTA24 31:0 same as C1FIFOSTA1 174 C1FIFOSTA25 31:0 same as C1FIFOSTA1 <	13C	C1FIFOUA19	31:0				same as C	1FIFOUA1						
148 C1FIFOUA20 31.0 same as C1FIFOCON1 140 C1FIFOCON21 31.0 same as C1FIFOCON1 150 C1FIFOUA21 31.0 same as C1FIFOCON1 154 C1FIFOUA21 31.0 same as C1FIFOUA1 158 C1FIFOUA22 31.0 same as C1FIFOUA1 150 C1FIFOUA22 31.0 same as C1FIFOUA1 161 C1FIFOUA22 31.0 same as C1FIFOUA1 162 C1FIFOUA23 31.0 same as C1FIFOUA1 164 C1FIFOUA23 31.0 same as C1FIFOUA1 164 C1FIFOUA23 31.0 same as C1FIFOUA1 166 C1FIFOUA23 31.0 same as C1FIFOUA1 177 C1FIFOUA24 31.0 same as C1FIFOUA1 178 C1FIFOCON25 31.0 same as C1FIFOCON1 170 C1FIFOCON25 31.0 same as C1FIFOCON1 171 C1FIFOCON25 31.0 same as C1FIFOCON1 172 C1FIFOCON25 31.0 same as C1FIFOCON1 178	140	C1FIFOCON20	31:0				same as C1	FIFOCON1						
14C C1FIFOCON21 31.0 same as C1FIFOSTA1 150 C1FIFOSTA21 31.0 same as C1FIFOSTA1 154 C1FIFOCON22 31.0 same as C1FIFOCON1 155 C1FIFOCON22 31.0 same as C1FIFOCON1 156 C1FIFOCON22 31.0 same as C1FIFOCON1 156 C1FIFOCON22 31.0 same as C1FIFOCON1 160 C1FIFOCON23 31.0 same as C1FIFOCON1 168 C1FIFOCON23 31.0 same as C1FIFOCON1 168 C1FIFOCON24 31.0 same as C1FIFOCON1 168 C1FIFOCON24 31.0 same as C1FIFOCON1 170 C1FIFOCON24 31.0 same as C1FIFOCON1 171 C1FIFOCON24 31.0 same as C1FIFOCON1 172 C1FIFOCON25 31.0 same as C1FIFOCON1 174 C1FIFOCON25 31.0 same as C1FIFOCON1 176 C1FIFOCON25 31.0 same as C1FIFOCON1 178 C1FIFOCON26 31.0 same as C1FIFOCON1	144	C1FIFOSTA20	31:0				same as C1	FIFOSTA1						
150 C1FIFOSTA21 31.0 same as C1FIFOUA1 154 C1FIFOUA21 31.0 same as C1FIFOUA1 158 C1FIFOCON22 31.0 same as C1FIFOSTA1 150 C1FIFOUA22 31.0 same as C1FIFOON1 156 C1FIFOUA22 31.0 same as C1FIFOON1 160 C1FIFOUA23 31.0 same as C1FIFOON1 168 C1FIFOSTA23 31.0 same as C1FIFOCON1 168 C1FIFOSTA23 31.0 same as C1FIFOCON1 168 C1FIFOCA24 31.0 same as C1FIFOCON1 170 C1FIFOUA23 31.0 same as C1FIFOCON1 171 C1FIFOCA24 31.0 same as C1FIFOCON1 178 C1FIFOUA24 31.0 same as C1FIFOCON1 178 C1FIFOCA25 31.0 same as C1FIFOCON1 180 C1FIFOCA25 31.0 same as C1FIFOCON1 181 C1FIFOCA26 31.0 same as C1FIFOCON1 182 C1FIFOCA26 31.0 same as C1FIFOCON1 184 C1FIFOCA26 31.0 same as C1FIFOCON1 185	148	C1FIFOUA20	31:0				same as C	1FIFOUA1						
150 C1FIFOSTA21 31.0 same as C1FIFOUA1 154 C1FIFOUA21 31.0 same as C1FIFOUA1 158 C1FIFOCON22 31.0 same as C1FIFOSTA1 150 C1FIFOUA22 31.0 same as C1FIFOON1 156 C1FIFOUA22 31.0 same as C1FIFOON1 160 C1FIFOUA23 31.0 same as C1FIFOON1 168 C1FIFOSTA23 31.0 same as C1FIFOCON1 168 C1FIFOSTA23 31.0 same as C1FIFOCON1 168 C1FIFOCA24 31.0 same as C1FIFOCON1 170 C1FIFOUA23 31.0 same as C1FIFOCON1 171 C1FIFOCA24 31.0 same as C1FIFOCON1 178 C1FIFOUA24 31.0 same as C1FIFOCON1 178 C1FIFOCA25 31.0 same as C1FIFOCON1 180 C1FIFOCA25 31.0 same as C1FIFOCON1 181 C1FIFOCA26 31.0 same as C1FIFOCON1 182 C1FIFOCA26 31.0 same as C1FIFOCON1 184 C1FIFOCA26 31.0 same as C1FIFOCON1 185	14C		31:0				same as C1	FIFOCON1						
154 C1FIFOUA21 31.0 same as C1FIFOUA1 158 C1FIFOCN22 31.0 same as C1FIFOCN1 160 C1FIFOUA22 31.0 same as C1FIFOCN1 160 C1FIFOUA22 31.0 same as C1FIFOCN1 164 C1FIFOUA22 31.0 same as C1FIFOCN1 168 C1FIFOUA23 31.0 same as C1FIFOCN1 178 C1FIFOCN24 31.0 same as C1FIFOCN1 178 C1FIFOCN24 31.0 same as C1FIFOCN1 170 C1FIFOCN24 31.0 same as C1FIFOCN1 177 C1FIFOCN24 31.0 same as C1FIFOCN1 178 C1FIFOCN25 31.0 same as C1FIFOCN1 179 C1FIFOCN25 31.0 same as C1FIFOCN1 180 C1FIFOSTA25 31.0 same as C1FIFOCN1 180 C1FIFOSTA26 31.0 same as C1FIFOCN1 181 C1FIFOCN26 31.0 same as C1FIFOCN1 182 C1FIFOCN26 31.0 same as C1FIFOCN1 184			31:0				same as C1	FIFOSTA1						
158 C1FIFOCON22 31:0 same as C1FIFOTA1 15C C1FIFOJA22 31:0 same as C1FIFOSTA1 160 C1FIFOLA22 31:0 same as C1FIFOUA1 164 C1FIFOLA22 31:0 same as C1FIFOUA1 164 C1FIFOCON23 31:0 same as C1FIFOSTA1 168 C1FIFOCON24 31:0 same as C1FIFOCON1 168 C1FIFOCON24 31:0 same as C1FIFOCON1 170 C1FIFOCON24 31:0 same as C1FIFOSTA1 171 C1FIFOUA24 31:0 same as C1FIFOSTA1 172 C1FIFOUA24 31:0 same as C1FIFOSTA1 174 C1FIFOUA25 31:0 same as C1FIFOSTA1 175 C1FIFOUA25 31:0 same as C1FIFOSTA1 176 C1FIFOUA25 31:0 same as C1FIFOCON1 180 C1FIFOCON26 31:0 same as C1FIFOCON1 182 C1FIFOCON27 31:0 same as C1FIFOUA1 190 C1FIFOUA27 31:0 same as C1FIFOCON1 184<	154		31:0				same as C	1FIFOUA1						
15C C1FIFOSTA22 31:0 same as C1FIFOUA1 160 C1FIFOUA22 31:0 same as C1FIFOUA1 164 C1FIFOUA22 31:0 same as C1FIFOUA1 166 C1FIFOUA23 31:0 same as C1FIFOUA1 167 C1FIFOUA23 31:0 same as C1FIFOUA1 168 C1FIFOUA24 31:0 same as C1FIFOUA1 170 C1FIFOUA24 31:0 same as C1FIFOUA1 171 C1FIFOUA24 31:0 same as C1FIFOUA1 172 C1FIFOUA24 31:0 same as C1FIFOUA1 173 C1FIFOUA25 31:0 same as C1FIFOUA1 174 C1FIFOUA25 31:0 same as C1FIFOUA1 172 C1FIFOUA25 31:0 same as C1FIFOUA1 180 C1FIFOUA25 31:0 same as C1FIFOUA1 184 C1FIFOUA26 31:0 same as C1FIFOUA1 185 C1FIFOUA26 31:0 same as C1FIFOUA1 190 C1FIFOUA27 31:0 same as C1FIFOUA1 194 C														
160 C1FIFOUA22 31:0 same as C1FIFOUA1 164 C1FIFOCON23 31:0 same as C1FIFOCON1 168 C1FIFOTA23 31:0 same as C1FIFOCON1 170 C1FIFOCON24 31:0 same as C1FIFOCON1 170 C1FIFOCON24 31:0 same as C1FIFOCON1 174 C1FIFOCON24 31:0 same as C1FIFOCON1 177 C1FIFOCON25 31:0 same as C1FIFOCON1 178 C1FIFOUA24 31:0 same as C1FIFOCON1 178 C1FIFOUA25 31:0 same as C1FIFOCON1 170 C1FIFOUA25 31:0 same as C1FIFOUA1 180 C1FIFOUA25 31:0 same as C1FIFOUA1 184 C1FIFOUA26 31:0 same as C1FIFOUA1 188 C1FIFOUA26 31:0 same as C1FIFOUA1 190 C1FIFOUA26 31:0 same as C1FIFOUA1 194 C1FIFOUA27 31:0 same as C1FIFOUA1 195 C1FIFOUA27 31:0 same as C1FIFOCON1 194														
164 CTFIFOCON23 31:0 same as CTFIFOCON1 168 C1FIFOUA23 31:0 same as C1FIFOUA1 170 C1FIFOUA23 31:0 same as C1FIFOCON1 171 C1FIFOUA23 31:0 same as C1FIFOCON1 172 C1FIFOUA24 31:0 same as C1FIFOCON1 173 C1FIFOUA24 31:0 same as C1FIFOUA1 174 C1FIFOUA24 31:0 same as C1FIFOCON1 177 C1FIFOUA24 31:0 same as C1FIFOUA1 176 C1FIFOUA25 31:0 same as C1FIFOUA1 177 C1FIFOUA25 31:0 same as C1FIFOUA1 180 C1FIFOUA25 31:0 same as C1FIFOCON1 180 C1FIFOUA26 31:0 same as C1FIFOCON1 182 C1FIFOUA26 31:0 same as C1FIFOCON1 184 C1FIFOUA26 31:0 same as C1FIFOCON1 198 C1FIFOUA27 31:0 same as C1FIFOUA1 194 C1FIFOUA28 31:0 same as C1FIFOUA1 194														
168 C1FIFOSTA23 31:0 same as C1FIFOSTA1 16C C1FIFOCON24 31:0 same as C1FIFOCON1 170 C1FIFOCON24 31:0 same as C1FIFOSTA1 174 C1FIFOCON24 31:0 same as C1FIFOSTA1 175 C1FIFOCON24 31:0 same as C1FIFOCON1 176 C1FIFOCON25 31:0 same as C1FIFOCON1 170 C1FIFOCON25 31:0 same as C1FIFOCON1 180 C1FIFOCON26 31:0 same as C1FIFOCON1 182 C1FIFOCON26 31:0 same as C1FIFOCON1 184 C1FIFOCON26 31:0 same as C1FIFOCON1 186 C1FIFOCON27 31:0 same as C1FIFOCON1 198 C1FIFOCON27 31:0 same as C1FIFOCON1 198 C1FIFOCON28 31:0 same as C1FIFOCON1														
16C C1FIFOUA23 31.0 same as C1FIFOUA1 170 C1FIFOCON24 31.0 same as C1FIFOCON1 174 C1FIFOUA24 31.0 same as C1FIFOUA1 178 C1FIFOUA24 31.0 same as C1FIFOUA1 178 C1FIFOUA24 31.0 same as C1FIFOUA1 170 C1FIFOUA24 31.0 same as C1FIFOCON1 180 C1FIFOUA25 31.0 same as C1FIFOUA1 180 C1FIFOUA25 31.0 same as C1FIFOUA1 184 C1FIFOUA26 31.0 same as C1FIFOUA1 188 C1FIFOCON26 31.0 same as C1FIFOUA1 180 C1FIFOUA26 31.0 same as C1FIFOUA1 190 C1FIFOUA26 31.0 same as C1FIFOCN1 191 C1FIFOUA27 31.0 same as C1FIFOCN1 192 C1FIFOUA27 31.0 same as C1FIFOCN1 194 C1FIFOCN28 31.0 same as C1FIFOCN1 194 C1FIFOUA27 31.0 same as C1FIFOCN1 194 <t< td=""><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></t<>														
170 C1FIFOCON24 31:0 same as C1FIFOCON1 174 C1FIFOSTA24 31:0 same as C1FIFOCON1 178 C1FIFOQUA24 31:0 same as C1FIFOUA1 170 C1FIFOCON25 31:0 same as C1FIFOCON1 170 C1FIFOCON25 31:0 same as C1FIFOCON1 180 C1FIFOCON25 31:0 same as C1FIFOCON1 184 C1FIFOCON26 31:0 same as C1FIFOCON1 188 C1FIFOCON26 31:0 same as C1FIFOCON1 180 C1FIFOCON26 31:0 same as C1FIFOCON1 181 C1FIFOCON26 31:0 same as C1FIFOCON1 182 C1FIFOCON27 31:0 same as C1FIFOCON1 190 C1FIFOCON27 31:0 same as C1FIFOCON1 194 C1FIFOCON27 31:0 same as C1FIFOCON1 198 C1FIFOCN28 31:0 same as C1FIFOCON1 190 C1FIFOCN28 31:0 same as C1FIFOCON1 1A4 C1FIFOCN28 31:0 same as C1FIFOCON1														
174 C1FIFOSTA24 31:0 same as C1FIFOSTA1 178 C1FIFOUA24 31:0 same as C1FIFOUA1 170 C1FIFOCN25 31:0 same as C1FIFOCN1 180 C1FIFOSTA25 31:0 same as C1FIFOSTA1 184 C1FIFOUA25 31:0 same as C1FIFOUA1 188 C1FIFOCN26 31:0 same as C1FIFOUA1 188 C1FIFOUA25 31:0 same as C1FIFOUA1 180 C1FIFOUA26 31:0 same as C1FIFOUA1 180 C1FIFOUA26 31:0 same as C1FIFOUA1 181 C1FIFOUA26 31:0 same as C1FIFOUA1 182 C1FIFOUA26 31:0 same as C1FIFOUA1 194 C1FIFOUA26 31:0 same as C1FIFOUA1 198 C1FIFOUA27 31:0 same as C1FIFOUA1 192 C1FIFOUA27 31:0 same as C1FIFOUA1 194 C1FIFOUA28 31:0 same as C1FIFOUA1 194 C1FIFOUA27 31:0 same as C1FIFOUA1 194 C1FIFOUA28 31:0 same as C1FIFOUA1 104 C1F														
178 C1FIFOUA24 31:0 same as C1FIFOUA1 17C C1FIFOCON25 31:0 same as C1FIFOCON1 180 C1FIFOUA25 31:0 same as C1FIFOUA1 184 C1FIFOUA25 31:0 same as C1FIFOUA1 188 C1FIFOUA26 31:0 same as C1FIFOUA1 188 C1FIFOUA26 31:0 same as C1FIFOUA1 188 C1FIFOUA26 31:0 same as C1FIFOUA1 180 C1FIFOUA26 31:0 same as C1FIFOUA1 180 C1FIFOUA26 31:0 same as C1FIFOUA1 190 C1FIFOUA27 31:0 same as C1FIFOUA1 194 C1FIFOUA27 31:0 same as C1FIFOUA1 196 C1FIFOUA27 31:0 same as C1FIFOUA1 197 C1FIFOUA28 31:0 same as C1FIFOUA1 144 C1FIFOUA28 31:0 same as C1FIFOUA1 1A4 C1FIFOUA28 31:0 same as C1FIFOUA1 1A4 C1FIFOUA28 31:0 same as C1FIFOUA1 1B0														
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184 C1FIFOUA25 31:0 same as C1FIFOUA1 188 C1FIFOCON26 31:0 same as C1FIFOCON1 180 C1FIFOUA26 31:0 same as C1FIFOCON1 190 C1FIFOUA26 31:0 same as C1FIFOUA1 194 C1FIFOUA26 31:0 same as C1FIFOCON1 198 C1FIFOCON27 31:0 same as C1FIFOCON1 198 C1FIFOUA27 31:0 same as C1FIFOCON1 199 C1FIFOUA27 31:0 same as C1FIFOUA1 190 C1FIFOUA27 31:0 same as C1FIFOUA1 191 C1FIFOUA27 31:0 same as C1FIFOUA1 140 C1FIFOUA28 31:0 same as C1FIFOCON1 1A4 C1FIFOUA28 31:0 same as C1FIFOUA1 1A4 C1FIFOUA28 31:0 same as C1FIFOCON1 1A6 C1FIFOUA28 31:0 same as C1FIFOCON1 1A7 C1FIFOUA29 31:0 same as C1FIFOCON1 1B8 C1FIFOCON30 31:0 same as C1FIFOCON1 1B8														
188 C1FIFCOCON26 31:0 same as C1FIFOCON1 18C C1FIFOUA26 31:0 same as C1FIFOUA1 190 C1FIFOUA26 31:0 same as C1FIFOUA1 194 C1FIFOCON27 31:0 same as C1FIFOCON1 198 C1FIFOUA27 31:0 same as C1FIFOCON1 198 C1FIFOUA27 31:0 same as C1FIFOCON1 190 C1FIFOUA27 31:0 same as C1FIFOCON1 198 C1FIFOUA27 31:0 same as C1FIFOUA1 190 C1FIFOUA28 31:0 same as C1FIFOCON1 1A0 C1FIFOSTA28 31:0 same as C1FIFOCON1 1A4 C1FIFOUA28 31:0 same as C1FIFOCON1 1A8 C1FIFOUA28 31:0 same as C1FIFOCON1 1A6 C1FIFOCON29 31:0 same as C1FIFOCON1 1B0 C1FIFOUA29 31:0 same as C1FIFOCON1 1B4 C1FIFOCON30 31:0 same as C1FIFOCON1 1B5 C1FIFOUA30 31:0 same as C1FIFOCON1 1B6<														
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190 C1FIFOUA26 31:0 same as C1FIFOUA1 194 C1FIFOCON27 31:0 same as C1FIFOCON1 198 C1FIFOSTA27 31:0 same as C1FIFOUA1 190 C1FIFOUA27 31:0 same as C1FIFOUA1 190 C1FIFOUA27 31:0 same as C1FIFOUA1 190 C1FIFOCON28 31:0 same as C1FIFOUA1 1A0 C1FIFOCON28 31:0 same as C1FIFOUA1 1A4 C1FIFOCON28 31:0 same as C1FIFOUA1 1A4 C1FIFOUA28 31:0 same as C1FIFOUA1 1A8 C1FIFOUA28 31:0 same as C1FIFOUA1 1A6 C1FIFOCON29 31:0 same as C1FIFOUA1 1AC C1FIFOCON29 31:0 same as C1FIFOCON1 1B0 C1FIFOUA29 31:0 same as C1FIFOUA1 1B4 C1FIFOUA30 31:0 same as C1FIFOCON1 1B8 C1FIFOUA30 31:0 same as C1FIFOUA1 1C0 C1FIFOUA30 31:0 same as C1FIFOCON1 1C4														
194 C1FIFOCON27 31:0 same as C1FIFOCON1 198 C1FIFOSTA27 31:0 same as C1FIFOSTA1 190 C1FIFOUA27 31:0 same as C1FIFOUA1 140 C1FIFOCON28 31:0 same as C1FIFOCON1 1A0 C1FIFOCON28 31:0 same as C1FIFOCON1 1A4 C1FIFOUA27 31:0 same as C1FIFOCON1 1A4 C1FIFOUA28 31:0 same as C1FIFOCON1 1A8 C1FIFOUA28 31:0 same as C1FIFOUA1 1A6 C1FIFOUA28 31:0 same as C1FIFOUA1 1A6 C1FIFOCON29 31:0 same as C1FIFOUA1 1AC C1FIFOUA29 31:0 same as C1FIFOUA1 1B0 C1FIFOUA29 31:0 same as C1FIFOUA1 1B4 C1FIFOUA30 31:0 same as C1FIFOUA1 1B6 C1FIFOUA30 31:0 same as C1FIFOCON1 1B7 C1FIFOUA30 31:0 same as C1FIFOUA1 1C0 C1FIFOUA30 31:0 same as C1FIFOUA1 1C4														
198 C1FIFOSTA27 31:0 same as C1FIFOSTA1 19C C1FIFOUA27 31:0 same as C1FIFOUA1 1A0 C1FIFOCON28 31:0 same as C1FIFOCON1 1A4 C1FIFOSTA28 31:0 same as C1FIFOSTA1 1A8 C1FIFOUA28 31:0 same as C1FIFOSTA1 1A8 C1FIFOUA28 31:0 same as C1FIFOUA1 1AC C1FIFOCON29 31:0 same as C1FIFOUA1 1AC C1FIFOSTA29 31:0 same as C1FIFOCON1 1B0 C1FIFOSTA29 31:0 same as C1FIFOCON1 1B4 C1FIFOUA29 31:0 same as C1FIFOUA1 1B8 C1FIFOCON30 31:0 same as C1FIFOCON1 1B8 C1FIFOSTA30 31:0 same as C1FIFOUA1 1BC C1FIFOUA30 31:0 same as C1FIFOUA1 1C4 C1FIFOUA30 31:0 same as C1FIFOCON1 1C8 C1FIFOSTA31 31:0 same as C1FIFOSTA1														
19C C1FIFOUA27 31:0 same as C1FIFOUA1 1A0 C1FIFOCON28 31:0 same as C1FIFOCON1 1A4 C1FIFOSTA28 31:0 same as C1FIFOSTA1 1A8 C1FIFOUA28 31:0 same as C1FIFOUA1 1A8 C1FIFOUA28 31:0 same as C1FIFOUA1 1AC C1FIFOCON29 31:0 same as C1FIFOCON1 1B0 C1FIFOSTA29 31:0 same as C1FIFOSTA1 1B4 C1FIFOUA29 31:0 same as C1FIFOUA1 1B4 C1FIFOUA29 31:0 same as C1FIFOUA1 1B4 C1FIFOUA30 31:0 same as C1FIFOUA1 1B8 C1FIFOCON30 31:0 same as C1FIFOUA1 1B6 C1FIFOUA30 31:0 same as C1FIFOUA1 1C0 C1FIFOUA30 31:0 same as C1FIFOUA1 1C4 C1FIFOCON31 31:0 same as C1FIFOCON1 1C8 C1FIFOSTA31 31:0 same as C1FIFOSTA1														
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1A8 C1FIFOUA28 31:0 same as C1FIFOUA1 1AC C1FIFOCON29 31:0 same as C1FIFOCON1 1B0 C1FIFOSTA29 31:0 same as C1FIFOSTA1 1B4 C1FIFOUA29 31:0 same as C1FIFOUA1 1B8 C1FIFOUA29 31:0 same as C1FIFOUA1 1B8 C1FIFOCN30 31:0 same as C1FIFOCON1 1BC C1FIFOSTA30 31:0 same as C1FIFOCON1 1BC C1FIFOUA30 31:0 same as C1FIFOUA1 1C0 C1FIFOUA30 31:0 same as C1FIFOUA1 1C4 C1FIFOCON31 31:0 same as C1FIFOCON1 1C8 C1FIFOSTA31 31:0 same as C1FIFOSTA1														
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1C0 C1FIFOUA30 31:0 same as C1FIFOUA1 1C4 C1FIFOCON31 31:0 same as C1FIFOCON1 1C8 C1FIFOSTA31 31:0 same as C1FIFOSTA1	1B8	C1FIFOCON30	31:0		same as C1FIFOCON1									
1C4 C1FIFOCON31 31:0 same as C1FIFOCON1 1C8 C1FIFOSTA31 31:0 same as C1FIFOSTA1	1BC	C1FIFOSTA30	31:0		same as C1FIFOSTA1									
1C8 C1FIFOSTA31 31:0 same as C1FIFOSTA1	1C0	C1FIFOUA30	31:0		same as C1FIFOUA1									
	1C4	C1FIFOCON31	31:0				same as C1	FIFOCON1						
	1C8	C1FIFOSTA31	31:0				same as C1	FIFOSTA1						
1CC C1FIFOUA31 31:0 same as C1FIFOUA1	1CC	C1FIFOUA31	31:0				same as C	1FIFOUA1						

TABLE 3-2: CAN FD CONTROLLER MODULE REGISTER SUMMARY (CONTINUED)

Note 1: The lower order byte of the 32-bit register resides at the low-order address.

Addr.	Name		Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
	C1FLTCON0	31:24	FLTEN3	_	—			F3BP<4:0>		
		23:16	FLTEN2	_	_			F2BP<4:0>		
		15:8	FLTEN1	—	—			F1BP<4:0>		
1D0		7:0	FLTEN0		—			F0BP<4:0>		
	C1FLTCON1	31:24	FLTEN7	—	—			F7BP<4:0>		
		23:16	FLTEN6	_	—			F6BP<4:0>		
		15:8	FLTEN5	_	_			F5BP<4:0>		
1D4		7:0	FLTEN4	_	_			F4BP<4:0>		
	C1FLTCON2	31:24	FLTEN11	_	_			F11BP<4:0>		
		23:16	FLTEN10	_	_			F10BP<4:0>		
		15:8	FLTEN9	_	_			F9BP<4:0>		
1D8		7:0	FLTEN8					F8BP<4:0>		
	C1FLTCON3	31:24	FLTEN15		_			F15BP<4:0>		
		23:16	FLTEN14		_			F14BP<4:0>		
		15:8	FLTEN13	_				F13BP<4:0>		
1DC		7:0	FLTEN12		_			F12BP<4:0>		
100	C1FLTCON4	31:24	FLTEN19		_			F19BP<4:0>		
		23:16	FLTEN18					F18BP<4:0>		
		15:8	FLTEN17					F17BP<4:0>		
150		7:0								
1E0			FLTEN16					F16BP<4:0>		
	C1FLTCON5	31:24	FLTEN23					F23BP<4:0>		
		23:16	FLTEN22					F22BP<4:0>		
. – .		15:8	FLTEN21		—			F21BP<4:0>		
1E4		7:0	FLTEN20		—			F20BP<4:0>		
	C1FLTCON6	31:24	FLTEN27		—			F27BP<4:0>		
		23:16	FLTEN26		—			F26BP<4:0>		
		15:8	FLTEN25		—			F25BP<4:0>		
1E8		7:0	FLTEN24	—	—			F24BP<4:0>		
	C1FLTCON7	31:24	FLTEN31	—	—			F31BP<4:0>		
		23:16	FLTEN30		—			F30BP<4:0>		
		15:8	FLTEN29	—	—			F29BP<4:0>		
1EC		7:0	FLTEN28		—			F28BP<4:0>		
	C1FLTOBJ0	31:24	_	EXIDE	SID11			EID<17:6>		
		23:16				EID<1	2:5>	1		
		15:8			EID<4:0>				SID<10:8>	
1F0		7:0				SID<	7:0>			
	C1MASK0	31:24	—	MIDE	MSID11			MEID<17:6>		
		23:16				MEID<	12:5>			
		15:8			MEID<4:0>				MSID<10:8>	
1F4		7:0				MSID<	<7:0>			
1F8	C1FLTOBJ1	31:0				same as C	IFLTOBJ0			
1FC	C1MASK1	31:0				same as C	1MASK0			
200	C1FLTOBJ2	31:0				same as C	IFLTOBJ0			
204	C1MASK2	31:0				same as C				
208	C1FLTOBJ3	31:0				same as C				
20C	C1MASK3	31:0				same as C				
210	C1FLTOBJ4	31:0				same as C				
214	C1MASK4	31:0				same as C				
218	C1FLTOBJ5	31:0				same as C				
21C	C1MASK5 : The lower o	31:0				same as C				

Note 1: The lower order byte of the 32-bit register resides at the low-order address.

Addr.	Name		Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0		
220	C1FLTOBJ6	31:0	0.11201.011	00/22/11/0		same as C						
224	C1MASK6	31:0				same as C						
228	C1FLTOBJ7	31:0				same as C						
22C	C1MASK7	31:0		same as C1MASK0								
230	C1FLTOBJ8	31:0				same as C						
234	C1MASK8	31:0				same as C						
238	C1FLTOBJ9	31:0				same as C						
23C	C1MASK9	31:0				same as C						
240	C1FLTOBJ10	31:0				same as C						
244	C1MASK10	31:0				same as C						
248	C1FLTOBJ11	31:0				same as C						
24C	C1MASK11	31:0				same as C						
250	C1FLTOBJ12	31:0				same as C						
254	C1MASK12	31:0				same as C						
258	C1FLTOBJ13	31:0				same as C						
25C	C1MASK13	31:0				same as C						
260	C1FLTOBJ14	31:0				same as C						
264	C1MASK14	31:0				same as C						
268	C1FLTOBJ15	31:0				same as C						
26C	C1MASK15	31:0				same as C						
270	C1FLTOBJ16	31:0				same as C						
274	C1MASK16	31:0				same as C						
278	C1FLTOBJ17	31:0				same as C						
27C	C1MASK17	31:0				same as C						
280	C1FLTOBJ18	31:0										
284	C1MASK18	31:0		same as C1FLTOBJ0 same as C1MASK0								
288	C1FLTOBJ19	31:0				same as C						
28C	C1MASK19	31:0				same as C						
290	C1FLTOBJ20	31:0				same as C						
294	C1MASK20	31:0				same as C						
294	C1FLTOBJ21	31:0				same as C						
290 29C	C1MASK21	31:0				same as C						
230 2A0	C1FLTOBJ22	31:0				same as C						
2A0 2A4	C1MASK22	31:0				same as C						
2A4 2A8	C1FLTOBJ23	31:0				same as C						
2AC	C1MASK23	31:0				same as C						
2R0 2B0	C1FLTOBJ24	31:0				same as C						
2B0	C1MASK24	31:0				same as C						
2B4	C1FLTOBJ25	31:0				same as C						
2BC	C1MASK25	31:0				same as C						
2D0	C1FLTOBJ26	31:0				same as C						
2C4	C1MASK26	31:0				same as C						
2C4	C1FLTOBJ27	31:0				same as C						
200 2CC	C1MASK27	31:0				same as C						
200 2D0	C1FLTOBJ28	31:0				same as C						
2D0 2D4	C1MASK28	31:0				same as C						
2D4 2D8	C1FLTOBJ29	31:0										
2D0 2DC	C1MASK29	31:0		same as C1FLTOBJ0								
2DC 2E0	C1FLTOBJ30	31:0		same as C1MASK0 same as C1FLTOBJ0								
2E0 2E4	C1MASK30	31:0				same as C						
2E4	C1FLTOBJ31	31:0				same as C						
2E0 2EC	C1MASK31	31:0				same as C						
					ides at the lo							

TABLE 3-2: CAN FD CONTROLLER MODULE REGISTER SUMMARY (CONTINUED)

Note 1: The lower order byte of the 32-bit register resides at the low-order address.

3.1 MCP2517FD Specific Registers

- Register 3-1: OSC
- Register 3-2: IOCON
- Register 3-3: CRC
- Register 3-4: ECCCON
- Register 3-5: ECCSTAT

TABLE 3-3: REGISTER LEGEND

Symbol	Description	Symbol	Description
R	Readable bit	HC	Cleared by Hardware only
W	Writable bit	HS	Set by Hardware only
U	Unimplemented bit, read as '0'	1	Bit is set at Reset
S	Settable bit	0	Bit is cleared at Reset
С	Clearable bit	x	Bit is unknown at Reset

EXAMPLE 3-1:

R/W - 0 indicates the bit is both readable and writable, and reads '0' after a Reset.

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MCP2517FD

REGISTER	3-1: OSC –	MCP2517F	D OSCILLATO	R CONTR	OL REGISTER		
U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	_	—	—	—	_
bit 31					· · ·		bit 24
U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
_	—		—		_		—
bit 23							bit 16
U-0	U-0	U-0	R-0	U-0	R-0	U-0	R-0
—	—	—	SCLKRDY	—	OSCRDY	—	PLLRDY
bit 15							bit 8
U-0	R/W-1	R/W-1	R/W-0	U-0	HS/C-0	U-0	R/W-0
	CLKOD	IV<1:0>	SCLKDIV ⁽¹⁾		OSCDIS ⁽²⁾	_	PLLEN ⁽¹⁾
bit 7							bit 0
Legend: R = Readab -n = Value a		W = Writable '1' = Bit is se		U = Unimpl '0' = Bit is c	emented bit, read	as '0' < = Bit is un	known
bit 31-13 bit 12	Unimplement SCLKRDY: Sy 1 = SCLKDIV 0 = SCLKDIV	/nchronized S					
bit 11	Unimplement	ed: Read as	'0'				
bit 10	OSCRDY: Clo 1 = Clock is ri 0 = Clock not	unning and st	able				
bit 9	Unimplement	ed: Read as	ʻ0'				
bit 8	PLLRDY: PLL 1 = PLL Lock 0 = PLL not re	ed					
bit 7	Unimplement	ed: Read as	ʻ0'				
bit 6-5	CLKODIV<1:0 11 =CLKO is 0 10 =CLKO is 0 01 =CLKO is 0 00 =CLKO is 0	divided by 10 divided by 4 divided by 2	put Divisor				
bit 4	SCLKDIV: Sys 1 = SCLK is c 0 = SCLK is c	livided by 2	ivisor ⁽¹⁾				
bit 3	Unimplement	-	'O'				
bit 2	OSCDIS: Cloc	k (Oscillator) abled, the dev		ode.			
	his bit can only be Clearing OSCDIS v		-		ce and put it back i	n Configura	ition mode.

REGISTER 3-1: OSC – MCP2517FD OSCILLATOR CONTROL REGISTER (CONTINUED)

- bit 1 Unimplemented: Read as '0'
- bit 0 **PLLEN:** PLL Enable⁽¹⁾
 - 1 = System Clock from 10x PLL
 - 0 = System Clock comes directly from XTAL oscillator
- **Note 1:** This bit can only be modified in Configuration mode.
 - 2: Clearing OSCDIS while in Sleep mode will wake-up the device and put it back in Configuration mode.

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U-0	R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-1	R/W-1
_	INTOD	SOF	TXCANOD	_		PM1	PM0
bit 31							bit 24
						DAA	D 44/
U-0	U-0	U-0	U-0	U-0	U-0	R/W-x	R/W-x
— 			—	—		GPI01	GPIO0
bit 23							bit 16
U-0	U-0	U-0	U-0	U-0	U-0	R/W-x	R/W-x
—	_	—		—	—	LAT1	LAT0
bit 15							bit 8
	DAM 0						DANA
U-0	R/W-0	U-0	U-0	U-0	U-0	R/W-1	R/W-1 TRIS0 ⁽¹⁾
	XSTBYEN	—		—	_	TRIS1 ⁽¹⁾	
bit 7							bit (
Legend:							
R = Readable	e bit	W = Writable	bit	U = Unimpler	mented bit, rea	ad as '0'	
-n = Value at I	POR	'1' = Bit is se	t	'0' = Bit is cle	ared	x = Bit is unkr	iown
bit 29 bit 28	1 = Open Dra 0 = Push/Pull SOF: Start-Of 1 = SOF sign 0 = Clock on TXCANOD: T	l Output -Frame signal al on CLKO p CLKO pin	'n				
511 20	1 = Open Dra 0 = Push/Pull	ain Output					
bit 27-26		Julpul					
	Unimplement	•	0'				
bit 25	PM1: GPIO P 1 = Pin is use	t ed: Read as in Mode ed a <u>s GP</u> IO1	0' erted when CilN	T.RXIF and R.	XIE are set		
	PM1: GPIO P 1 = Pin is use 0 = Interrupt PM0: GPIO P 1 = Pin is use	ted: Read as in Mode ed a <u>s GP</u> IO1 Pin INT1, asse in Mode ed a <u>s GP</u> IO0					
bit 24	PM1: GPIO P 1 = Pin is use 0 = Interrupt PM0: GPIO P 1 = Pin is use	ted: Read as in Mode ed a <u>s GP</u> IO1 Pin INT1, asse in Mode ed a <u>s GP</u> IO0 Pin INT0, asse	erted when CilN erted when CilN				
bit 24 bit 23-18	PM1: GPIO P 1 = Pin is use 0 = Interrupt PM0: GPIO P 1 = Pin is use 0 = Interrupt Unimplement GPIO1: GPIO	ted: Read as in Mode ed a <u>s GP</u> IO1 Pin INT1, asse in Mode ed a <u>s GP</u> IO0 Pin INT0, asse ted: Read as 1 Status	erted when CilN erted when CilN				
bit 24 bit 23-18	PM1: GPIO P 1 = Pin is use 0 = Interrupt PM0: GPIO P 1 = Pin is use 0 = Interrupt Unimplement	ted: Read as in Mode ed a <u>s GP</u> IO1 Pin INT1, asse in Mode ed a <u>s GP</u> IO0 Pin INT0, asse ted: Read as 1 Status VIH	erted when CilN erted when CilN				
bit 25 bit 24 bit 23-18 bit 17 bit 16	PM1: GPIO P 1 = Pin is use 0 = Interrupt PM0: GPIO P 1 = Pin is use 0 = Interrupt Unimplement GPIO1: GPIO 1 = VGPIO1 >	ted: Read as in Mode ed as <u>GP</u> IO1 Pin INT1, asse in Mode ed a <u>s GP</u> IO0 Pin INT0, asse ted: Read as 1 Status VIH VIL	erted when CilN erted when CilN				
bit 24 bit 23-18 bit 17	PM1: GPIO P 1 = Pin is use 0 = Interrupt PM0: GPIO P 1 = Pin is use 0 = Interrupt Unimplement GPIO1: GPIO 1 = VGPIO1 > 0 = VGPIO1 <	ted: Read as in Mode ed a <u>s GP</u> IO1 Pin INT1, asse in Mode ed a <u>s GP</u> IO0 Pin INT0, asse ted: Read as 1 Status VIH VIL 0 Status VIH	erted when CilN erted when CilN				
bit 24 bit 23-18 bit 17	PM1: GPIO P 1 = Pin is use 0 = Interrupt PM0: GPIO P 1 = Pin is use 0 = Interrupt Unimplement GPIO1: GPIO 1 = VGPIO1 > 0 = VGPIO1 <	ted: Read as in Mode ed as <u>GP</u> IO1 Pin INT1, asse in Mode ed a <u>s GP</u> IO0 Pin INT0, asse ted: Read as 1 Status VIH VIL 0 Status VIH VIL	erted when CiIN erted when CiIN 0'				

REGISTER 3-2: IOCON – INPUT/OUTPUT CONTROL REGISTER

REGISTER 3-2: IOCON – INPUT/OUTPUT CONTROL REGISTER (CONTINUED)

bit 9	LAT1: GPIO1 Latch
	1 = Drive Pin High
	0 = Drive Pin Low
bit 8	LAT0: GPIO0 Latch
	1 = Drive Pin High
	0 = Drive Pin Low
bit 7	Unimplemented: Read as '0'
bit 6	XSTBYEN: Enable Transceiver Standby Pin Control
	1 = XSTBY control enabled
	0 = XSTBY control disabled
bit 5-2	Unimplemented: Read as '0'
bit 1	TRIS1: GPIO1 Data Direction ⁽¹⁾
	1 = Input Pin
	0 = Output Pin
bit 0	TRIS0: GPIO0 Data Direction ⁽¹⁾
	1 = Input Pin
	0 = Output Pin
Note 1	If $PMx = 0$, TPISy will be ignored and the nin will be an outp

Note 1: If PMx = 0, TRISx will be ignored and the pin will be an output.

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REGISTER 3	-3: CRC –	CRC REGIST	ER				
U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
	_	—	_	_	—	FERRIE	CRCERRIE
bit 31							bit 24
U-0	U-0	U-0	U-0	U-0	U-0	HS/C-0	HS/C-0
_	_	_	_	_	—	FERRIF	CRCERRIF
bit 23							bit 16
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
			CRC<1	5:8>			
bit 15							bit 8
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
			CRC<	7:0>			
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable b	bit	U = Unimpler	mented bit, rea	ad as '0'	
-n = Value at F	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unl	known
bit 31-26	Unimplement	ed: Read as '0	,				
DIL J 1-20	ommpicment						
bit 31-20 bit 25	-	Command For		rrupt Enable			
	FERRIE: CRC		mat Error Inte	rrupt Enable			
bit 25	FERRIE: CRC CRCERRIE: C	Command For	mat Error Inte upt Enable	rrupt Enable			
bit 25 bit 24	FERRIE: CRC CRCERRIE: C Unimplement	Command For CRC Error Interr	mat Error Inte rupt Enable	·			
bit 25 bit 24 bit 23-18	FERRIE: CRC CRCERRIE: C Unimplement FERRIF: CRC 1 = Number c	Command For CRC Error Interr ced: Read as '0	mat Error Inte upt Enable mat Error Inte ch during "SPI	rrupt Flag with CRC" cc	ommand occur	red	
bit 25 bit 24 bit 23-18	FERRIE: CRC CRCERRIE: C Unimplement FERRIF: CRC 1 = Number c 0 = No SPI C	Command For CRC Error Interr ted: Read as '0 Command For of Bytes mismat	mat Error Inte rupt Enable mat Error Inte ch during "SPI ormat error oc	rrupt Flag with CRC" cc	ommand occur	red	
bit 25 bit 24 bit 23-18 bit 17	FERRIE: CRC CRCERRIE: C Unimplement FERRIF: CRC 1 = Number C 0 = No SPI C CRCERRIF: C 1 = CRC miss	Command For CRC Error Interr ced: Read as '0 Command For of Bytes mismat RC command for	mat Error Inte rupt Enable mat Error Inte ch during "SPI ormat error oc rupt Flag	rrupt Flag with CRC" cc	ommand occur	red	

REGISTER 3-4	ECCC	ON – ECC CC	NTROL RE	GISTER			
U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—		—		—		—	—
bit 31							bit 24
U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	_		_				
bit 23							bit 16
U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
				PARITY<6:0>			
bit 15							bit 8
U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	_		_		DEDIE	SECIE	ECCEN
bit 7							bit 0
· · ·							1
Legend:							
R = Readable bi	t	W = Writable I	bit		nented bit, rea	d as '0'	
-n = Value at PC	R	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unk	nown
bit 31-15	Unimplemen	ted: Read as '0)'				

- bit 14-8 **PARITY<6:0>:** Parity bits used during write to RAM when ECC is disabled
- bit 7-3 Unimplemented: Read as '0'
- bit 2 DEDIE: Double Error Detection Interrupt Enable Flag
- bit 1 SECIE: Single Error Correction Interrupt Enable Flag
- bit 0 ECCEN: ECC Enable
 - 1 = ECC enabled
 - 0 = ECC disabled

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U-0	U-0	U-0	U-0	R-0	R-0	R-0	R-0
_	—	_	_		ERRAD	DR<11:8>	
bit 31			•				bit 24
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
			ERRADE)R<7:0>			
bit 23							bit 16
U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	_	_	_	_	—	— —
bit 15							bit 8
U-0	U-0	U-0	U-0	U-0	HS/C-0	HS/C-0	U-0
—	_	—	_	—	DEDIF	SECIF	—
bit 7	· · ·			·			bit 0
1 4							
Legend: R = Readable	- h:t \		L:4		mented bit men	d aa (0)	
		N = Writable		-	mented bit, rea		
-n = Value at	POR	1' = Bit is set		'0' = Bit is cle	eared	x = Bit is unkr	iown
h:+ 04 00		d. Dood oo (o'				
bit 31-28	Unimplemente			0			
bit 27-16	ERRADDR<11:			C error occurr	ed		
bit 15-3	Unimplemente	d: Read as '	0'				
bit 2	DEDIF: Double	Error Detect	ion Interrupt Fl	ag			
	1 = Double Err						
	0 = No Double	Error Detect	ion occurred				
bit 1	SECIF: Single I	Error Correct	ion Interrupt FI	ag			
	1 = Single Erro						
	0 = No Single I	Error occurre	d				

REGISTER 3-5: ECCSTAT – ECC STATUS REGISTER

bit 0 Unimplemented: Read as '0'

3.2 CAN FD Controller Module Registers

Configuration Registers

- Register 3-6: CiCON
- Register 3-7: CiNBTCFG
- Register 3-8: CiDBTCFG
- Register 3-9: CiTDC
- Register 3-10: CiTBC
- Register 3-11: CiTSCON

Interrupt and Status Registers

- Register 3-12: CiVEC
- Register 3-13: CiINT
- Register 3-14: CiRXIF
- Register 3-15: CiRXOVIF
- Register 3-16: CiTXIF
- Register 3-17: CiTXATIF
- Register 3-18: CiTXREQ

Error and Diagnostic Registers

- Register 3-19: CiTREC
- Register 3-20: CiBDIAG0
- Register 3-21: CiBDIAG1

TABLE 3-4: REGISTER LEGEND

Fifo Control and Status Registers

- Register 3-22: CiTEFCON
- Register 3-23: CiTEFSTA
- Register 3-24: CiTEFUA
- Register 3-25: CiTXQCON
- Register 3-26: CiTXQSTA
- Register 3-27: CiTXQUA
- Register 3-28: CiFIFOCONm m = 1 to 31
- Register 3-29: CiFIFOSTAm m = 1 to 31
- Register 3-30: CiFIFOUAm m = 1 to 31

Filter Configuration and Control Registers

- Register 3-31: CiFLTCONm m = 0 to 7
- Register 3-32: CiFLTOBJm m = 0 to 31
- Register 3-33: CiMASKm m = 0 to 31

Note: The 'i' shown in the register identifier denotes CANi, e.g., C1CON. The MCP2517FD contains one CAN FD Controller Module.

Sym	Description	Sym	Description
R	Readable bit	HC	Cleared by Hardware only
W	Writable bit	HS	Set by Hardware only
U	Unimplemented bit, read as '0'	1	Bit is set at Reset
S	Settable bit	0	Bit is cleared at Reset
С	Clearable bit	х	Bit is unknown at Reset

EXAMPLE 3-2:

R/W - 0 indicates the bit is both readable and writable, and reads '0' after a Reset.

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REGISTER 3-6: CiCON – CAN CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-0
	TXBWS	6<3:0>		ABAT	I	REQOP<2:0>	
bit 31							bit 24
R-1	R-0	R-0	R/W-1	R/W-1	R/W-0	R/W-0	R/W-0
K-1	OPMOD<2:0>	K-0	TXQEN ⁽¹⁾	STEF ⁽¹⁾	SERR2LOM	ESIGM ⁽¹⁾	RTXAT ⁽¹⁾
	OF MOD <2.02			STERY		LOIGINI	RIARI [®] /
bit 23					· · · ·		bit 16
U-0	U-0	U-0	R/W-0	R-0	R/W-1	R/W-1	R/W-1
	_		BRSDIS	BUSY	WFT<	:1:0>	WAKFIL ⁽¹⁾
bit 15							bit 8
U-0	R/W-1	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
_	PXEDIS ⁽¹⁾	ISOCRCEN			DNCNT<4:0>		
bit 7							bit (
Legend:							
R = Readable		W = Writable I	oit		mented bit, read		
-n = Value at	POR	'1' = Bit is set		'0' = Bit is cle	eared	x = Bit is unki	nown
	0000 = No de 0001 = 2 0010 = 4 0011 = 8 0100 = 16 0101 = 32 0110 = 64 0111 = 128 1000 = 256 1001 = 512 1010 = 1024 1011 = 2048 1111-1100	= 4096			ion bit times)		
bit 27	1 = Signal all	All Pending Tran transmit FIFOs vill clear this bit	to abort trans		e aborted		
bit 26-24	000 = Set No 001 = Set Sle 010 = Set Inte 011 = Set List 100 = Set Co 101 = Set Ext 110 = Set No	ep mode ernal Loopback ten Only mode nfiguration mod ernal Loopback	node; supports mode le < mode node; possible	mixing of CA	N FD and Classi on CAN FD fram		mes

Note 1: These bits can only be modified in Configuration mode.

REGISTER 3-6:	CICON – CAN CONTROL	REGISTER ((CONTINUED)	1

bit 23-21	OPMOD<2:0> : Operation Mode Status bits 000 = Module is in Normal CAN FD mode; supports mixing of CAN FD and Classic CAN 2.0 frames 001 = Module is in Sleep mode 010 = Module is in Internal Loopback mode 011 = Module is in Listen Only mode 100 = Module is in Configuration mode 101 = Module is in External Loopback mode 110 = Module is Normal CAN 2.0 mode; possible error frames on CAN FD frames 111 = Module is Restricted Operation mode
bit 20	TXQEN : Enable Transmit Queue bit ⁽¹⁾ 1 = Enables TXQ and reserves space in RAM 0 = Don't reserve space in RAM for TXQ
bit 19	 STEF: Store in Transmit Event FIFO bit⁽¹⁾ 1 = Saves transmitted messages in TEF and reserves space in RAM 0 = Don't save transmitted messages in TEF
bit 18	SERR2LOM : Transition to Listen Only Mode on System Error bit ⁽¹⁾ 1 = Transition to Listen Only Mode 0 = Transition to Restricted Operation Mode
bit 17	ESIGM : Transmit ESI in Gateway Mode bit ⁽¹⁾ 1 = ESI is transmitted recessive when ESI of message is high or CAN controller error passive 0 = ESI reflects error status of CAN controller
bit 16	RTXAT : Restrict Retransmission Attempts bit ⁽¹⁾ 1 = Restricted retransmission attempts, CiFIFOCONm.TXAT is used 0 = Unlimited number of retransmission attempts, CiFIFOCONm.TXAT will be ignored
bit 15-13	Unimplemented: Read as '0'
bit 12	 BRSDIS: Bit Rate Switching Disable bit 1 = Bit Rate Switching is Disabled, regardless of BRS in the Transmit Message Object 0 = Bit Rate Switching depends on BRS in the Transmit Message Object
bit 11	BUSY : CAN Module is Busy bit 1 = The CAN module is transmitting or receiving a message 0 = The CAN module is inactive
bit 10-9	WFT<1:0>: Selectable Wake-up Filter Time bits 00 = T00FILTER 01 = T01FILTER 10 = T10FILTER 11 = T11FILTER
	Note: Please refer to Table 7-5.
bit 8	 WAKFIL: Enable CAN Bus Line Wake-up Filter bit⁽¹⁾ 1 = Use CAN bus line filter for wake-up 0 = CAN bus line filter is not used for wake-up
bit 7	Unimplemented: Read as '0'
bit 6	 PXEDIS: Protocol Exception Event Detection Disabled bit⁽¹⁾ A recessive "res bit" following a recessive FDF bit is called a Protocol Exception. 1 = Protocol Exception is treated as a Form Error. 0 = If a Protocol Exception is detected, the CAN FD Controller Module will enter Bus Integrating state.
bit 5	 ISOCRCEN: Enable ISO CRC in CAN FD Frames bit⁽¹⁾ 1 = Include Stuff Bit Count in CRC Field and use Non-Zero CRC Initialization Vector according to ISO 11898-1:2015 0 = Do NOT include Stuff Bit Count in CRC Field and use CRC Initialization Vector with all zeros

Note 1: These bits can only be modified in Configuration mode.

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REGISTER 3-6: CiCON – CAN CONTROL REGISTER (CONTINUED)

bit 4-0 DNCNT<4:0>: Device Net Filter Bit Number bits 10011-11111 = Invalid Selection (compare up to 18-bits of data with EID) 10010 = Compare up to data byte 2 bit 6 with EID17

> 00001 = Compare up to data byte 0 bit 7 with EID0 00000 = Do not compare data bytes

Note 1: These bits can only be modified in Configuration mode.

	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			BRP<	<7:0>			
bit 31							bit 24
R/W-0	R/W-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-0
			TSEG1	<7:0>			
bit 23							bit 1
	DAM 0						
U-0	R/W-0	R/W-0	R/W-0	R/W-1 TSEG2<6:0>	R/W-1	R/W-1	R/W-1
 bit 15				13EG2<0.0>			bit
							Ditt
U-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-1	R/W-1	R/W-1
_				SJW<6:0>			
bit 7							bit (
Legend:							
- J							
-	e bit	W = Writable	bit	U = Unimplen	nented bit, rea	ad as '0'	
R = Readable -n = Value at		W = Writable '1' = Bit is set		U = Unimplen '0' = Bit is clea		ad as '0' x = Bit is unk	nown
R = Readable -n = Value at	POR	'1' = Bit is set		•			nown
R = Readable	POR BRP<7:0>: B	'1' = Bit is set aud Rate Presc	caler bits	•			nown
R = Readable -n = Value at	POR BRP<7:0>: B	'1' = Bit is set	caler bits	•			nown
R = Readable -n = Value at	POR BRP<7:0>: B 1111 1111 =	'1' = Bit is set aud Rate Presc - TQ = 256/Fsys	caler bits	•			nown
R = Readable -n = Value at	POR BRP<7:0>: B 1111 1111 = 0000 0000 = TSEG1<7:0>:	'1' = Bit is set aud Rate Presc = TQ = 256/Fsys = TQ = 1/Fsys = Time Segmen	caler bits s t 1 bits (Propa	•	ared	x = Bit is unk	nown
R = Readable -n = Value at bit 31-24	POR BRP<7:0>: B 1111 1111 = 0000 0000 = TSEG1<7:0>:	'1' = Bit is set aud Rate Presc = TQ = 256/Fsys = TQ = 1/Fsys	caler bits s t 1 bits (Propa	ʻ0' = Bit is cle	ared	x = Bit is unk	nown
R = Readable -n = Value at bit 31-24	POR BRP<7:0>: B: 1111 1111 = 0000 0000 = TSEG1<7:0>: 1111 1111 = 	'1' = Bit is set aud Rate Presc = TQ = 256/Fsys = TQ = 1/Fsys : Time Segmen = Length is 256	caler bits s t 1 bits (Propa x TQ	ʻ0' = Bit is cle	ared	x = Bit is unk	nown
R = Readable -n = Value at bit 31-24	POR BRP<7:0>: Bi 1111 1111 = 0000 0000 = TSEG1<7:0> 1111 1111 = 0000 0000	'1' = Bit is set aud Rate Presc = TQ = 256/Fsys = TQ = 1/Fsys = Time Segmen	caler bits s t 1 bits (Propa x Tq Tq	ʻ0' = Bit is cle	ared	x = Bit is unk	nown
R = Readable -n = Value at bit 31-24 bit 23-16	POR BRP<7:0>: B 1111 1111 = 0000 0000 = TSEG1<7:0>: 1111 1111 = 0000 0000 Unimplemen	'1' = Bit is set aud Rate Presc TQ = 256/Fsys TQ = 1/Fsys Time Segmen Length is 256 = Length is 1 x	caler bits s t 1 bits (Propa x TQ TQ	ʻ0' = Bit is clea	ared	x = Bit is unk	nown
R = Readable -n = Value at bit 31-24 bit 23-16 bit 15	POR BRP<7:0>: B 1111 1111 = 0000 0000 = TSEG1<7:0>: 1111 1111 = 0000 0000 Unimplemen TSEG2<6:0>:	'1' = Bit is set aud Rate Presc = TQ = 256/Fsys = TQ = 1/Fsys : Time Segmen = Length is 256 = Length is 1 x ted: Read as '0	caler bits s t 1 bits (Propa x TQ TQ)' t 2 bits (Phase	ʻ0' = Bit is clea	ared	x = Bit is unk	nown
R = Readable -n = Value at bit 31-24 bit 23-16 bit 15	POR BRP<7:0>: B: 1111 1111 = 0000 0000 = TSEG1<7:0>: 1111 1111 = 0000 0000 Unimplemen TSEG2<6:0>: 111 1111 = 	'1' = Bit is set aud Rate Prese = TQ = 256/Fsys = TQ = 1/Fsys = Time Segment = Length is 256 = Length is 1 x ted: Read as '0' = Time Segment Length is 128 x	caler bits s t 1 bits (Propa x TQ TQ)' t 2 bits (Phase x TQ	ʻ0' = Bit is clea	ared	x = Bit is unk	nown
R = Readable -n = Value at bit 31-24 bit 23-16 bit 15 bit 14-8	POR BRP<7:0>: B 1111 1111 = 0000 0000 = TSEG1<7:0>: 1111 1111 = 0000 0000 Unimplemen TSEG2<6:0>: 111 1111 = 000 0000 =	'1' = Bit is set aud Rate Preso = $TQ = 256/Fsys$ = $TQ = 1/Fsys$: Time Segment = Length is 256 = Length is 1 x ted: Read as '0' : Time Segment Length is 1 x To Length is 1 x To	caler bits s t 1 bits (Propa x TQ TQ)' t 2 bits (Phase x TQ	ʻ0' = Bit is clea	ared	x = Bit is unk	nown
R = Readable -n = Value at bit 31-24 bit 23-16 bit 15 bit 14-8 bit 7	POR BRP<7:0>: Bi 1111 1111 = 0000 0000 = TSEG1<7:0>: 1111 1111 = 0000 0000 Unimplemen TSEG2<6:0>: 111 1111 = 000 0000 = Unimplemen	'1' = Bit is set aud Rate Presc = TQ = 256/Fsys = TQ = 1/Fsys : Time Segment = Length is 256 = Length is 1 x ted: Read as '0 Length is 1 x To ted: Read as '0	caler bits s t 1 bits (Propa x TQ TQ ,' t 2 bits (Phase x TQ Q	'0' = Bit is clea	ared	x = Bit is unk	nown
R = Readable -n = Value at bit 31-24 bit 23-16 bit 15 bit 14-8	POR BRP<7:0>: B: 1111 1111 = 0000 0000 = TSEG1<7:0>: 1111 1111 = 0000 0000 Unimplement TSEG2<6:0>: 111 1111 = 000 0000 = Unimplement SJW<6:0>: S	'1' = Bit is set aud Rate Preso = $TQ = 256/Fsys$ = $TQ = 1/Fsys$: Time Segment = Length is 256 = Length is 1 x ted: Read as '0' : Time Segment Length is 1 x To Length is 1 x To	caler bits s t 1 bits (Propa x TQ TQ)' t 2 bits (Phase x TQ Q) Jump Width b	'0' = Bit is clea	ared	x = Bit is unk	nown
R = Readable -n = Value at bit 31-24 bit 23-16 bit 15 bit 14-8 bit 7	POR BRP<7:0>: B: 1111 1111 = 0000 0000 = TSEG1<7:0>: 1111 1111 = 0000 0000 Unimplement TSEG2<6:0>: 111 1111 = 000 0000 = Unimplement SJW<6:0>: S 111 1111 = 	'1' = Bit is set aud Rate Preso = TQ = 256/Fsys = TQ = 1/Fsys = Time Segment = Length is 256 = Length is 1 x ted: Read as '0 Length is 1 x To ted: Read as '0 ynchronization	caler bits s t 1 bits (Propa x TQ TQ '' t 2 bits (Phase x TQ Q 2 Jump Width b : TQ	'0' = Bit is clea	ared	x = Bit is unk	nown

REGISTER 3-7: CINBTCFG – NOMINAL BIT TIME CONFIGURATION REGISTER

REGISTER 3-8: CIDBTCFG – DATA BIT TIME CONFIGURATION REGISTER

	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			BRP<	:7:0>			
bit 31							bit 2
U-0	U-0	U-0	R/W-0	R/W-1	R/W-1	R/W-1	R/W-0
—	—	—			TSEG1<4:0>		
bit 23							bit 1
U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-1	R/W-1
—	_	—	_		TSEG	2<3:0>	
bit 15							bit
U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-1	R/W-1
_	—	—	_		SJW	<3:0>	
bit 7							bit
Legend: R = Readabl	e bit	W = Writable	bit	U = Unimpler	nented bit, read	d as '0'	
-n = Value at		vv = vvritable (1) = Bit is set		0 = Unimpler		x = Bit is unki	
					areu		101011
bit 31-24	_	aud Rate Prese					
	1111 1111 =	: TQ = 256/Fsy	S				
		$T_{0} = 1/F_{0}/c$					
	0000 0000 =	· IQ - 1/FSYS					
bit 23-21		ted: Read as '	כי				
bit 23-21 bit 20-16	Unimplemen TSEG1<4:0>:	ted: Read as '	it 1 bits (Propa	gation Segmen	t + Phase Seg	ment 1)	
	Unimplemen TSEG1<4:0>:	ted: Read as 'o Time Segmen ngth is 32 x To	it 1 bits (Propa	gation Segmen	t + Phase Seg	ment 1)	
	Unimplement TSEG1<4:0>: 1 1111 = Ler 0 0000 = Ler	ted: Read as 'o Time Segmen ngth is 32 x To	it 1 bits (Propa	gation Segmen	t + Phase Seg	ment 1)	
bit 20-16	Unimplement TSEG1<4:0>: 1 1111 = Ler 0 0000 = Ler Unimplement TSEG2<3:0>:	ted: Read as ' Time Segmen ngth is 32 x To ngth is 1 x To ted: Read as ' Time Segmen	it 1 bits (Propa		t + Phase Seg	ment 1)	
bit 20-16 bit 15-12	Unimplement TSEG1<4:0>: 1 1111 = Ler 0 0000 = Ler Unimplement TSEG2<3:0>: 1111 = Lengt 	ted: Read as ' Time Segmen ngth is 32 x To ngth is 1 x To ted: Read as ' Time Segmen h is 16 x To	t 1 bits (Propa		t + Phase Seg	ment 1)	
bit 20-16 bit 15-12 bit 11-8	Unimplement TSEG1<4:0>: 1 1111 = Ler 0 0000 = Ler Unimplement TSEG2<3:0>: 1111 = Lengt 0000 = Lengt	ted: Read as ' Time Segmen ngth is 32 x To ngth is 1 x To ted: Read as ' Time Segmen h is 16 x To	t 1 bits (Propag)' It 2 bits (Phase		t + Phase Seg	ment 1)	
bit 20-16 bit 15-12	Unimplement TSEG1<4:0>: 1 1111 = Ler 0 0000 = Ler Unimplement TSEG2<3:0>: 1111 = Lengt 0000 = Lengt Unimplement	ted: Read as '(Time Segmen ngth is 32 x To ngth is 1 x To ted: Read as '(Time Segmen h is 16 x To h is 1 x To ted: Read as '(ynchronization	t 1 bits (Propag)' It 2 bits (Phase	e Segment 2)	t + Phase Seg	ment 1)	
bit 20-16 bit 15-12 bit 11-8 bit 7-4	Unimplement TSEG1<4:0>: 1 1111 = Ler 0 0000 = Ler Unimplement TSEG2<3:0>: 1111 = Lengt 0000 = Lengt Unimplement SJW<3:0>: S	ted: Read as '(Time Segmen ngth is $32 \times T_Q$ ngth is $1 \times T_Q$ ted: Read as '(Time Segmen h is $16 \times T_Q$ h is $1 \times T_Q$ ted: Read as '(ynchronization h is $16 \times T_Q$	t 1 bits (Propag)' it 2 bits (Phase	e Segment 2)	t + Phase Seg	ment 1)	

bit 31 bit 3 U-0 U-0 U-0 U-0 RW-1 RW-0 RW-1 RW-0 <	REGISTER	3-9. CIID(DATION REG	IJIER	
bit 31 bit 3 U-0 U-0 U-0 U-0 RW-1 RW-0 RW-1 RW-0 <	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
U-0 U-0 U-0 U-0 R/W-1 R/W-0 TDCMOD bit 0:123 bit bit bit bit bit U-0 R/W-0 R/W-0 R/W-1 R/W-0	_			—	—	—	EDGFLTEN	SID11EN
- - - - - TDCMOD<1:0> bit 23 bit bit bit bit U-0 R/W-0 R/W-0 R/W-0 R/W-0 R/W-0 R/W-0 - - TDCO<6:0> bit bit Dit 15 - TDCV<5:0> bit - - - TDCV<5:0> bit - - - TDCV<5:0> bit Legend: R = Readable bit W = Writable bit U = Unimplemented bit, read as '0' bit - - - - TDCV<5:0> bit Legend: R = Readable bit W = Writable bit U = Unimplemented bit, read as '0' bit - - - - - Bit Sunknown bit 31-26 Unimplemented: Read as '0' - EBGFLTEN: Enable Edge Filtering during Bus Integration state bit 1 = RRS is used as '0' 1 = RRS is used as '0' SUD 1 = RRS is used as '0' 1 = RRS is used as '0' 1 = RRS is used as '0' 1 = Cola + Lon Concola +	bit 31							bit 2
- - - - - TDCMOD<1:0> bit 23 bit bit bit bit U-0 R/W-0 R/W-0 R/W-0 R/W-0 R/W-0 R/W-0 - - TDCO<6:0> bit bit Dit 15 - TDCV<5:0> bit - - - TDCV<5:0> bit - - - TDCV<5:0> bit Legend: R = Readable bit W = Writable bit U = Unimplemented bit, read as '0' bit - - - - TDCV<5:0> bit Legend: R = Readable bit W = Writable bit U = Unimplemented bit, read as '0' bit - - - - - Bit Sunknown bit 31-26 Unimplemented: Read as '0' - EBGFLTEN: Enable Edge Filtering during Bus Integration state bit 1 = RRS is used as '0' 1 = RRS is used as '0' SUD 1 = RRS is used as '0' 1 = RRS is used as '0' 1 = RRS is used as '0' 1 = Cola + Lon Concola +								
bit 23 bit U-0 RW-0 R/W-0 R/W-1 R/W-0	U-0	<u> </u>	<u> </u>	U-0	<u> </u>	U-0		
U-0 R/W-0 R/W-1 R/W-0 R		—	—	_	—	—	TDCMO	
- TDCO<6:0> bit 15 bit - - <	DIL 23							DIL
- TDCO<6:0> bit 15 bit - - <	U-0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0
U-0 U-0 RW-0 R/W-0 R/W -0 R/W -0 R/	_							
- - TDCV<5:0> bit 7 bit Clegend: W = Writable bit U = Unimplemented bit, read as '0' on = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown bit 31-26 Unimplemented: Read as '0' EDGFLTEN: Enable Edge Filtering during Bus Integration state bit 1 = Edge Filtering enabled, according to ISO 11898-1:2015 0 = Edge Filtering enabled, according to ISO 11898-1:2015 bit 24 SID11EN: Enable 12-Bit SID in CAN FD Base Format Messages bit 1 = RRS is used as SID11 in CAN FD Base Format Messages: SID<11:0> = {SID<10:0>, SID11} 0 = Don't use RRS; SID<0:0> according to ISO 11898-1:2015 bit 23-18 bit 17-16 TDCMOD-1:0>: Transmitter Delay Compensation Mode bits; Secondary Sample Point (SSP) 10-11 = Auto; measure delay and add TDCO. 01 = Manual; Don't measure, use TDCV + TDCO from register 00 = TDC Disabled 01 bit 15 Unimplemented: Read as '0' TbCO<6:0>: Transmitter Delay Compensation Offset bits; Secondary Sample Point (SSP) Two's complement; offset can be positive, zero, or negative. 011 11111 = 63 x TSYSCLK """"""""""""""""""""""""""""""""""""	bit 15							bit
- - TDCV<5:0> bit 7 bit Clegend: W = Writable bit U = Unimplemented bit, read as '0' on = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown bit 31-26 Unimplemented: Read as '0' EDGFLTEN: Enable Edge Filtering during Bus Integration state bit 1 = Edge Filtering enabled, according to ISO 11898-1:2015 0 = Edge Filtering enabled, according to ISO 11898-1:2015 bit 24 SID11EN: Enable 12-Bit SID in CAN FD Base Format Messages bit 1 = RRS is used as SID11 in CAN FD Base Format Messages: SID<11:0> = {SID<10:0>, SID11} 0 = Don't use RRS; SID<0:0> according to ISO 11898-1:2015 bit 23-18 bit 17-16 TDCMOD-1:0>: Transmitter Delay Compensation Mode bits; Secondary Sample Point (SSP) 10-11 = Auto; measure delay and add TDCO. 01 = Manual; Don't measure, use TDCV + TDCO from register 00 = TDC Disabled 01 bit 15 Unimplemented: Read as '0' TbCO<6:0>: Transmitter Delay Compensation Offset bits; Secondary Sample Point (SSP) Two's complement; offset can be positive, zero, or negative. 011 11111 = 63 x TSYSCLK """"""""""""""""""""""""""""""""""""								
bit 7 bit Legend: R = Readable bit W = Writable bit U = Unimplemented bit, read as '0' n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown bit 31-26 Unimplemented: Read as '0' EDGFLTEN: Enable Edge Filtering during Bus Integration state bit 1 = Edge Filtering enabled, according to ISO 11898-1:2015 0 = Edge Filtering enabled, according to ISO 11898-1:2015 0 = Edge Filtering disabled bit 24 SID11EN: Enable 12-Bit SID in CAN FD base format Messages: SID<11:0> = {SID<10:0>, SID11} 0 = Don't use RRS; SID<10:0> according to ISO 11898-1:2015 bit 23-18 Unimplemented: Read as '0' ID on't use RRS; SID<10:0> according to ISO 11898-1:2015 bit 17-16 TDCMOD-1:0>: Transmitter Delay Compensation Mode bits; Secondary Sample Point (SSP) 10 - 11 = Auto; measure delay and add TDCO. 0 = Manual; Don't measure, use TDCV + TDCO from register 00 = TDC Disabled Dit 15 Unimplemented: Read as '0' Dit 14-8 TDCO-6:0>: Transmitter Delay Compensation Offset bits; Secondary Sample Point (SSP) Two's complement; offset can be positive, zero, or negative. 011 1111 = 63 x TSYSCLK .	U-0	U-0	R/W-0	R/W-0	-	-	R/W-0	R/W-0
Legend: R = Readable bit W = Writable bit U = Unimplemented bit, read as '0' -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown bit 31-26 Unimplemented: Read as '0' EDGFLTEN: Enable Edge Filtering during Bus Integration state bit 1 = Edge Filtering enabled, according to ISO 11898-1:2015 0 = Edge Filtering disabled bit 24 SID11EN: Enable 12-Bit SID in CAN FD Base Format Messages bit 1 = RRS is used as SID11 in CAN FD Base Format Messages bit 0 = Don't use RRS; SID-10:0-> according to ISO 11898-1:2015 bit 23-18 Unimplemented: Read as '0' 10 = Don't use RRS; SID-10:0-> according to ISO 11898-1:2015 bit 17-16 TDCMOD<1:0-> it manual; Don't measure delay and add TDCO. 01 = Manual; Don't measure, use TDCV + TDCO from register 00 = TDC Disabled bit 15 Unimplemented: Read as '0' Two's complement; offset can be positive, zero, or negative. 011 1111 = 63 x TSYSCLK 00 0000 = 0 x TSYSCLK	_				TDC	V<5:0>		
R = Readable bit W = Writable bit U = Unimplemented bit, read as '0' en = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown bit 31-26 Unimplemented: Read as '0' EDGFLTEN: Enable Edge Filtering during Bus Integration state bit 1 = Edge Filtering enabled, according to ISO 11898-1:2015 bit 25 EDGFLTEN: Enable Edge Filtering during bus Integration state bit 1 = Edge Filtering disabled bit 24 SID11EN: Enable 12-Bit SID in CAN FD Base Format Messages bit 1 = RRS is used as SID11 in CAN FD base format messages: SID<11:0> = {SID<10:0>, SID11} 0 = Don't use RRS; SID<10:0> according to ISO 11898-1:2015 bit 23-18 Unimplemented: Read as '0' bit 17-16 TDCMOD<1:0>: Transmitter Delay Compensation Mode bits; Secondary Sample Point (SSP) 10-11 = Auto; measure delay and add TDCO. 01 = Manual; Don't measure, use TDCV + TDCO from register 00 = TDC Disabled bit 15 Unimplemented: Read as '0' Two's complement; offset can be positive, zero, or negative. 011 1111 = 63 x TSYSCLK </td <td>bit 7</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>bit</td>	bit 7							bit
R = Readable bit W = Writable bit U = Unimplemented bit, read as '0' en = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown bit 31-26 Unimplemented: Read as '0' EDGFLTEN: Enable Edge Filtering during Bus Integration state bit 1 = Edge Filtering enabled, according to ISO 11898-1:2015 bit 25 EDGFLTEN: Enable Edge Filtering during bus Integration state bit 1 = Edge Filtering disabled bit 24 SID11EN: Enable 12-Bit SID in CAN FD Base Format Messages bit 1 = RRS is used as SID11 in CAN FD base format messages: SID<11:0> = {SID<10:0>, SID11} 0 = Don't use RRS; SID<10:0> according to ISO 11898-1:2015 bit 23-18 Unimplemented: Read as '0' bit 17-16 TDCMOD<1:0>: Transmitter Delay Compensation Mode bits; Secondary Sample Point (SSP) 10-11 = Auto; measure delay and add TDCO. 01 = Manual; Don't measure, use TDCV + TDCO from register 00 = TDC Disabled bit 15 Unimplemented: Read as '0' Two's complement; offset can be positive, zero, or negative. 011 1111 = 63 x TSYSCLK </td <td>Legend:</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td>	Legend:							
n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown bit 31-26 Unimplemented: Read as '0' EDGFLTEN: Enable Edge Filtering during Bus Integration state bit 1 = Edge Filtering enabled, according to ISO 11898-1:2015 0 = Edge Filtering disabled bit 24 SID11EN: Enable 12-Bit SID in CAN FD Base Format Messages bit 1 = RRS is used as SID11 in CAN FD Base format messages: SID<11:0> = {SID<10:0>, SID11} 0 = Don't use RRS; SID<10:0> according to ISO 11898-1:2015 0 = Don't use RRS; SID<10:0> according to ISO 11898-1:2015 bit 23-18 Unimplemented: Read as '0' 10 = 11 = Auto; measure delay and add TDCO. 10 = Manual; Don't measure, use TDCV + TDCO from register 00 = TDC Disabled bit 15 Unimplemented: Read as '0' bit 14-8 TDCO<6:0>: Transmitter Delay Compensation Offset bits; Secondary Sample Point (SSP) Two's complement; offset can be positive, zero, or negative. 011 1111 = 63 x TSYSCLK 00 0000 = 0 x TSYSCLK Tim 01 111 111 = -64 x TSYSCLK Tim 01 111 = 63 x TSYSCLK Tim 01 111 = 63 x TSYSCLK Tim 01 00000 = 0 x TSYSCLK Tim 01 00000 = 0 x TSYSCLK Tim 01 <t< td=""><td>-</td><td>le hit</td><td>W = Writable</td><td>hit</td><td>II = Unimple</td><td>mented hit re</td><td>ad as '0'</td><td></td></t<>	-	le hit	W = Writable	hit	II = Unimple	mented hit re	ad as '0'	
bit 31-26 Unimplemented: Read as '0' bit 25 EDGFLTEN: Enable Edge Filtering during Bus Integration state bit 1 = Edge Filtering enabled, according to ISO 11898-1:2015 0 = Edge Filtering disabled bit 24 SID11EN: Enable 12-Bit SID in CAN FD Base Format Messages bit 1 = RRS is used as SID11 in CAN FD base format messages: SID<11:0> = {SID<10:0>, SID11} 0 = Don't use RRS; SID<10:0> according to ISO 11898-1:2015 bit 23-18 Unimplemented: Read as '0' TDCMOD<1:0>: Transmitter Delay Compensation Mode bits; Secondary Sample Point (SSP) 10-11 = Auto; measure delay and add TDCO. 01 = Manual; Don't measure, use TDCV + TDCO from register 00 = TDC Disabled bit 15 Unimplemented: Read as '0' TbCO<6:0>: Transmitter Delay Compensation Offset bits; Secondary Sample Point (SSP) Two's complement; offset can be positive, zero, or negative. 011 1111 = 63 x TSYSCLK 111 1111 = -64 x TSYSCLK 111 1111 = -64 x TSYSCLK 00 0000 = 0 x TSYSCLK 011 1111 = 63 x TSYSCLK 011 1111 = 63 x TSYSCLK 011 00000 = 0 x TSYSCLK 011 1111 = 63 x TSYSCLK 011 00000 = 0 x TSYSCLK					•			nown
bit 23-18 Unimplemented: Read as '0' TDCMOD<1:0>: Transmitter Delay Compensation Mode bits; Secondary Sample Point (SSP) 10-11 = Auto; measure delay and add TDCO. 01 = Manual; Don't measure, use TDCV + TDCO from register 00 = TDC Disabled bit 15 Unimplemented: Read as '0' bit 14-8 TDCO<6:0>: Transmitter Delay Compensation Offset bits; Secondary Sample Point (SSP) Two's complement; offset can be positive, zero, or negative. 011 1111 = 63 x TSYSCLK 111 1111 = -64 x TSYSCLK bit 7-6 Unimplemented: Read as '0' TDCV<5:0>: Transmitter Delay Compensation Value bits; Secondary Sample Point (SSP) 11 1111 = 63 x TSYSCLK 00 0000 = 0 x TSYSCLK 00 0000 = 0 x TSYSCLK	bit 24	0 = Edge Fil SID11EN : Er 1 = RRS is u	tering disabled nable 12-Bit SID used as SID11 i) in CAN FD B n CAN FD bas	ase Format Me se format mess	essages bit sages: SID<11:	0> = {SID<10:0>	>, SID11}
bit 17-16 TDCMOD<1:0>: Transmitter Delay Compensation Mode bits; Secondary Sample Point (SSP) 10-11 = Auto; measure delay and add TDCO. 01 = Manual; Don't measure, use TDCV + TDCO from register 00 = TDC Disabled 00 = TDCO bit 15 Unimplemented: Read as '0' TDCO<6:0>: Transmitter Delay Compensation Offset bits; Secondary Sample Point (SSP) Two's complement; offset can be positive, zero, or negative. 011 1111 = 63 x TSYSCLK 00 0000 = 0 x TSYSCLK bit 5-0 TDCV<5:0>: Transmitter Delay Compensation Value bits; Secondary Sample Point (SSP)	bit 23-18			•				
bit 14-8 TDCO<6:0>: Transmitter Delay Compensation Offset bits; Secondary Sample Point (SSP) Two's complement; offset can be positive, zero, or negative. 011 1111 = 63 x TSYSCLK 000 0000 = 0 x TSYSCLK 111 1111 = -64 x TSYSCLK bit 7-6 Unimplemented: Read as '0' TDCV<5:0>: Transmitter Delay Compensation Value bits; Secondary Sample Point (SSP) 11 1111 = 63 x TSYSCLK 00 0000 = 0 x TSYSCLK 00 0000 = 0 x TSYSCLK	bit 17-16	TDCMOD<1 10-11 = Au 01 = Manual	:0> : Transmitter uto; measure de ; Don't measure	⁻ Delay Comp elay and add 1	FDCO.		ry Sample Point	(SSP)
Two's complement; offset can be positive, zero, or negative. 011 1111 = 63 x TSYSCLK 000 0000 = 0 x TSYSCLK 111 1111 = -64 x TSYSCLK bit 7-6 Unimplemented: Read as '0' TDCV<5:0>: Transmitter Delay Compensation Value bits; Secondary Sample Point (SSP) 11 1111 = 63 x TSYSCLK 00 0000 = 0 x TSYSCLK	bit 15	Unimplemer	nted: Read as '	0'				
 iii 1111 = -64 x TSYSCLK bit 7-6 Unimplemented: Read as '0' bit 5-0 TDCV<5:0>: Transmitter Delay Compensation Value bits; Secondary Sample Point (SSP) 11 1111 = 63 x TSYSCLK iii 00 0000 = 0 x TSYSCLK 	bit 14-8	Two's comple	ement; offset ca	in be positive,			Sample Point (SS	SP)
bit 7-6 Unimplemented: Read as '0' bit 5-0 TDCV<5:0>: Transmitter Delay Compensation Value bits; Secondary Sample Point (SSP) 11 1111 = 63 x TSYSCLK 00 0000 = 0 x TSYSCLK		 000 0000 =	0 x TSYSCLK					
bit 5-0 TDCV<5:0> : Transmitter Delay Compensation Value bits; Secondary Sample Point (SSP) 11 1111 = 63 x TSYSCLK 00 0000 = 0 x TSYSCLK		 111 1111 =	= -64 x TSYSC	LK				
11 1111 = 63 x TSYSCLK 00 0000 = 0 x TSYSCLK	bit 7-6	Unimplemer	nted: Read as '	0'				
	bit 5-0				ation Value bits	; Secondary S	ample Point (SS	P)
Note 1: This register can only be modified in Configuration mode.		 00 0000 = 0	x TSYSCLK					
	Note 1: T	his register can o	only be modified	d in Configura	tion mode.			

REGISTER 3-9: CITDC – TRANSMITTER DELAY COMPENSATION REGISTER

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REGISTER 3-10: CITBC – TIME BASE COUNTER REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
			TBC<	31:24>			-	
bit 31							bit 24	
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
			TBC<	23:16>				
bit 23							bit 16	
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
			TBC	<15:8>				
bit 15							bit 8	
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
			TBC	<7:0>				
bit 7							bit C	
Legend:								
R = Readable	bit	W = Writable	bit	it U = Unimplemented bit, rea				
-n = Value at POR		'1' = Bit is set		'0' = Bit is cleared		x = Bit is unknown		

bit 31-0 **TBC<31:0>**: Time Base Counter bits

This is a free running timer that increments every TBCPRE clocks when TBCEN is set

Note 1: The TBC will be stopped and reset when TBCEN = 0.

2: The TBC prescaler count will be reset on any write to CiTBC (CiTSCON.TBCPRE will be unaffected).

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—		_	_
bit 31							bit 24
U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	_	_	—	_	TSRES	TSEOF	TBCEN
bit 23		·					bit 16
U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
_		_	_	_	_		E<9:8>
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			TBCPRE	=<7:0>			
bit 7							bit C
Legend:							
R = Readabl		W = Writable		•	nented bit, rea		
-n = Value at	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unki	nown
bit 31-19	Unimplemer	nted: Read as 'o)'				
bit 18	1 = at sample	e Stamp res bit (e point of the bit le point of SOF					
bit 17	1 = Time Sta - RX no	e Stamp EOF bi imp when frame error until last b	is taken valid:				
	0 = Time Sta - Classic	error until the ei imp at "beginnir al Frame: at sai	nd of EOF lg" of Frame: mple point of S				
bit 16	0 = Time Sta - Classic - FD Fra	error until the ei imp at "beginnir al Frame: at sai me: see TSRES e Base Counter FBC	nd of EOF Ig" of Frame: mple point of S 5 bit.				
	0 = Time Sta - Classic - FD Fra TBCEN : Time 1 = Enable T 0 = Stop and	error until the ei imp at "beginnir al Frame: at sai me: see TSRES e Base Counter FBC	nd of EOF Ig" of Frame: mple point of S bit. Enable bit				
bit 16 bit 15-10 bit 9-0	0 = Time Sta - Classic - FD Fra TBCEN : Time 1 = Enable T 0 = Stop and Unimplemen TBCPRE<9: (error until the en imp at "beginnir al Frame: at san me: see TSRES e Base Counter FBC t reset TBC	nd of EOF Ig" of Frame: mple point of S bit. Enable bit , Counter Presca	OF aler bits			

REGISTER 3-12: CiVEC – INTERRUPT CODE REGISTER

U-0	R-1	R-0	R-0	R-0	R-0	R-0	R-0		
_		-	-	XCODE<6:0>(-	-			
bit 31							bit 24		
U-0	R-1	R-0	R-0	R-0	R-0	R-0	R-0		
			T.	XCODE<6:0>(1)				
bit 23							bit 16		
U-0	U-0	U-0	R-0	R-0	R-0	R-0	R-0		
_		<u> </u>			FILHIT<4:0> ⁽¹)			
bit 15							bit 8		
U-0	R-1	R-0	R-0	R-0	R-0	R-0	R-0		
0-0	R-I	R-0	-	CODE<6:0>(1)	-	K-U	K-0		
 bit 7					, 		bit 0		
							DILO		
Legend:									
R = Readable	bit	W = Writable b	pit	U = Unimpler	mented bit, rea	d as '0'			
-n = Value at F	POR	'1' = Bit is set		'0' = Bit is cle		x = Bit is unkr	nown		
	•	2.1.0 001							
bit 31	Unimplemen	ted: Read as '0'	,						
bit 30-24	-			de bits ⁽¹⁾					
nt 30-24	RXCODE<6:0> : Receive Interrupt Flag Code bits ⁽¹⁾ 1000001-1111111 = Reserved								
	1000000 = No interrupt								
	010000-011	1111 = Reserved	ł						
	0011111 = F	IFO 31 Interrupt	: (RFIF<31> s	et)					
		IFO 2 Interrupt (IFO 1 Interrupt (
		leserved. FIFO (
bit 23	Unimplemen	ted: Read as '0'	,						
bit 22-16	TXCODE<6:0)>: Transmit Inte	errupt Flag Co	de bits ⁽¹⁾					
		11111 = Reserv	ved						
	1000000 = N	lo interrupt 11111 = Reserv	ved						
	0100000-01		veu						
	0011111 = F	IFO 31 Interrupt	: (TFIF<31> s	et)					
		IEO 1 Interrupt (
		IFO 1 Interrupt (XQ Interrupt (TF							
bit 15-13		ted: Read as '0'							
bit 12-8	•	Filter Hit Numb							
	11111 = Filte	er 31							
	11110 = Filte	er 30							
	 00001 = Filte	er 1							
	00000 = Filte								
bit 7	Unimplemen	ted: Read as '0'	3						

REGISTER 3-12: CIVEC – INTERRUPT CODE REGISTER (CONTINUED)

- bit 6-0 **ICODE[6:0]**: Interrupt Flag Code bits⁽¹⁾
 - 1001011-1111111 = Reserved
 - 1001010 = Transmit Attempt Interrupt (any bit in CiTXATIF set)
 - 1001001 = Transmit Event FIFO Interrupt (any bit in CiTEFIF set)
 - 1001000 = Invalid Message Occurred (IVMIF/IE)
 - 1000111 = Operation Mode Change Occurred (MODIF/IE)
 - 1000110 = TBC Overflow (TBCIF/IE)
 - 1000101 = RX/TX MAB Overflow/Underflow (RX: message received before previous message was saved to memory; TX: can't feed TX MAB fast enough to transmit consistent data.) (SERRIF/IE)
 - 1000100 = Address Error Interrupt (illegal FIFO address presented to system) (SERRIF/IE)
 - 1000011 = Receive FIFO Overflow Interrupt (any bit in CiRXOVIF set)
 - 1000010 = Wake-up interrupt (WAKIF/WAKIE)
 - 1000001 = Error Interrupt (CERRIF/IE)
 - 1000000 = No interrupt
 - 0100000-0111111 = Reserved
 - 0011111 = FIFO 31 Interrupt (TFIF<31> or RFIF<31> set)
 - 0000001 = FIFO 1 Interrupt (TFIF<1> or RFIF<1> set) 0000000 = TXQ Interrupt (TFIF<0> set)
- **Note 1:** If multiple interrupts are pending, the interrupt with the highest number will be indicated.

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R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
IVMIE	WAKIE	CERRIE	SERRIE	RXOVIE	TXATIE	SPICRCIE	ECCIE
bit 31							bit 24
U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			TEFIE	MODIE	TBCIE	RXIE	TXIE
bit 23							bit 16
HS/C-0	HS/C-0	HS/C-0	HS/C-0	R-0	R-0	R-0	R-0
IVMIF ⁽¹⁾	WAKIF ⁽¹⁾	CERRIF ⁽¹⁾	SERRIF ⁽¹⁾	RXOVIF	TXATIF	SPICRCIF	ECCIF
bit 15							bit 8
			D 0	110/0.0	110/0.0		
U-0	U-0	U-0	R-0	HS/C-0 MODIF ⁽¹⁾	HS/C-0 TBCIF ⁽¹⁾	R-0	R-0
			TEFIF	MODIF	I BCIF(')	RXIF	TXIF
bit 7							bit (
Legend:							
R = Readable I	hit	W = Writable	hit	II = I Inimplen	nented bit, rea	d as '0'	
-n = Value at P		'1' = Bit is set		'0' = Bit is clea		x = Bit is unkn	
		1 - Dit 13 301			aicu	X – Dit 13 uliki	
bit 31		Message Inter	runt Enable bit				
bit 30		Nake Up Interr	•	L			
bit 29		N Bus Error Inte	•	it			
bit 28		tem Error Interr	-				
bit 27	•	eive FIFO Ove	•	Enable bit			
bit 26		smit Attempt In	•				
bit 25		PI CRC Error Ir	-				
bit 24		Error Interrupt	•				
bit 23-21		ted: Read as '0					
bit 20	-	mit Event FIFO		ole bit			
bit 19		e Change Interr					
bit 18		Base Counter I	-	e bit			
bit 17		e FIFO Interrup	-				
bit 16		it FIFO Interrup					
bit 15		Message Inter)			
bit 14		Vake Up Interru					
bit 13		Bus Error Inte		1)			
bit 12		em Error Interr					
	1 = A system	error occurred n error occurre					
bit 11		eive Object Ov FIFO overflow o		t Flag bit			
				4			
hit 10	0 = No receiv	e FIFO overflo	w has occurred				
bit 10 bit 9	0 = No receiv TXATIF : Trans		w has occurred terrupt Flag bit				

REGISTER 3-13: CIINT – INTERRUPT REGISTER (CONTINUED)

bit 8	ECCIF: ECC Error Interrupt Flag bit
bit 7-5	Unimplemented: Read as '0'
bit 4	TEFIF : Transmit Event FIFO Interrupt Flag bit 1 = TEF interrupt pending 0 = No TEF interrupts pending
bit 3	 MODIF: Operation Mode Change Interrupt Flag bit⁽¹⁾ 1 = Operation mode change occurred (OPMOD has changed) 0 = No mode change occurred
bit 2	TBCIF : Time Base Counter Overflow Interrupt Flag bit ⁽¹⁾ 1 = TBC has overflowed 0 = TBC didn't overflow
bit 1	 RXIF: Receive FIFO Interrupt Flag bit 1 = Receive FIFO interrupt pending 0 = No receive FIFO interrupts pending
bit 0	TXIF : Transmit FIFO Interrupt Flag bit 1 = Transmit FIFO interrupt pending 0 = No transmit FIFO interrupts pending
Note 1:	Flags are set by hardware and cleared by application.

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REGISTER 3-14: CIRXIF – RECEIVE INTERRUPT STATUS REGISTER

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
			RFIF	<31:24>			
bit 31							bit 24
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
			RFIF	<23:16>			
bit 23							bit 16
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
				<15:8>			
bit 15							bit 8
R-0	R-0	R-0	R-0	R-0	R-0	R-0	U-0
			RFIF<7:1>				—
bit 7							bit (
Legend:							
R = Readable b	it	W = Writable	bit	U = Unimpler	nented bit, re	ead as '0'	
-n = Value at PC	DR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unknown	

1 = One or more enabled receive FIFO interrupts are pending
 0 = No enabled receive FIFO interrupts are pending

bit 0 Unimplemented: Read as '0'

Note 1: RFIF = 'or' of enabled RXFIFO flags; flags will be cleared when the condition of the FIFO terminates.

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
			RFOVI	F<31:24>			
bit 31							bit 24
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
			RFOVI	F<23:16>			
bit 23							bit 16
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
			RFOV	IF<15:8>			
bit 15							bit 8
R-0	R-0	R-0	R-0	R-0	R-0	R-0	U-0
		R	OVIF<7:1	>			—
bit 7							bit (
Legend:							
R = Readable bi	t	W = Writable bi	t	U = Unimplen	nented bit, re	ead as '0'	
-n = Value at POR '1' = Bit is set			'0' = Bit is cleared		x = Bit is unknown		

REGISTER 3-15: CIRXOVIF – RECEIVE OVERFLOW INTERRUPT STATUS REGISTER

1 = Interrupt is pending

0 = Interrupt not pending

bit 0 Unimplemented: Read as '0'

Note 1: Flags need to be cleared in FIFO register

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REGISTER 3-16:	CITXIF – TRANSMIT INTERRUPT STATUS REGISTER	
----------------	---	--

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
			TFIF<	31:24>			
bit 31							bit 24
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
			TFIF<2	3:16> ⁽¹⁾			
bit 23							bit 10
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
			TFIF<1	5:8> ⁽¹⁾			
bit 15							bit 8
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
			TFIF<	7:0> ⁽¹⁾			
bit 7							bit
Legend:							
R = Readable I	bit	W = Writable bit		U = Unimpler	nented bit, re	ead as '0'	
-n = Value at P	OR	'1' = Bit is set		'0' = Bit is cleared x = Bit is unknown			nown

TFIF<31:0>: Transmit FIFO/TXQ ⁽²⁾ Interrupt Pending bits⁽¹⁾ 1 = One or more enabled transmit FIFO/TXQ interrupts are pending bit 31-0

0 = No enabled transmit FIFO/TXQ interrupt are pending

Note 1: TFIF = 'or' of the enabled TXFIFO flags; flags will be cleared when the condition of the FIFO terminates.

2: TFIF<0> is for the Transmit Queue.

			TFATIF	<7:0> ⁽¹⁾			
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
bit 15							bit
			TFATIF	<15:8> ⁽¹⁾			
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
bit 23							bit 1
			TFATIF	<23:16> ⁽¹⁾			
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
bit 51							Dit 2
bit 31			IFAILES	-31.242(7)			bit 2
R-0	R-0	R-0	R-0	R-0 <31:24> ⁽¹⁾	R-0	R-0	R-0

REGISTER 3-17: CITXATIF – TRANSMIT ATTEMPT INTERRUPT STATUS REGISTER

bit 31-0 **TFATIF<31:0>**: Transmit FIFO/TXQ ⁽²⁾ Attempt Interrupt Pending bits⁽¹⁾ 1 = Interrupt is pending 0 = Interrupt not pending

Note 1: Flags need to be cleared in FIFO register.

2: TFATIF<0> is for the Transmit Queue.

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REGISTER 3-18: CITXREQ – TRANSMIT REQUEST REGISTER

S/HC-0	S/HC-0	S/HC-0	S/HC-0	S/HC-0	S/HC-0	S/HC-0	S/HC-0
			TXREQ	<31:24>			
bit 31							bit 24
S/HC-0	S/HC-0	S/HC-0	S/HC-0	S/HC-0	S/HC-0	S/HC-0	S/HC-0
			TXREQ	<23:16>			
bit 23							bit 16
0/110-0	0/110.0	0/110 0	0/110.0	0/110 0	0/110.0	0/110 0	0/110 0
S/HC-0	S/HC-0	S/HC-0	S/HC-0	S/HC-0	S/HC-0	S/HC-0	S/HC-0
h:+ 4 F			IXREG	(<15:8>			bit 0
bit 15							bit 8
S/HC-0	S/HC-0	S/HC-0	S/HC-0	S/HC-0	S/HC-0	S/HC-0	S/HC-0
			TXRE	Q<7:0>			
bit 7							bit 0
Legend:							
R = Readable	hit	W = Writable	hit	II – Unimplor	monted hit rea	vd aa '0'	
				U = Unimplemented bit, read as '0' '0' = Bit is cleared x = Bit is u			20112
-n = Value at F	UR .	'1' = Bit is set		U = Bit is cie	ared	x = Bit is unk	nown
bit 31-1	<u>TXEN= 1</u> (O Setting this t The bit will a This bit can	1>: Message Se bject configured bit to '1' requests utomatically clea NOT be used f bject configured no effect	as a Transmi s sending a m ar when the m or aborting a	t Object) essage. lessage(s) quet l transmission .		ct is (are) succ	essfully sent.
bit 0	Setting this t The bit will a	Transmit Queue bit to '1' requests utomatically clea	s sending a m ar when the m	essage. Iessage(s) quei	ied in the obje	ct is (are) succ	essfully sent.

This bit can NOT be used for aborting a transmission.

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
_	_	—	—		—	—	
bit 31							bit 24
U-0	U-0	R-1	R-0	R-0	R-0	R-0	R-0
		ТХВО	TXBP	RXBP	TXWARN	RXWARN	EWARN
bit 23							bit 16
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
			TEC<	7:0>			
bit 15							bit 8
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
			REC<	7:0>			
bit 7							bit 0
Lananda							
Legend:			L:4		mented bit rea		
R = Readab		W = Writable I	DIT	-	mented bit, rea		
-n = Value a	TPOR	'1' = Bit is set		'0' = Bit is cle	eared	x = Bit is unkr	IOWN
bit 31-22	Unimplemen	ted: Read as '0	,				
bit 21	-	mitter in Bus Of		C > 255)			
					not on the bus.		
bit 20	TXBP: Transr	nitter in Error P	assive State bi	it (TEC > 127))		
bit 19	RXBP: Recei	ver in Error Pas	sive State bit (REC > 127)			
bit 18	TXWARN: Tra	ansmitter in Erro	or Warning Sta	te bit (128 > 1	TEC > 95)		
bit 17	RXWARN: Re	eceiver in Error	Warning State	bit (128 > RE	C > 95)		
bit 16	EWARN: Trar	nsmitter or Rece	eiver is in Error	r Warning Stat	te bit		

REGISTER 3-19: CITREC – TRANSMIT/RECEIVE ERROR COUNT REGISTER

TEC<7:0>: Transmit Error Counter bits

REC<7:0>: Receive Error Counter bits

bit 15-8

bit 7-0

REGISTER 3-20: CiBDIAG0 – BUS DIAGNOSTIC REGISTER 0

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			DTERRO	CNT<7:0>			
bit 31							bit 24
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			DRERRO	CNT<7:0>			
bit 23							bit 16
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			NTERRO	CNT<7:0>			
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			NRERR	CNT<7:0>			
bit 7							bit 0
Legend:							
R = Readab	le bit	W = Writable	bit	U = Unimpler	mented bit, re	ad as '0'	
-n = Value at POR '1' = Bit is set			'0' = Bit is cle	ared	x = Bit is unknown		
bit 31-24	DTERRCNT	[<7:0> : Data Bit	Rate Transmi	t Error Counter	bits		
bit 23-16	DRERRCN	Г<7:0> : Data Bit	Rate Receive	Error Counter I	bits		
bit 15-8	NTERRONT	[<7:0> : Nominal	Bit Rate Tran	smit Error Coun	ter hits		

bit 15-8 NTERRCNT<7:0>: Nominal Bit Rate Transmit Error Counter bits

bit 7-0 NRERRCNT<7:0>: Nominal Bit Rate Receive Error Counter bits

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0		
DLCMM	ESI	DCRCERR	DSTUFERR	DFORMERR	_	DBIT1ERR	DBIT0ERR		
bit 31							bit 24		
R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
TXBOERR	—	NCRCERR	NSTUFERR	NFORMERR	NACKERR	NBIT1ERR	NBIT0ERR		
bit 23							bit 16		
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
	-		EFMSGC	NT<15:8>	-	-			
bit 15							bit 8		
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
10,00-0	10.00-0	10.00-0	EFMSGC	-	10.00-0	1000-0	10.00-0		
bit 7			21 110000				bit 0		
Legend:									
R = Readable bit W = Writable bit			bit	U = Unimplemented bit, read as '0'					
-n = Value at F	OR	'1' = Bit is set		'0' = Bit is clea	ared	x = Bit is unk	nown		
bit 31 bit 30	During a tran	C Mismatch bit smission or reco of a received C			rger than the F	PLSIZE of the F	FIFO element.		
bit 29	-	Same as for nor		-					
bit 28		Same as for no	•						
bit 27		: Same as for n							
bit 26	Unimplemer	nted: Read as 'o)'						
bit 25	DBIT1ERR: S	Same as for nor	minal bit rate (s	ee below).					
bit 24	DBIT0ERR: S	Same as for nor	ninal bit rate (s	see below).					
bit 23	TXBOERR: [Device went to b	ous-off (and au	to-recovered).					
bit 22	Unimplemer	nted: Read as 'o)'						
bit 21		The CRC checl es not match wit					f an incoming		
bit 20	•	More than 5 e					ved message		
bit 19	NFORMERR	: A fixed format	part of a receiv	ved frame has t	he wrong form	at.			
bit 18		Transmitted me	-		-				
bit 17		During the trans ed to send a rea							
bit 16	flag), the de	During the transi vice wanted to is value was rec	send a domin						
bit 15-0	EFMSGCNT	<15:0>: Error Fi	ree Message C	Counter bits					

REGISTER 3-21: CiBDIAG1 – BUS DIAGNOSTICS REGISTER 1

REGISTER 3-22:	CITEFCON – TRANSMIT EVENT FIFO CONTROL REGISTER
----------------	---

	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
_	—	—			FSIZE<4:0> ⁽¹⁾		
oit 31							bit 2
U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
0-0	0-0	0-0	0-0	0-0	0-0	0-0	0-0
 bit 23							 bit 1
U-0	U-0	U-0	U-0	U-0	S/HC-1	U-0	S/HC-0
—	—	—	_	—	FRESET	_	UINC
bit 15							bit
U-0	U-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
		TEFTSEN ⁽¹⁾	_	TEFOVIE	TEFFIE	TEFHIE	TEFNEIE
bit 7							bit
Legend:							
R = Readable bitW = Writable bitU = Unimplemented bit, read							
n = Value at	t POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unk	nown
	0_0010 = FI 	FO is 2 Message FO is 3 Message FO is 32 Message	es deep				
bit 23-11		nted: Read as '0					
oit 10	FRESET: FIF						
		Il be reset when	bit is set. clea				
	0 = No effect		efore taking a		are when FIFO	was reset. Th	ne user shou
bit 9			efore taking a		are when FIFO	was reset. Th	ie user shou
	Unimplemen UINC: Increm	t n ted: Read as '0 nent Tail bit	efore taking a ,	ny action.		was reset. Th	ie user shou
bit 8	Unimplement UINC: Increment When this bir	t n ted: Read as '0 nent Tail bit t is set, the FIFO	efore taking a , tail will increr	ny action.		was reset. Th	ne user shou
bit 8 bit 7-6	Unimplement UINC: Increment When this bir Unimplement	t nted: Read as '0 nent Tail bit t is set, the FIFO nted: Read as '0	efore taking a , , tail will increr ,	ny action. ment by a single	e message.	was reset. Tr	ne user shou
bit 8 bit 7-6	Unimplement UINC: Increment When this bit Unimplement TEFTSEN: T 1 = Time Sta	t nted: Read as '0 nent Tail bit t is set, the FIFO nted: Read as '0 Transmit Event Fl amp objects in TI	efore taking a , tail will increr , FO Time Star EF	ny action. ment by a single	e message.	was reset. Tr	ie user shou
bit 8 bit 7-6 bit 5	Unimplement UINC: Increment When this bir Unimplement TEFTSEN: T 1 = Time State 0 = Don't Time	t nted: Read as '0 nent Tail bit t is set, the FIFO nted: Read as '0 Transmit Event FI	efore taking a , tail will increr , FO Time Star EF s in TEF	ny action. ment by a single	e message.	was reset. Tr	ne user shou
bit 9 bit 8 bit 7-6 bit 5 bit 4 bit 3	Unimplement UINC: Increment When this bit Unimplement TEFTSEN: T 1 = Time Sta 0 = Don't Time Unimplement TEFOVIE: The 1 = Interrupt	et nted: Read as '0 nent Tail bit t is set, the FIFO nted: Read as '0 Transmit Event Fi amp objects in Ti me Stamp object	efore taking a , tail will increr , FO Time Star EF s in TEF , FO Overflow I rflow event	ny action. ment by a single np Enable bit ^{(1}	e message.)	was reset. Tr	ie user shou
pit 8 pit 7-6 pit 5 pit 4	Unimplement UINC: Increment When this bit Unimplement TEFTSEN: T 1 = Time Stat 0 = Don't Time Unimplement TEFOVIE: The 1 = Interrupt 0 = Interrupt TEFFIE: Transition 1 = Interrupt	et nted: Read as '0 nent Tail bit t is set, the FIFO nted: Read as '0 Transmit Event FI amp objects in TI me Stamp object nted: Read as '0 ransmit Event FII t enabled for ove	efore taking a , tail will increr FO Time Star FF s in TEF , FO Overflow I rflow event orflow event o Full Interrup O full	ny action. ment by a single mp Enable bit ^{(1} Interrupt Enable	e message.)	was reset. Th	ie user shou

REGISTER 3-22: CITEFCON – TRANSMIT EVENT FIFO CONTROL REGISTER (CONTINUED)

bit 1	TEFHIE : Transmit Event FIFO Half Full Interrupt Enable bit
	1 = Interrupt enabled for FIFO half full0 = Interrupt disabled for FIFO half full
bit 0	TEFNEIE: Transmit Event FIFO Not Empty Interrupt Enable

- ole bit
 - 1 = Interrupt enabled for FIFO not empty
 - 0 = Interrupt disabled for FIFO not empty
- **Note 1:** These bits can only be modified in Configuration mode.

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U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	_		_	_		—	—
bit 31				•			bit 24
U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
_	_	_	_	_	_	_	_
bit 23				L			bit 16
U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	_	_	_	_	_	—	—
bit 15	·					•	bit 8
U-0	U-0	U-0	U-0	HS/C-0	R-0	R-0	R-0
	_			TEFOVIF	TEFFIF ⁽¹⁾	TEFHIF ⁽¹⁾	TEFNEIF ⁽¹⁾
bit 7							bit 0
Legend:							
R = Readabl	le bit	W = Writable	bit	U = Unimpler	mented bit, rea	d as '0'	
-n = Value at	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unk	nown
bit 31-4	Unimplemen	ted: Read as '	0'				
bit 3	1 = Overflow	ansmit Event Fl event has occ low event occu	urred	nterrupt Flag b	it		
bit 2	TEFFIF: Tran 1 = FIFO is fi 0 = FIFO is n		O Full Interrup	t Flag bit ^(1)			
bit 1	TEFHIF : Tran 1 = FIFO is ≥ 0 = FIFO is <		O Half Full Inte	errupt Flag bit ⁽	1)		
bit 0		ansmit Event Fl			bit ⁽¹⁾		

1 = FIFO is not empty, contains at least one message

0 = FIFO is empty

Note 1: This bit is read only and reflects the status of the FIFO.

R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
			TEFUA	<31:24>			
bit 31							bit 24
R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
			TEFUA	<23:16>			
bit 23							bit 16
R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
			TEFU	A<15:8>			
bit 15							bit 8
R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
			TEFU	A<7:0>			
bit 7							bit C
Legend:							
R = Readable bit		W = Writable bit		U = Unimpler	nented bit, re	ead as '0'	
-n = Value at POR		'1' = Bit is set	0' = Bit is cleared x = Bit is unknown				nown

REGISTER 3-24: CITEFUA – TRANSMIT EVENT FIFO USER ADDRESS REGISTER

bit 31-0 TEFUA<31:0>: Transmit Event FIFO User Address bits

A read of this register will return the address where the next object is to be read (FIFO tail).

Note 1: This register is not guaranteed to read correctly in Configuration mode and should only be accessed when the module is not in Configuration mode.

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REGISTER 3-25: CITXQCON – TRANSMIT QUEUE CONTROL REGI	STER
---	------

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PLSIZE<2:0> ⁽¹⁾				FSIZE<4:0>(1)		
bit 31							bit 2
U-0	R/W-1	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
		۲ <u>۲</u> ۲-۱:0>		10.00-0	TXPRI<4:0>	1000-0	1444-0
bit 23	1700	1.0			1741141-4.02		bit 1
U-0	U-0	U-0	U-0	U-0	S/HC-1	R/W/HC-0	S/HC-0
		_	_	_	FRESET ⁽³⁾	TXREQ ⁽²⁾	UINC
bit 15							bit 8
R-1	U-0	U-0	R/W-0	U-0	R/W-0	U-0	R/W-0
TXEN			TXATIE	_	TXQEIE		TXQNIE
bit 7			170 the		indelle		bit (
Legend:							
R = Readabl	e bit	W = Writable	bit	•	mented bit, read	d as '0'	
-n = Value at	POR	'1' = Bit is set	t	'0' = Bit is cl	eared	x = Bit is unkn	own
	010 = 16 data 011 = 20 data 100 = 24 data 101 = 32 data 110 = 48 data 111 = 64 data	a bytes a bytes a bytes a bytes a bytes					
bit 28-24	0_0000 = FIF 0_0001 = FIF	FIFO Size bits FO is 1 Messag FO is 2 Messag FO is 3 Messag	je deep jes deep				
	1_1111 = FIF	O is 32 Messa	ages deep				
bit 23	Unimplemen	ted: Read as '	0'				
bit 22-21	This feature is 00 = Disable 01 = Three re 10 = Unlimite	Retransmissior s enabled when retransmission etransmission a d number of re d number of re	n CiCON.RTXA attempts attempts transmission a	ttempts			
bit 20-16		Message Tran est Message P		S			
2: T	11111 = High hese bits can onl his bit is updated RESET is set wh	when a messa	n Configuration	(or aborts) or			

REGISTER 3-25: CITXQCON – TRANSMIT QUEUE CONTROL REGISTER (CONTINUED)

bit 15-11	Unimplemented: Read as '0'						
bit 10	 FRESET: FIFO Reset bit⁽³⁾ 1 = FIFO will be reset when bit is set; cleared by hardware when FIFO was reset. User should wait until this bit is clear before taking any action. 0 = No effect 						
bit 9	 TXREQ: Message Send Request bit⁽²⁾ 1 = Requests sending a message; the bit will automatically clear when all the messages queued the TXQ are successfully sent. 0 = Clearing the bit to '0' while set ('1') will request a message abort. 						
bit 8	UINC : Increment Head bit When this bit is set, the FIFO head will increment by a single message.						
bit 7	TXEN : TX Enable 1 = Transmit Message Queue. This bit always reads as '1'.						
bit 6-5	Unimplemented: Read as '0'						
bit 4	TXATIE : Transmit Attempts Exhausted Interrupt Enable bit 1 = Enable interrupt 0 = Disable interrupt						
bit 3	Unimplemented: Read as '0'						
bit 2	TXQEIE : Transmit Queue Empty Interrupt Enable bit 1 = Interrupt enabled for TXQ empty 0 = Interrupt disabled for TXQ empty						
bit 1	Unimplemented: Read as '0'						
bit 0	TXQNIE : Transmit Queue Not Full Interrupt Enable bit 1 = Interrupt enabled for TXQ not full 0 = Interrupt disabled for TXQ not full						
Note 1:	These bits can only be modified in Configuration mode.						
2:	This bit is updated when a message completes (or aborts) or when the FIFO is reset.						

3: FRESET is set while in Configuration mode and is automatically cleared in Normal mode.

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REGISTER 3-26: CITXQSTA – TRANSMIT QUEUE STATUS REGISTER

		STA - TRANC					
U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
<u> </u>			_	—		_	
bit 31							bit 2
U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
			_	_		_	_
bit 23							bit 1
U-0	U-0	U-0	R-0	R-0	R-0	R-0	R-0
_	_	_			TXQCI<4:0>(1)		
bit 15							bit
HS/C-0	HS/C-0	HS/C-0	HS/C-0	U-0	R-1	U-0	R-1
TXABT ⁽²⁾⁽³⁾	TXLARB (2)(3)	TXERR ⁽²⁾⁽³⁾	TXATIF	-	TXQEIF	_	TXQNIF
bit 7							bit
Legend:							
R = Readable I	hit	W = Writable b	vit	II = I Inimple	mented bit, read	1 as 'O'	
-n = Value at P		'1' = Bit is set	Л	'0' = Bit is cle		x = Bit is unl	(00)//0
bit 7	TXABT: Mess	sage Aborted Sta was aborted	atus bit ⁽²⁾⁽³⁾		e that the FIFO w		
bit 6	0 = Message TXLARB: Me	completed suce ssage Lost Arbi	tration Status				
	0 = Message	lost arbitration did not loose a	rbitration while	e being sent			
bit 5	1 = A bus err	r Detected Durin or occurred whi or did not occur	le the messag	ge was being s			
bit 4		smit Attempts E pending		•	•		
bit 3	•	ted: Read as '0	,				
bit 2	•	nsmit Queue Em		Flag bit			
	1 = TXQ is e			-	transmitted		
bit 1		ted: Read as '0	-	1			
bit 0	-	nsmit Queue No ot full		t Flag bit			
					e TXQ. If the TX on the state of t		ges deep
	-	when TXREQ is					
			-		when the TXQ is	reset.	

R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
			TXQUA	<31:24>			
bit 31							bit 24
R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
			TXQUA	<23:16>			
bit 23							bit 16
R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
			TXQU	٩<15:8>			
bit 15							bit 8
R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
			TXQU	A<7:0>			
bit 7							bit (
Legend:							
R = Readable bit		W = Writable	oit	U = Unimpler	mented bit, re	ead as '0'	
-n = Value at POR		'1' = Bit is set		'0' = Bit is cle		x = Bit is unk	nown

REGISTER 3-27: CITXQUA – TRANSMIT QUEUE USER ADDRESS REGISTER

bit 31-0 TXQUA<31:0>: TXQ User Address bits

A read of this register will return the address where the next message is to be written (TXQ head).

Note 1: This register is not guaranteed to read correctly in Configuration mode and should only be accessed when the module is not in Configuration mode.

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R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PLSIZE<2:0>(1)			FSIZE<4:0>(1)	
bit 31							bit 2
	- - - - - - - - - -	D a a a a	B 444 A	-	54446	B 844 6	
U-0	R/W-1	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
-	TXA	T<1:0>			TXPRI<4:0>		
bit 23							bit 1
U-0	U-0	U-0	U-0	U-0	S/HC-1	R/W/HC-0	S/HC-0
	_	—		_	FRESET ⁽³⁾	TXREQ ⁽²⁾	UINC
bit 15							bit
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
TXEN ⁽¹⁾	RTREN	RXTSEN ⁽¹⁾	TXATIE	RXOVIE	TFERFFIE	TFHRFHIE	TFNRFNIE
bit 7							bit
Legend:			.:4		mented bit me	d ee (0)	
R = Readabl		W = Writable k	DIT	•	mented bit, rea		
-n = Value at	POR	'1' = Bit is set		'0' = Bit is cl	eared	x = Bit is unk	nown
	010 = 16 dat 011 = 20 dat 100 = 24 dat 101 = 32 dat 110 = 48 dat 111 = 64 dat	a bytes a bytes a bytes a bytes a bytes					
bit 28-24	FSIZE<4:0>:	FIFO Size bits ⁽	1)				
	0_0001 = FI	FO is 1 Message FO is 2 Message FO is 3 Message	es deep				
	1_1111 = F	IFO is 32 Messa	iges deep				
bit 23	Unimplemer	nted: Read as '0	,				
bit 22-21	This feature i 00 = Disable 01 = Three r 10 = Unlimite	Retransmission is enabled when retransmission at etransmission at ed number of retu- ed number of retu-	CiCON.RTX attempts tempts ransmission a	AT is set. attempts			
bit 20-16	TXPRI<4:0> 00000 = Lor	: Message Trans west Message P	smit Priority b	-			
	 11111 = Hig	hest Message P	riority				
Note 1: T	hese bits can on	-	-	n mode.			
2: TI	his bit is updated	l when a messag	ge completes	(or aborts) or	when the FIFO	is reset.	
3: FI	RESET is set wh	nile in Configurat	ion mode and	d is automatica	Ily cleared in No	ormal mode.	

3: FRESET is set while in Configuration mode and is automatically cleared in Normal mode.

REGIS	STER	3-28: CIFIFOCONm – FIFO CONTROL REGISTER m, (m = 1 TO 31) (CONTINUED)
bit 15- ⁻ bit 10	11	 Unimplemented: Read as '0' FRESET: FIFO Reset bit⁽³⁾ 1 = FIFO will be reset when bit is set; cleared by hardware when FIFO was reset. User should wait until this bit is clear before taking any action. 0 = No effect
bit 9		 TXREQ: Message Send Request bit⁽²⁾ <u>TXEN = 1</u> (FIFO configured as a Transmit FIFO) 1 = Requests sending a message; the bit will automatically clear when all the messages queued in the FIFO are successfully sent. 0 = Clearing the bit to '0' while set ('1') will request a message abort. <u>TXEN = 0</u> (FIFO configured as a Receive FIFO) This bit has no effect.
bit 8		UINC: Increment Head/Tail bit <u>TXEN = 1</u> (FIFO configured as a Transmit FIFO) When this bit is set, the FIFO head will increment by a single message. <u>TXEN = 0</u> (FIFO configured as a Receive FIFO) When this bit is set, the FIFO tail will increment by a single message.
bit 7		TXEN: TX/RX FIFO Selection bit ⁽¹⁾ 1 = Transmit FIFO 0 = Receive FIFO
bit 6		RTREN : Auto RTR Enable bit 1 = When a remote transmit is received, TXREQ will be set. 0 = When a remote transmit is received, TXREQ will be unaffected.
bit 5		 RXTSEN: Received Message Time Stamp Enable bit⁽¹⁾ 1 = Capture time stamp in received message object in RAM. 0 = Don't capture time stamp.
bit 4		 TXATIE: Transmit Attempts Exhausted Interrupt Enable bit 1 = Enable interrupt 0 = Disable interrupt
bit 3		RXOVIE : Overflow Interrupt Enable bit 1 = Interrupt enabled for overflow event 0 = Interrupt disabled for overflow event
bit 2		TFERFFIE : Transmit/Receive FIFO Empty/Full Interrupt Enable bit <u>TXEN = 1</u> (FIFO configured as a Transmit FIFO) Transmit FIFO Empty Interrupt Enable 1 = Interrupt enabled for FIFO empty 0 = Interrupt disabled for FIFO empty <u>TXEN = 0</u> (FIFO configured as a Receive FIFO) Receive FIFO Full Interrupt Enable 1 = Interrupt enabled for FIFO full 0 = Interrupt disabled for FIFO full
bit 1		TFHRFHIE : Transmit/Receive FIFO Half Empty/Half Full Interrupt Enable bit <u>TXEN = 1</u> (FIFO configured as a Transmit FIFO) Transmit FIFO Half Empty Interrupt Enable 1 = Interrupt enabled for FIFO half empty 0 = Interrupt disabled for FIFO half empty <u>TXEN = 0</u> (FIFO configured as a Receive FIFO) Receive FIFO Half Full Interrupt Enable 1 = Interrupt enabled for FIFO half full 0 = Interrupt disabled for FIFO half full 0 = Interrupt disabled for FIFO half full
Note 2		hese bits can only be modified in Configuration mode. his bit is updated when a message completes (or aborts) or when the FIFO is reset.

^{3:} FRESET is set while in Configuration mode and is automatically cleared in Normal mode.

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REGISTER 3-28: CiFIFOCONm – FIFO CONTROL REGISTER m, (m = 1 TO 31) (CONTINUED)

- bit 0 TFNRFNIE: Transmit/Receive FIFO Not Full/Not Empty Interrupt Enable bit
 - <u>TXEN = 1</u> (FIFO configured as a Transmit FIFO)
 - Transmit FIFO Not Full Interrupt Enable
 - 1 = Interrupt enabled for FIFO not full
 - 0 = Interrupt disabled for FIFO not full
 - <u>TXEN = 0</u> (FIFO configured as a Receive FIFO)
 - Receive FIFO Not Empty Interrupt Enable
 - 1 = Interrupt enabled for FIFO not empty
 - 0 = Interrupt disabled for FIFO not empty
- **Note 1:** These bits can only be modified in Configuration mode.
 - 2: This bit is updated when a message completes (or aborts) or when the FIFO is reset.
 - **3:** FRESET is set while in Configuration mode and is automatically cleared in Normal mode.

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
_	_	—	—		—	_	_
bit 31							bit 24
U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	_	—		—	—
bit 23							bit 1
U-0	U-0	U-0	R-0	R-0	R-0	R-0	R-0
		_			FIFOCI<4:0> ⁽¹)	
bit 15							bit 8
	110/0.0	110/0 0	110/0 0	110/0.0			
HS/C-0	HS/C-0	HS/C-0	HS/C-0	HS/C-0	R-0	R-0	R-0
TXABT ⁽²⁾⁽³⁾	TXLARB (2)(3)	TXERR ⁽²⁾⁽³⁾	TXATIF	RXOVIF	TFERFFIF	TFHRFHIF	TFNRFNIF
bit 7							bit
							
Legend: R = Readable I	hit	W = Writable t	nit	II = I Inimplei	mented bit, rea	d as 'O'	
-n = Value at P		'1' = Bit is set	JIL	'0' = Bit is cle			2014/2
	-	1 Bit lo oot			areu	x = Bit is unkı	IUWII
					areu	X = BIT IS UNKI	IOWII
	FIFOCI<4:0>	ted: Read as '0 : FIFO Message	e Index bits ⁽¹⁾			x = Bit is unki	
	FIFOCI<4:0> TXEN = 1 (FII A read of this TXEN = 0 (FII	ted: Read as '0 : FIFO Message FO is configured bit field will retu FO is configured s bit field will re	e Index bits ⁽¹⁾ d as a Transm ırn an index to d as a Receive	it FIFO) the message FIFO)	that the FIFO v	vill next attemp	t to transmit.
bit 12-8	FIFOCI<4:0> <u>TXEN = 1</u> (FII A read of this <u>TXEN = 0</u> (FII A read of this message	ted: Read as '0 : FIFO Message FO is configured bit field will retu FO is configured s bit field will re	e Index bits ⁽¹⁾ d as a Transm Irn an index to d as a Receive turn an index	it FIFO) the message FIFO)	that the FIFO v	vill next attemp	t to transmit.
bit 12-8	FIFOCI<4:0>: <u>TXEN = 1</u> (FII A read of this <u>TXEN = 0</u> (FII A read of this message TXABT: Mess 1 = Message	ted: Read as '0 FIFO Message FO is configured bit field will retu FO is configured s bit field will re sage Aborted St was aborted	e Index bits ⁽¹⁾ d as a Transm urn an index to d as a Receive turn an index atus bit ⁽²⁾⁽³⁾	it FIFO) the message FIFO)	that the FIFO v	vill next attemp	t to transmit.
bit 12-8 bit 7	FIFOCI<4:0>: <u>TXEN = 1</u> (FII A read of this <u>TXEN = 0</u> (FII A read of this message TXABT: Mess 1 = Message 0 = Message	ted: Read as '0 FIFO Message FO is configured bit field will retu FO is configured bit field will retu sage Aborted St was aborted completed suc	e Index bits ⁽¹⁾ d as a Transm irn an index to d as a Receive aturn an index atus bit ⁽²⁾⁽³⁾ cessfully	it FIFO) the message FIFO) to the messa	that the FIFO v	vill next attemp	t to transmit.
bit 31-13 bit 12-8 bit 7 bit 6	FIFOCI<4:0> TXEN = 1 (FIR A read of this TXEN = 0 (FIR A read of this message TXABT: Mess 1 = Message 0 = Message TXLARB: Me	ted: Read as '0 FIFO Message FO is configured bit field will retu FO is configured s bit field will retu sage Aborted St was aborted completed suc ssage Lost Arbi	e Index bits ⁽¹⁾ d as a Transm urn an index to d as a Receive sturn an index atus bit ⁽²⁾⁽³⁾ cessfully itration Status	it FIFO) the message FIFO) to the messa bit ⁽²⁾⁽³⁾	that the FIFO v	vill next attemp	t to transmit.
bit 12-8 bit 7	FIFOCI<4:0>: <u>TXEN = 1</u> (FIR A read of this <u>TXEN = 0</u> (FIR A read of this message TXABT: Mess 1 = Message TXLARB: Me 1 = Message	ted: Read as '0 FIFO Message FO is configured bit field will retu FO is configured s bit field will retu sage Aborted St was aborted completed suc ssage Lost Arbit lost arbitration	e Index bits ⁽¹⁾ d as a Transm irn an index to d as a Receive eturn an index atus bit ⁽²⁾⁽³⁾ cessfully itration Status while being se	it FIFO) the message FIFO) to the messa bit ⁽²⁾⁽³⁾	that the FIFO v	vill next attemp	t to transmit.
bit 12-8 bit 7 bit 6	FIFOCI<4:0>: <u>TXEN = 1</u> (FII A read of this <u>TXEN = 0</u> (FII A read of this message TXABT: Mess 1 = Message 0 = Message 1 = Message 0 = Message 0 = Message	ted: Read as '0 FIFO Message FO is configured bit field will retu FO is configured bit field will retu FO is configured bit field will retu sage Aborted St was aborted completed suc ssage Lost Arbit lost arbitration did not lose arbitration	e Index bits ⁽¹⁾ d as a Transm irn an index to d as a Receive aturn an index atus bit ⁽²⁾⁽³⁾ cessfully itration Status while being se pitration while	it FIFO) the message FIFO) to the messa bit ⁽²⁾⁽³⁾ ent being sent	that the FIFO v	vill next attemp	t to transmit.
bit 12-8 bit 7	FIFOCI<4:0>: <u>TXEN = 1</u> (FII A read of this <u>TXEN = 0</u> (FII A read of this message TXABT: Mess 1 = Message 0 = Message 0 = Message TXLARB: Me 1 = Message 0 = Message	ted: Read as '0 FIFO Message FO is configured bit field will retu FO is configured bit field will retu FO is configured bit field will retu sage Aborted St was aborted completed suc ssage Lost Arbit lost arbitration did not lose artured r Detected Durin	e Index bits ⁽¹⁾ d as a Transm irn an index to d as a Receive aturn an index atus bit ⁽²⁾⁽³⁾ cessfully itration Status while being se pitration while ng Transmissio	it FIFO) the message FIFO) to the messa bit ⁽²⁾⁽³⁾ ent being sent on bit ⁽²⁾⁽³⁾	that the FIFO v ge that the FIF	vill next attemp	t to transmit.
bit 12-8 bit 7 bit 6	FIFOCI<4:0>: <u>TXEN = 1</u> (FII A read of this <u>TXEN = 0</u> (FII A read of this message TXABT: Mess 1 = Message 0 = Message 0 = Message 0 = Message TXERR: Error 1 = A bus err	ted: Read as '0 FIFO Message FO is configured bit field will retu FO is configured bit field will retu FO is configured bit field will retu sage Aborted St was aborted completed suc ssage Lost Arbit lost arbitration did not lose arbitration	e Index bits ⁽¹⁾ d as a Transm irn an index to d as a Receive turn an index atus bit ⁽²⁾⁽³⁾ cessfully itration Status while being se pitration while ng Transmissio ile the messag	it FIFO) the message FIFO) to the messa bit ⁽²⁾⁽³⁾ ent being sent on bit ⁽²⁾⁽³⁾ je was being s	that the FIFO v ge that the FIF	vill next attemp	t to transmit.
bit 12-8 bit 7 bit 6	FIFOCI<4:0>: <u>TXEN = 1</u> (FII A read of this <u>TXEN = 0</u> (FII A read of this <u>message</u> TXABT: Mess 1 = Message 0 = Message 1 = Message 0 = Message TXLARB: Me 1 = Message 0 = Message TXERR: Error 1 = A bus error 0 = A bus error	ted: Read as '0 FIFO Message FO is configured bit field will retu FO is configured bit field will retu FO is configured bit field will retu FO is configured bit field will return age Aborted St was aborted completed suc ssage Lost Arbit lost arbitration did not lose arb r Detected Durin for occurred whi	e Index bits ⁽¹⁾ d as a Transm irn an index to d as a Receive aturn an index atus bit ⁽²⁾⁽³⁾ cessfully itration Status while being se pitration while ng Transmissio de the messag	it FIFO) the message FIFO) to the messa bit ⁽²⁾⁽³⁾ ent being sent on bit ⁽²⁾⁽³⁾ ge was being s ssage was bei	that the FIFO v ge that the FIF ent ng sent	vill next attemp	t to transmit.
bit 12-8 bit 7 bit 6 bit 5	FIFOCI<4:0>: <u>TXEN = 1</u> (FII A read of this <u>TXEN = 0</u> (FII A read of this message TXABT: Mess 1 = Message 0 = Message 0 = Message TXLARB: Me 1 = Message 0 = Message TXERR: Error 1 = A bus err 0 = A bus err TXATIF: Tran <u>TXEN = 1</u> (FII	ted: Read as '0 FIFO Message FO is configured bit field will retu FO is configured bit field will retu FO is configured bit field will retu FO is configured bit field will return age Aborted St was aborted completed suc ssage Lost Arbit lost arbitration did not lose artur or occurred whit or did not occur smit Attempts E FO is configured	e Index bits ⁽¹⁾ d as a Transm irn an index to d as a Receive aturn an index atus bit ⁽²⁾⁽³⁾ cessfully itration Status while being se pitration while ng Transmissio ile the message while the message	it FIFO) the message FIFO) to the messa bit ⁽²⁾⁽³⁾ ent being sent on bit ⁽²⁾⁽³⁾ ge was being s ssage was being rrupt Pending	that the FIFO v ge that the FIF ent ng sent	vill next attemp	t to transmit.
bit 12-8 bit 7 bit 6 bit 5	FIFOCI<4:0>: <u>TXEN = 1</u> (FII A read of this <u>TXEN = 0</u> (FII A read of this message TXABT: Mess 1 = Message 0 = Message 0 = Message TXLARB: Me 1 = Message 0 = Message TXERR: Error 1 = A bus err 0 = A bus err TXATIF: Tran <u>TXEN = 1</u> (FII 1 = Interrupt	ted: Read as '0 FIFO Message FO is configured bit field will retu FO is configured bit field will retu FO is configured bit field will retu FO is configured bit field will return sage Aborted St was aborted completed suc ssage Lost Arbit lost arbitration did not lose artur or occurred whit or did not occur smit Attempts E FO is configured pending	e Index bits ⁽¹⁾ d as a Transm irn an index to d as a Receive aturn an index atus bit ⁽²⁾⁽³⁾ cessfully itration Status while being se pitration while ng Transmissio ile the message while the message	it FIFO) the message FIFO) to the messa bit ⁽²⁾⁽³⁾ ent being sent on bit ⁽²⁾⁽³⁾ ge was being s ssage was being rrupt Pending	that the FIFO v ge that the FIF ent ng sent	vill next attemp	t to transmit.
bit 12-8 bit 7 bit 6 bit 5	FIFOCI<4:0>: <u>TXEN = 1</u> (FII A read of this <u>TXEN = 0</u> (FII A read of this message TXABT: Mess 1 = Message 0 = Message 0 = Message TXLARB: Me 1 = Message 0 = Message TXERR: Error 1 = A bus err 0 = A bus err TXATIF: Tran <u>TXEN = 1</u> (FII 1 = Interrupt 0 = Interrupt	ted: Read as '0 FIFO Message FO is configured bit field will retu FO is configured s bit field will retu FO is configured s bit field will retu sage Aborted St was aborted completed suc ssage Lost Arbit lost arbitration did not lose art r Detected Durin for occurred whi for did not occur smit Attempts E FO is configured pending not pending	e Index bits ⁽¹⁾ d as a Transm irn an index to d as a Receive aturn an index atus bit ⁽²⁾⁽³⁾ cessfully itration Status while being se bitration while ng Transmissio ile the message while the message while the message while the message while the message while the message while the message	it FIFO) the message FIFO) to the messa bit ⁽²⁾⁽³⁾ ent being sent on bit ⁽²⁾⁽³⁾ ge was being s ssage was bei grrupt Pending it FIFO)	that the FIFO v ge that the FIF ent ng sent	vill next attemp	t to transmit.
bit 12-8 bit 7 bit 6 bit 5	FIFOCI<4:0>: <u>TXEN = 1</u> (FII A read of this <u>TXEN = 0</u> (FII A read of this message TXABT: Mess 1 = Message 0 = Message 0 = Message TXLARB: Me 1 = Message 0 = Message TXERR: Error 1 = A bus err 0 = A bus err TXATIF: Tran <u>TXEN = 1</u> (FII 1 = Interrupt 0 = Interrupt	ted: Read as '0 FIFO Message FO is configured bit field will retu FO is configured bit field will retu FO is configured bit field will retu FO is configured bit field will return sage Aborted St was aborted completed suc ssage Lost Arbit lost arbitration did not lose artur or occurred whit or did not occur smit Attempts E FO is configured pending	e Index bits ⁽¹⁾ d as a Transm irn an index to d as a Receive aturn an index atus bit ⁽²⁾⁽³⁾ cessfully itration Status while being se bitration while ng Transmissio ile the message while the message while the message while the message while the message while the message while the message	it FIFO) the message FIFO) to the messa bit ⁽²⁾⁽³⁾ ent being sent on bit ⁽²⁾⁽³⁾ ge was being s ssage was bei grrupt Pending it FIFO)	that the FIFO v ge that the FIF ent ng sent	vill next attemp	t to transmit.
bit 12-8 bit 7 bit 6 bit 5 bit 4 Note 1: FIF(FIFOCI<4:0>: <u>TXEN = 1</u> (FII A read of this <u>TXEN = 0</u> (FII A read of this <u>message</u> TXABT: Mess 1 = Message 0 = Message TXLARB: Me 1 = Message 0 = Message TXERR: Error 1 = A bus err 0 = A bus err TXATIF: Tran <u>TXEN = 1</u> (FII 1 = Interrupt 0 = Interrupt <u>TXEN = 0</u> (FII Read as '0' OCI<4:0> gives	ted: Read as '0 FIFO Message FO is configured bit field will retur FO is configured s bit field will retur FO is configured s age Aborted St was aborted completed such ssage Lost Arbit lost arbitration did not lose arbit ro occurred whi or did not occur smit Attempts E FO is configured pending not pending FO is configured s a zero-indexed	e Index bits ⁽¹⁾ d as a Transm irn an index to d as a Receive sturn an index atus bit ⁽²⁾⁽³⁾ cessfully itration Status while being se pitration while ng Transmissio the the message while the message while the message d as a Receive d value to the new	it FIFO) the message FIFO) to the messa bit ⁽²⁾⁽³⁾ ent being sent on bit ⁽²⁾⁽³⁾ ge was being s ssage was being rrupt Pending it FIFO) e FIFO) message in the	that the FIFO v ge that the FIF ent ng sent bit	vill next attemp O will use to s	t to transmit. save the ne:
bit 12-8 bit 7 bit 6 bit 5 bit 4 Note 1: FIF((FSI	FIFOCI<4:0>: <u>TXEN = 1</u> (FII A read of this <u>TXEN = 0</u> (FII A read of this <u>TXEN = 0</u> (FII A read of this message TXABT: Mess 1 = Message 0 = Message TXLARB: Me 1 = Message 0 = Message TXERR: Error 1 = A bus err 0 = A bus err TXATIF: Tran <u>TXEN = 1</u> (FII 1 = Interrupt 0 = Interrupt <u>TXEN = 0</u> (FII Read as '0' DCI<4:0> gives IZE=5'h03) FIF	ted: Read as '0 FIFO Message FO is configured bit field will retur FO is configured s bit field will retur FO is configured s aborted St was aborted St was aborted St was aborted such ssage Lost Arbit lost arbitration did not lose art r Detected Durin for occurred whi for did not occur smit Attempts E FO is configured pending not pending FO is configured	e Index bits ⁽¹⁾ d as a Transm irn an index to d as a Receive aturn an index atus bit ⁽²⁾⁽³⁾ cessfully itration Status while being se bitration while ng Transmissio le the message while the message while the message d as a Receive d value to the m n a value of 0 t	it FIFO) the message FIFO) to the messa bit ⁽²⁾⁽³⁾ ent being sent on bit ⁽²⁾⁽³⁾ ge was being s ssage was bei grupt Pending it FIFO) e FIFO) message in the o 3 depending	that the FIFO v ge that the FIF ent ng sent bit	vill next attemp O will use to s	t to transmit save the ne:

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REGISTER 3-29: CiFIFOSTAM – FIFO STATUS REGISTER m, (m = 1 TO 31) (CONTINUED)

bit 3	RXOVIF: Receive FIFO Overflow Interrupt Flag bit <u>TXEN = 1</u> (FIFO is configured as a Transmit FIFO) Unused, Read as '0' <u>TXEN = 0</u> (FIFO is configured as a Receive FIFO) 1 = Overflow event has occurred 0 = No overflow event has occurred
bit 2	TFERFFIF: Transmit/Receive FIFO Empty/Full Interrupt Flag bit <u>TXEN = 1</u> (FIFO is configured as a Transmit FIFO) Transmit FIFO Empty Interrupt Flag 1 = FIFO is empty 0 = FIFO is not empty; at least one message queued to be transmitted <u>TXEN = 0</u> (FIFO is configured as a Receive FIFO) Receive FIFO Full Interrupt Flag 1 = FIFO is empty 0 = FIFO is not full
bit 1	TFHRFHIF: Transmit/Receive FIFO Half Empty/Half Full Interrupt Flag bit <u>TXEN = 1</u> (FIFO is configured as a Transmit FIFO) Transmit FIFO Half Empty Interrupt Flag $1 = FIFO$ is \leq half full 0 = FIFO is $>$ half full <u>TXEN = 0</u> (FIFO is configured as a Receive FIFO) Receive FIFO Half Full Interrupt Flag $1 = FIFO$ is \geq half full 0 = FIFO is $<$ half full
bit 0	TFNRFNIF: Transmit/Receive FIFO Not Full/Not Empty Interrupt Flag bit <u>TXEN = 1</u> (FIFO is configured as a Transmit FIFO) Transmit FIFO Not Full Interrupt Flag 1 = FIFO is not full 0 = FIFO is full <u>TXEN = 0</u> (FIFO is configured as a Receive FIFO) Receive FIFO Not Empty Interrupt Flag 1 = FIFO is not empty, contains at least one message 0 = FIFO is empty
Note 1:	FIFOCI<4:0> gives a zero-indexed value to the message in the FIFO. If the FIFO is 4 messages deep (FSIZE=5'h03) FIFOCI will take on a value of 0 to 3 depending on the state of the FIFO.

- 2: This bit is cleared when TXREQ is set or by writing a 0 using the SPI.
- 3: This bit is updated when a message completes (or aborts) or when the FIFO is reset.

R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x	
			FIFOU	A<31:24>				
bit 31							bit 24	
R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x	
				A<23:16>				
bit 23							bit 16	
R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x	
			FIFOL	JA<15:8>				
bit 15							bit 8	
R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x	
			FIFO	JA<7:0>				
bit 7							bit 0	
Legend:								
R = Readable	bit	W = Writable bit		U = Unimpler	nented bit, re	ead as '0'		
-n = Value at POR '1' = Bit is set				'0' = Bit is cle	ared	x = Bit is unknown		

REGISTER 3-30: CiFIFOUAm – FIFO USER ADDRESS REGISTER m, (m = 1 TO 31)

 Sit 31-0
 FIFOUA<31:0>: FIFO User Address bits

 TXEN = 1 (FIFO is configured as a Transmit FIFO)
 A read of this register will return the address where the next message is to be written (FIFO head).

 TXEN = 0 (FIFO is configured as a Receive FIFO)
 A read of this register will return the address where the next message is to be read (FIFO tail).

Note 1: This bit is not guaranteed to read correctly in Configuration mode and should only be accessed when the module is not in Configuration mode.

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REGISTER 3-31: CiFLTCONm – FILTER CONTROL REGISTER m, (m = 0 TO 7)

	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0				
FLTEN3	—				F3BP<4:0> ⁽¹⁾						
bit 31							bit 24				
R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0				
FLTEN2	—				F2BP<4:0> ⁽¹⁾						
bit 23							bit 16				
R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0				
FLTEN1	_				F1BP<4:0> ⁽¹⁾						
bit 15							bit 8				
R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0				
FLTEN0	_				F0BP<4:0> ⁽¹⁾						
bit 7							bit C				
Legend:											
R = Readable	bit	W = Writable	bit	U = Unimpler	mented bit, read	as '0'					
-n = Value at F	POR	'1' = Bit is set		'0' = Bit is cleared x = Bit is unknown							
bit 31	FLTEN3: Ena	ble Filter 3 to A	Accept Messad	pes bit							
bit 51	1 = Filter is e			Jes bit							
	0 = Filter is d										
bit 30-29	Unimplemented: Read as '0'										
bit 28-24	F3BP<4:0>: F	Pointer to FIFO	when Filter 3	hits bits ⁽¹⁾							
	1_1111 = Message matching filter is stored in FIFO 31										
	1_1110 = Message matching filter is stored in FIFO 30										
	0_0010 = Message matching filter is stored in FIFO 2										
		ssage matchin									
					ceive messages	i					
bit 23	FLTEN2>: En	able Filter 2 to	Accept Messa	ages bit							
	1 = Filter is e										
	0 = Filter is d	isabled									
bit 22-21	0 = Filter is d)'								
	Unimplemen	ted: Read as '		hits hits ⁽¹⁾							
	Unimplemen F2BP<4:0>: F	t ed: Read as 'd Pointer to FIFO	when Filter 2								
	Unimplemen F2BP<4:0>: F 1_1111 = Me	ted: Read as '	when Filter 2 g filter is store	ed in FIFO 31							
	Unimplement F2BP<4:0>: F 1_1111 = Me 1_1110 = Me	ted: Read as ' Pointer to FIFO essage matchin essage matchin	when Filter 2 g filter is store g filter is store	ed in FIFO 31 ed in FIFO 30							
	Unimplement F2BP<4:0>: F 1_1111 = Me 1_1110 = Me 0_0010 = Me 0_0001 = Me	ted: Read as ' Pointer to FIFO essage matchin essage matchin essage matchin essage matchin	when Filter 2 g filter is store g filter is store g filter is store g filter is store	ed in FIFO 31 ed in FIFO 30 ed in FIFO 2 ed in FIFO 1							
bit 22-21 bit 20-16 bit 15	Unimplement F2BP<4:0>: F 1_1111 = Me 1_1110 = Me 0_0010 = Me 0_0001 = Me 0_0000 = Re	ted: Read as ' Pointer to FIFO essage matchin essage matchin essage matchin essage matchin served FIFO 0	when Filter 2 g filter is store g filter is store g filter is store g filter is store is the TX Que	ed in FIFO 31 ed in FIFO 30 ed in FIFO 2 ed in FIFO 1 eue and can't re	ceive messages						
bit 20-16	Unimplement F2BP<4:0>: F 1_1111 = Me 1_1110 = Me 0_0010 = Me 0_0001 = Me 0_0000 = Re FLTEN1: Ena	ted: Read as ' Pointer to FIFO essage matchin essage matchin essage matchin essage matchin served FIFO 0 ble Filter 1 to A	when Filter 2 g filter is store g filter is store g filter is store g filter is store is the TX Que	ed in FIFO 31 ed in FIFO 30 ed in FIFO 2 ed in FIFO 1 eue and can't re	ceive messages						
	Unimplement F2BP<4:0>: F 1_1111 = Me 1_1110 = Me 0_0010 = Me 0_0001 = Me 0_0000 = Re	ted: Read as ' Pointer to FIFO essage matchin essage matchin essage matchin essage matchin served FIFO 0 ble Filter 1 to A nabled	when Filter 2 g filter is store g filter is store g filter is store g filter is store is the TX Que	ed in FIFO 31 ed in FIFO 30 ed in FIFO 2 ed in FIFO 1 eue and can't re	ceive messages						
bit 20-16	Unimplement F2BP<4:0>: F 1_1111 = Me 1_1110 = Me 0_0010 = Me 0_0001 = Me 0_0000 = Re FLTEN1: Ena 1 = Filter is e 0 = Filter is d	ted: Read as ' Pointer to FIFO essage matchin essage matchin essage matchin essage matchin served FIFO 0 ble Filter 1 to A nabled	when Filter 2 g filter is store g filter is store g filter is store g filter is store is the TX Que accept Messag	ed in FIFO 31 ed in FIFO 30 ed in FIFO 2 ed in FIFO 1 eue and can't re	ceive messages						

REGISTER 3-31: CIFLTCONM – FILTER CONTROL REGISTER m, (m = 0 TO 7) (CONTINUED)

bit 12-8	F1BP<4:0>: Pointer to FIFO when Filter 1 hits bits ⁽¹⁾ 1_1111 = Message matching filter is stored in FIFO 31 1_1110 = Message matching filter is stored in FIFO 30
	0_0010 = Message matching filter is stored in FIFO 2 0_0001= Message matching filter is stored in FIFO 1 0_0000 = Reserved FIFO 0 is the TX Queue and can't receive messages
bit 7	FLTEN0: Enable Filter 0 to Accept Messages bit
	1 = Filter is enabled0 = Filter is disabled
bit 6-5	Unimplemented: Read as '0'
bit 4-0	F0BP<4:0>: Pointer to FIFO when Filter 0 hits bits ⁽¹⁾ 1_1111 = Message matching filter is stored in FIFO 31 1_1110 = Message matching filter is stored in FIFO 30
	0_0010 = Message matching filter is stored in FIFO 2 0_0001 = Message matching filter is stored in FIFO 1 0_0000 = Reserved FIFO 0 is the TX Queue and can't receive messages

Note 1: This bit can only be modified if the corresponding filter is disabled (FLTEN = 0).

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						-	
U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	EXIDE	SID11			EID<17:13>		
bit 31							bit 24
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			EID<	:12:5>			
bit 23							bit 16
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
		EID<4:0>				SID<10:8>	
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			SID	<7:0>			
bit 7							bit C
Legend:							
R = Readabl	e bit	W = Writable	bit	U = Unimple	mented bit, rea	ad as '0'	
-n = Value at		'1' = Bit is set		•	'0' = Bit is cleared		nown
bit 31	Unimpleme	nted: Read as '0)'				
bit 30	EXIDE: Exte	ended Identifier E	Enable bit				
	If MIDE = 1:						
		only messages w					
	0 = Match c	only messages w	ith standard i	dentifier			
bit 29	SID11: Stan	dard Identifier filt	er bit				
bit 28-11	EID<17:0>:	Extended Identif	ier filter bits				
	In DeviceNe	t mode, these ar	e the filter bit	s for the first 18	data bits		
bit 10-0	SID<10:0>:	Standard Identifi	er filter bits				

REGISTER 3-32: CIFLTOBJM – FILTER OBJECT REGISTER m,(m = 0 TO 31)

Note 1: This register can only be modified when the filter is disabled(CiFLTCON.FLTENm = 0).

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
_	MIDE	MSID11			MEID<17:13>	•	
bit 31							bit 24
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			MEID	<12:5>			
bit 23							bit 16
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
		MEID<4:0>				MSID<10:8>	
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			MSID	<7:0>			
bit 7							bit 0
Legend:							
R = Readable	e bit	W = Writable	bit	U = Unimpler	nented bit, rea	id as '0'	
-n = Value at	POR	'1' = Bit is set		0° = Bit is cleared x = Bit is u			nown
bit 31	Unimplemer	nted: Read as '0)'				
bit 30	MIDE: Identi	fier Receive mod	de bit				
		nly message typ					t in filter
		oth standard and		essage frames	if filters match		
bit 29	MSID11: Sta	ndard Identifier I	Mask bit				
bit 28-11		: Extended Iden		-			
	In DeviceNet	mode, these ar	e the mask bi	ts for the first 18	3 data bits		
bit 10-0	MSID<10:0>	: Standard Ident	ifier Mask bits	3			

REGISTER 3-33: CIMASKm – MASK REGISTER m, (m = 0 TO 31)

MCP2517FD

NOTES:

3.3 Message Memory

The MCP2517FD contains a 2 KB RAM that is used to store message objects. There are three different kinds of message objects:

- Table 3-5: Transmit Message Objects used by the TXQ and by TX FIFOs.
- Table 3-6: Receive Message Objects used by RX FIFOs.
- Table 3-7: TEF objects.

Figure 3-2 illustrates how message objects are mapped into RAM. The number of message objects for the TEF, the TXQ, and for each FIFO is configurable. Only the message objects for FIFO2 are shown in detail. The number of data bytes per message object (payload) is individually configurable for the TXQ and each FIFO.

FIFOs and message objects can only be configured in Configuration mode.

The TEF objects are allocated first. Space in RAM will only be reserved if CiCON.STEF = 1.

Next the TXQ objects are allocated. Space in RAM will only be reserved if CiCON.TXQEN = 1.

Next the message objects for FIFO1 through FIFO31 are allocated.

This highly flexible configuration results in an efficient usage of the RAM.

The addresses of the message objects depend on the selected configuration. The application doesn't have to calculate the addresses. The User Address field provides the address of the next message object to read from or write to.

3.3.1 RAM ECC

The RAM is protected with an Error Correction Code (ECC). The ECC logic supports Single Error Correction (SEC), and Double Error Detection (DED).

SEC/DED requires seven parity bits in addition to the 32 data bits.

Figure 3-3 shows the block diagram of the ECC logic.

3.3.1.1 ECC Enable and Disable

The ECC logic can be enabled by setting ECCCON.ECCEN. When ECC is enabled, the data written to the RAM is encoded, and the data read from RAM is decoded.

When the ECC logic is disabled, the data is written to RAM, the parity bits are taken from ECCCON.PARITY. This enables the testing of the ECC logic by the user. During a read the parity bits are stripped out and the data is read back unchanged.

3.3.1.2 RAM Write

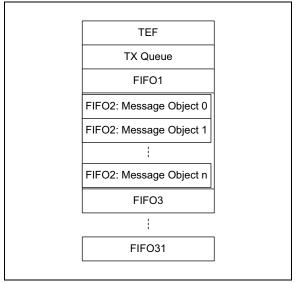
During a RAM write, the Encoder calculates the parity bits and adds the parity bits to the input data.

3.3.1.3 RAM READ

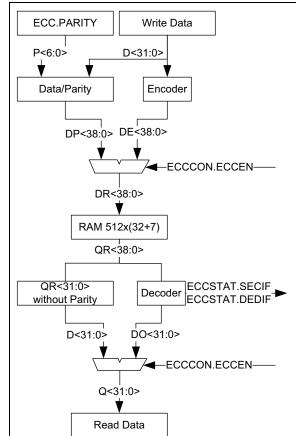
During a RAM read, the Decoder checks the output data from RAM for consistency and removes the parity bits. It corrects single bit errors and detects double bit errors.

FIGURE 3-2: N

MESSAGE MEMORY ORGANIZATION







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Word		Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0	
Т0	31:24			SID11			EID<17:6>			
	23:16				EID<	12:5>				
	15:8			EID<4:0>				SID<10:8>		
	7:0				SID<	<7:0>	•			
T1	31:24									
	23:16									
	15:8	SEQ<6:0> Es								
	7:0	FDF	BRS	RTR	IDE		DLC	<3:0>		
T2 (1)	31:24				Transmit D	Data Byte 3				
	23:16				Transmit D	oata Byte 2				
	15:8				Transmit D	oata Byte 1				
	7:0				Transmit D	ata Byte 0				
Т3	31:24				Transmit D	ata Byte 7				
	23:16				Transmit D	0ata Byte 6				
	15:8				Transmit D	0ata Byte 5				
	7:0				Transmit D	ata Byte 4				
Ti	31:24				Transmit D)ata Byte n				
	23:16				Transmit Da	ata Byte n-1				
	15:8				Transmit Da	ata Byte n-2				
	7:0				Transmit Da	ata Byte n-3				

TABLE 3-5: TRANSMIT MESSAGE OBJECT (TXQ AND TX FIFO)

bit T0.31-30 Unimplemented: Read as 'x'

- bit T0.29 SID11: In FD mode the standard ID can be extended to 12 bit using r1
- bit T0.28-11 EID<17:0>: Extended Identifier
- bit T0.10-0 SID<10:0>: Standard Identifier
- bit T1.31-16 Unimplemented: Read as 'x'
- bit T1.15-9 SEQ<6:0>: Sequence to keep track of transmitted messages in Transmit Event FIFO
- bit T1.8 ESI: Error Status Indicator

In CAN to CAN gateway mode (CiCON.ESIGM=1), the transmitted ESI flag is a "logical OR" of T1.ESI and error passive state of the CAN controller;

- In normal mode ESI indicates the error status
- 1 = Transmitting node is error passive
- 0 = Transmitting node is error active
- bit T1.7 **FDF:** FD Frame; distinguishes between CAN and CAN FD formats
- bit T1.6 **BRS:** Bit Rate Switch; selects if data bit rate is switched
- bit T1.5 RTR: Remote Transmission Request; not used in CAN FD
- bit T1.4 **IDE:** Identifier Extension Flag; distinguishes between base and extended format
- bit T1.3-0 DLC<3:0>: Data Length Code
- Note 1: Data Bytes 0-n: payload size is configured individually in control register (CiFIFOCONm.PLSIZE<2:0>).

IABLE 3-6:												
Word		Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0			
R0	31:24			SID11			EID<17:6>					
	23:16		•	•	EID<	12:5>						
	15:8			EID<4:0>			SID<10:8>					
	7:0				SID<	<7:0>						
R1	31:24											
	23:16											
	15:8		•	FILHIT<4:0>	•				ESI			
	7:0	FDF	BRS	RTR	IDE		DLC<	<3:0>				
R2 ⁽²⁾	31:24	RXMSGTS<31:24>										
	23:16				RXMSGT	S<23:16>						
	15:8				RXMSG	「S<15:8>						
	7:0	RXMSGTS<7:0>										
R3 (1)	31:24	Receive Data Byte 3										
	23:16	Receive Data Byte 2										
	15:8	Receive Data Byte 1										
	7:0				Receive D	ata Byte 0						
R4	31:24				Receive D	ata Byte 7						
	23:16				Receive D	ata Byte 6						
	15:8				Receive D	ata Byte 5						
	7:0				Receive D	ata Byte 4						
Ri	31:24				Receive D	ata Byte n						
	23:16				Receive Da	ata Byte n-1						
	15:8				Receive Da	ata Byte n-2						
	7:0				Receive Da	ata Byte n-3						

TABLE 3-6: RECEIVE MESSAGE OBJECT

- bit R0.31-30 Unimplemented: Read as 'x'
- bit R0.29 SID11: In FD mode the standard ID can be extended to 12 bit using r1
- bit R0.28-11 EID<17:0>: Extended Identifier
- bit R0.10-0 SID<10:0>: Standard Identifier
- bit R1.31-16 Unimplemented: Read as 'x'
- bit R1.15-11 FILTHIT<4:0>: Filter Hit, number of filter that matched
- bit R1.10-9 Unimplemented: Read as 'x'
- bit R1.8 ESI: Error Status Indicator
 - 1 = Transmitting node is error passive
 - 0 = Transmitting node is error active
- bit R1.7 FDF: FD Frame; distinguishes between CAN and CAN FD formats
- bit R1.6 BRS: Bit Rate Switch; indicates if data bit rate was switched
- bit R1.5 RTR: Remote Transmission Request; not used in CAN FD
- bit R1.4 **IDE:** Identifier Extension Flag; distinguishes between base and extended format
- bit R1.3-0 DLC<3:0>: Data Length Code
- bit R2.31-0 RXMSGTS<31:0>: Receive Message Time Stamp
- Note 1: RXMOBJ: Data Bytes 0-n: payload size is configured individually in the FIFO control register (CiFIFOCONm.PLSIZE<2:0>).
 - 2: R2 (RXMSGTS) only exits in objects where CiFIFOCONm.RXTSEN is set.

Word		Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
TE0	31:24			SID11			EID<17:6>		
	23:16				EID<	12:5>			
	15:8			EID<4:0>				SID<10:8>	
	7:0	SID<7:0>							
TE1	31:24								
	23:16								
	15:8				SEQ<6:0>			•	ESI
	7:0	FDF	BRS	RTR	IDE		DLC<		
TE2 ⁽¹⁾	31:24				TXMSGT	S<31:24>			
	23:16				TXMSGT	S<23:16>			
	15:8				TXMSGT	S<15:8>			
	7:0				TXMSG	FS<7:0>			

TABLE 3-7: TRANSMIT EVENT FIFO OBJECT

bit TE0.31-30 Unimplemented: Read as 'x'

bit TE0.29 SID11: In FD mode the standard ID can be extended to 12 bit using r1

bit TE0.28-11 EID<17:0>: Extended Identifier

- bit TE0.10-0 SID<10:0>: Standard Identifier
- bit TE1.31-16 Unimplemented: Read as 'x'
- bit TE1.15-9 **SEQ<6:0>:** Sequence to keep track of transmitted messages
- bit TE1.8 ESI: Error Status Indicator
 - 1 = Transmitting node is error passive
 - 0 = Transmitting node is error active
- bit TE1.7 **FDF:** FD Frame; distinguishes between CAN and CAN FD formats
- bit TE1.6 **BRS:** Bit Rate Switch; selects if data bit rate is switched
- bit TE1.5 RTR: Remote Transmission Request; not used in CAN FD
- bit TE1.4 IDE: Identifier Extension Flag; distinguishes between base and extended format
- bit TE1.3-0 DLC<3:0>: Data Length Code
- bit TE2.31-0 TXMSGTS<31:0>: Transmit Message Time Stamp⁽¹⁾
- Note 1: TE2 (TXMSGTS) only exits in objects where CiTEFCON.TEFTSEN is set.

4.0 SPI INTERFACE

The MCP2517FD is designed to interface directly with an Serial Peripheral Interface (SPI) port available on most microcontrollers. The SPI in the microcontroller must be configured in mode 0,0 or 1,1 in 8-bit operating mode.

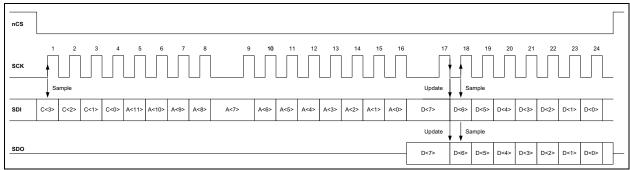
SFR and Message Memory (RAM) are accessed using SPI instructions. Figure 4-1 illustrates the generic format of the SPI instructions (SPI mode 0,0). Each instruction starts with driving nCS low (falling edge on nCS). The 4-bit command and the 12-bit address are shifted into SDI on the rising edge of SCK. During a write instruction, data bits are shifted into SDI on the rising edge of SCK. During a read instruction, data bits are shifted out of SDO on the falling edge of SCK. One or more data bytes are transfered with one instruction. Data bits are updated on the falling edge of SCK and must be valid on the rising edge of SCK. Each instruction ends with driving nCS high (rising edge on nCS).

FIGURE 4-1: SPI INSTRUCTION FORMAT

Refer to Figure 7-1 for detailed input and output timing for both mode 0,0 and mode 1,1.

Table 4-1 lists the SPI instructions and their format.

- Note 1: The frequency of SCK has to be less than or equal to half the frequency of SYSCLK. This ensures that the synchronization between SCK and SYSCLK works correctly.
 - 2: In order to minimize the Sleep current, the SDO pin of the MCP2517FD must not be left floating while the device is in Sleep mode. This can be achieved by enabling a pull-up or pull-down resistor inside the MCU on the pin that is connected to the SDO pin of the MCP2517FD, while the MCP2517FD is in Sleep mode.



Name	Format	Description				
RESET	C = 0b0000; A = 0x000	Resets internal registers to default state; selects Configuration mode.				
READ	C = 0b0011; A; D = SDO	Read SFR/RAM from address A.				
WRITE	C = 0b0010; A; D = SDI	/rite SFR/RAM to address A.				
READ_CRC	C = 0b1011; A; N; D = SDO; CRC = SDO	Read SFR/RAM from address A. N data bytes. Two bytes CRC. CRC is calculated on C, A, N and D.				
WRITE_CRC	C = 0b1010; A; N; D = SDI; CRC = SDI	Write SFR/RAM to address A. N data bytes. Two bytes CRC. CRC is calculated on C, A, N and D.				
WRITE_SAFE	C = 0b1100; A; D = SDI; CRC = SDI	Write SFR/RAM to address A. Check CRC before write. CRC is calculated on C, A and D.				

TABLE 4-1: SPI INSTRUCTIONS

Legend: C = Command (4 bit), A = Address (12 bit), D = Data (1 to n bytes), N = Number of Bytes (1 byte), CRC (2 bytes)

4.1 SFR Access

The SFR access is byte-oriented. Any number of data bytes can be read or written with one instruction. The address is incremented by one automatically after every data byte. The address rolls over from 0x3FF to 0x000 and from 0xFFF to 0xE00.

The following SPI instructions only show the different fields and their values. Every instruction follows the generic format illustrated in Figure 4-1.

4.1.1 RESET

Figure 4-2 illustrates the RESET instruction. The instruction starts with nCS going low. The Command (C<3:0> = 0b0000) is followed by the Address (A<11:0> = 0x000). The instruction ends when nCS goes high.

The RESET instruction should only be issued after the device has entered Configuration mode. All SFR and State Machines are reset just like during a Power-on Reset (POR), and the device transitions immediately to Configuration mode.

The Message Memory is not changed.

The actual reset happens at the end of the instruction when nCS goes high.

FIGURE 4-3: SFR READ INSTRUCTION

4.1.2 SFR READ - READ

Figure 4-3 illustrates the READ instruction, while accessing SFR. The instruction starts with nCS going low. The Command (C<3:0> = 0b0011), is followed by the Address (A<11:0>). Afterwards, the data byte from address A (DB[A]) is shifted out, followed by data byte from address A+1 (DB[A+1]). Any number of data bytes can be read. The instruction ends when nCS goes high.

4.1.3 SFR WRITE - WRITE

Figure 4-4 illustrates the WRITE instruction, while accessing SFR. The instruction starts with nCS going low. The Command (C<3:0> = 0b0010), is followed by the Address (A<11:0>). Afterwards, the data byte is shifted into address A (DB[A]), next into address A+1 (DB[A+1]). Any number of data bytes can be written. The instruction ends when nCS goes high.

Data bytes are written to the register with the falling edge on SCK following the 8th data bit.

FIGURE 4-2: RESET INSTRUCTION

nCS Low	0b0000	0x000	nCS High
---------	--------	-------	----------

nCS Low	0b0011	A<11:0>	DB[A]	DB[A+1]	 DB[A+n-1]	nCS High

FIGURE 4-4: SFR WRITE INSTRUCTION

nCS Low	0b0010	A<11:0>	DB[A]	DB[A+1]		DB[A+n-1]	nCS High
					1		

4.2 Message Memory Access

The Message Memory (RAM) access is Word-oriented (4 bytes at a time). Any multiple of 4 data bytes can be read or written with one instruction. The address is incremented by one automatically after every data byte. The address rolls over from 0xBFF to 0x400.

The following SPI instructions only show the different fields and their values. Every instruction follows the generic format illustrated in Figure 4-1.

4.2.1 MESSAGE MEMORY READ - READ

Figure 4-5 illustrates the READ instruction, while accessing RAM. The instruction starts with nCS going low. The Command (C<3:0> = 0b0011), is followed by the Address (A<11:0>). Afterwards, the data byte from address A (DB[A]) is shifted out, followed by data byte from address A+1 (DB[A+1]). The instruction ends when nCS goes high.

Read commands from RAM must always read a multiple of 4 data bytes. A word is internally read from RAM after the address field, and after every fourth data byte read on the SPI. In case nCS goes high before a multiple of 4 data bytes is read on SDO, the incomplete read should be discarded by the microcontroller.

4.2.2 MESSAGE MEMORY WRITE -WRITE

Figure 4-6 illustrates the WRITE instruction, while accessing RAM. The instruction starts with nCS going low. The Command (C<3:0> = 0b0010), is followed by the Address (A<11:0>). Afterwards, the data byte is shifted into address A (DB[A]), next into address A+1 (DB[A+1]). The instruction ends when nCS goes high.

Write commands must always write a multiple of 4 data bytes. After every fourth data byte, with the falling edge on SCK, the RAM Word gets written. In case nCS goes high before a multiple of 4 data bytes is received on SDI, the data of the incomplete Word will not be written to RAM.

FIGURE 4-5: MESSAGE MEMORY READ INSTRUCTION

nCS Low 0b0011	A<11:0>		DW	/[A]		nCS High	
	A>11.02	DB[A]	DB[A+1]	DB[A+2]	DB[A+3]	nCS High	

FIGURE 4-6: MESSAGE MEMORY WRITE INSTRUCTION

nCS Low 0b0010	4-11:05		DW	/[A]		nCS High
	A<11:0>	DB[A]	DB[A+1]	DB[A+2]	DB[A+3]	nCS High

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4.3 SPI Commands with CRC

In order to detect or avoid bit errors during SPI communication, SPI commands with CRC are available.

4.3.1 CRC CALCULATION

In parallel with the SPI shift register, the CRC is calculated, see Figure 4-7.

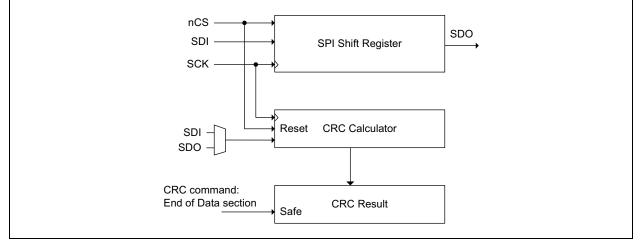
When nCS is asserted, the CRC calculator is reset to $\ensuremath{\mathsf{0xFFFF}}$

The result of the CRC calculation is available after the Data section of a CRC command. The result of the CRC calculation is written to the CRC register in case a CRC mismatch is detected. In case of a CRC mismatch, CRC.CRCERRIF is set.

The MCP2517FD uses the following generator polynomial: CRC-16/USB (0x8005). CRC-16 detects all single and double-bit errors, all errors with an odd number of bits, all burst errors of length 16 or less, and most errors for longer bursts. This allows an excellent detection of SPI communication errors that can happen in the system, and heavily reduces the risk of miscommunication, even under noisy environments.

The maximum number of data bits is used while reading and writing TX or RX Message Objects. A RX Message Object with 64 Bytes of data + 12 Bytes ID and Time Stamp contains 76 Bytes or 608 bits. In comparison, USB data packets contain up to 1024 bits. CRC-16 has a Hamming Distance of 4 up to 1024 bits.

FIGURE 4-7: CRC CALCULATION



4.3.2 SFR READ WITH CRC - READ_CRC

Figure 4-8 illustrates the READ_CRC instruction, while accessing SFR. The instruction starts with nCS going low. The Command (C<3:0> = 0b1011), is followed by the Address (A<11:0>), and the number of data bytes (N<7:0>). Afterwards, the data byte from address A (DB[A]) is shifted out, followed by the data byte from address A+1 (DB[A+1]). Any number of data bytes can be read. Next the CRC is shifted out (CRC<15:0>). The instruction ends when nCS goes high.

The CRC is provided to the microcontroller. The microcontroller checks the CRC. No interrupt is generated on CRC mismatch during a READ_CRC command inside the MCP2517FD.

If nCS goes high before the last byte of the CRC is shifted out, a CRC Form Error interrupt is generated: CRC.FERRIF.

4.3.3 SFR WRITE WITH CRC -WRITE_CRC

Figure 4-9 illustrates the WRITE_CRC instruction, while accessing SFR. The instruction starts with nCS going low. The Command (C<3:0> = 0b1010), is followed by the Address (A<11:0>), and the number of data bytes (N<7:0>). Afterwards, the data byte is shifted into address A (DB[A]), next into address A+1 (DB[A+1]). Any number of data bytes can be written. Next the CRC is shifted in (CRC<15:0>). The instruction ends when nCS goes high.

The SFR is written to the register after the data byte was shifted in on SDI, with the falling edge on SCK. Data bytes are written to the register before the CRC is checked.

The CRC is checked at the end of the write access. In case of a CRC mismatch, a CRC Error interrupt is generated: CRC.CRCERRIF.

If nCS goes high before the last byte of the CRC is shifted in, a CRC Form Error interrupt is generated: CRC.FERRIF.

FIGURE 4-8: SFR READ WITH CRC INSTRUCTION

L										
l	nCS Low	0b1011	A<11:0>	N<7:0>	DB[A]	DB[A+1]	 DB[A+n-1]	CRC<15:8>	CRC<7:0>	nCS High

FIGURE 4-9: SFR WRITE WITH CRC INSTRUCTION

nCS Low	0b1010	A<11:0>	N<7:0>	DB[A]	DB[A+1]][DB[A+n-1]	CRC<15:8>	CRC<7:0>	nCS High

4.3.4 SFR WRITE SAFE WITH CRC -WRITE_SAFE

This instruction ensures that only correct data is written to the SFR.

Figure 4-10 illustrates the WRITE_SAFE instruction, while accessing SFR. The instruction starts with nCS going low. The Command (C<3:0> = 0b1100), is followed by the Address (A<11:0>). Afterwards, one data byte is shifted into address A (DB[A]). Next the CRC (CRC<15:0>) is shifted in. The instruction ends when nCS goes high.

The data byte is only written to the SFR after the CRC is checked and if it matches.

If the CRC mismatches, the data byte is not written to the SFR and a CRC Error interrupt is generated: CRC.CRCERRIF.

If nCS goes high before the last byte of the CRC is shifted in, a CRC Form Error interrupt is generated: CRC.FERRIF.

FIGURE 4-10: SFR WRITE SAFE WITH CRC INSTRUCTION

nCS Low 0b	b1100	A<11:0>	DB[A]	CRC<15:8>	CRC<7:0>	nCS High
------------	-------	---------	-------	-----------	----------	----------

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4.3.5 MESSAGE MEMORY READ WITH CRC- READ_CRC

Figure 4-11 illustrates the READ_CRC instruction, while accessing RAM. The instruction starts with nCS going low. The Command (C<3:0> = 0b1011), is followed by the Address (A<11:0>), and the number of data Words (N<7:0>). Afterwards, the data byte from address A (DB[A]) is shifted out, followed by data byte from address A+1 (DB[A+1]). Next the CRC (CRC<15:0>) is shifted out. The instruction ends when nCS goes high.

Read commands should always read a multiple of 4 data bytes. A word is internally read from RAM after the "N" field, and after every fourth data byte read on the SPI. In case nCS goes high before a multiple of 4 data bytes are read on SDO, the incomplete read should be discarded by the microcontroller.

The CRC is provided to the microcontroller. The microcontroller checks the CRC. No interrupt is generated on CRC mismatch during a READ_CRC command inside the MCP2517FD.

If nCS goes high before the last byte of the CRC is shifted out, a CRC Form Error interrupt is generated: CRC.FERRIF.

4.3.6 MESSAGE MEMORY WRITE WITH CRC - WRITE_CRC

Figure 4-12 illustrates the WRITE instruction, while accessing RAM. The instruction starts with nCS going low. The Command (C<3:0> = 0b1010), is followed by the Address (A<11:0>), and the number of data Words (N<7:0>). Afterwards, the data byte is shifted into address A (DB[A]), next into address A+1 (DB[A+1]). Next the CRC (CRC<15:0>) is shifted in. The instruction ends when nCS goes high.

Write commands must always write a multiple of 4 data bytes. After every fourth data byte, with the falling edge on SCK, the RAM gets written. In case nCS goes high before a multiple of 4 data bytes is received on SDI, the data of the incomplete Word will not be written to RAM.

The CRC is checked at the end of the write access. In case of a CRC mismatch, a CRC interrupt is generated: CRC.CRCERRIF.

If nCS goes high before the last byte of the CRC is shifted in, a CRC interrupt is generated: CRC.FERRIF.

FIGURE 4-11: MESSAGE MEMORY READ WITH CRC INSTRUCTION

nCS Low	051011	0b1011 A<11:0>		DW[A]			CRC<15:8>	CRC<7:0>	nCS High	
IIC3 LOW	001011	A 11.02	N-7.02	DB[A]	DB[A+1]	DB[A+2]	DB[A+3]	610313.02	010-1.02	neo riigii

FIGURE 4-12: MESSAGE MEMORY WRITE WITH CRC INSTRUCTION

	0b1010	A<11:0>	N<7:0>		DW[A]				CRC<7:0>	nCS Hiah
IICS LOW	001010	A<11.02	N~7.02	DB[A]	DB[A+1]	DB[A+2]	DB[A+3]	CRC<15:8>	CRC<7.02	IICS High

4.3.7 MESSAGE MEMORY WRITE SAFE WITH CRC - WRITE SAFE

This instruction ensures that only correct data is written to RAM.

Figure 4-10 illustrates the WRITE_SAFE instruction, while accessing RAM. The instruction starts with nCS going low. The Command (C<3:0> = 0b1100), is followed by the Address (A<11:0>). Afterwards, the data byte is shifted into address A (DB[A]), next into

address A+1 (DB[A+1]), A+2 (DB[A+2]), and A+3 (DB[A+3]). Next the CRC (CRC<15:0>) is shifted in. The instruction ends when nCS goes high.

The data word is only written to RAM after the CRC is checked and if it matches.

If the CRC mismatches, the data word is not written to RAM and a CRC Error interrupt is generated: CRC.CRCERRIF.

If nCS goes high before the last byte of the CRC is shifted in, a CRC interrupt is generated: CRC.FERRIF.

FIGURE 4-13: MESSAGE MEMORY WRITE SAFE WITH CRC INSTRUCTION

nCS Low	ow 0b1100 A<11:0>			DW	CRC<15:8>	CRC<7:0>	nCS High	
HOG EOW	NCS LOW 001100 A<11:0>	DB[A]	DB[A+1]	DB[A+2]	DB[A+3]	010 10.02	01001.02	neo rign

5.0 OSCILLATOR

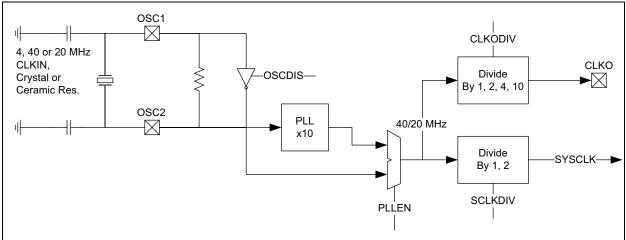
Figure 5-1 shows the block diagram of the oscillator in the MCP2517FD. The oscillator system generates the SYSCLK, which is used in the CAN FD Controller Module and for RAM accesses. It is recommended by the CAN FD community to use either a 40 or 20 MHz SYSCLK. The time reference for clock generation can be an external 40, 20 or 4 MHz crystal, ceramic resonator or external clock.

The OSC register controls the oscillator. The PLL can be enabled to multiply the 4 MHz clock by 10.

The internal 40/20 MHz can be divided by two.

The internally generated clock can be divided and provided on the CLKO pin.





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6.0 I/O CONFIGURATION

The IOCON register is used to configure the I/O pins:

- CLKO/SOF: select Clock Output or Start of Frame.
- TXCANOD: TXCAN can be configured as Push-Pull or as Open Drain output. Open Drain outputs allows the user to connect multiple controllers together to build a CAN network without using a transceiver.
- INT0 and INT1 can be configured as GPIO with similar registers as in the PIC microcontrollers or as Transmit and Receive interrupts.
- INT0/GPIO0/XSTBY can also be used to automatically control the standby pin of the transceiver.

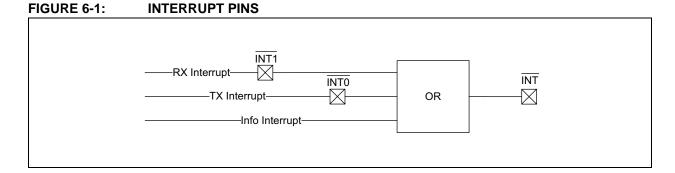
• INTOD: The interrupt pins can be configured as open-drain or push/pull outputs.

6.1 Interrupt Pins

The MCP2517FD contains three different interrupt pins, see Figure 6-1:

- INT is asserted on any interrupt in the CiINT register (xIF & xIE), including the RX and TX interrupts.
- INT1/GPIO1 can be configured as GPIO or RX interrupt pin (CIINT.RXIF & RXIE).
- INT0/GPIO0 can be configured as GPIO or TX interrupt pin (CIINT.TXIF & TXIE).

All interrupt pins are active low.



7.0 ELECTRICAL SPECIFICATIONS

7.1 Absolute Maximum Ratings†

VDD	–0.3V to 6.0V
DC Voltage at all I/O w.r.t GND	–0.3V to VDD + 0.3V
Virtual Junction Temperature, TvJ (IEC60747-1)	40°C to +165°C
Soldering temperature of leads (10 seconds)	+300°C
ESD protection on all pins (IEC 801; Human Body Model)	±4 kV
ESD protection on all pins (IEC 801; Machine Model)	±400V
ESD protection on all pins (IEC 801; Charge Device Model)	±750V

† NOTICE: Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

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DC Specifications High (H): TAMB = -40°C to +150°C; '						2 7V to 5 5V		
Sym.	Characteristic	Min. Typ. Max. Units Conditions/Com						
VDD Pin		1						
Vdd	Voltage Range	2.7		5.5	V	RAM data retention guaranteed		
VPORH	Power-on Reset Voltage			2.65	V	Highest voltage on VDD before device releases POR		
VPORL	Power-on Reset Voltage	2.2			V	Lowest voltage on VDD before device asserts POR		
SVDD	VDD Rise Rate to ensure POR	0.05			V/ms	Note 1		
Idd	Supply Current		15	20	mA	40 MHz SYSCLK, 20 MHz SPI activity		
IDDS	Sleep Current		10	60	μA	Clock is stopped TAMB ≤ +85°C (Note 1)		
				550		Clock is stopped TAMB ≤ +150°C		
Digital Inp	ut Pins:							
VIH	High-Level Input Voltage	0.7 Vdd		VDD + 0.3	V			
VIL	Low-Level Input Voltage	-0.3		0.3 Vdd	V			
VOSCPP	OSC1 detection Voltage	0.5			V	Minimum peak-to-peak voltage on OSC1 pin (Note 1)		
Iц	Input Leakage Current							
	OSC1	-5		+5	μA			
	All other	-1		+1	μA			
Digital Out	tput Pins:							
Voн	High-Level Output Voltage	VDD - 0.7			V	Юн = –2 mA, VDD = 2.7V		
Vol	Low-Level Output Voltage							
	TXCAN			0.6	V	IOL = 8 mA, VDD = 2.7V		
	All other	1		0.6	V	IOL = 2 mA, VDD = 2.7V		

TABLE 7-1: DC CHARACTERISTICS

Note 1: Characterized; not 100% tested.

TABLE 7-2: CLKOUT AND SOF AC CHARACTERISTICS

AC Specific	cations	Electrical Characteristics: High (H): TAMB = -40°C to +150°C; VDD = 2.7V to 5.5V					
Sym.	Characteristic	Min.	Тур.	Max.	Units	Conditions/Comments	
TCLKOH	CLKO Output High	8			ns	@ 40 MHz (Note 1)	
TCLKOL	CLKO Output Low	8			ns	Note 1	
TCLKOR	CLKO Output Rise			5	ns	Note 1	
TCLKOF	CLKO Output Fall			5	ns	Note 1	
TSOFH	SOF Output High		31 Tosc		ns	Note 2	
TSOFPD	SOF Propagation Delay: RXCAN falling edge to SOF rising edge		1 Tosc		ns	Note 2	

Note 1: Characterized; not 100% tested.

2: Design guidance only.

AC Specifica	ations	Electrical Characteristics:							
		High (H): TAMB = -40°C to +150°C; VDD = 2.7V to 5.5V							
Sym.	Characteristic	Min.	Тур.	Max.	Units	Conditions/Comments			
Fosc1,CLKI	OSC1 Input Frequency	2	40	40	MHz	External digital clock			
FOSC1,4M	OSC1 Input Frequency	4 – 0.5%	4	4+0.5%	MHz	4 MHz crystal/resonator (Note 1)			
Fdrift	SYSCLK frequency drift			10	ppm	Additional frequency drift of SYSCLK due to internal PLL @ 4 MHz (Note 1)			
Fosc1,20M	OSC1 Input Frequency	20 – 0.5%	20	20+0.5%	MHz	20 MHz crystal/resonator (Note 1)			
Fosc1,40M	OSC1 Input Frequency	40 – 0.5%	40	40+0.5%	MHz	40 MHz crystal/resonator (Note 1)			
Tosc1	TOSC1=1/FOSC1,x	25			ns				
Tosc1H	OSC1 Input High	0.45 * Tosc		0.55 * TOSC	ns	Note 1			
TOSC1L	OSC1 Input Low	0.45 * Tosc		0.55 * TOSC	ns	Note 1			
TOSC1R	OSC1 Input Rise			20	ns	Note 2			
TOSC1F	OSC1 Input Fall			20	ns	Note 2			
DCosc1	Duty Cycle on OSC1	45	50	55	%	External clock duty cycle requirement (Note 1)			
TOSCSTAB	Oscillator stabilization period			3	ms	From POR to final frequency (Note 1)			
TOSCSLEEP	Oscillator stabilization from Sleep			3	ms	From Sleep to final frequency (Note 1)			
Gм,4M	Transconductance	1470		2210	μA/V	4 MHz crystal (Note 2)			
Gм,40M	Transconductance	2040		3060	μ A /V	40 MHz crystal (Note 2)			

TABLE 7-3: CRYSTAL OSCILLATOR AC CHARACTERISTICS

Note 1: Characterized; not 100% tested.

2: Design guidance only.

TABLE 7-4: CAN BIT RATE

AC Specific	ations	Electrical Characteristics: High (H): TAMB = -40°C to +150°C; VDD = 2.7V to 5.5V Min. Typ. Max. Units Conditions/Commen				
Sym.	Characteristic	Min.	Тур.	Max.	Conditions/Comments	
BRNOM	Nominal Bit Rate	0.125	0.5	1	Mbps	
BRDATA	Data Bit Rate	0.5	2	8	Mbps	BRDATA ≥ BRNOM

Note 1: Tested bit rates. Device allows the configuration of more bit rates, including slower bit rates than the minimum stated.

TABLE 7-5:CAN RX FILTER AC CHARACTERISTICS

AC Specific	ations	Electrical Characteristics: High (H): TAMB = –40°C to +150°C; VDD = 2.7V to 5.5V					
Sym.	Characteristic	Min.	Min. Typ. Max. Units Conditions/Comm				
TPROP	Filter propagation delay		1		ns	Note 2	
TFILTER	Filter time (Note 3)	40 70 125 225		75 120 215 390	ns	T00filter T01filter T10filter T11filter	
TREVO- CERY	Minimum high time on input for output to go high again	5			ns	Note 2	

Note 1: Characterized; not 100% tested.

2: Design guidance only.

3: Pulses on RXCAN shorter than the minimum TFILTER time will be ignored; pulses longer than the maximum TFILTER time will wake-up the device.

TABLE 7-6: SPI AC CHARACTERISTICS

			Electrical Characteristics: High (H): TAMB = -40°C to +150°C; VDD = 2.7V to 5.5V				
Param.	Sym.	Characteristic	Min.	Тур.	Max.	Units	Conditions
	Fsck	SCK Input Frequency			20	MHz	Note 3
	Тѕск	SCK Period, TSCK=1/FSCK	50			ns	Note 3
1	Тѕскн	SCK High Time	20			ns	
2	TSCKL	SCK Low Time	20			ns	
3	TSCKR	SCK Rise Time			100	ns	Note 2
4	TSCKF	SCK Fall Time			100	ns	Note 2
5	TCS2SCK	nCS ↓ to SCK ↑	Tsck/2			ns	
6	TSCK2CS	SCK ↑ to nCS ↑	Тѕск			ns	
7	TSDI2SCK	SDI Setup: SDI ‡ to SCK ↑	5			ns	
8	TSCK2SDI	SDI Hold: SCK ↑ to SDI ↓	5			ns	
9	TSCK2SDO	SDO Valid: SCK ↓ to SDO ↓			20	ns	CLOAD = 50 pF
10	TCS2SDOZ	SDO High Z: nCS ↑ to SDO Z			2 Tsck	ns	CLOAD = 50 pF
11	TCSD	nCS ↑ to nCS ↓	Тѕск			ns	Note 2

Note 1: Characterized; not 100% tested.

- 2: Design guidance only.
- 3: FSCK must be less than or equal to FSYSCLK/2.

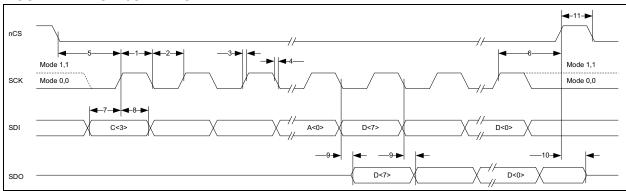


FIGURE 7-1: SPI I/O TIMING

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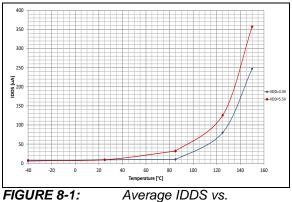
TABLE 7-7. TEMPERATURE SPECIFICATIONS								
Parameters	Sym.	Min.	Тур.	Max.	Units	Conditions		
Temperature Ranges								
Operating Temperature Range	TA	-40		+150	°C			
Storage Temperature Range	TA	-55		+150	°C			
Thermal Package Resistance								
Thermal Resistance for SOIC-14	θJA	_	+149.5		°C/W			
Thermal Resistance for DFN-14	θJA	_	+64.1	_	°C/W			

TABLE 7-7: TEMPERATURE SPECIFICATIONS

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8.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

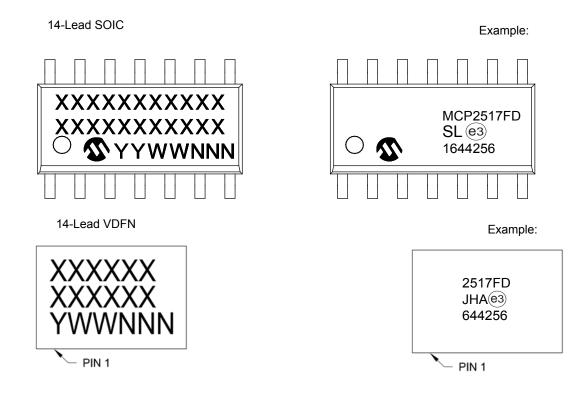


Temperature

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9.0 PACKAGING INFORMATION

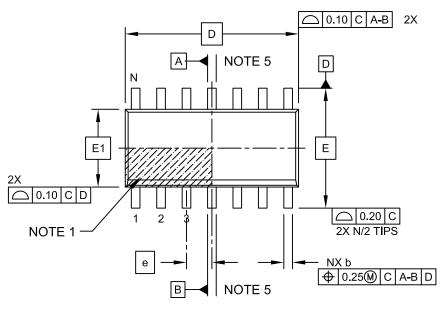
9.1 Package Marking Information



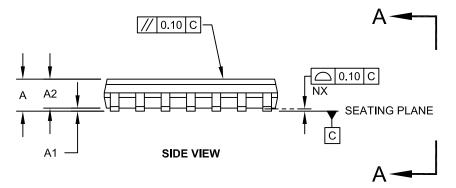
 Year code (last digit of calendar year) Year code (last 2 digits of calendar year) W Week code (week of January 1 is week '01') N Alphanumeric traceability code Pb-free JEDEC[®] designator for Matte Tin (Sn) This package is Pb-free. The Pb-free JEDEC designator (e3)
 W Week code (week of January 1 is week '01') IN Alphanumeric traceability code B Pb-free JEDEC[®] designator for Matte Tin (Sn)
IN Alphanumeric traceability code B) Pb-free JEDEC [®] designator for Matte Tin (Sn)
B) Pb-free JEDEC [®] designator for Matte Tin (Sn)
can be found on the outer packaging for this package.
e event the full Microchip part number cannot be marked on one line, it will be carried over to ext line, thus limiting the number of available characters for customer-specific information.

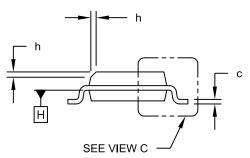
14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



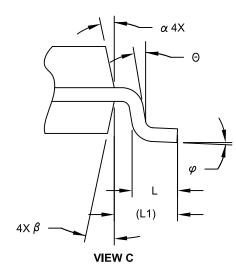


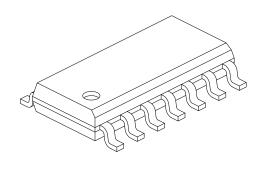


Microchip Technology Drawing No. C04-065C Sheet 1 of 2

14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging





	MILLIMETERS				
Dimension Lin	nits	MIN	NOM	MAX	
Number of Pins	N		14		
Pitch	е		1.27 BSC		
Overall Height	A	-	-	1.75	
Molded Package Thickness	A2	1.25	-	-	
Standoff §	A1	0.10	-	0.25	
Overall Width	E	6.00 BSC			
Molded Package Width	E1	3.90 BSC			
Overall Length	D	8.65 BSC			
Chamfer (Optional)	h	0.25	-	0.50	
Foot Length	L	0.40	-	1.27	
Footprint	L1	1.04 REF			
Lead Angle	Θ	0°	-	-	
Foot Angle	φ	0°	-	8°	
Lead Thickness	с	0.10	-	0.25	
Lead Width	b	0.31	-	0.51	
Mold Draft Angle Top	α	5°	-	15°	
Mold Draft Angle Bottom	β	5°	-	15°	

Notes:

- 1. Pin 1 visual index feature may vary, but must be located within the hatched area.
- 2. § Significant Characteristic
- 3. Dimension D does not include mold flash, protrusions or gate burrs, which shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25 mm per side.
- 4. Dimensioning and tolerancing per ASME Y14.5M
 - BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

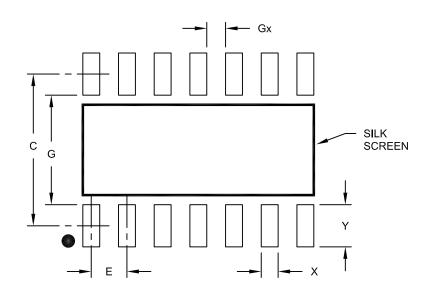
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-065C Sheet 2 of 2

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14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

	Units	MILLIMETERS				
Dimension		MIN	NOM	MAX		
Contact Pitch	E 1.27 BSC					
Contact Pad Spacing	С		5.40			
Contact Pad Width	X			0.60		
Contact Pad Length	Y			1.50		
Distance Between Pads	Gx	0.67				
Distance Between Pads	G	3.90				

Notes:

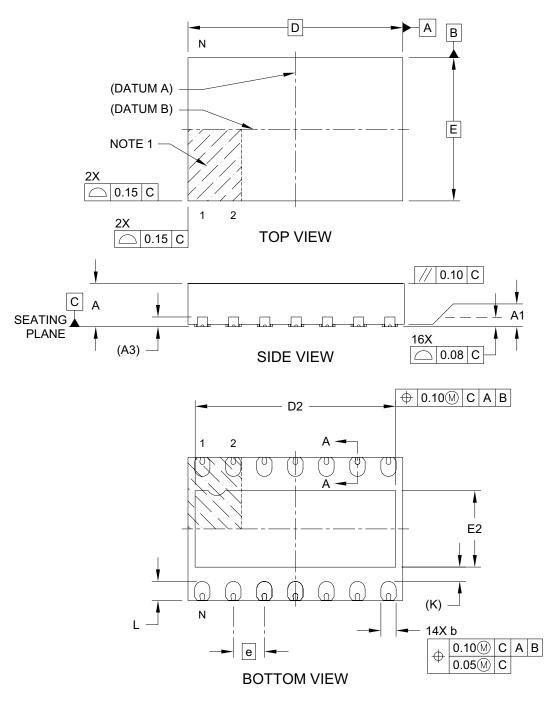
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2065A

14-Lead Very Thin Plastic Quad Flat, No Lead Package (JHA) - 4.5x3.0 mm Body [VDFN] With Dimpled Wettable Flanks

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

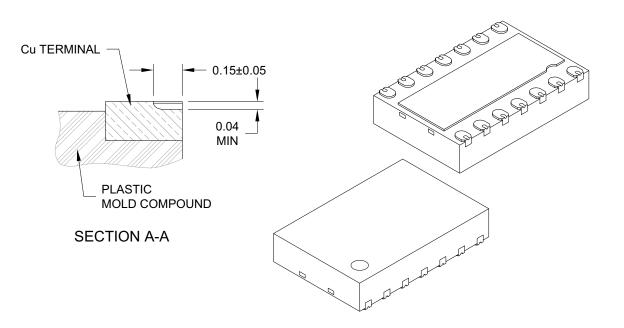


Microchip Technology Drawing C04-1198A Sheet 1 of 2

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14-Lead Very Thin Plastic Quad Flat, No Lead Package (JHA) - 4.5x3.0 mm Body [VDFN] With Dimpled Wettable Flanks

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units	MILLIMETERS			
Dimensior	n Limits	MIN	NOM	MAX	
Number of Terminals	N		14		
Pitch	е		0.65 BSC		
Overall Height	A	0.80	0.85	0.90	
Standoff	A1	0.00	0.02	0.05	
Terminal Thickness	A3	0.203 REF			
Overall Length	D	4.50 BSC			
Exposed Pad Length	D2	4.15	4.20	4.25	
Overall Width	E		3.00 BSC		
Exposed Pad Width	E2	1.55	1.60	1.65	
Terminal Width	b	0.29	0.32	0.35	
Terminal Length	L	0.35	0.40	0.45	
Terminal-to-Exposed-Pad	K		0.30 REF		

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

- 2. Package is saw singulated
- 3. Dimensioning and tolerancing per ASME Y14.5M

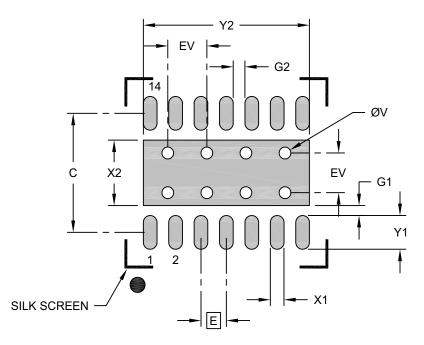
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-1198A Sheet 2 of 2

14-Lead Very Thin Plastic Quad Flat, No Lead Package (JHA) - 4.5x3.0 mm Body [VDFN] With Dimpled Wettable Flanks

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

	MILLIMETERS			
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Optional Center Pad Width	X2			1.65
Optional Center Pad Length	Y2			4.25
Contact Pad Spacing	С		3.00	
Contact Pad Width (X14)	X1			0.35
Contact Pad Length (X14)	Y1			0.85
Contact Pad to Center Pad (X14)	G1	0.25		
Spacing Between Contacts (X12)	G1	0.30		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-3198A

APPENDIX A: REVISION HISTORY

Revision B (May 2018)

The following is the list of modifications:

- 1. Updated the Active Current value in the **Features** section.
- 2. Updated Register 3-28, Register 3-29 and Register 3-32.
- 3. Updated Section 6.1 "Interrupt Pins".
- 4. Updated Table 7-4.

Revision A (August 2017)

• Original Release of this Document.

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ISO 11898-1:2015 lists non-mandatory features. Table B-1 clarifies which optional features are

implemented.

APPENDIX B: CAN FD CONFORMANCE

The MCP2517FD passed the CAN FD conformance tests specified in ISO 16845-1:2016.

TABLE B-1: ISO OPTIONAL FEATURES

No.	Optional Feature	Implemented	
1	FD frame format	Yes	
2	Disabling of frame formats	Yes. Classical CAN frame format.	
3	Limited LLC frames	No. Full range of IDs and DLCs implemented.	
4	No transmission of frames including padding bytes	N/A. See No. 3.	
5	LLC Abort interface	Yes	
6	ESI and BRS bit values	Yes	
7	Method to provide MAC data consistency	Yes	
8	Time and time triggering	Start of Frame output.	
9	Time stamping	Yes. 32 bit TBC.	
10	Bus monitoring mode	Yes	
11	Handle	Yes	
12	Restricted operation	Yes	
13	Separate prescalers for nominal bits and for data bits	Yes	
14	Disabling of automatic retransmission	Yes	
15	Maximum number of retransmissions	Yes. One, 3, or unlimited.	
16	Disabling of protocol exception event on res bit detected recessive	Yes. Selectable.	
17	PCS_Status	No	
18	Edge filtering during the bus integration state	Yes. Selectable.	
19	Time resolution for SSP placement	Yes. 128 To. Measured, manual or disabled.	
20	FD_T/R message	TX and RX interrupts.	

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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	[X] ⁽¹⁾ –X /XX	Examples:			
Device Tape and Reel Temperature Package Range		a) b)		22517FD-H/SL: 22517FDT-H/SL:	High Temperature, Plastic SOIC (150 mil Body), 14-Lead Tape and Reel,
Device:	MCP2517FD: CAN FD Controller				High Temperature, Plastic SOIC (150 mil Body), 14-Lead
Tape and Reel Option:	Blank = Standard packaging (tube or tray) T = Tape and Reel ⁽¹⁾	c)	MCF	2517FD-H/JHA:	High Temperature, VDFN (4.5x3 mm Body), 14-Lead with Dimpled
	i = Tape and Reel ()				Wettable Flanks
Temperature Range:	H = -40°C to +150°C (High)	d)	MCF	2517FDT-H/JHA:	High Temperature, VDFN (4.5x3 mm Body), 14-Lead with Dimpled Wettable Flanks
Package:	SL = Plastic SOIC (150 mil Body), 14-Lead JHA = Plastic VDFN (4.5x3 mm Body), 14-Lead with Dimpled Wettable Flanks	Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.			

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