

14-24-Logic-EVM User's Guide

This user's guide contains support documentation for the 14-24-Logic Evaluation Module (EVM). Included is a description of how to set up and configure the EVM, the printed circuit board (PCB) layout, the schematic, and the bill of materials (BOM) of the 14-24-Logic-EVM.

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Trademarks

1 Introduction

The 14-24-Logic-EVM is a generic EVM developed to support leaded Logic devices in the PW, DB, D, DW, NS, N, P, and DGV packages. This EVM can be used to evaluate any device in the package family and pin counts described in [Table 1](#). The PCB can be broken down into six sections with each section supporting certain packages indicated on the board. This EVM allows the user to have a great amount of flexibility when evaluating leaded Logic devices.

Table 1. Package and Pin Support Table

TI Package Name	Package Family	# of Pins
PW	TSSOP	14, 16, 20, 24
DB	SSOP	14, 16, 20, 24
NS	SOP	14, 16, 20, 24
DGV	TVSOP	14, 16, 20, 24
D	SOIC	14, 16, 20, 24
DW	SOIC	14, 16, 20, 24
N	PDIP	14, 16, 20
P	PDIP	14, 16, 20

1.1 Kit Contents

Table 2. 14-24-Logic-EVM Kit Contents

Item	Description	Quantity
14-24-Logic-EVM	PCB	1
Headers	12 position, 100-mil (2.54 mm), thru-hole	6

1.2 Features

The 14-24-Logic-EVM has the following features:

- Multiple package support
- Breadboard compatible
- Easy-to-use / Flexible evaluation

2 Hardware

2.1 PCB Overview

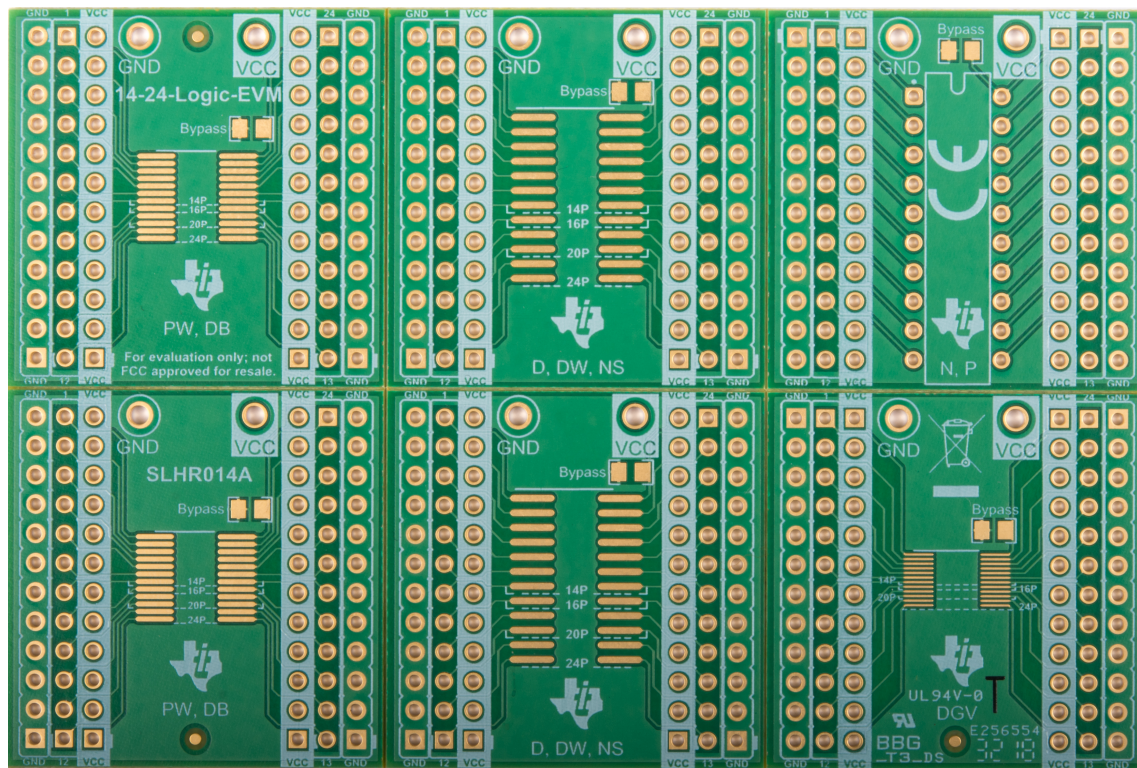


Figure 1. 14-24-Logic-EVM PCB

The 14-24-Logic-EVM PCB is designed to be straightforward for new users to begin evaluating leaded Logic devices. This section will highlight a few aspects of the PCB that are helpful to the user.

- Board breakable into six sections with inclusion of v-scored grooves
- Each section has headers connected to device pins, V_{CC} , and GND
- Dashed lines included to assist with the placement of devices with less than 24 pins
- Designated supply inputs which can support thru-hole test points
- Bypass capacitor footprint included for device V_{CC}

2.2 Hardware Setup

This section will cover the six steps to take when evaluating a leaded Logic device using this EVM.

1. Identify the package you will be using for the device being evaluated. As stated previously, this EVM has six sections each of which contains a footprint in which a logic device can be placed. Break off the selected section (optional).
2. Solder down the device. Some sections support multiple packages so carefully solder down the device to make sure it is aligned properly. If a device with less than 24 pins is being evaluated, it should be placed towards the top of the footprint.
3. Ensure device V_{CC} pin is connected to the bypass capacitor. If pin 1 of the device is connected to pin 1 of the footprint then it will be connected correctly. [Figure 2](#) shows an example of a 14-pin device in the D package placed correctly on the EVM.

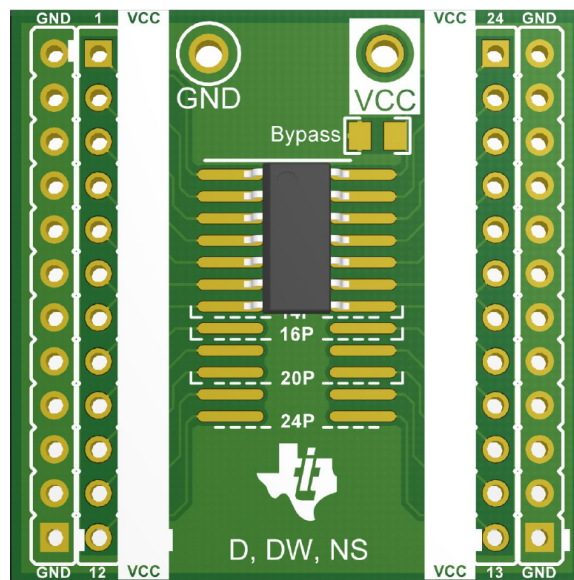


Figure 2. 14-Pin Device in D Package

4. Interface with device pins. The kit includes six 12-pin headers which will allow the user to fully populate a single section. An example of this, with the addition of test points and a bypass capacitor for the supply, can be seen in [Figure 3](#).

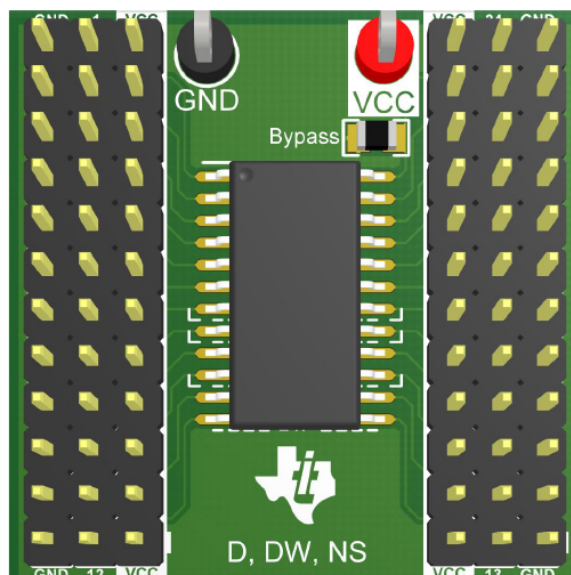


Figure 3. Fully Populated Section

- The device V_{CC} pin will need to be connected to the V_{CC} of the EVM. If using the headers, this can be accomplished using a simple shunt. If the headers are not being used then a simple solder bridge can be formed from the I/O header pad to the V_{CC} header pad.
- Repeat step 5 for the GND pin and any unused input pins of the device. [Figure 4](#) shows an example of how to use shunts to both power the device and tie unused inputs to a defined logic state to prevent them from floating. For more information on why it is important to avoid floating inputs, see the [Implications of Slow or Floating CMOS Inputs](#) application report.

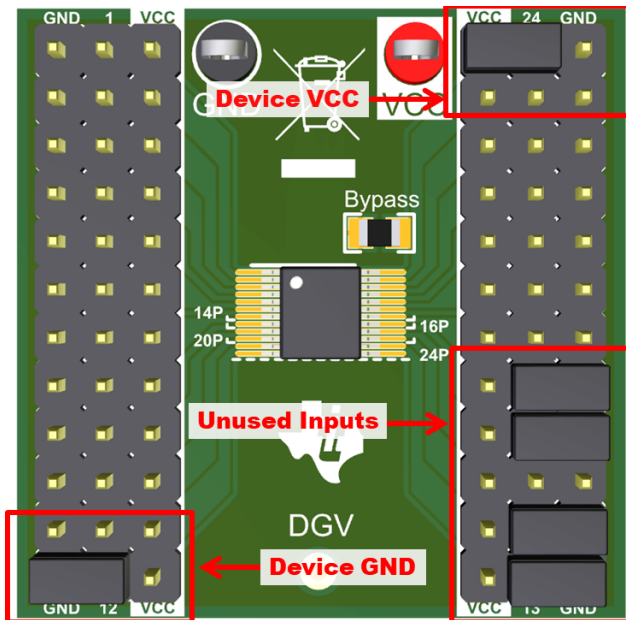


Figure 4. Shunt Usage for Device Evaluation

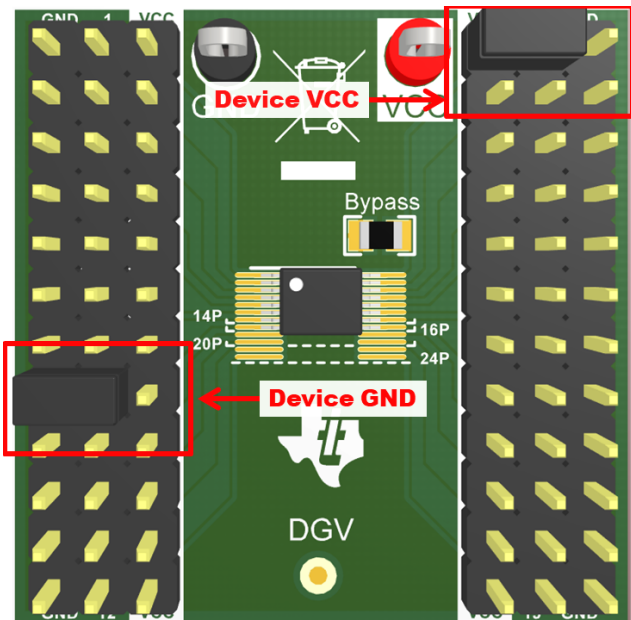


Figure 5. Shunt Usage for 16-pin Device

[Figure 5](#) is included to highlight that the GND shunt will shift up as the device pin count decreases even though the V_{CC} will always be shunted in the top right assuming the device is placed correctly.

3 Board Layout

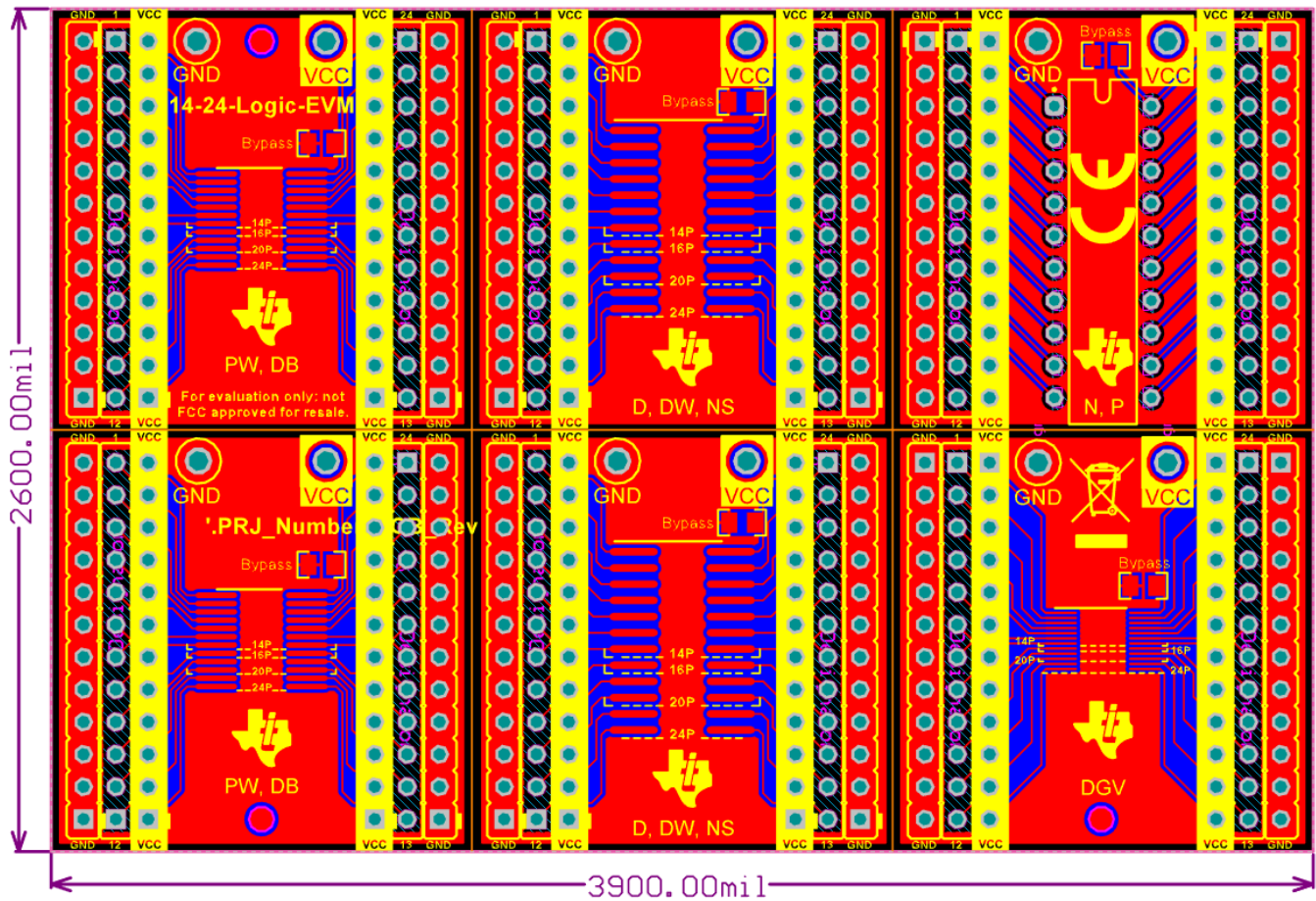


Figure 6. 14-24-Logic-EVM Layout

4 Bill of Materials

This section will provide information on the components that can be used with the 14-24-Logic-EVM. Other components can be used as long as they are able to fit the provided plated holes and pads.

Table 3. Bill of Materials

Item	Value	Description	Package Reference	Part Number	Manufacturer
Bypass Capacitor	0.1 μ F	CAP, CERM, 0.1 μ F, 50 V, \pm 20%, X7R, 0805	0805	08055C104MAT2A	AVX
Header		Header, 2.54 mm, 12x1, Gold, TH	Header, 2.54 mm, 12x1, TH	PBC12SABN	Sullins Connector Solutions
Red Test Point		Test Point, Multipurpose, Red, TH	Red Multipurpose Testpoint	5010	Keystone
Black Test Point		Test Point, Multipurpose, Black, TH	Black Multipurpose Testpoint	5011	Keystone

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