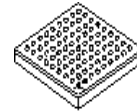




i.MX28

i.MX28 Applications Processors for Consumer Products



Package Information

Plastic package

Case MAPBGA-289, 14 x 14 mm, 0.8 mm pitch

Ordering Information

See [Table](#) on [page 3](#) for ordering information.

1 Introduction

The i.MX28 is a low-power, high-performance applications processor optimized for the general embedded industrial and consumer markets. The core of the i.MX28 is NXP's fast, power-efficient implementation of the ARM926EJ-S™ core, with speeds of up to 454 MHz.

The device is suitable for a wide range of applications, including the following:

- Human-machine interface (HMI) panels: industrial, home
- Industrial drive, PLC, I/O control display, factory robotics display, graphical remote controls
- Handheld scanners and printers
- Patient-monitoring, portable medical devices
- Smart energy meters, energy gateways
- Media phones, media gateways

The integrated power management unit (PMU) on the i.MX28 is composed of a triple output DC-DC switching converter and multiple linear regulators. These provide

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power sequencing for the device and its I/O peripherals such as memories and SD cards, as well as provide battery charging capability for Li-Ion batteries.

The i.MX28 processor includes an additional 128-Kbyte on-chip SRAM to make the device ideal for eliminating external RAM in applications with small footprint RTOS.

The i.MX28 supports connections to various types of external memories, such as mobile DDR, DDR2 and LV-DDR2, SLC and MLC NAND Flash.

The i.MX28 can be connected to a variety of external devices such as high-speed USB2.0 OTG, CAN, 10/100 Ethernet, and SD/SDIO/MMC.

1.1 Device Features

The following lists the features of the i.MX28:

- ARM926EJ-S CPU running at 454 MHz:
 - 16-Kbyte instruction cache and 32-Kbyte data cache
 - Arm embedded trace macrocell (CoreSight™ ETM9™)
 - Parallel JTAG interface
- 128 KBytes of integrated low-power on-chip SRAM
- 128 KBytes of integrated mask-programmable on-chip ROM
- 1280 bits of on-chip one-time-programmable (OCOTP) ROM
- 16-bit mobile DDR (mDDR) (1.8 V), DDR2 (1.8 V) and LV-DDR2 (1.5 V), up to 205 MHz DDR clock frequency with voltage overdrive
- Support for up to eight NAND Flash memory devices with up to 20-bit BCH ECC
- Four synchronous serial ports (SSP) for SDIO/MMC/MS/SPI: SSP0, SSP1, SSP2, and SSP3. SSP0 and SSP1 can support three modes, 1-bit, 4-bit, and 8-bit, whereas SSP2 and SSP3 can support only 1-bit and 4-bit modes.
- 10/100-Mbps Ethernet MAC compatible with IEEE Std 802.3™:
 - Single 10/100 Ethernet with GMII/RMII or Dual 10/100 Ethernet with RMII interface
 - Supporting IEEE Std 1588™-compatible hardware timestamp
 - Supporting 50-MHz/25-MHz clock output for external Ethernet PHY
- Two 2.0B protocol-compatible Controller Area Network (CAN) interfaces
- One USB2.0 OTG device/host controller and PHY
- One USB2.0 host controller and PHY
- LCD controller, up to 24-bit RGB (DOTCK) modes and 24-bit system-mode
- Pixel-processing pipeline (XP) supports full path from color-space conversion, scaling, alpha-blending to rotation without intermediate memory access.
- SPDIF transmitter
- Dual serial audio interface (SAIF) to support full-duplex transmit and receive operations; each SAIF supports three stereo pairs

- Five application Universal Asynchronous Receiver-Transmitters (UARTs), up to 3.25 Mbps with hardware flow control
- One debug UART operating at up to 115 Kb/s using programmed I/O
- Two I²C master/slave interfaces, up to 400 kbps
- Four 32-bit timers and a rotary decoder
- Eight Pulse Width Modulators (PWMs)
- Real-time clock (RTC)
- GPIO with interrupt capability
- Power Management Unit (PMU) supports a triple output DC-DC switching converter, multiple linear regulators, battery charger, and detector.
- 16-channel Low-Resolution A/D Converter (LRADC). There are 16 physical channels but they can only be mapped to 8 virtual channels at a time.
- Single channel High Speed A/D Converter (HSADC), up to 2 Msp/s data rate
- 4/5-wire touchscreen controller
- Up to 8X8 keypad matrix with button-detect circuit
- Security features:
 - Read-only unique ID for Digital Rights Management (DRM) algorithms
 - Secure boot using 128-bit AES hardware decryption
 - SHA-1 and SHA256 hashing hardware
 - High assurance boot (HAB4)
- Offered in 289-pin Ball Grid Array (BGA)

1.2 Ordering Information and Functional Part Differences

Table 1 provides the ordering information for the i.MX28.

Table 1. Ordering Information

| Part Number | Projected Temperature Range (°C) | Package |
|---------------|----------------------------------|--------------------------------------|
| MCIMX280DVM4B | -20 to +70 | 14 x 14 mm, 0.8mm pitch, MAPBGA-289 |
| MCIMX280DVM4C | -20 to +70 | 14 x 14 mm, 0.8mm pitch, MAPBGA-289 |
| MCIMX280CVM4B | -40 to +85 | 14 x 14 mm, 0.8mm pitch, MAPBGA-289 |
| MCIMX280CVM4C | -40 to +85 | 14 x 14 mm, 0.8mm pitch, MAPBGA-289 |
| MCIMX283DVM4B | -20 to +70 | 14 x 14 mm, 0.8 mm pitch, MAPBGA-289 |
| MCIMX283DVM4C | -20 to +70 | 14 x 14 mm, 0.8 mm pitch, MAPBGA-289 |
| MCIMX283CVM4B | -40 to +85 | 14 x 14 mm, 0.8 mm pitch, MAPBGA-289 |
| MCIMX283CVM4C | -40 to +85 | 14 x 14 mm, 0.8 mm pitch, MAPBGA-289 |
| MCIMX286DVM4B | -20 to +70 | 14 x 14 mm, 0.8 mm pitch, MAPBGA-289 |
| MCIMX286DVM4C | -20 to +70 | 14 x 14 mm, 0.8 mm pitch, MAPBGA-289 |

Table 1. Ordering Information (continued)

| Part Number | Projected Temperature Range (°C) | Package |
|---------------|----------------------------------|--------------------------------------|
| MCIMX286CVM4B | –40 to +85 | 14 x 14 mm, 0.8 mm pitch, MAPBGA-289 |
| MCIMX286CVM4C | –40 to +85 | 14 x 14 mm, 0.8 mm pitch, MAPBGA-289 |
| MCIMX287CVM4B | –40 to +85 | 14 x 14 mm, 0.8 mm pitch, MAPBGA-289 |
| MCIMX287CVM4C | –40 to +85 | 14 x 14 mm, 0.8 mm pitch, MAPBGA-289 |

Table 2 provides the functional differences between the i.MX280, i.MX283, i.MX286, and i.MX287.

Table 2. i.MX28 Functional Differences

| Function | i.MX280 | i.MX283 | i.MX286 | i.MX287 |
|--------------------------|------------------------|------------------------|------------------------|------------------------|
| Application UART | x5 | x5 | x5 | x5 |
| Debug UART | x1 | x1 | x1 | x1 |
| CAN | — | — | x2 | x2 |
| Ethernet | x1 | x1 | x1 | x2 |
| High-speed ADC | x1 | x1 | x1 | x1 |
| L2 Switch | — | — | — | Yes |
| LCD Interface | — | Yes | Yes | Yes |
| LRADC ¹ | x8 | x8 | x8 | x8 |
| PWM | x8 | x8 | x8 | x8 |
| S/PDIF Tx | — | — | Yes | Yes |
| SD/SDIO/MMC ² | x4 | x4 | x4 | x4 |
| Security | Yes | Yes | Yes | Yes |
| SPI | x4 | x4 | x4 | x4 |
| Touch Screen | — | Yes | Yes | Yes |
| USB 2.0 | OTG HS with HS PHY x1 | OTG HS with HS PHY x1 | OTG HS with HS PHY x1 | OTG HS with HS PHY x1 |
| | HS Host with HS PHY x1 | HS Host with HS PHY x1 | HS Host with HS PHY x1 | HS Host with HS PHY x1 |

¹ There are 16 physical channels but they can only be mapped to 8 virtual channels at a time.

² For SD/SDIO/MMC, four synchronous serial ports (SSP) are available: SSP0, SSP1, SSP2, and SSP3. SSP0 and SSP1 can support three modes, 1-bit, 4-bit, and 8-bit, whereas SSP2 and SSP3 can support only 1-bit and 4-bit modes.

1.3 Block Diagram

Figure 1 shows the simplified interface block diagram.

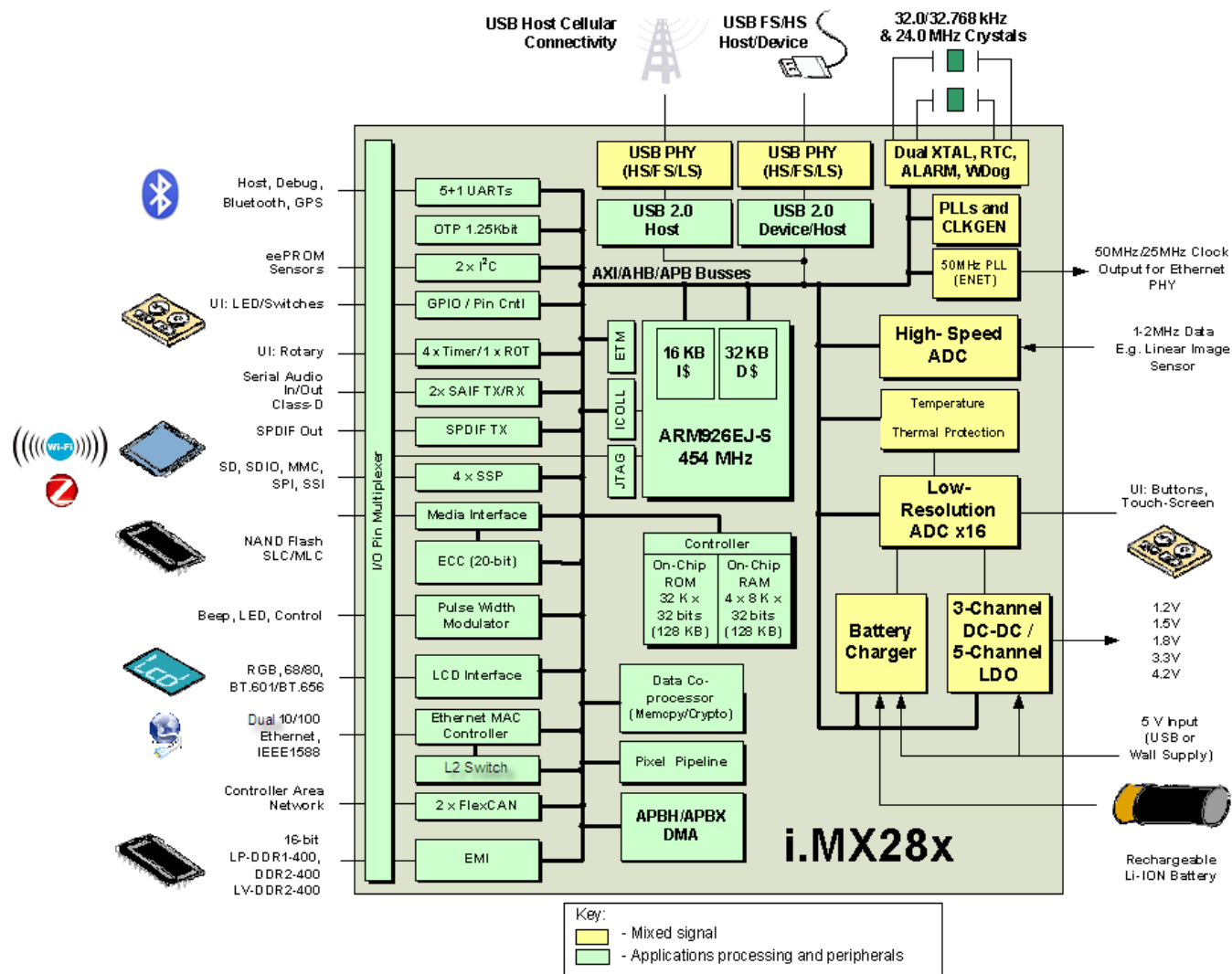


Figure 1. i.MX28 Simplified Interface Block Diagram

2 Features

Table 3 shows the device functions.

Table 3. i.MX28 Functions

| Function | BGA289 |
|---|--------------------------------------|
| External Memory Interface (EMI) (1.5 V LV-DDR2, 1.8 V DDR2, 1.8 V LP-DDR1) | Yes |
| General-Purpose Media Interface (GPMI): <ul style="list-style-type: none"> • NAND data width • Number of external NANDs supported | 8-bit 4 dedicated / 8 with muxing |
| Pulse Width Modulator (PWM) | 5 dedicated / 8 with muxing |
| Application UART (AUART): Interfaces supported | 4 dedicated / 5 with muxing |
| Synchronous Serial Port (SSP): Supported through dedicated pins | 3 dedicated / 4 with muxing |
| I ² C | 1 dedicated / 2 with muxing |
| SPDIF | 1 |
| SAIF | 2 |
| FlexCAN | 2 |
| LCD interface | 24 bits |
| High-speed ADC | Yes |
| LRADC (touchscreen, keypad...) | Yes |
| Ethernet MAC and switch | Up to 2 MACs with switch |
| Universal Serial Bus (USB) | 2 |

Table 4 describes the digital and analog modules of the device.

Table 4. i.MX28 Digital and Analog Modules

| Block Mnemonic | Block Name | Subsystem | Brief Description |
|----------------|--------------------------------|--------------------------|--|
| APBHDMA | AHB to APBH Bridge with DMA | System control | The AHB to APBH bridge with DMA includes the AHB-to-APB PIO bridge for memory-mapped I/O to the APB devices, as well a central DMA facility for devices on this bus. The bridge provides a peripheral attachment bus running on the AHB's HCLK. (The 'H' in APBH denotes that the APBH is synchronous to HCLK, as compared to APBX, which runs on the crystal-derived XCLK.) The DMA controller transfers read and write data to and from each peripheral on APBH bridge. |
| APBXDMA | AHB to APBX Bridge with DMA | System control | The AHB-to-APBX bridge includes the AHB-to-APB PIO bridge for memory-mapped I/O to the APB devices, as well a central DMA facility for devices on this bus. The AHB-to-APBX bridge provides a peripheral attachment bus running on the AHB's XCLK. (The 'X' in APBX denotes that the APBX runs on a crystal-derived clock, as compared to APBH, which is synchronous to HCLK.) The DMA controller transfers read and write data to and from each peripheral on APBX bridge. |
| Arm9 or ARM926 | ARM926EJ-S CPU | Arm® | The ARM926 Platform consists of the ARM926EJ-S™ core and the ETM real-time debug modules. It contains the 16-Kbyte L1 instruction cache, 32-Kbyte L1 data cache, 128-Kbyte ROM and 128-Kbyte RAM. |
| AUART(5) | Application UART interface | Connectivity peripherals | Each of the UART modules supports the following serial data transmit/receive protocols and configurations: <ul style="list-style-type: none"> • 7- or 8-bit data words, one or two stop bits, programmable parity (even, odd, or none) • Programmable baud rates up to 3.25 MHz. This is a higher maximum baud rate than the 1.875 MHz specified by the TIA/EIA-232-F standard and previous NXP UART modules. 16-byte FIFO on Tx and 16-byte FIFO on Rx supporting auto-baud detection |
| BCH | Bit-correcting ECC accelerator | Connectivity peripherals | The Bose, Ray-Chaudhuri, Hocquenghem (BCH) Encoder and Decoder module is capable of correcting from 2 to 20 single bit errors within a block of data no larger than about 900 bytes (512 bytes is typical) in applications such as protecting data and resources stored on modern NAND Flash devices. |
| BSI | Boundary Scan Interface | Connectivity peripherals | The boundary scan interface is provided to enable board level testing. There are five pins on the device which is used to implement the IEEE Std 1149.1™ boundary scan protocol. |
| CLKCTRL | Clock control module | Clocks | The clock control module, or CLKCTRL, generates the clock domains for all components in the i.MX28 system. The crystal clock or PLL clock are the two fundamental sources used to produce most of the clock domains. For lower performance and reduced power consumption, the crystal clock is selected. The PLL is selected for higher performance requirements but requires increased power consumption. In most cases, when the PLL is used as the source, a Phase Fractional Divider (PFD) can be programmed to reduce the PLL clock frequency by up to a factor of 2. |
| DCP | Data co-processor | Security | This module provides support for general encryption and hashing functions typically used for security functions. Because its basic job is moving data from memory to memory, it also incorporates a memory-copy (memcpy) function for both debugging and as a more efficient method of copying data between memory blocks than the DMA-based approach. |

Table 4. i.MX28 Digital and Analog Modules (continued)

| Block Mnemonic | Block Name | Subsystem | Brief Description |
|---------------------|---------------------------------|--------------------------|--|
| DFLPT | Default first-level page table | System control | The DFLPT provides a unique method of implementing the Arm MMU first-level page table (L1PT) using a hardware-based approach. |
| DIGCTL | Digital control and on-chip RAM | System control | The digital control module includes sections for controlling the SRAM, the performance monitors, high-entropy pseudo-random number seed, free-running microseconds counter, and other chip control functions. |
| DUART | Debug UART | Connectivity peripherals | The Debug UART performs the following data conversions: <ul style="list-style-type: none"> Serial-to-parallel conversion on data received from a peripheral device Parallel-to-serial conversion on data transmitted to the peripheral device |
| EMI | External memory interface | Connectivity peripherals | The i.MX28 supports off-chip DRAM storage through the EMI controller, which is connected to the four internal AHB/AXI busses. The EMI supports multiple external memory types, including: <ul style="list-style-type: none"> 1.8-V Mobile DDR1 (LP-DDR1) Standard 1.8-V DDR2 Low Voltage 1.5-V DDR2 (LV-DDR2) |
| ENET | Ethernet MAC Controller | Connectivity peripherals | Ethernet MAC controller connected to the uDMA (unified DMA). Supports 10/100 Mbps with TCP/UDP/IP Acceleration and IEEE 1588 Functions; also supports RMII or MII connectivity. |
| FlexCAN(2) | Controller area network module | Connectivity peripherals | The Controller Area Network (CAN) protocol is a message based protocol used for serial data. It was designed specifically for automotive but is also used in industrial control and medical applications. The serial data bus runs at 1 Mbps. |
| GPMI | General-purpose media interface | Connectivity peripherals | The General-Purpose Media Interface (GPMI) controller is a flexible NAND Flash controller with 8-bit data width, up to 50-MBps I/O speed and individual chip-select and DMA channels for up to 8 NAND devices. It also provides a interface to 20-bit BCH for ECC. |
| HSADC | High-speed ADC | Connectivity peripherals | The high-speed ADC block is designed to sample an analog input with 12-bit resolution and a sample rate of up to 2 Msps. The output of the HSADC block can be moved to the external memory through APBH-DMA. A typical user case of the HSADC is to work with the PWM block to drive an external linear image scanner sensor. |
| I ² C(2) | I ² C module | Connectivity peripherals | The I ² C is a standard two-wire serial interface used to connect the chip with peripherals or host controllers. The I ² C operates up to 400 kbps in either I ² C master or I ² C slave mode. Each I ² C has a dedicated DMA channel and can also be controlled by CPU in PIO or PIO queue modes. It supports both 7-bit and 10-bit device address in master mode, and has programmable 7-bit address in slave mode. |
| ICOLL | Interrupt Collector | System control | The Arm9 CPU core has two interrupt input lines, IRQ and FIQ. The interrupt collector (ICOLL) can steer any of 128 interrupt sources to either the FIQ or IRQ line of the Arm9 CPU. |
| L2 Switch | 3-Port L2 Switch | Network Control | Programmable 3-Port Ethernet Switch with QOS |

Table 4. i.MX28 Digital and Analog Modules (continued)

| Block Mnemonic | Block Name | Subsystem | Brief Description |
|------------------|-------------------------------|----------------------------|---|
| LCDIF | LCD Interface | Multimedia peripherals | The LCDIF provides display data for external LCD panels from simple text-only displays to WVGA, 16/18/24 bpp color TFT panels. The LCDIF supports all of these different interfaces by providing fully programmable functionality and sharing register space, FIFOs, and ALU resources at the same time. The LCDIF supports RGB (DOTCLK) modes as well as system mode including both VSYNC and WSYNC modes. |
| LRADC | Low resolution ADC module | Connectivity peripherals | The sixteen-channel 12-bit low-resolution ADC (LRADC) block is used for voltage measurement. Channels 0 – 6 measure the voltage on the seven application-dependent LRADC pins. The auxiliary channels can be used for a variety of uses, including a resistor-divider-based wired remote control, external temperature sensing, touch-screen, and other measurement functions. |
| OCOTP Controller | On-chip OTP controller | Security | The on-chip one-time-programmable (OCOTP) ROM serves the functions of hardware and software capability bits, NXP operations and unique-ID, the customer-programmable cryptography key, and storage of various ROM configuration bits. |
| PINCTRL | Pin control and GPIO | System control peripherals | Used for general purpose input/output to external ICs. Each GPIO bank supports 32 bits of I/O. |
| PMU | Power management Unit (DC-DC) | Power management system | The i.MX28 integrates a comprehensive power supply subsystem, including the following features: <ul style="list-style-type: none"> • One integrated DC-DC converter that supports Li-Ion battery. • Four linear regulators directly power the supply rails from 5-V. • Linear battery charger for Li-Ion cells. • Battery voltage and brownout detection monitoring for VDDD, VDDA, VDDIO, VDD4P2 and 5-V supplies. • Integrated current limiter from 5-V power source. • Reset controller. • System monitors for temperature and speed. • Generates USB-Host 5-V from Li-Ion battery (using PWM). • Support for on-the-fly transitioning between 5-V and battery power. • VDD4P2, a nominal 4.2-V supply, is available when the i.MX28 is connected to a 5-V source and allows the DCDC to run from a 5-V source with a depleted battery. • The 4.2-V regulated output also allows for programmable current limits: <ul style="list-style-type: none"> – Battery Charge current + DCDC input current < the 5-V current limit – DCDC input current (which ultimately provides current to the on-chip and off-chip loads) as the priority and battery charge current is automatically reduced if the 5-V current limit is reached |
| PWM(8) | Pulse width modulation | Connectivity peripherals | There are eight PWM output controllers that can be used in place of GPIO pins. Applications include HSADC driving signals and LED & backlight brightness control. Independent output control of each phase allows 0, 1, or high-impedance to be independently selected for the active and inactive phases. Individual outputs can be run in lock step with guaranteed non-overlapping portions for differential drive applications. |
| PXP | Pixel Pipeline | Multimedia | The pixel pipeline (PXP) is used to perform alpha blending of graphic or video buffers with graphics data before sending to an LCD display. The PXP also supports image rotation for hand-held devices that require both portrait and landscape image support. |

Table 4. i.MX28 Digital and Analog Modules (continued)

| Block Mnemonic | Block Name | Subsystem | Brief Description |
|-------------------|----------------------------------|--------------------------|--|
| RTC | Real-time clock, alarm, watchdog | Clocks | The real-time clock (RTC) and alarm share a one-second pulse time domain. The watchdog reset and millisecond counter run on a one-millisecond time domain. The RTC, alarm, and persistent bits reside in a special power domain (crystal domain) that remains powered up even when the rest of the chip is in its powered-down state. |
| SAIF(2) | Serial audio interface | Connectivity peripherals | SAIF provides a half-duplex serial port for communication with a variety of serial devices, including industry-standard codecs and DSPs. It supports a continuous range of sample rates from 8 kHz–192 kHz using a high-resolution fractional divider driven by the PLL. Samples are transferred to/from the FIFO through the APBX DMA interface, a FIFO service interrupt, or software polling. |
| SPDIF | SPDIF | Connectivity peripherals | The Sony-Philips Digital Interface Format (SPDIF) transmitter module transmits data according to the SPDIF digital audio interface standard (IEC-60958). |
| SSP(4) | Synchronous serial port | Connectivity peripherals | The synchronous serial port is a flexible interface for inter-IC and removable media control and communication. The SSP supports master operation of SPI, Texas Instruments SSI; 1-bit, 4-bit, and 8-bit SD/SDIO/MMC and 1-bit and 4-bit MS modes. The SPI mode has enhancements to support 1-bit legacy MMC cards. SPI master dual (2-bit) and quad (4-bit) mode reads are also supported. The SSP also supports slave operation for the SPI and SSI modes. The SSP has a dedicated DMA channel in the bridge and can also be controlled directly by the CPU through PIO registers. Each of the four SSP modules is independent of the other and can have separate SSPCLK frequencies. |
| TIMROT | Timers and Rotary Decoder | Timer peripherals | This module implements four timers and a rotary decoder. The timers and decoder can take their inputs from any of the pins defined for PWM, rotary encoders, or certain divisions from the 32-kHz clock input. Thus, the PWM pins can be inputs or outputs, depending on the application. |
| USBOTG USBHOST | High-speed USB on-the-go | Connectivity peripherals | The USB module provides high-performance USB On-The-Go (OTG) and host functionality (up to 480 Mbps), compliant with the USB 2.0 specification and the OTG supplement. The module has DMA capabilities for handling data transfer between internal buffers and system memory. When the OTG controller works in device mode, it can only work in FS or HS mode. Two USB2.0 PHYs are also integrated (one for the OTG port, another for the host port.) |
| USBPHY | Integrated USB PHY | Connectivity peripherals | The integrated USB 2.0 PHY macrocells are capable of connecting to USB host/device systems at the USB low-speed (LS) rate of 1.5 Mbps, full-speed (FS) rate of 12 Mbps or at the USB 2.0 high-speed (HS) rate of 480 Mbps. The integrated PHYs provide a standard UTM interface. The USB_DP and USB_DN pins connect directly to a USB connector. |

2.1 Special Signal Considerations

Special signal considerations are listed in [Table 5](#). The package contact assignment is found in [Section 4](#), “[Package Information and Contact Assignments](#).” Signal descriptions are provided in the reference manual.

Table 5. Signal Considerations

| Signal | Descriptions |
|------------------------|---|
| PSWITCH | The pin is used for chip power on or recovery. VDDIO can be applied to PSWITCH through a 10 k Ω resistor. This is necessary in order to enter the chip’s firmware recovery. The on-chip circuitry prevents the actual voltage on the pin from exceeding acceptable levels. |
| VDDXTAL | This pin is an output of i.MX28. Should be coupled to ground with a 0.1 uF capacitor. User should not supply external power to this pin. |
| BATTERY | This pin should be connected to the battery with minimal resistance. It provides charging current to the battery. See the “Power Supply” section of the reference manual for details. |
| DCDC_BATTERY | This pin is an input of i.MX28 that provides supply to the DCDC converter. It should be connected to the battery with minimal resistance. See the “Power Supply” section of the reference manual for details. |
| XTALI XTALO | These analog pins are connected to an external 24 MHz crystal circuit. This crystal provides the clock source for on-chip PLLs. |
| RTC_XTALO RTC_XTALI | These analog pins are connected to an external 32.768/32.0 kHz crystal circuit. This crystal provides clock source to the on-chip real-time counter circuits. |
| RESETN | This pin resets the chip if it is low. This pin is pulled up to VDDIO33 with an internal 10 k Ω resistor. No external pull up resistors are needed. |
| DEBUG | This pin is used for JTAG interface. DEBUG=0: JTAG interface works for boundary scan. DEBUG=1: JTAG interface works for Arm debugging. |
| TESTMODE | For NXP factory use only. Must be externally connected to GND for normal operation. |

3 Electrical Characteristics

This section provides the device-level and module-level electrical characteristics for the i.MX28.

3.1 i.MX28 Device-Level Conditions

This section provides the device-level electrical characteristics for the IC.

3.1.1 DC Absolute Maximum Ratings

[Table 6](#) provides the DC absolute maximum operating conditions.

CAUTION

- Stresses beyond those listed under [Table 6](#) may cause permanent damage to the device.

Electrical Characteristics

- Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- [Table 6](#) gives stress ratings only—functional operation of the device is not implied beyond the conditions indicated in [Table 8](#).

Table 6. DC Absolute Maximum Ratings

| Parameter | Symbol | Min | Max | Unit |
|--|---------------------------|------|-----------|------|
| Battery Pin | BATT, V _{DD4P2V} | -0.3 | 4.242 | V |
| 5-Volt Source Pin - transient, t<30ms, duty cycle <0.05% | V _{DD5V} | -0.3 | 7.00 | V |
| 5 Volt Source Pin - static | V _{DD5V} | -0.3 | 6.00 | V |
| Analog Supply Voltage | V _{DDA} | -0.3 | 2.10 | V |
| Digital Core Supply Voltage | V _{DDD} | -0.3 | 1.575 | V |
| Non-EMI Digital I/O Supply | V _{DDIO} | -0.3 | 3.63 | V |
| EMI Digital I/O Supply | V _{DDIO.EMI} | -0.3 | 3.63 | V |
| DC-DC Converter ¹ | DCDC_BATT | -0.3 | BATT | V |
| Input Voltage on Any Digital I/O Pin Relative to Ground | — | -0.3 | VDDIO+0.3 | V |
| Input Voltage on USB_DP and USB_DN Pins Relative to Ground ² | — | -0.3 | 3.63 | V |
| Analog I/O absolute maximum ratings (exceptions: XTALI, XTALO, RTC_XTALI, RTC_XTALO) | — | -0.3 | VDDIO+0.3 | V |
| Storage Temperature | — | -40 | 125 | °C |

¹ Application should include a Schottky diode between BATT and VDD4P2.

² USB_DN and USB_DP can tolerate 5V for up to 24 hours. Note that while 5V is applied to USB_DN or USB_DP, LRADC readings can be corrupted.

[Table 7](#) shows the electrostatic discharge immunity.

Table 7. Electrostatic Discharge Immunity

| 289-Pin BGA Package | Tested Level |
|--|--------------|
| Human Body Model (HBM) ¹ | 2 kV |
| Charge Device Model (CDM) ¹ | 500 V |

¹ HBM and CDM pass ESD testing per AEC-Q100.

3.1.2 DC Operating Conditions

[Table 8](#) provides the DC recommended operating conditions.

Table 8. Recommended Power Supply Operating Conditions

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|------------------|------|-----|------|------|
| Analog Core Supply Voltage | V _{DDA} | 1.62 | — | 2.10 | V |
| Digital Core Supply Voltage <i>Specification dependent on frequency.</i> ^{1, 2} | V _{DDD} | 1.35 | — | 1.55 | V |

Table 8. Recommended Power Supply Operating Conditions (continued)

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|-------------------|------------|--------------|---------|
| Digital Supply Voltages: • VDDIO33/VDDIO33_EMI • VDDIO18 | $V_{DDIO33}/V_{DDIO33_EMI}/V_{DDIO18}$ | 3.0 1.7 | — — | 3.6 1.9 | V |
| EMI Digital I/O Supply Voltage: • DDR2/mDDR • LVDDR2 | $V_{DDIO.EMI}/V_{DDIO_EMIQ}$ | 1.7 1.425 | 1.8 1.5 | 1.9 1.625 | V |
| Battery / DCDC Input Voltage—BATT, DCDC_BATT | BATT DCDC_BATT | 3.10 ³ | — | 4.242 | V |
| VDD5V Supply Voltage | — | 4.75 | 5.00 | 5.25 | V |
| Offstate Current: ⁴ • 32-kHz RTC off, BATT = 4.2 V • 32-kHz RTC on, BATT = 4.2 V | — — | — — | 21 23 | 47 51 | μ A |

¹ For optimum USB jitter performance, $V_{DDP} = 1.35$ V or greater.

² V_{DDP} supply minimum voltage includes 75 mV guardband.

³ Tested with only the i.MX28 processor loading the MX28 PMU output rails during start up. With external loadings (for example, one DDR2 device and SD Card/NAND Flash), MX28 PMU was tested at BATT/DCDC_BATT > 3.30 V.

⁴ When the real-time clock is enabled, the chip consumes additional current in the OFF state to keep the crystal oscillator and the real-time clock running.

Table 9 provides the DC operating temperature conditions.

Table 9. Operating Temperature Conditions

| Parameter ^{1, 2, 3} | Symbol | Min | Typ | Max | Unit |
|--|--------|-----|-----|-----|------|
| Commercial Ambient Operating Temperature Range | T_A | -20 | — | 70 | °C |
| Commercial Junction Temperature Range | T_J | -20 | — | 85 | °C |
| Industrial Ambient Operating Temperature Range | T_A | -40 | — | 85 | °C |
| Industrial Junction Temperature Range | T_J | -40 | — | 105 | °C |

¹ In most portable systems designs, battery and display specifications limits the operating range to well within these specifications. Most battery manufacturers recommend enabling battery charge only when the ambient temperature is between 0°C and 40°C. To ensure that battery charging does not occur outside the recommended temperature range, the system ambient temperature may be monitored by connecting a thermistor to the LRADC0 or LRADC6 pin on the i.MX28.

² For applications powered by external 5V only, the Maximum Ambient Operating Temperature specified in Table 9 may not be achieved. Application developers need to do the worst-case power consumption estimation, and then calculate the Total On-chip Power Dissipation based on the equations specified in note 3 below.

Electrical Characteristics

- ³ Maximum Ambient Operating Temperature may be limited due to on-chip power dissipation. $T_{A(MAX)} \leq T_J - (\Theta_{JA} \times P_D)$ where:
 T_J = Maximum Junction Temperature
 Θ_{JA} = Package Thermal Resistance. See [Section 3.2, "Thermal Characteristics."](#)
 P_D = Total On-chip Power Dissipation = $P_{VDD4P2} + P_{BatteryCharger} + P_{DCDC} + P_{LinearRegulators} + P_{Internal}$. Depending on the application, some of these power dissipation terms may not apply.
 P_{VDD4P2} = VDD4P2 On-Chip Power Dissipation = $(VDD5V - VDD4P2) \times IDD4P2$
 $P_{BatteryCharger}$ = Battery Charger On-Chip Power Dissipation = $(VDD5V - BATT) \times ICHARGE$
 P_{DCDC} = DC-DC Converter On-Chip Power Dissipation = $(BATT \times DCDC \text{ Input Current}) \times (1 - \text{efficiency})$
 $P_{LinearRegulators}$ = Linear Regulator On-Chip Power Dissipation = $(VDD5V - VDDIO) \times (IDDIO + IDDA + IDDD + IDD1P5) + (VDDIO - VDDA) \times (IDDA + IDDD) + (VDDA - VDDD) \times IDDD + (VDDA - VDD1P5) \times IDD1P5$
 $P_{Internal}$ = Internal Digital On-Chip Power Dissipation = $\sim VDDD \times IDDD$

[Table 10](#) provides the recommended analog operating conditions.

Table 10. Recommended Analog Operating Conditions

| Parameter | Min | Typ | Max | Unit |
|--|-----|-----|-----|------|
| Low Resolution ADC Input Impedance (CH0 - CH5) | >1 | — | — | MΩ |

[Table 11](#) shows the PSWITCH input characteristics. See the reference schematics for the recommended PSWITCH button circuitry.

Table 11. PSWITCH Input Characteristics

| Parameter | HW_PWR_STS_PSWITCH | Min | Max | Unit |
|--|--------------------|--------------------------|------|------|
| PSWITCH LOW LEVEL | 0x00 | 0.00 | 0.30 | V |
| PSWITCH MID LEVEL & STARTUP ¹ | 0x01 | 0.65 | 1.50 | V |
| PSWITCH HIGH LEVEL ² | 0x11 | $(1.1 * VDDXTAL) + 0.58$ | 2.45 | V |

¹ A MID LEVEL PSWITCH state can be generated by connecting the VDDXTAL output of the SoC to PSWITCH through a switch.

² PSWITCH acts like a high impedance input (>300 kΩ) when the voltage applied to it is less than 1.5V. However, above 1.5V it becomes lower impedance. To simplify design, it is recommended that a 10 kΩ resistor to VDDIO be applied to PSWITCH to set the HIGH LEVEL state (the PSWITCH input can tolerate voltages greater than 2.45 V as long as there is a 10 kΩ resistor in series to limit the current).

[Table 12](#) shows a test case example for Run IDD.

Table 12. Run IDD Test Case^{1,2}

| Power Rail | Conditions | Min | Typ | Max | Unit |
|------------|------------|-----|------|------|------|
| VDDD | 1.57 V | — | 150 | 188 | mA |
| VDDIO33 | 3.62 V | — | 31 | 34 | mA |
| VDDA | 2.12 V | — | 1.11 | 1.17 | mA |
| VDDIO_EMI | 1.92 V | — | 1.01 | 1.08 | mA |
| VDDIO18 | 1.92 V | — | 0.61 | 2.97 | μA |

¹ CPUCLK = 300 MHz, AHBCLK = 150 MHz.

² Continuous read / write to the cache memory.

Table 13 illustrates the power supply characteristics.

Table 13. Power Supply Characteristics

| Parameter | Min | Typ | Max | Unit |
|---|-----|-----|-----|------|
| Linear Regulators | | | | |
| Output Voltage Accuracy (V_{DDIO} , V_{DDA} , V_{DDM} , V_{DDD}) ¹ | -3 | — | +3 | % |
| V_{DDIO} Maximum Output Current ($V_{DDIO} = 3.30$ V, $V_{DD5V} = 4.75$ V) ^{2, 3} | 270 | — | — | mA |
| V_{DDM} Maximum Output Current ($V_{DDM} = 1.5$ V) ² | 160 | — | — | mA |
| V_{DDA} Maximum Output Current ($V_{DDA} = 1.8$ V) ^{2, 3} | 225 | — | — | mA |
| V_{DDD} Maximum Output Current ($V_{DDD} = 1.2$ V) ^{2, 3} | 200 | — | — | mA |
| DCDC Converters | | | | |
| Output Voltage Accuracy (DCDC_VDDIO, DCDC_VDDA, DCDC_VDDD) ¹ | -3 | — | +3 | % |
| DCDC_VDDD Maximum Output Current ($V_{DDD} = 1.55$ V) ^{4, 5} | 250 | — | — | mA |
| DCDC_VDDA Maximum Output Current ($V_{DDA} = 1.8$ V) ^{4, 5} | 200 | — | — | mA |
| DCDC_VDDIO Maximum Output Current ($V_{DDIO} = 3.15$ V, 3.3 V < BATT < 4.242 V) ^{4, 5, 6} | 250 | — | — | mA |
| VDD4P2 Regulated Output | | | | |
| VDD4P2 Output Voltage Accuracy (TARGET=4.2V) ¹ | -3 | — | +3 | % |
| VDD4P2 Output Current Limit Accuracy ($V_{DD5V} = 4.75$ V, ILIMIT=480 mA) ⁷ | 480 | 500 | 520 | mA |
| VDD4P2 Output Current Limit Accuracy ($V_{DD5V}=4.75$ V, ILIMIT=100 mA) ⁷ | 100 | 120 | 140 | mA |
| Battery Charger | | | | |
| Final Charge Voltage Accuracy (TARGET=4.2 V) | -2 | — | +1 | % |

¹ No load.

² Maximum output current measured when output voltage droops 100 mV from the programmed target voltage with no load present.

³ Because the internal linear regulators are cascaded, it is not possible to simultaneously operate the V_{DDIO} , V_{DDA} , V_{DDM} , and V_{DDD} linear regulators at the maximum specified load current. For example, the V_{DDIO} linear regulator provides current to both the V_{DDIO} 3.3 V supply rail as well as the V_{DDM} and V_{DDA} linear regulator inputs. Likewise, the V_{DDA} linear regulator provides current to both the 1.8 V supply rail as well as the V_{DDD} linear regulator input. The application designer should ensure the following two conditions are met:

$$(V_{DDIO} \text{ Load Current} + V_{DDM} \text{ Load Current} + V_{DDA} \text{ Load Current}) < V_{DDIO} \text{ Maximum Output Current}$$

$$(V_{DDA} \text{ Load Current} + V_{DDD} \text{ Load Current}) < V_{DDA} \text{ Maximum Output Current}$$

⁴ DCDC Double FETs Enabled, Inductor Value = 15 μ H.

⁵ The DCDC Converter is a triple output buck converter. The maximum output current capability of each output of the converter is dependent on the loads on the other two outputs. For a given output, it may be possible to achieve a maximum output current higher than that specified by ensuring the load on the other outputs is well below the maximum.

⁶ Assumes simultaneous load of $I_{DDD} = 250$ mA@ 1.55 V and $I_{DDA} = 200$ mA@1.8 V.

⁷ Untuned.

3.1.2.1 Recommended Operating Conditions for Specific Clock Targets

Table 14 through Table 17 provide the recommended operating conditions for specific clock targets.

Table 14. Recommended Operating States—289-Pin BGA Package

| VDDD (V) | VDDD Brown-out (V) | HW_DIGCTRL ARMCACHE ¹ | CPUCLK / clk_p Frequency (MHz) | HW_CLKCTRL CPU_DIV_CPU | HW_CLKCTRL FRAC_CPUFRC / PFD | AHBCLK / clk_h Frequency (MHz) | HW_CLKCTRL HBUS_DIV | EMICLK / clk_emi Frequency (MHz) | HW_CLKCTRL EMI_DIV_EMI | HW_CLKCTRL FRAC_EMIFRAC | Supported DRAM |
|----------|--------------------|-------------------------------------|-----------------------------------|---------------------------|---------------------------------|-----------------------------------|------------------------|-------------------------------------|---------------------------|----------------------------|----------------|
| 1.300 | 1.200 | 00 | 64 | 5 | 27 | 64 | 1 | 130.91 | 2 | 33 | DDR2 mDDR |
| 1.350 | 1.250 | 00 | 261.81 | 1 | 33 | 130.91 | 2 | 130.91 | 2 | 33 | DDR2 mDDR |
| 1.350 | 1.250 | 00 | 360 | 1 | 24 | 120.00 | 3 | 130.91 | 2 | 33 | DDR2 mDDR |
| 1.450 | 1.350 | 00 | 392.72 | 1 | 22 | 130.91 | 3 | 160.00 | 2 | 27 | DDR2 mDDR |
| 1.550 | 1.450 | 00 | 454.73 | 1 | 19 | 151.57 | 3 | 205.71 | 2 | 21 | DDR2 mDDR |

¹ All timing control bit fields in HW_DIGCTRL_ARMCACHE should be set to the same value.

Table 15. Recommended Operating Conditions—CPU Clock (clk_p)

| VDDD (V) | VDDD _{Brown-out} (V) | HW_DIGCTRL ARMCACHE ¹ | HW_CLKCTRL FRAC_CPUFRC / PFD | CPUCLK / clk_p Frequency max (MHz) |
|----------|-------------------------------|-------------------------------------|---------------------------------|---------------------------------------|
| 1.350 | 1.250 | 00 | 18 - 35 | 360 |
| 1.450 | 1.350 | 00 | 18 - 35 | 392.72 |
| 1.550 | 1.450 | 00 | 18 - 35 | 454.73 |

¹ All timing control bit fields in HW_DIGCTRL_ARMCACHE should be set to the same value.

Table 16. Recommended Operating Conditions—AHB Clock (clk_h)

| VDDD (V) | VDDD _{Brown-out} (V) | HW_DIGCTRL ARMCACHE ¹ | HW_CLKCTRL FRAC_CPUFRC / PFD | AHBCLK / clk_h Frequency max (MHz) |
|----------|-------------------------------|-------------------------------------|---------------------------------|---------------------------------------|
| 1.350 | 1.250 | 00 | 18 - 35 | 160 |
| 1.450 | 1.350 | 00 | 18 - 35 | 196 |
| 1.550 | 1.45 | 00 | 18 - 35 | 206 |

¹ All timing control bit fields in HW_DIGCTRL_ARMCACHE should be set to the same value.

Table 17. Frequency vs. Voltage for EMICLK—289-Pin BGA Package

| VDDD (V) | VDDD _{Brownout} (V) | EMICLK Fmax (MHz) | |
|----------|------------------------------|-------------------|--------|
| | | DDR2 | mDDR |
| 1.550 | 1.450 | 205.71 | 205.71 |
| 1.450 | 1.350 | 196.36 | 196.36 |
| 1.350 | 1.250 | 196.36 | 196.36 |

3.1.3 Fusebox Supply Current Parameters

Table 18 lists the fusebox supply current parameters.

Table 18. Fusebox Supply Current Parameters

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|----------------------|-------|-------|-------|------|
| eFuse Program Current ¹ Current to program one eFuse bit efuse_vddq=2.5V | I _{program} | 21.39 | 25.05 | 33.54 | mA |
| eFuse Read Current ² Current to read an 8-bit eFuse word vdd_fusebox = 3.3 V | I _{read} | — | — | 4.07 | mA |

¹ The current I_{program} is during program time.

² The current I_{read} is present for approximately 10 ns of the read access to the 8-bit word.

3.1.4 Interface Frequency Limits

Table 19 provides information for interface frequency limits.

Table 19. Interface Frequency Limits

| Parameter | Min | Typ | Max | Unit |
|----------------------------------|-----|-------------|-----|------|
| JTAG: TCK Frequency of Operation | — | — | 10 | MHz |
| OSC24M_XTAL Oscillator | — | 24.000 | — | MHz |
| OSC32K_XTAL Oscillator | — | 32.768/32.0 | — | kHz |

3.1.5 Power Modes

Table 20 describes the core, clock, and module settings for the different power modes of the processor.

Table 20. Power Mode Settings

| Core/Clock/Module | Offstate | Standby | Run |
|-----------------------|----------|---------|-----|
| Arm Core | Off | Off | On |
| USB0 PLL (System PLL) | Off | Off | On |
| OSC24M | Off | On | On |

Table 20. Power Mode Settings (continued)

| Core/Clock/Module | Offstate | Standby | Run |
|-------------------|----------|---------|--------|
| OSC32K | On | On | On |
| DCDC | Off | On | On |
| RTC | On | On | On |
| Other Modules | Off | On/Off | On/Off |

3.1.6 Supply Power-Up/Power-Down Requirements

There is no special power-up sequence. After applying 5 V or battery in any order, the rest of the power supplies are internally generated and automatically come up in a safe way.

There is no special power-down sequence. 5 V or the battery can be removed at any time.

3.1.7 Reset Timing

Because the i.MX28 is a PMU and an SoC, power-on reset is generated internally and there is no timing requirement on external pins.

The i.MX28 can be reset by asserting the external pin RESETN for at least 100 mS and later deasserting RESETN.

If the reset occurs while the device is only powered by the battery, then the reset kills all of the power supplies and the system reboots on the assertion of PSWITCH. If auto-restart is set up ahead of time, the system reboots immediately.

If the chip is powered by 5 V, then the reset serves to reset the digital sections of the chip. If the DCDC is operating at the time of the reset, then power switches back to the default linear regulators powered by 5 V.

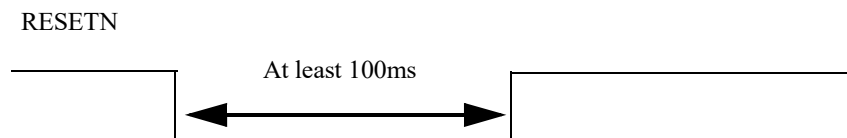


Figure 2. RESETN Timing

3.2 Thermal Characteristics

The thermal resistance characteristics for the device are given in [Table 21](#). These values are measured under the following conditions:

- Two layer Substrate
- Substrate solder mask thickness: 0.025 mm
- Substrate metal thicknesses: 0.016 mm
- Substrate core thickness: 0.160 mm
- Core via I.D: 0.068 mm, Core via plating 0.016 mm
- Flag: trace style with ground balls under the die connected to the flag

- Die Attach: 0.033 mm non-conductive die attach, $k = 0.3 \text{ W/m K}$
- Mold Compound: generic mold compound, $k = 0.9 \text{ W/m K}$

Table 21. Thermal Resistance Data

| Rating | Condition | Symbol | Value | Unit |
|---|-------------------------|--------------------|-------|------|
| Junction to ambient ¹ natural convection | Single layer board (1s) | $R_{\theta JA}$ | 62 | °C/W |
| Junction to ambient ¹ natural convection | Four layer board (2s2p) | $R_{\theta JA}$ | 36 | °C/W |
| Junction to ambient ¹ (@200 ft/min) | Single layer board (1s) | $R_{\theta JMA}$ | 53 | °C/W |
| Junction to ambient ¹ (@200 ft/min) | Four layer board (2s2p) | $R_{\theta JMA}$ | 33 | °C/W |
| Junction to boards ² | — | $R_{\theta JB}$ | 24 | °C/W |
| Junction to case (top) ³ | — | $R_{\theta JCTop}$ | 15 | °C/W |
| Junction to package top ⁴ | Natural Convection | Ψ_{JT} | 3 | °C/W |

¹ Junction-to-Ambient Thermal Resistance determined per JEDEC JESD51-2 and JESD51-6. Thermal test board meets JEDEC specification for this package.

² Junction-to-Board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package.

³ Junction-to-Case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.

⁴ Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

3.3 I/O DC Parameters

This section includes the DC parameters of the following I/O types:

- DDR I/O: Mobile DDR (LPDDR1), standard 1.8 V DDR2, and low-voltage 1.5 V DDR2 (LVDDR2)
- General purpose I/O (GPIO)

3.3.1 DDR I/O DC Parameters

Table 22 shows the EMI digital pin DC characteristics.

NOTE

The current values and the I-V curves of the I/O DC characteristics are estimated based on an overly conservative device model. They are updated upon the measurement results of the first silicon.

Table 22. EMI Digital Pin DC Characteristics

| Parameter | Symbol | Min | Max | Unit |
|--------------------------|----------|-----------------------|-----------------------|------|
| Input voltage high (dc) | V_{IH} | $V_{REF} + 0.125$ | $V_{DDIO_EMI} + 0.3$ | V |
| Input voltage low (dc) | V_{IL} | 0.3 | $V_{REF} - 0.125$ | V |
| Output voltage high (dc) | V_{OH} | $0.8 * V_{DDIO_EMI}$ | — | V |

Table 22. EMI Digital Pin DC Characteristics (continued)

| Parameter | Symbol | Min | Max | Unit |
|---|-----------------------|------|-----------------|------|
| Output voltage low (dc) | VOL | — | 0.2 * VDDIO_EMI | V |
| Output source current (dc) LVDDR2 Mode | IOH ¹ —Low | -6.2 | — | mA |
| | IOH—Medium | -7.2 | — | mA |
| | IOH—High | -9.7 | — | mA |
| Output sink current (dc) LVDDR2 Mode | IOL ² —Low | 5.7 | — | mA |
| | IOL—Medium | 7.3 | — | mA |
| | IOL—High | 10.0 | — | mA |
| Output source current (dc) mDDR, DDR2 Mode | IOH—Low | -5.7 | — | mA |
| | IOH—High | -7.5 | — | mA |
| Output sink current (dc) mDDR, DDR2 Mode | IOL—Low | 5.4 | — | mA |
| | IOL—High | 8.8 | — | mA |

¹ IOH is the output current at which the VOH specification is met.

² IOL is the output current at which the VOL specification is met.

Table 23 shows the ON impedance of EMI drivers for different drive strengths.

Table 23. ON Impedance of EMI Drivers for Different Drive Strengths¹

| Mode | Drive | Min (Ω) | Typ (Ω) | Max (Ω) |
|------------------|--------|---------|---------|---------|
| 1.5 LVDDR2 | Low | 26 | 38 | 58 |
| | Medium | 17 | 25 | 36 |
| | High | 15 | 20 | 27 |
| 1.8 DDR2/mDDR | Low | 36 | 53 | 78 |
| | Medium | 17 | 27 | 42 |
| | High | 16 | 19 | 28 |

¹ ON impedance of the EMI drivers are guaranteed by design and are not tested during production.

Table 24 shows the external devices supported by the EMI.

Table 24. External Devices Supported by the EMI

| DRAM Device | Max Load ^{1, 2} | Pad Voltage |
|-------------|--------------------------|-------------|
| DDR2 | 15 pF | 1.8 V |
| mDDR | 15 pF | 1.8 V |
| LVDDR2 | 15 pF | 1.5 V |

¹ Max load includes capacitive load due to PCB traces, pad capacitance and driver self-loading.

- ² Setting is for worst case. NXP's EMI interface uses less powerful drivers than those typically used in mDDR devices. A possible transmission-line effect on the PC board must be suppressed by minimizing the trace length combined with NXP's slower edge-rate drivers. The i.MX28 provides up to 16 mA programmable drive strength. However, the 16-mA mode is an experimental mode. With the 16-mA mode, the EMI function may be impaired by Simultaneous Switching Output (SSO) noise. In general, the stronger the driver mode, the noisier the on-chip power supply. NXP recommends not using a stronger driver mode than is required. Because on-chip power and ground noise is proportional to the inductance of its return path, users should make their best effort to reduce inductance between the EMI power and ground balls and the PC board power and ground planes.

3.3.2 GPIO I/O DC Parameters

Max load includes capacitive load due to PCB traces, pad capacitance and driver self-loading. For the internal pull up setting of each pad, see the "Pin Control and GPIO" section of the reference manual.

Table 25 shows the digital pin DC characteristics for GPIO in 3.3-V mode. Measurements are valid for eight pins loaded using the 4mA driver, four pins loaded using the 8mA driver, and two pins loaded using either the 12mA or 16mA driver.

Table 25. Digital Pin DC Characteristics for GPIO in 3.3-V Mode

| Parameter | Symbol | Min | Max | Unit |
|--|--------------------|-------------|-------|------|
| Input voltage high (DC) | V _{IH} | 2 | VDDIO | V |
| Input voltage low (DC) | V _{IL} | — | 0.8 | V |
| Output voltage high (DC) | V _{OH} | 0.8 × VDDIO | — | V |
| Output voltage low (DC) | V _{OL} | — | 0.4 | V |
| Output source current ¹ (DC) <i>gpio</i> | IOH – Low | -5.0 | — | mA |
| | IOH – Medium | -9.5 | — | mA |
| | IOH – High | -11.4 | — | mA |
| Output sink current (DC) <i>gpio</i> | IOL – Low | 3.8 | — | mA |
| | IOL – Medium | 7.7 | — | mA |
| | IOL – High | 9.0 | — | mA |
| Output source current (DC) <i>gpio_clk</i> | IOH – Low | -9.2 | — | mA |
| | IOH – High | -15.2 | — | mA |
| Output sink current (DC) <i>gpio_clk</i> | IOL – Low | 7.6 | — | mA |
| | IOL – High | 12.0 | — | mA |
| 10-K pull-up resistance ² | R _{pu10k} | 8 | 12 | kΩ |
| 47-K pull-up resistance | R _{pu47k} | 39 | 56 | kΩ |

¹ The conditions of the current measurements for all different drives are as follows:

IOL: at 0.4 V

IOH: at VDDIO * 0.8 V

Maximum corner for 3.3 V mode: 3.6 V, -40°C, fast process.

Minimum corner for 3.3 V mode: 3.0 V, 105°C, slow process.

8 *gpio* pins (LCD_D0-D7) and 2 *gpio_clk* pins (LCD_DOTCLK and LCD_WR_RWN) simultaneously loaded.

Electrical Characteristics

² See the i.MX28 reference manual for detailed pull-up configuration of each I/O.

Table 26 shows the digital pin DC characteristics for GPIO in 1.8 V mode.

Table 26. Digital Pin DC Characteristics for GPIO in 1.8 V Mode

| Parameter | Symbol | Min | Max | Unit |
|--|--------------------|---------------------------|---------------------------|------|
| Input voltage high (DC) | V _{IH} | 0.7 × V _{DDIO18} | V _{DDIO18} | V |
| Input voltage low (DC) | V _{IL} | — | 0.3 × V _{DDIO18} | V |
| Output voltage high (DC) | V _{OH} | 0.8 * V _{DDIO18} | — | V |
| Output voltage low (DC) | V _{OL} | — | 0.2 × V _{DDIO18} | V |
| Output source current ¹ (DC) <i>gpio</i> | IOH – low | -2.2 | — | mA |
| | IOH – medium | -3.5 | — | mA |
| | IOH – high | -4.0 | — | mA |
| Output sink current (DC) <i>gpio</i> | IOL – low | 3.3 | — | mA |
| | IOL – medium | 7.0 | — | mA |
| | IOL – high | 7.5 | — | mA |
| Output source current (DC) <i>gpio_clk</i> | IOH – low | -4.2 | — | mA |
| | IOH – high | -6.0 | — | mA |
| Output sink current (DC) <i>gpio_clk</i> | IOL – low | 6.8 | — | mA |
| | IOL – high | 11.5 | — | mA |
| 10-K pull-up resistance ² | R _{pu10k} | 8 | 12 | kΩ |
| 47-K pull-up resistance | R _{pu47k} | 39 | 56 | kΩ |

¹ The condition of the current measurements for all different drives are as follows:

Maximum corner for 1.8 V mode: 1.9 V, -40°C, Fast process.

Minimum corner for 1.8 V mode: 1.7 V, 105°C, Slow process.

1 *gpio* pin (GPMI_D0) and 1 *gpio_clk* pin (GPMI_WRN) simultaneously loaded.

² See the i.MX28 reference manual for detailed pull-up configuration of each I/O.

3.4 I/O AC Timing and Parameters

Figure 3 and Figure 4 show the Driver Used for AC Simulation Testpoint and the Output Pad Transition Waveform.

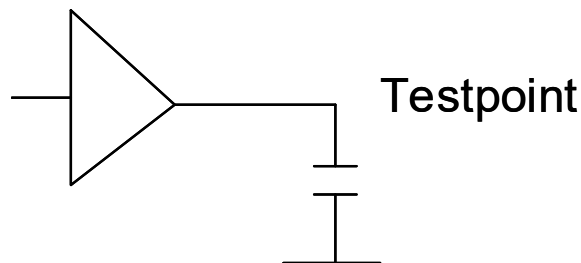


Figure 3. Driver Used for AC Simulation Testpoint



Figure 4. Output Pad Transition Waveform

Table 27 shows the base GPIO AC timing and parameters.

Table 27. Base GPIO

| Parameters | Symbol | Test Voltage | Test Capacitance | Min Rise/Fall | | MaxRise/Fall | | Unit | Notes |
|---|--------|--------------|------------------|---------------|------|--------------|-------|------|-------|
| | | | | | | | | | |
| Duty cycle | Fduty | — | — | — | — | — | — | % | — |
| Output pad transition times (maximum drive) | tpr | 1.7~1.9V | 10 pF | 0.82 | 0.91 | 1.93 | 1.97 | ns | — |
| | | 1.7~1.9V | 20 pF | 1.18 | 1.22 | 2.69 | 2.71 | | |
| | | 1.7~1.9V | 50 pF | 2.11 | 2.03 | 4.62 | 4.44 | | |
| | | 3.0~3.6V | 10 pF | 1.04 | 1.08 | 2.46 | 2.18 | | |
| | | 3.0~3.6V | 20 pF | 1.42 | 1.5 | 3.29 | 3 | | |
| | | 3.0~3.6V | 50 pF | 2.46 | 2.61 | 5.34 | 5.12 | | |
| Output pad transition times (medium drive) | tpr | 1.7~1.9V | 10 pF | 1.02 | 1.08 | 2.34 | 2.38 | ns | — |
| | | 1.7~1.9V | 20 pF | 1.51 | 1.5 | 3.34 | 3.28 | | |
| | | 1.7~1.9V | 50 pF | 2.91 | 2.62 | 6.24 | 5.67 | | |
| | | 3.0~3.6V | 10 pF | 1.26 | 1.29 | 2.9 | 2.6 | | |
| | | 3.0~3.6V | 20 pF | 1.8 | 1.88 | 4 | 3.67 | | |
| | | 3.0~3.6V | 50 pF | 3.3 | 3.46 | 6.91 | 6.64 | | |
| Output pad transition times (low drive) | tpr | 1.7~1.9V | 10 pF | 1.62 | 1.68 | 3.65 | 3.68 | ns | — |
| | | 1.7~1.9V | 20 pF | 2.55 | 2.45 | 5.59 | 5.37 | | |
| | | 1.7~1.9V | 50 pF | 5.42 | 4.62 | 11.46 | 10.01 | | |
| | | 3.0~3.6V | 10 pF | 1.95 | 2.12 | 4.43 | 4.25 | | |
| | | 3.0~3.6V | 20 pF | 2.96 | 3.21 | 6.36 | 6.25 | | |
| | | 3.0~3.6V | 50 pF | 5.89 | 6.39 | 12.02 | 12.18 | | |

Table 27. Base GPIO (continued)

| Parameters | Symbol | Test Voltage | Test Capacitance | Min Rise/Fall | | Max Rise/Fall | | Unit | Notes |
|--------------------------------------|--------|--------------|------------------|---------------|------|---------------|------|------|-------|
| | | | | | | | | | |
| Output pad slew rate (maximum drive) | tps | 1.7~1.9V | 10 pF | 1.39 | 1.25 | 0.53 | 0.52 | V/ns | — |
| | | 1.7~1.9V | 20 pF | 0.97 | 0.93 | 0.38 | 0.38 | | — |
| | | 1.7~1.9V | 50 pF | 0.54 | 0.56 | 0.22 | 0.23 | | — |
| | | 3.0~3.6V | 10 pF | 2.08 | 2.00 | 0.73 | 0.83 | | — |
| | | 3.0~3.6V | 20 pF | 1.52 | 1.44 | 0.55 | 0.60 | | — |
| | | 3.0~3.6V | 50 pF | 0.88 | 0.83 | 0.34 | 0.35 | | — |
| Output pad slew rate (medium drive) | tps | 1.7~1.9V | 10 pF | 1.12 | 1.06 | 0.44 | 0.43 | V/ns | — |
| | | 1.7~1.9V | 20 pF | 0.75 | 0.76 | 0.31 | 0.31 | | — |
| | | 1.7~1.9V | 50 pF | 0.39 | 0.44 | 0.16 | 0.18 | | — |
| | | 3.0~3.6V | 10 pF | 1.71 | 1.67 | 0.62 | 0.69 | | — |
| | | 3.0~3.6V | 20 pF | 1.20 | 1.15 | 0.45 | 0.49 | | — |
| | | 3.0~3.6V | 50 pF | 0.65 | 0.62 | 0.26 | 0.27 | | — |
| Output pad slew rate (low drive) | tps | 1.7~1.9V | 10 pF | 1.17 | 1.13 | 0.47 | 0.46 | V/ns | — |
| | | 1.7~1.9V | 20 pF | 0.75 | 0.78 | 0.30 | 0.32 | | — |
| | | 1.7~1.9V | 50 pF | 0.35 | 0.41 | 0.15 | 0.17 | | — |
| | | 3.0~3.6V | 10 pF | 1.11 | 1.02 | 0.41 | 0.42 | | — |
| | | 3.0~3.6V | 20 pF | 0.73 | 0.67 | 0.28 | 0.29 | | — |
| | | 3.0~3.6V | 50 pF | 0.37 | 0.34 | 0.15 | 0.15 | | — |
| Input pad average hysteresis | tih | 1.7 V–1.9 V | — | 100 | | 75 | | mV | — |
| | | 3.0 V–3.6 V | — | 100 | | 50 | | | — |

Table 28 shows the F-type GPIO AC timing and parameters.

Table 28. F-type GPIO

| Parameters | Symbol | Test Voltage | Test Capacitance | Min Rise/Fall | | Max Rise/Fall | | Unit | Notes |
|---|--------|--------------|------------------|---------------|------|---------------|------|------|-------|
| | | | | | | | | | |
| Duty cycle | Fduty | — | — | — | | — | | % | — |
| Output pad transition times (maximum drive) | tpr | 1.7~1.9V | 10 pF | 0.58 | 0.61 | 1.29 | 1.33 | ns | — |
| | | 1.7~1.9V | 20 pF | 0.89 | 0.88 | 1.94 | 1.88 | | — |
| | | 1.7~1.9V | 50 pF | 1.83 | 1.59 | 3.88 | 3.39 | | — |
| | | 3.0~3.6V | 10 pF | 0.71 | 0.68 | 1.47 | 1.34 | | — |
| | | 3.0~3.6V | 20 pF | 1.02 | 1.04 | 2.11 | 1.99 | | — |
| | | 3.0~3.6V | 50 pF | 1.98 | 2.09 | 3.97 | 3.96 | | — |

Table 28. F-type GPIO (continued)

| Parameters | Symbol | Test Voltage | Test Capacitance | Min Rise/Fall | | Max Rise/Fall | | Unit | Notes |
|--|--------|--------------|------------------|---------------|------|---------------|-------|------|-------|
| | | | | | | | | | |
| Output pad transition times (medium drive) | tpr | 1.7~1.9V | 10 pF | 0.76 | 0.76 | 1.68 | 1.61 | ns | — |
| | | 1.7~1.9V | 20 pF | 1.23 | 1.13 | 2.63 | 2.38 | | — |
| | | 1.7~1.9V | 50 pF | 2.66 | 2.18 | 5.61 | 4.6 | | — |
| | | 3.0~3.6V | 10 pF | 0.9 | 0.88 | 1.84 | 1.7 | | — |
| | | 3.0~3.6V | 20 pF | 1.36 | 1.4 | 2.76 | 2.67 | | — |
| | | 3.0~3.6V | 50 pF | 2.85 | 3.02 | 5.59 | 5.67 | | — |
| Output pad transition times (low drive) | tpr | 1.7~1.9V | 10 pF | 1.32 | 1.26 | 2.88 | 2.72 | ns | — |
| | | 1.7~1.9V | 20 pF | 2.27 | 1.98 | 4.84 | 4.23 | | — |
| | | 1.7~1.9V | 50 pF | 5.23 | 4.13 | 10.95 | 8.8 | | — |
| | | 3.0~3.6V | 10 pF | 1.46 | 1.55 | 3.05 | 3 | | — |
| | | 3.0~3.6V | 20 pF | 2.46 | 2.62 | 4.92 | 5.02 | | — |
| | | 3.0~3.6V | 50 pF | 5.56 | 5.96 | 10.78 | 11.22 | | — |
| Output pad slew rate (maximum drive) | tps | 1.7~1.9V | 10 pF | 1.97 | 1.87 | 0.79 | 0.77 | ns | — |
| | | 1.7~1.9V | 20 pF | 1.28 | 1.30 | 0.53 | 0.54 | | — |
| | | 1.7~1.9V | 50 pF | 0.62 | 0.72 | 0.26 | 0.30 | | — |
| | | 3.0~3.6V | 10 pF | 3.04 | 3.18 | 1.22 | 1.34 | | — |
| | | 3.0~3.6V | 20 pF | 2.12 | 2.08 | 0.85 | 0.90 | | — |
| | | 3.0~3.6V | 50 pF | 1.09 | 1.03 | 0.45 | 0.45 | | — |
| Output pad slew rate (medium drive) | tps | 1.7~1.9V | 10 pF | 1.50 | 1.50 | 0.61 | 0.63 | ns | — |
| | | 1.7~1.9V | 20 pF | 0.93 | 1.01 | 0.39 | 0.43 | | — |
| | | 1.7~1.9V | 50 pF | 0.43 | 0.52 | 0.18 | 0.22 | | — |
| | | 3.0~3.6V | 10 pF | 2.40 | 2.45 | 0.98 | 1.06 | | — |
| | | 3.0~3.6V | 20 pF | 1.59 | 1.54 | 0.65 | 0.67 | | — |
| | | 3.0~3.6V | 50 pF | 0.76 | 0.72 | 0.32 | 0.32 | | — |
| Output pad slew rate (low drive) | tps | 1.7~1.9V | 10 pF | 1.44 | 1.51 | 0.59 | 0.63 | ns | — |
| | | 1.7~1.9V | 20 pF | 0.84 | 0.96 | 0.35 | 0.40 | | — |
| | | 1.7~1.9V | 50 pF | 0.36 | 0.46 | 0.16 | 0.19 | | — |
| | | 3.0~3.6V | 10 pF | 1.48 | 1.39 | 0.59 | 0.60 | | — |
| | | 3.0~3.6V | 20 pF | 0.88 | 0.82 | 0.37 | 0.36 | | — |
| | | 3.0~3.6V | 50 pF | 0.39 | 0.36 | 0.17 | 0.16 | | — |
| Input pad average hysteresis | tih | 1.7 V~1.9 V | — | 100 | | 75 | | mV | — |
| | | 3.0 V~3.6 V | — | 100 | | 50 | | | — |

Electrical Characteristics

Table 29 shows the CLK-type GPIO AC timing and parameters.

Table 29. CLK-Type GPIO

| Parameters | Symbol | Test Voltage | Test Capacitance | Min Rise/Fall | | Max Rise/Fall | | units | Notes |
|---|--------|--------------|------------------|---------------|------|---------------|------|-------|-------|
| Duty cycle | Fduty | — | — | — | | — | | % | — |
| Output pad transition times (maximum drive) | tpr | 1.7~1.9V | 10 pF | 0.48 | 0.52 | 1.08 | 1.12 | ns | — |
| | | 1.7~1.9V | 20 pF | 0.72 | 0.74 | 1.56 | 1.56 | | — |
| | | 1.7~1.9V | 50 pF | 1.41 | 1.28 | 3.04 | 2.7 | | — |
| | | 3.0~3.6V | 10 pF | 0.61 | 0.57 | 1.25 | 1.12 | | — |
| | | 3.0~3.6V | 20 pF | 0.85 | 0.85 | 1.73 | 1.63 | | — |
| | | 3.0~3.6V | 50 pF | 1.56 | 1.63 | 3.13 | 3.08 | | — |
| Output pad transition times (medium drive) | tpr | 1.7~1.9V | 10 pF | 0.76 | 0.76 | 1.67 | 1.62 | ns | — |
| | | 1.7~1.9V | 20 pF | 1.22 | 1.14 | 2.64 | 2.41 | | — |
| | | 1.7~1.9V | 50 pF | 2.66 | 2.2 | 5.61 | 4.62 | | — |
| | | 3.0~3.6V | 10 pF | 0.9 | 0.89 | 1.83 | 1.72 | | — |
| | | 3.0~3.6V | 20 pF | 1.37 | 1.41 | 2.77 | 2.69 | | — |
| | | 3.0~3.6V | 50 pF | 2.85 | 3.03 | 5.59 | 5.72 | | — |
| Output pad slew rate (maximum drive) | tps | 1.7~1.9V | 10 pF | 2.38 | 2.19 | 0.94 | 0.91 | ns | — |
| | | 1.7~1.9V | 20 pF | 1.58 | 1.54 | 0.65 | 0.65 | | — |
| | | 1.7~1.9V | 50 pF | 0.81 | 0.89 | 0.34 | 0.38 | | — |
| | | 3.0~3.6V | 10 pF | 3.54 | 3.79 | 1.44 | 1.61 | | — |
| | | 3.0~3.6V | 20 pF | 2.54 | 2.54 | 1.04 | 1.10 | | — |
| | | 3.0~3.6V | 50 pF | 1.38 | 1.33 | 0.58 | 0.58 | | — |
| Output pad slew rate (medium drive) | tps | 1.7~1.9V | 10 pF | 1.50 | 1.50 | 0.61 | 0.63 | ns | — |
| | | 1.7~1.9V | 20 pF | 0.93 | 1.00 | 0.39 | 0.42 | | — |
| | | 1.7~1.9V | 50 pF | 0.43 | 0.52 | 0.18 | 0.22 | | — |
| | | 3.0~3.6V | 10 pF | 2.40 | 2.43 | 0.98 | 1.05 | | — |
| | | 3.0~3.6V | 20 pF | 1.58 | 1.53 | 0.65 | 0.67 | | — |
| | | 3.0~3.6V | 50 pF | 0.76 | 0.71 | 0.32 | 0.31 | | — |
| Input pad average hysteresis | tih | 1.7 V–1.9 V | — | 100 | | 75 | | mV | — |
| | | 3.0 V–3.6 V | — | 100 | | 50 | | | — |

3.5 Module Timing and Electrical Parameters

3.5.1 ADC Electrical Specifications

This section describes the electrical specifications, including DC and AC information, of Low-Resolution ADC (LRADC) and High-Speed ADC (HSADC).

3.5.1.1 LRADC Electrical Specifications

Table 30 shows the electrical specifications for the LRADC.

Table 30. LRADC Electrical Specifications

| Parameter | Conditions | Min | Typ | Max | Unit |
|--|---------------------------------|-----|-----|-------|---------------|
| AC Electrical Specification | | | | | |
| Input capacitance (C_p) | No pin/pad capacitance included | — | 0.5 | — | pF |
| Resolution | — | 12 | | | bits |
| Maximum sampling rate ¹ (fs) | — | — | — | 428 | kHz |
| Power-up time ² | — | 1 | | | sample cycles |
| DC Electrical Specification | | | | | |
| DC input voltage | — | 0 | | 1.85 | V |
| Current consumption ³ VDDA | — | — | 10 | — | μA |
| Touchscreen Interface | | | | | |
| Expected plate resistance | — | 200 | — | 50000 | Ω |

¹ There is no sample and hold circuit in LRADC, so it is only for DC input voltage or ones with very small slope.

² This comprises only the required initial dummy conversion cycle, NOT including the Analog part power-up time.

³ This value only includes the ADC and the driver switches, but it does not take into account the current consumption in the touchscreen plate. For example, if the plate resistance is 200 ohm, the total current consumption is about 11 mA.

3.5.1.2 HSADC Electrical Specification

Table 31 shows the electrical specifications for the HSADC

Table 31. HSADC Electrical Specification

| Parameter | Conditions | Min | Typ | Max | Unit |
|--------------------------------------|---------------------------------|-----|-----|-----|------|
| AC Electrical Specification | | | | | |
| Input sampling capacitance (C_s) | No pin/pad capacitance included | — | 0.5 | — | pF |
| Resolution | — | 12 | | | bits |

Table 31. HSADC Electrical Specification (continued)

| Parameter | Conditions | Min | Typ | Max | Unit |
|------------------------------------|--------------------------|-----|-----|----------|---------------|
| Maximum sampling rate (fs) | — | — | — | 2 | MHz |
| Power-up time | — | 1 | | | sample cycles |
| DC Electrical Specification | | | | | |
| DC input voltage | — | 0.5 | — | VDDA-0.5 | V |
| Current Consumption VDDA | — | — | 10 | — | μA |
| DNL | $f_{in} = 1 \text{ kHz}$ | — | 0.5 | 1.2 | LSB |
| INL | $f_{in} = 1 \text{ kHz}$ | — | 0.5 | 1.2 | LSB |

3.5.2 DPLL Electrical Specifications

This section includes descriptions of the USB PLL electrical specifications and Ethernet PLL electrical specifications.

3.5.2.1 USB PLL Electrical Specifications

The i.MX28 integrates a high-frequency USB PLL that provides the 480-MHz clock for the USB and other system blocks.

Table 32 lists the USB PLL output electrical specifications.

Table 32. USB PLL Specifications

| Parameter | Test Conditions | Min | Typ | Max | Unit |
|---------------|-----------------|-----|-----|-----|------|
| PLL lock time | — | — | — | 10 | μs |

3.5.2.2 Ethernet PLL Electrical Specifications

i.MX28 provides a 50-MHz/25-MHz output clock, called the Ethernet PLL output.

Table 33 lists the Ethernet PLL output electrical specifications.

Table 33. Ethernet PLL Specifications

| Parameter | Test Conditions | Min | Typ | Max | Unit |
|---|-----------------|-----|-----|-----|------|
| Output Duty Cycle | — | 45 | 50 | 55 | % |
| PLL lock time | — | — | — | 10 | μs |
| Cycle to cycle jitter | — | — | 25 | — | ps |
| Clock output frequency tolerance ¹ | — | — | — | ±20 | ppm |

¹ This Ethernet output clock tolerance specification is the contribution from the PLL only and assumes a perfect 24 MHz clock/crystal source with 0 ppm deviation. The 24 MHz crystal frequency tolerance/deviation should be added to this number for the total Ethernet clock output frequency tolerance.

3.5.3 EMI AC Timing

This section includes descriptions of the electrical specifications of EMI module which interfaces external DDR2 and Mobile-DDR1 (LP-DDR1) memory devices.

3.5.3.1 EMI Command and Address AC Timing

Figure 5 and Table 34 specify the timing related to the address and command pins that interfaces DDR2 and Mobile-DDR1 memory devices.

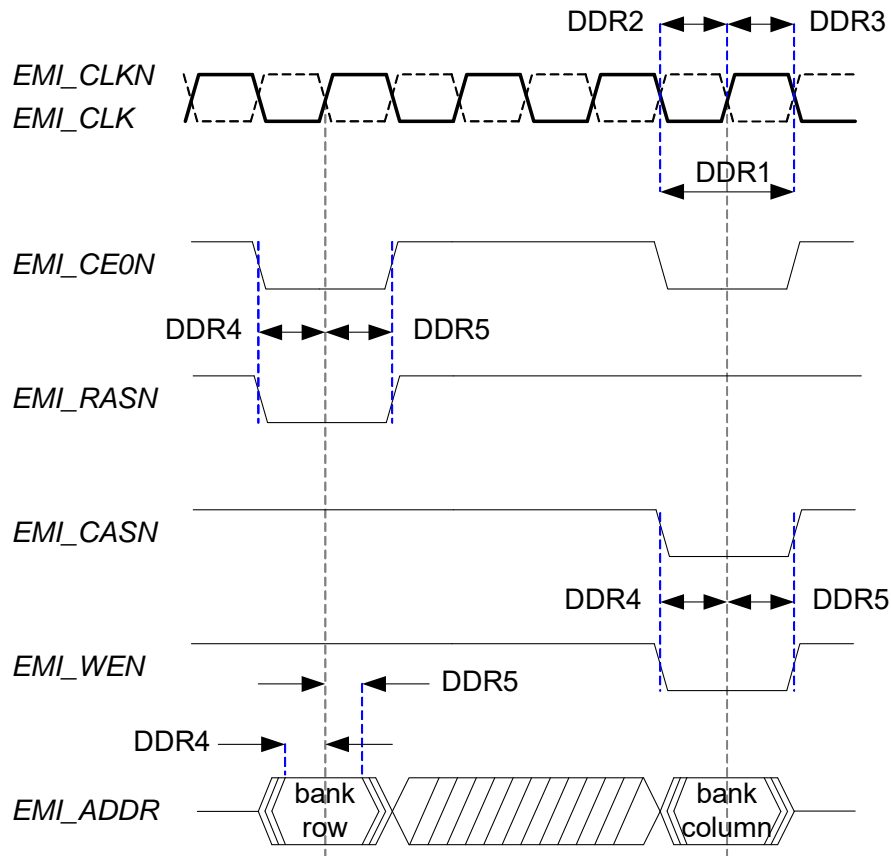


Figure 5. EMI Command/Address AC Timing

Table 34. EMI Command/Address AC Timing

| ID | Description | Symbol | Min | Max | Unit |
|------|---------------------|--------|-----------------|------------------|------|
| DDR1 | CK cycle time | tCK | 4.86 | — | ns |
| DDR2 | CK high level width | tCH | 0.5 tCK -0.5 | 0.5 tCK + 0.5 | ns |
| DDR3 | CK low level width | tCL | 0.5 tCK -0.5 | 0.5 tCK + 0.5 | ns |

Table 34. EMI Command/Address AC Timing (continued)

| ID | Description | Symbol | Min | Max | Unit |
|------|---------------------------------------|--------|---------------|-----------------|------|
| DDR4 | Address and control output setup time | tIS | $0.5 tCK - 1$ | $0.5 tCK + 0.5$ | ns |
| DDR5 | Address and control output hold time | tIH | $0.5 tCK - 1$ | $0.5 tCK + 0.5$ | ns |

3.5.3.2 DDR Output AC Timing

Figure 6 and Table 35 show the DDR output AC timing defined for all DDR types: LPDDR1, standard DDR2 (1.8 V), and LVDDR2 (1.5 V).

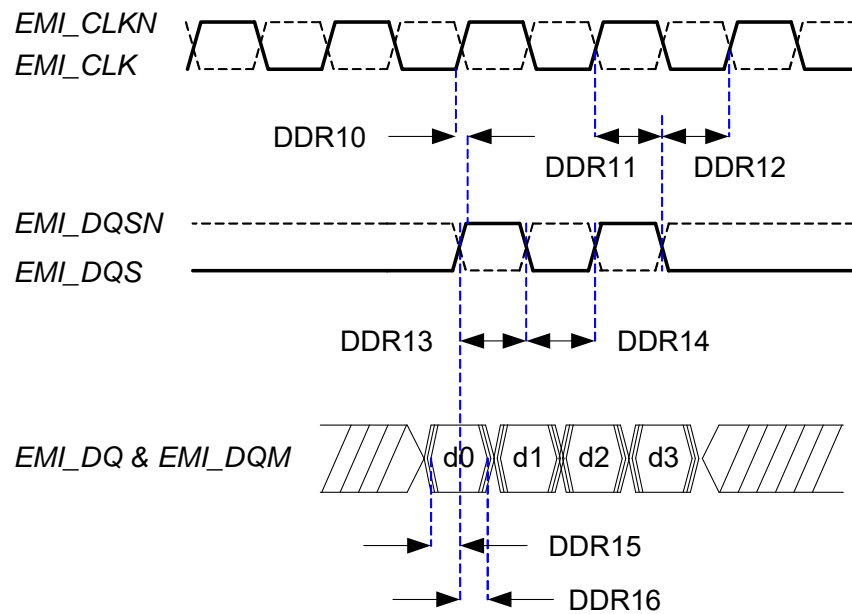


Figure 6. DDR Output AC Timing

Table 35. DDR Output AC Timing

| ID | Description | Symbol | Min | Max | Unit |
|-------|--|--------|-----------------|-----------------|------|
| DDR10 | Positive DQS latching edge to associated CK edge | tDQSS | -0.5 | +0.5 | ns |
| DDR11 | DQS falling edge from CK rising edge—hold time | tDSH | $0.5 tCK - 0.5$ | $0.5 tCK + 0.5$ | ns |
| DDR12 | DQS falling edge to CK rising edge—setup time | tDSS | $0.5 tCK - 0.5$ | $0.5 tCK + 0.5$ | ns |
| DDR13 | DQS output high pulse width | tDQSH | $0.5 tCK - 0.5$ | $0.5 tCK + 0.5$ | ns |
| DDR14 | DQS output low pulse width | tDQSL | $0.5 tCK - 0.5$ | $0.5 tCK + 0.5$ | ns |

Table 35. DDR Output AC Timing (continued)

| ID | Description | Symbol | Min | Max | Unit |
|-------|--|--------|-----------------|-----------------|------|
| DDR15 | DQ & DQM output setup time relative to DQS | tDS | 1/4 tCK -0.8 | 1/4 tCK -0.5 | ns |
| DDR16 | DQ & DQM output hold time relative to DQS | tDH | 1/4 tCK -0.8 | 1/4 tCK -0.5 | ns |

3.5.3.3 DDR2 Input AC Timing

Figure 7 and Table 36 show input AC timing for standard DDR2 and LVDDR2.

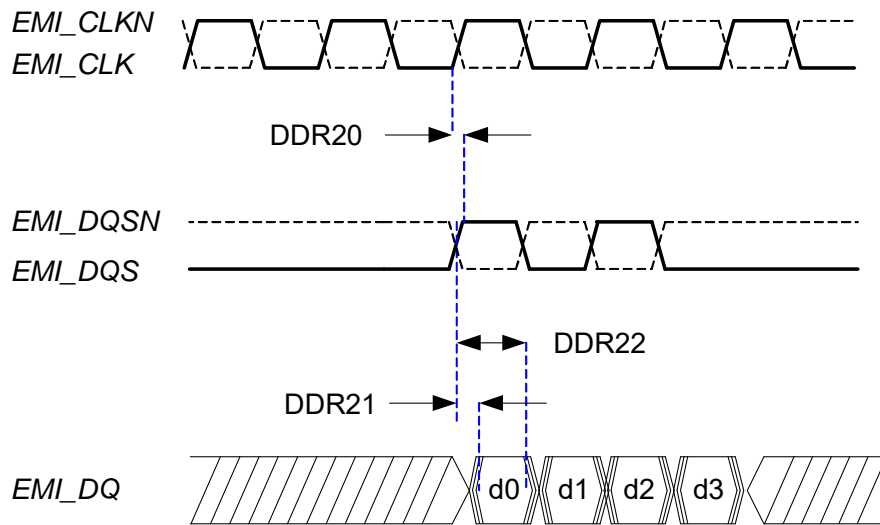


Figure 7. DDR2 Input AC Timing

Table 36. DDR2 Input AC Timing

| ID | Description | Symbol | Min | Max | Unit |
|-------|--|--------|-------------------|------------------|------|
| DDR20 | Positive DQS latching edge to associated CK edge | tDQSCK | -0.5 | 0.5 | ns |
| DDR21 | DQS to DQ input skew | tDQSQ | 0.25 tCK -0.85 | 0.25 tCK -0.5 | ns |
| DDR22 | DQS to DQ input hold time | tQH | 0.25 tCK +0.75 | 0.25 tCK +1 | ns |

3.5.3.4 LPDDR1 Input AC Timing

Figure 8 and Table 37 show input AC timing for LPDDR1.

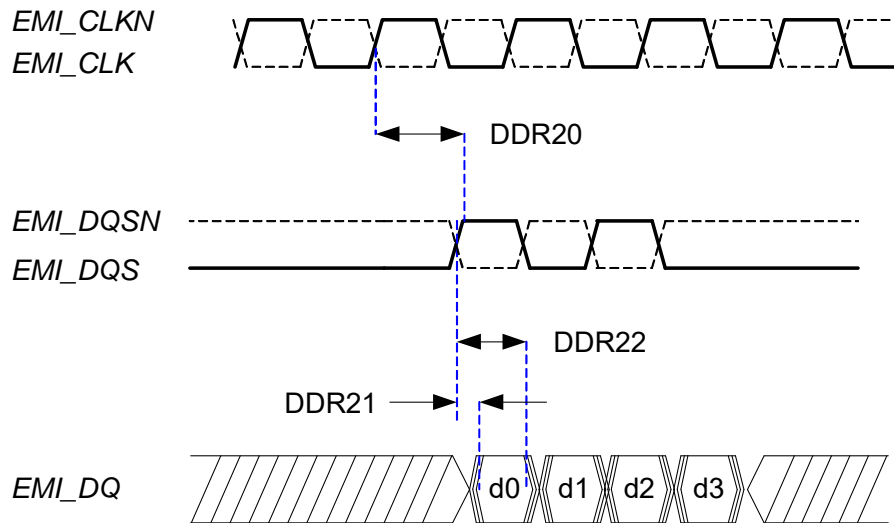


Figure 8. LPDDR1 Input AC Timing

Table 37. LPDDR1 Input AC Timing

| ID | Description | Symbol | Min | Max | Unit |
|-------|--|--------|--------------------|-------------------|------|
| DDR20 | Positive DQS latching edge to associated CK edge | tDQSCK | 2 | 6 | ns |
| DDR21 | DQS to DQ input skew | tDQSQ | 0.25 tCK - 0.85 | 0.25 tCK - 0.5 | ns |
| DDR22 | DQS to DQ input hold time | tQH | 0.25 tCK + 0.75 | 0.25 tCK + 1 | ns |

3.5.4 Ethernet MAC Controller (ENET) Timing

The ENET is designed to support both 10- and 100-Mbps Ethernet networks compliant with IEEE 802.3. An external transceiver interface and transceiver function are required to complete the interface to the media. The ENET supports 10/100-Mbps MII (18 pins altogether), 10/100-Mbps RMII (10 pins, including serial management interface), for connection to an external Ethernet transceiver. All signals are compatible with transceivers operating at a voltage of 3.3 V.

The following subsections describe the timing for MII and RMII modes.

3.5.4.1 ENET MII Mode Timing

This subsection describes MII receive, transmit, asynchronous inputs, and serial management signal timings.

3.5.4.1.1 MII Receive Signal Timing (ENET0_RXD[3:0], ENET0_RX_DV, ENET0_RX_ER, and ENET0_RX_CLK)

The receiver functions correctly up to an ENET0_RX_CLK maximum frequency of 25 MHz + 1%. There is no minimum frequency requirement. Additionally, the processor clock frequency must exceed twice the ENET0_RX_CLK frequency.

Figure 9 shows MII receive signal timings. Table 38 describes the timing parameters (M1–M4) shown in the figure.

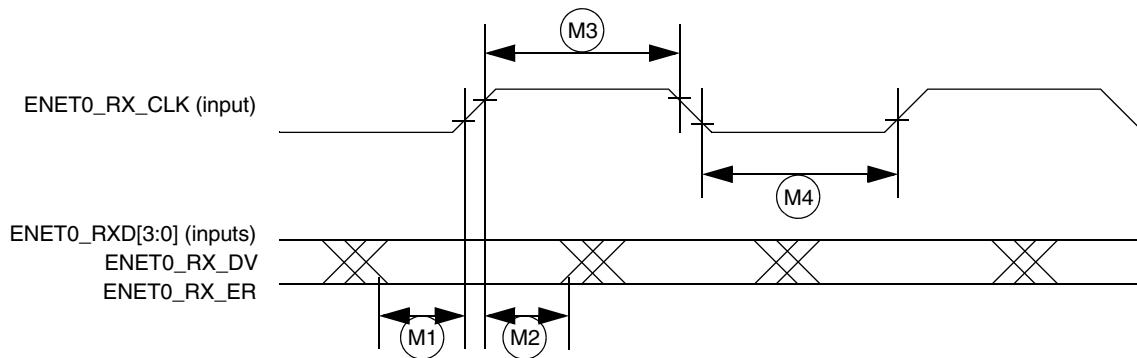


Figure 9. MII Receive Signal Timing Diagram

Table 38. MII Receive Signal Timing

| ID | Characteristic ¹ | Min | Max | Unit |
|----|--|-----|-----|---------------------|
| M1 | ENET0_RXD[3:0], ENET0_RX_DV, ENET0_RX_ER to ENET0_RX_CLK setup | 5 | — | ns |
| M2 | ENET0_RX_CLK to ENET0_RXD[3:0], ENET0_RX_DV, ENET0_RX_ER hold | 5 | — | ns |
| M3 | ENET0_RX_CLK pulse width high | 35% | 65% | ENET0_RX_CLK period |
| M4 | ENET0_RX_CLK pulse width low | 35% | 65% | ENET0_RX_CLK period |

¹ ENET0_RX_DV, ENET0_RX_CLK, and ENET0_RXD0 have the same timing in 10 Mbps 7-wire interface mode.

3.5.4.1.2 MII Transmit Signal Timing (ENET0_TXD[3:0], ENET0_TX_EN, ENET0_TX_ER, and ENET0_TX_CLK)

The transmitter functions correctly up to an ENET0_TX_CLK maximum frequency of 25 MHz + 1%. There is no minimum frequency requirement. Additionally, the processor clock frequency must exceed twice the ENET0_TX_CLK frequency.

Figure 10 shows MII transmit signal timings. Table 39 describes the timing parameters (M5–M8) shown in the figure.

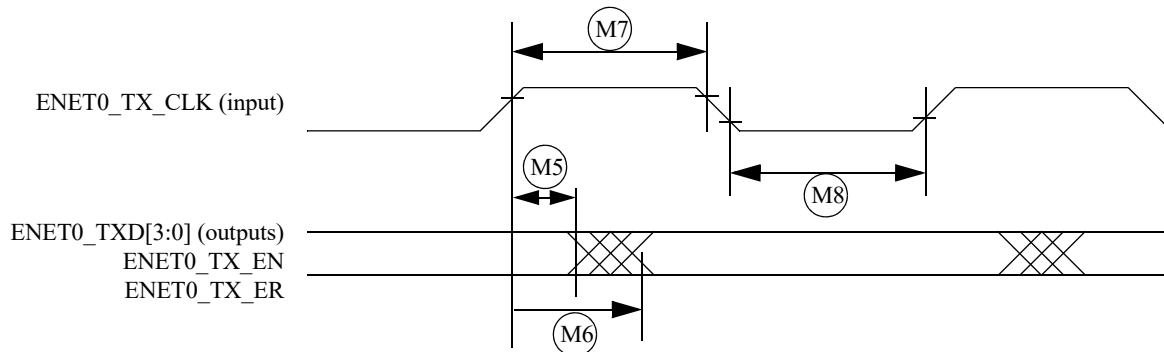


Figure 10. MII Transmit Signal Timing Diagram

Table 39. MII Transmit Signal Timing

| ID | Characteristic ¹ | Min | Max | Unit |
|----|--|-----|-----|---------------------|
| M5 | ENET0_TX_CLK to ENET0_TXD[3:0], ENET0_TX_EN, ENET0_TX_ER invalid | 5 | — | ns |
| M6 | ENET0_TX_CLK to ENET0_TXD[3:0], ENET0_TX_EN, ENET0_TX_ER valid | — | 20 | ns |
| M7 | ENET0_TX_CLK pulse width high | 35% | 65% | ENET0_TX_CLK period |
| M8 | ENET0_TX_CLK pulse width low | 35% | 65% | ENET0_TX_CLK period |

¹ ENET0_TX_EN, ENET0_TX_CLK, and ENET0_TXD0 have the same timing in 10-Mbps 7-wire interface mode.

3.5.4.1.3 MII Asynchronous Inputs Signal Timing (ENET0_CRIS and ENET0_COL)

Figure 11 shows MII asynchronous input timings. Table 40 describes the timing parameter (M9) shown in the figure.

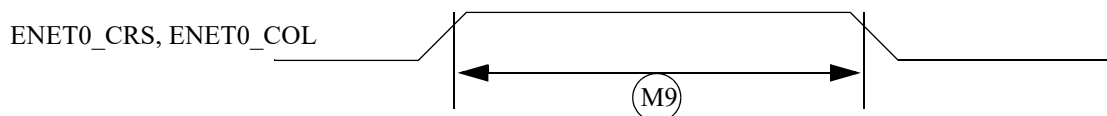


Figure 11. MII Async Inputs Timing Diagram

Table 40. MII Asynchronous Inputs Signal Timing

| ID | Characteristic | Min | Max | Unit |
|-----------------|---|-----|-----|---------------------|
| M9 ¹ | ENET0_CRIS to ENET0_COL minimum pulse width | 1.5 | — | ENET0_TX_CLK period |

¹ ENET0_COL has the same timing in 10-Mbit 7-wire interface mode.

3.5.4.1.4 MII Serial Management Channel Timing (ENET0_MDIO and ENET0_MDC)

The MDC frequency is designed to be equal to or less than 2.5 MHz to be compatible with the IEEE 802.3 MII specification. However the ENET can function correctly with a maximum MDC frequency of 15 MHz.

Figure 12 shows MII asynchronous input timings. Table 41 describes the timing parameters (M10–M15) shown in the figure.

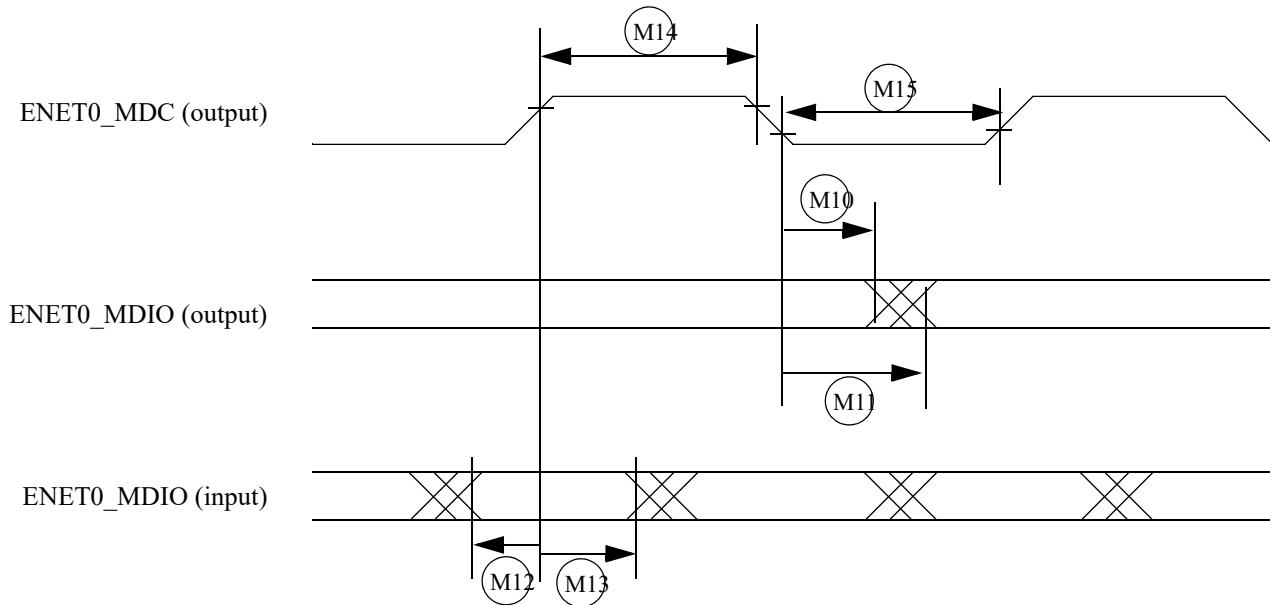


Figure 12. MII Serial Management Channel Timing Diagram

Table 41. MII Serial Management Channel Timing

| ID | Characteristic | Min | Max | Unit |
|-----|--|-----|-----|------------------|
| M10 | ENET0_MDC falling edge to ENET0_MDIO output invalid (min. propagation delay) | 0 | — | ns |
| M11 | ENET0_MDC falling edge to ENET0_MDIO output valid (max. propagation delay) | — | 5 | ns |
| M12 | ENET0_MDIO (input) to ENET0_MDC rising edge setup | 18 | — | ns |
| M13 | ENET0_MDIO (input) to ENET0_MDC rising edge hold | 0 | — | ns |
| M14 | ENET0_MDC pulse width high | 40% | 60% | ENET0_MDC period |
| M15 | ENET0_MDC pulse width low | 40% | 60% | ENET0_MDC period |

3.5.4.2 RMII Mode Timing

In RMII mode, ENET_CLK is used as the REF_CLK, which is a 50 MHz ± 50 ppm continuous reference clock. ENET0_RX_DV is used as the CRS_DV in RMII. Other signals under RMII mode include ENET0_TX_EN, ENET0_TXD[1:0], ENET0_RXD[1:0] and ENET0_RX_ER.

Figure 13 shows RMI mode timings. Table 42 describes the timing parameters (M16–M21) shown in the figure.

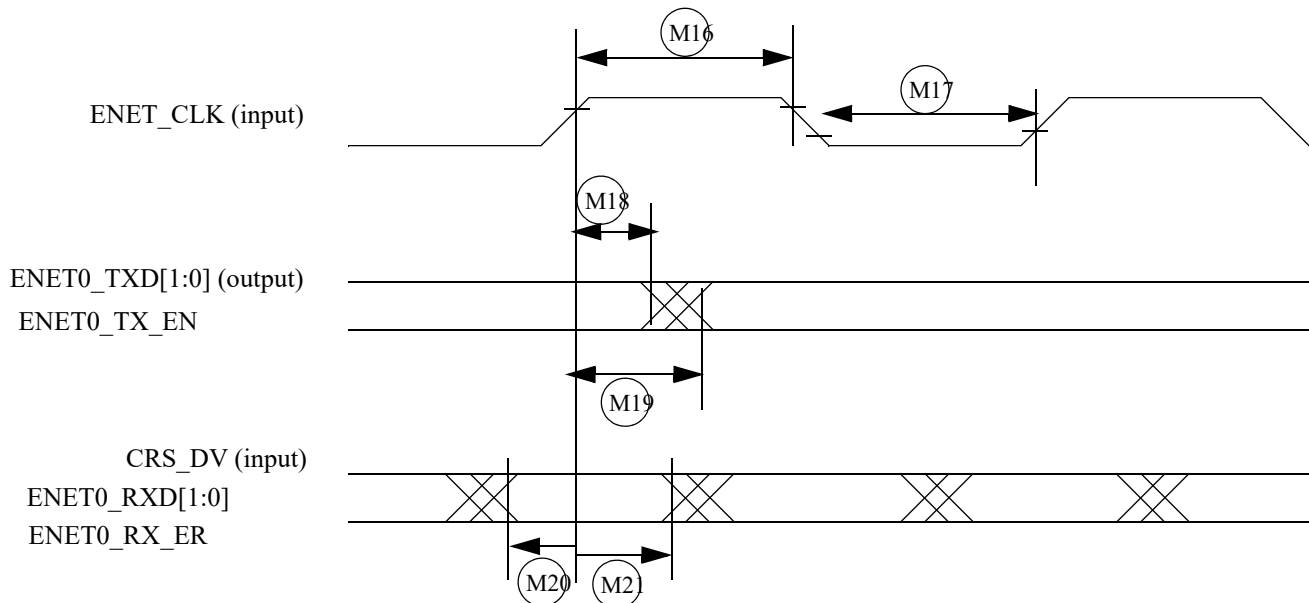


Figure 13. RMI Mode Signal Timing Diagram

Table 42. RMI Signal Timing

| ID | Characteristic | Min | Max | Unit |
|-----|--|-----|-----|-----------------|
| M16 | ENET_CLK pulse width high | 35% | 65% | ENET_CLK period |
| M17 | ENET_CLK pulse width low | 35% | 65% | ENET_CLK period |
| M18 | ENET_CLK to ENET0_TXD[1:0], ENET0_TX_EN invalid | 3 | — | ns |
| M19 | ENET_CLK to ENET0_TXD[1:0], ENET0_TX_EN valid | — | 12 | ns |
| M20 | ENET0_RXD[1:0], CRS_DV(ENET0_RX_DV), ENET0_RX_ER to ENET_CLK setup | 2 | — | ns |
| M21 | ENET_CLK to ENET0_RXD[1:0], ENET0_RX_DV, ENET0_RX_ER hold | 2 | — | ns |

3.5.5 Coresight ETM9 AC Interface Timing

The following timing specifications are given as a guide for a TPA that supports TRACECLK (ETM_TCLK) frequencies up to 80 MHz. TRACECLK is the ETM_TCLK signal which can be made functional by using some IOMUX configurations. See the reference manual for detailed information.

3.5.5.1 TRACECLK Timing

This section describes TRACECLK timings.

Figure 14 shows TRACECLK signal timings. Table 43 describes the timing parameters shown in the figure.

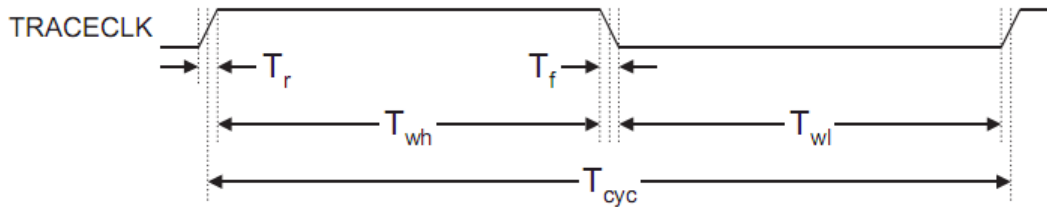


Figure 14. TRACECLK Signal Timing Diagram

Table 43. TRACECLK Signal Timing

| ID | Characteristic ¹ | Min | Max | Unit |
|------|-----------------------------|------|-----|------|
| Tr | Clock and data raise time | 3 | — | ns |
| Tf | Clock and data fall time | 3 | — | ns |
| Twh | High pulse wide | 2 | — | ns |
| Twl | Low pulse wide | 2 | — | ns |
| Tcyc | Clock period | 12.5 | — | ns |

3.5.5.2 Trace Data Signal Timing

Figure 15 shows the setup and hold requirements of the trace data pins with respect to TRACECLK. Table 44 describes the timing parameters shown in the figure.

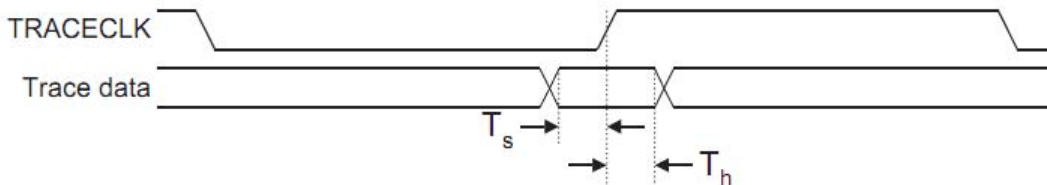


Figure 15. Trace Data Signal Timing Diagram

Table 44. Trace Data Signal Timing

| ID | Characteristic ¹ | Min | Max | Unit |
|----|-----------------------------|-----|-----|------|
| Ts | Data setup | 2 | — | ns |
| Th | Data hold | 2 | — | ns |

3.5.6 FlexCAN AC Timing

Table 45 and Table 46 show voltage requirements for the FlexCAN transceiver Tx and Rx pins.

Table 45. Tx Pin Characteristics

| Parameter | Symbol | Min | Typ | Max | Unit |
|---------------------------|--------|-----|-----|------------------|------|
| High-level output voltage | VOH | 2 | — | $V_{CC}^1 + 0.3$ | V |
| Low-level output voltage | VOL | — | 0.8 | — | V |

¹ $V_{CC} = +3.3\text{ V} \pm 5\%$

Table 46. Rx Pin Characteristics

| Parameter | Symbol | Min | Typ | Max | Unit |
|--------------------------|--------|-----------------------|-----|------------|------|
| High-level input voltage | VIH | $0.8 \times V_{CC}^1$ | — | V_{CC}^1 | V |
| Low-level input voltage | VIL | — | 0.4 | — | V |

¹ $V_{CC} = +3.3\text{ V} \pm 5\%$

Figure 16 through Figure 19 show the FlexCAN timing, including timing of the standby and shutdown signals.

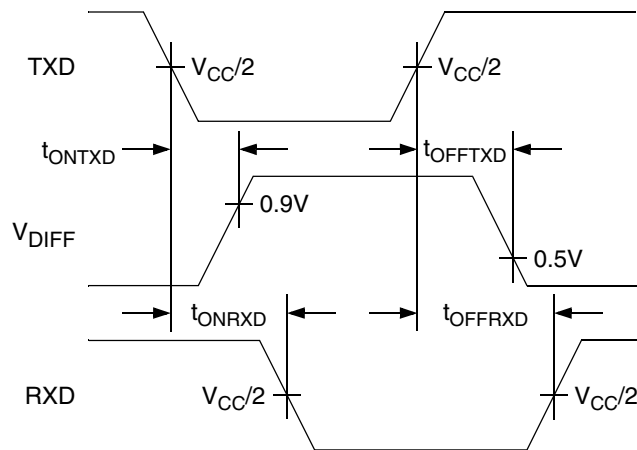


Figure 16. FlexCAN Timing Diagram

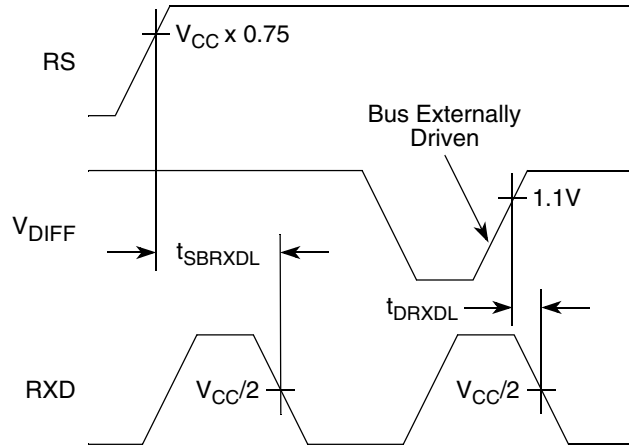


Figure 17. Timing Diagram for FlexCAN Standby Signal

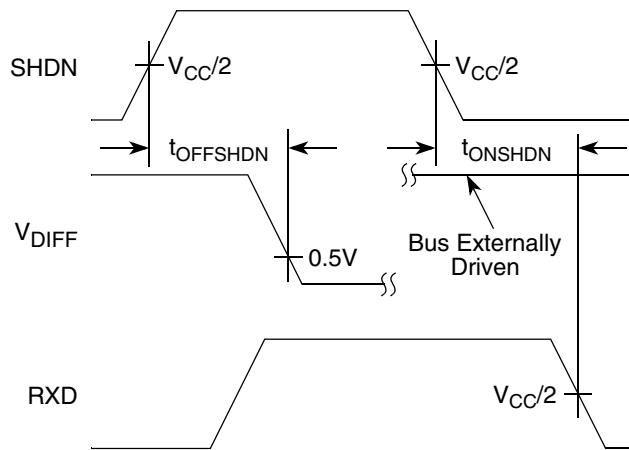


Figure 18. Timing Diagram for FlexCAN Shutdown Signal

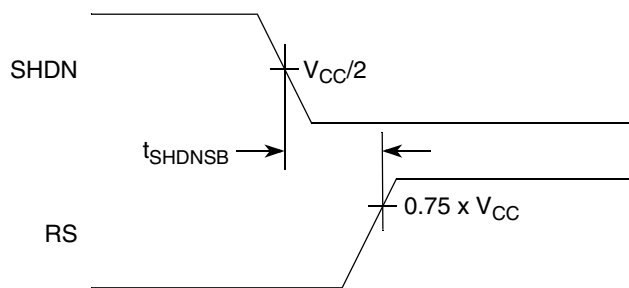


Figure 19. Timing Diagram for FlexCAN Shutdown-to-Standby Signal

3.5.7 General-Purpose Media Interface (GPMI) Timing

The i.MX28 GPMI controller is a flexible interface NAND Flash controller with 8-bit data width, up to 50MB/s I/O speed and individual chip-select.

It supports normal timing mode, using two Flash clock cycles for one access of \overline{RE} and \overline{WE} . AC timings are provided as multiplications of the clock cycle and fixed delay. Figure 20, Figure 21, Figure 22 and Figure 23 depict the relative timing between GPMI signals at the module level for different operations under normal mode. Table 47 describes the timing parameters (NF1–NF17) that are shown in the figures.

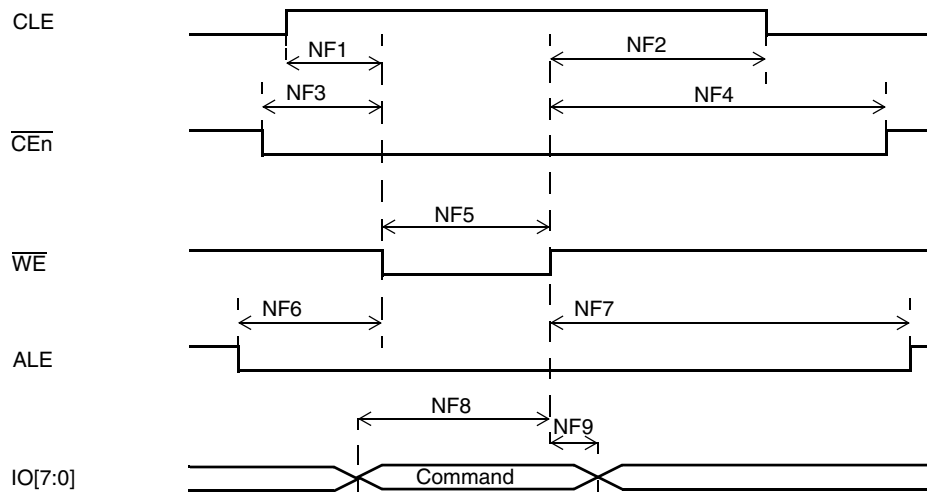


Figure 20. Command Latch Cycle Timing Diagram

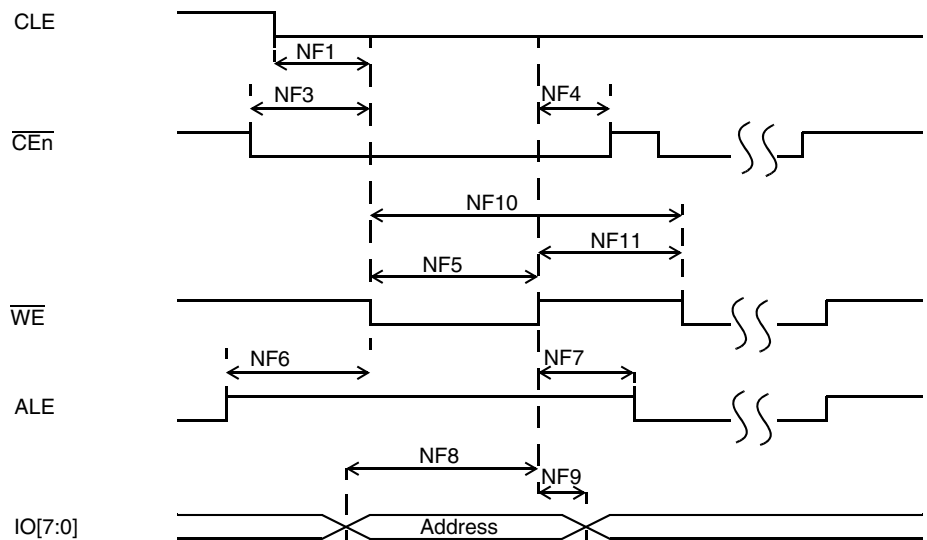


Figure 21. Address Latch Cycle Timing Diagram

Electrical Characteristics

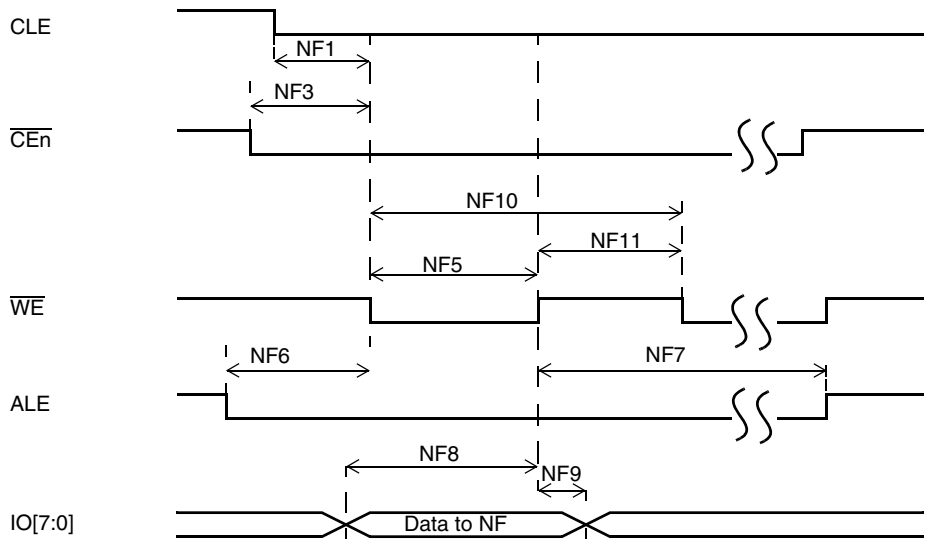


Figure 22. Write Data Latch Cycle Timing Diagram

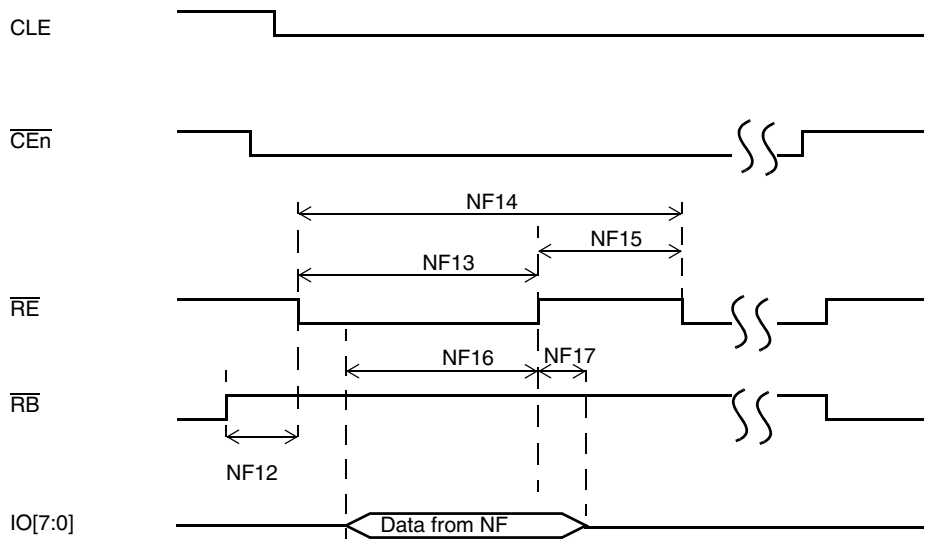


Figure 23. Read Data Latch Cycle Timing Diagram

Table 47. NFC Timing Parameters¹

| ID | Parameter | Symbol | Timing T = GPMI Clock Cycle | | Example Timing for GPMI Clock \approx 100MHz T = 10ns | | Unit |
|------|--------------------------------|--------|--------------------------------|-----|---|-----|------|
| | | | Min | Max | Min | Max | |
| NF1 | CLE setup time | tCLS | $(AS+1)*T$ | — | 10 | — | ns |
| NF2 | CLE hold time | tCLH | $(DH+1)*T$ | — | 20 | — | ns |
| NF3 | \overline{CEn} setup time | tCS | $(AS+1)*T$ | — | 10 | — | ns |
| NF4 | \overline{CE} hold time | tCH | $(DH+1)*T$ | — | 20 | — | ns |
| NF5 | \overline{WE} pulse width | tWP | DS*T | | 10 | | ns |
| NF6 | ALE setup time | tALS | $(AS+1)*T$ | — | 10 | — | ns |
| NF7 | ALE hold time | tALH | $(DH+1)*T$ | — | 20 | — | ns |
| NF8 | Data setup time | tDS | DS*T | — | 10 | — | ns |
| NF9 | Data hold time | tDH | DH*T | — | 10 | — | ns |
| NF10 | Write cycle time | tWC | $(DS+DH)*T$ | | 20 | | ns |
| NF11 | \overline{WE} hold time | tWH | DH*T | | 10 | | ns |
| NF12 | Ready to \overline{RE} low | tRR | $(AS+1)*T$ | — | 10 | — | ns |
| NF13 | \overline{RE} pulse width | tRP | DS*T | — | 10 | — | ns |
| NF14 | READ cycle time | tRC | $(DS+DH)*T$ | — | 20 | — | ns |
| NF15 | \overline{RE} high hold time | tREH | DH*T | | 10 | — | ns |
| NF16 | Data setup on read | tDSR | N/A | | 10 | — | ns |
| NF17 | Data hold on read | tDHR | N/A | | 10 | — | ns |

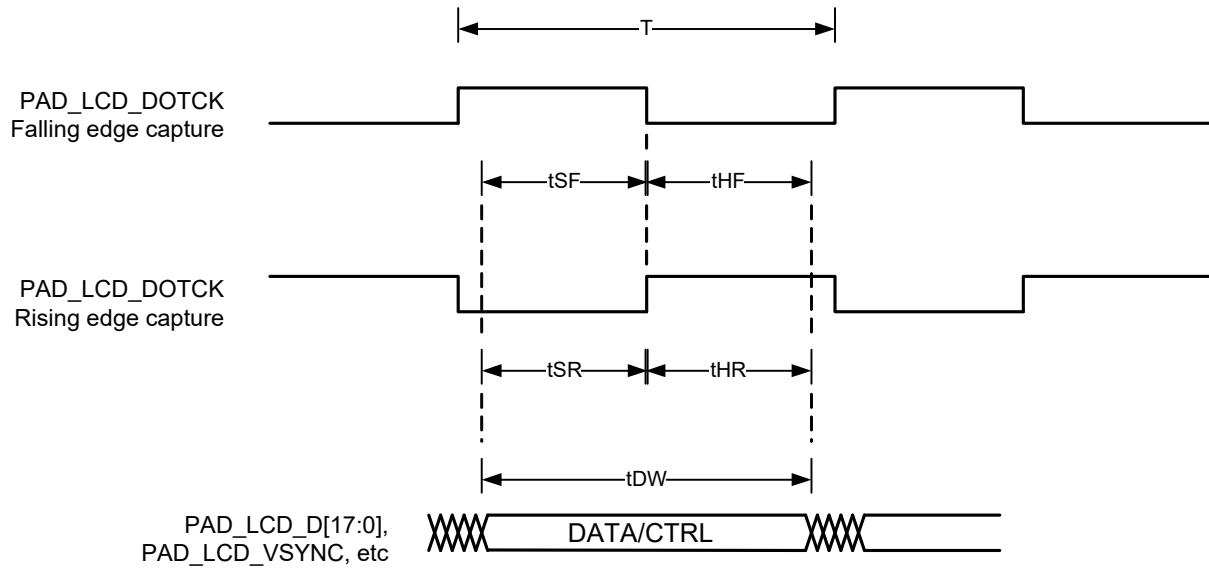
¹ The Flash clock maximum frequency is 100 MHz.

2) GPMI's output timing could be controlled by module's internal register, say HW_GPMI_TIMING0_ADDRESS_SETUP, HW_GPMI_TIMING0_DATA_SETUP, HW_GPMI_TIMING0_DATA_HOLD, this AC timing depends on these registers' setting. In the above table we use AS/DS/DH representing these settings each.

3) AS minimum value could be 0, while DS/DH minimum value is 1.

3.5.8 LCD AC Output Electrical Specifications

Figure 24 depicts the AC output timing for the LCD module. Table 48 lists the LCD module timing parameters.



- Notes:**
 T = LCD interface clock period
 I/O Drive Strength = 4mA
 I/O Voltage = 3.3V
 Cck = Capacitance load on DOTCK pad
 Cd = Capacitance load on DATA/CTRL pad

Figure 24. LCD AC Output Timing Diagram

Table 48. LCD AC Output Timing Parameters

| ID | Parameter | Description |
|-----|-----------------------------|---|
| tSF | Data setup for falling edge | $DOTCK = T/2 - 1.97ns + 0.15 * Cck - 0.19 * Cd$ |
| tHF | Data hold for falling edge | $DOTCK = T/2 + 0.29ns + 0.09 * Cd - 0.10 * Cck$ |
| tSR | Data setup for rising edge | $DOTCK = T/2 - 2.09ns + 0.18 * Cck - 0.19 * Cd$ |
| tHR | Data hold for rising edge | $DOTCK = T/2 + 0.40ns + 0.09 * Cd - 0.10 * Cck$ |
| tDW | Data valid window | $tDW = T - 1.45ns$ |

3.5.9 Inter IC (I²C) Timing

The I²C module is designed to support up to 400-Kbps I²C connection compliant with I²C bus protocol. The following section describes I²C SDA and SCL signal timings.

Figure 25 shows the timing of the I²C module. Table 49 describes the I²C module timing parameters (IC1–IC11) shown in the figure.

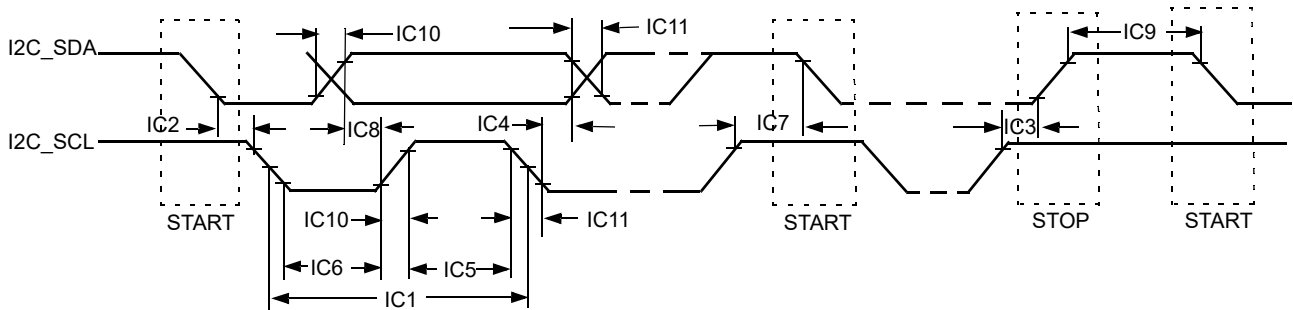


Figure 25. I²C Module Timing Diagram

Table 49. I²C Module Timing Parameters: 1.8 V – 3.6 V

| ID | Parameter | Standard Mode | | Fast Mode | | Unit |
|------|---|----------------|-------------------|-----------------------------------|------------------|------|
| | | Min | Max | Min | Max | |
| IC1 | I2C_SCL cycle time | 10 | — | 2.5 | — | μs |
| IC2 | Hold time (repeated) START condition | 4.0 | — | 0.6 | — | μs |
| IC3 | Set-up time for STOP condition | 4.0 | — | 0.6 | — | μs |
| IC4 | Data hold time | 0 ¹ | 3.45 ² | 0 ¹ | 0.9 ² | μs |
| IC5 | HIGH Period of I2C_SCL clock | 4.0 | — | 0.6 | — | μs |
| IC6 | LOW Period of the I2C_SCL clock | 4.7 | — | 1.3 | — | μs |
| IC7 | Set-up time for a repeated START condition | 4.7 | — | 0.6 | — | μs |
| IC8 | Data set-up time | 250 | — | 100 ³ | — | ns |
| IC9 | Bus free time between a STOP and START condition | 4.7 | — | 1.3 | — | μs |
| IC10 | Rise time of both I2C_SDA and I2C_SCL signals | — | 1000 | 20+0.1C _b ⁴ | 300 | ns |
| IC11 | Fall time of both I2C_SDA and I2C_SCL signals | — | 300 | 20+0.1C _b ⁴ | 300 | ns |
| IC12 | Capacitive load for each bus line (C _b) | — | 400 | — | 400 | pF |

¹ A device must internally provide a hold time of at least 300 ns for the I2C_SDA signal in order to bridge the undefined region of the falling edge of I2C_SCL.

² The maximum IC4 has to be met only if the device does not stretch the LOW period (ID no IC5) of the I2C_SCL signal.

³ A fast-mode I2C bus device can be used in a standard-mode I2C bus system, but the requirement of Set-up time (ID No IC7) of 250 ns must then be met. This is automatically the case if the device does not stretch the LOW period of the I2C_SCL signal. If such a device does stretch the LOW period of the I2C_SCL signal, it must output the next data bit to the I2C_SDA line max_rise_time (ID No IC9) + data_setup_time (ID No IC7) = 1000 + 250 = 1250 ns (according to the standard-mode I2C bus specification) before the I2C_SCL line is released.

⁴ C_b = total capacitance of one bus line in pF.

3.5.10 JTAG Interface Timing

Figure 26 through Figure 29 show respectively the test clock input, boundary scan, test access port, and TRST timings for the SJC. Table 50 describes the SJC timing parameters (SJ1–SJ13) indicated in the figures.

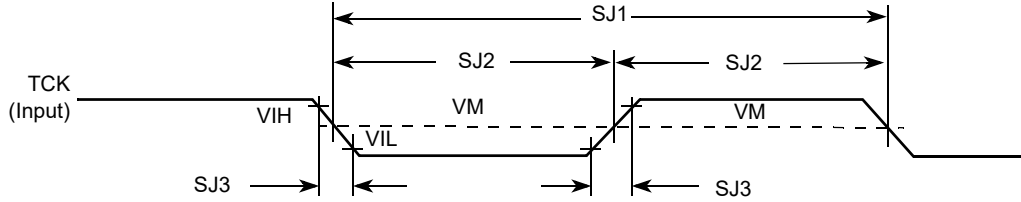


Figure 26. Test Clock Input Timing Diagram

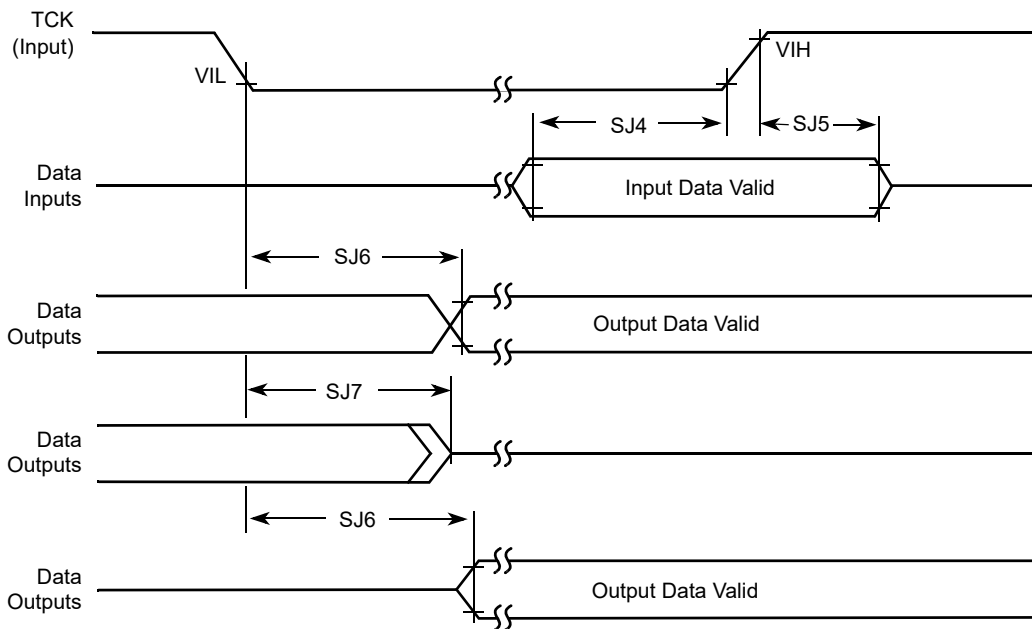


Figure 27. Boundary Scan (JTAG) Timing Diagram

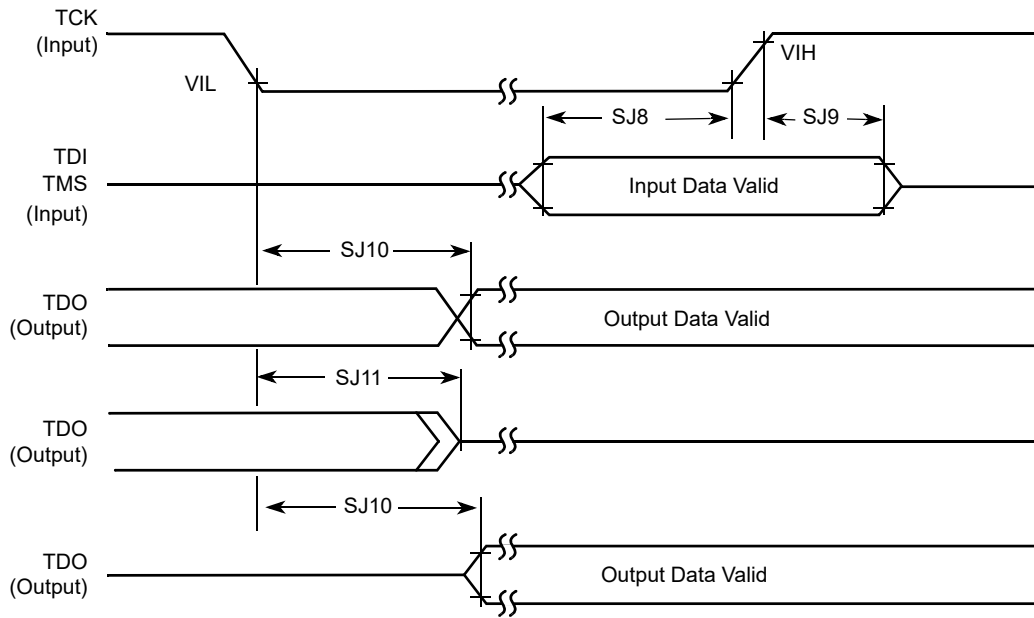


Figure 28. Test Access Port Timing Diagram

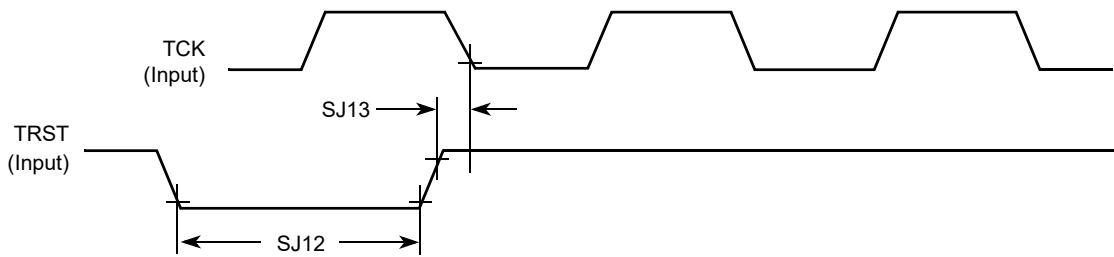


Figure 29. TRST Timing Diagram

Table 50. SJC Timing Parameters

| ID | Parameter | All Frequencies | | Unit |
|-----|---|-----------------|-----|------|
| | | Min | Max | |
| SJ1 | TCK cycle time | 100 | — | ns |
| SJ2 | TCK clock pulse width measured at V_M^1 | 40 | — | ns |
| SJ3 | TCK rise and fall times | — | 3 | ns |
| SJ4 | Boundary scan input data set-up time | 10 | — | ns |
| SJ5 | Boundary scan input data hold time | 50 | — | ns |
| SJ6 | TCK low to output data valid | — | 50 | ns |
| SJ7 | TCK low to output high impedance | — | 50 | ns |
| SJ8 | TMS, TDI data set-up time | 10 | — | ns |
| SJ9 | TMS, TDI data hold time | 50 | — | ns |

Table 50. SJC Timing Parameters (continued)

| ID | Parameter | All Frequencies | | Unit |
|------|---|-----------------|-----|------|
| | | Min | Max | |
| SJ10 | TCK low to TDO data valid | — | 44 | ns |
| SJ11 | TCK low to TDO high impedance | — | 44 | ns |
| SJ12 | $\overline{\text{TRST}}$ assert time | 100 | — | ns |
| SJ13 | $\overline{\text{TRST}}$ set-up time to TCK low | 40 | — | ns |

¹ V_M - mid point voltage.

3.5.11 Pulse Width Modulator (PWM) Timing

Figure 30 depicts the timing of the PWM, and Table 51 lists the PWM timing characteristics.

The PWM can be programmed to select one of two clock signals as its source frequency: xtal clock or hsadc clock. The selected clock signal is passed through a prescaler before being input to the counter. The output is available at the pulse width modulator output (PWMO) external pin.

PWM also supports MATT mode. In this mode, it can be programmed to select one of two clock signals as its source frequency, 24-MHz or 32-kHz crystal clock. For a 32-kHz source clock input, the PWM outputs the 32-kHz clock directly to PAD.

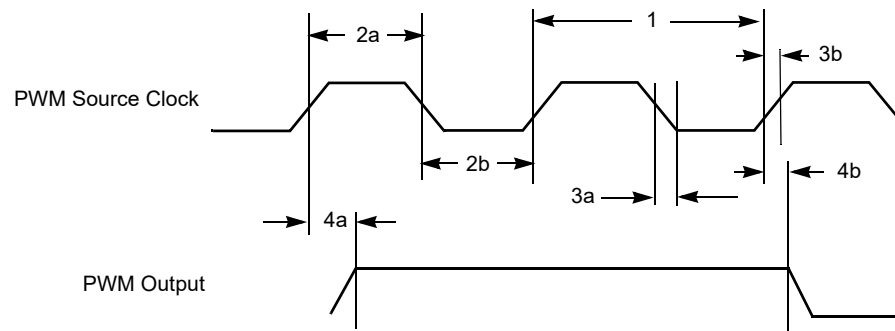


Figure 30. PWM Timing

Table 51. PWM Output Timing Parameter: Xtal clock

| Ref No. | Parameter | Min | Max | Unit |
|---------|-----------------------------------|-------|-------|------|
| 1 | System CLK frequency ¹ | 0 | 24MHz | MHz |
| 2a | Clock high time | 21 | — | ns |
| 2b | Clock low time | 21 | — | ns |
| 3a | Clock fall time | — | 0.3 | ns |
| 3b | Clock rise time | — | 0.3 | ns |
| 4a | Output delay time | — | 15.08 | ns |
| 4b | Output setup time | 15.77 | — | ns |

¹ CL of PWMO = 30 pF.

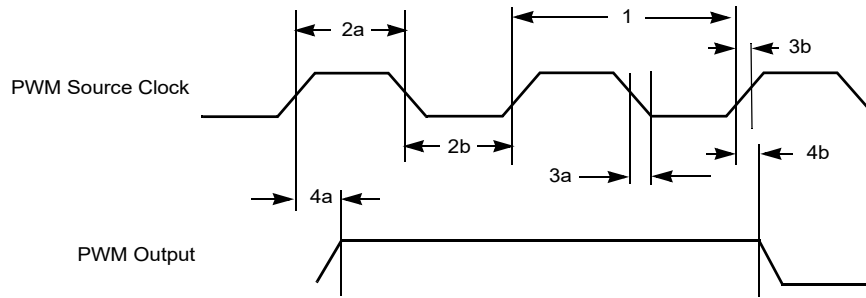


Figure 31. PWM Timing

Table 52. PWM Output Timing Parameter: HSADC clock

| Ref No. | Parameter | Min | Max | Unit |
|---------|-----------------------------------|--------|-------|------|
| 1 | System CLK frequency ¹ | 0 | 32 | MHz |
| 2a | Clock high time | 6.813 | — | ns |
| 2b | Clock low time | 24.432 | — | ns |
| 3a | Clock fall time | — | 0.3 | ns |
| 3b | Clock rise time | — | 0.3 | ns |
| 4a | Output delay time | — | 14.93 | ns |
| 4b | Output setup time | 15.71 | — | ns |

¹ CL of PWMO = 30 pF.

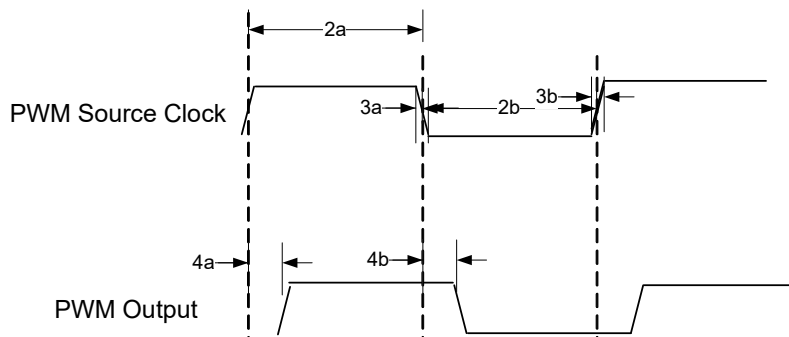


Figure 32. PWM Timing

Table 53. PWM Output Timing Parameter: MATT Mode 24 MHz Crystal Clock

| Ref No. | Parameter | Min | Max | Unit |
|---------|-----------------------------------|-------|-----|------|
| 1 | System CLK frequency ¹ | 24 | 24 | MHz |
| 2a | Clock high time | 20.99 | — | ns |
| 2b | Clock low time | 21.01 | — | ns |

Table 53. PWM Output Timing Parameter: MATT Mode 24 MHz Crystal Clock (continued)

| Ref No. | Parameter | Min | Max | Unit |
|---------|-------------------|-------|-------|------|
| 3a | Clock fall time | — | 0.3 | ns |
| 3b | Clock rise time | — | 0.3 | ns |
| 4a | Output delay time | — | 15.23 | ns |
| 4b | Output setup time | 15.92 | — | ns |

¹ CL of PWMO = 30 pF

3.5.12 Serial Audio Interface (SAIF) AC Timing

The following subsections describe SAIF timing in two cases:

- Transmitter
- Receiver

3.5.12.1 SAIF Transmitter Timing

Figure 33 shows the timing for SAIF transmitter with internal clock, and Table 54 describes the timing parameters (SS1–SS13).

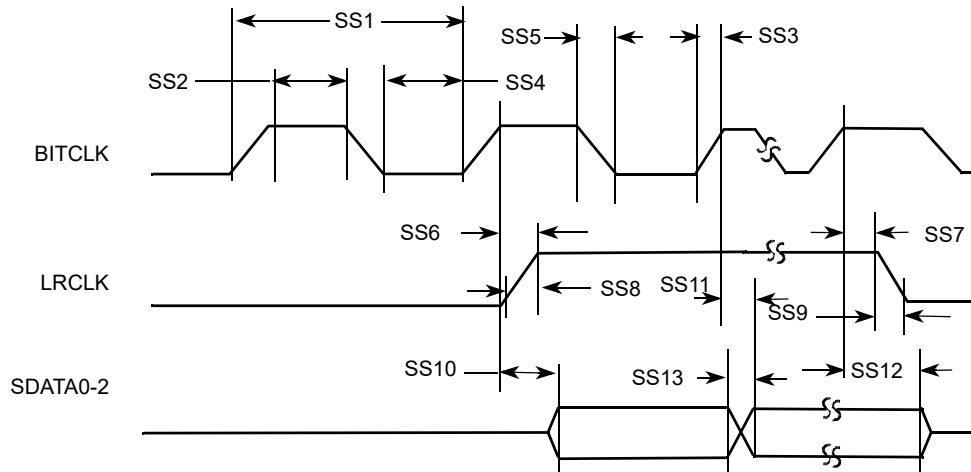


Figure 33. SAIF Transmitter Timing Diagram

Table 54. SAIF Transmitter Timing

| ID | Parameter | Min | Max | Unit |
|-----|---------------------------|------|------|------|
| SS1 | BITCLK period | 81.4 | — | ns |
| SS2 | BITCLK high period | 36.0 | — | ns |
| SS3 | BITCLK rise time | — | 6.0 | ns |
| SS4 | BITCLK low period | 36.0 | — | ns |
| SS5 | BITCLK fall time | — | 6.0 | ns |
| SS6 | BITCLK high to LRCLK high | — | 15.0 | ns |

Table 54. SAIF Transmitter Timing (continued)

| ID | Parameter | Min | Max | Unit |
|------|--|-----|------|------|
| SS7 | BITCLK high to LRCLK low | — | 15.0 | ns |
| SS8 | LRCLK rise time | — | 6.0 | ns |
| SS9 | LRCLK fall time | — | 6.0 | ns |
| SS10 | BITCLK high to SDATA valid from high impedance | — | 15.0 | ns |
| SS11 | BITCLK high to SDATA high/low | — | 15.0 | ns |
| SS12 | BITCLK high to SDATA high impedance | — | 15.0 | ns |
| SS13 | SDATA rise/fall time | — | 6.0 | ns |

3.5.12.2 SAIF Receiver Timing

Figure 34 shows the timing for the SAIF receiver with internal clock. Table 55 describes the timing parameters (SS1–SS17) shown in the figure.

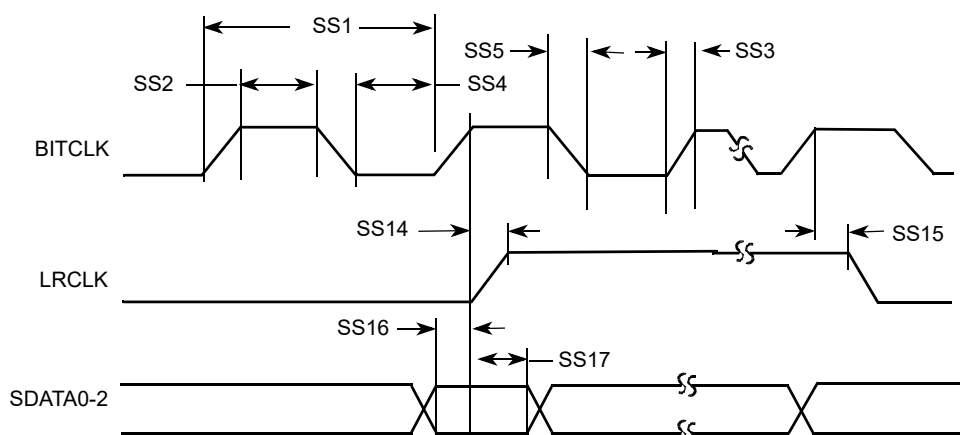


Figure 34. SAIF Receiver Timing Diagram

Table 55. SAIF Receiver Timing with Internal Clock

| ID | Parameter | Min | Max | Unit |
|------|-------------------------------------|------|------|------|
| SS1 | BITCLK period | 81.4 | — | ns |
| SS2 | BITCLK high period | 36.0 | — | ns |
| SS3 | BITCLK rise time | — | 6.0 | ns |
| SS4 | BITCLK low period | 36.0 | — | ns |
| SS5 | BITCLK fall time | — | 6.0 | ns |
| SS14 | BITCLK high to LRCLK high | — | 15.0 | ns |
| SS15 | BITCLK high to LRCLK low | — | 15.0 | ns |
| SS16 | SDATA setup time before BITCLK high | 10.0 | — | ns |
| SS17 | SDATA hold time after BITCLK high | 0.0 | — | ns |

3.5.13 SPDIF AC Timing

SPDIF data is sent using bi-phase marking code. When encoding, the SPDIF data signal is modulated by a clock that is twice the bit rate of the data signal.

The following Table 56 shows SPDIF timing parameters, including the timing of the modulating Tx clock (spdif_clk) in SPDIF transmitter as shown in the Figure 35.

Table 56. SPDIF Timing

| Characteristics | Symbol | Timing Parameter Range | | Unit |
|--|---------|------------------------|------|------|
| | | Min | Max | |
| SPDIFOUT output (Load = 30pf) | — | — | — | ns |
| • Skew | — | — | 1.5 | |
| • Transition Rising | — | — | 13.6 | |
| • Transition Falling | — | — | 18.0 | |
| Modulating Tx clock (spdif_clk) period | spclkp | 81.4 | — | ns |
| spdif_clk high period | spclkph | 65.1 | — | ns |
| spdif_clk low period | spclkpl | 65.1 | — | ns |

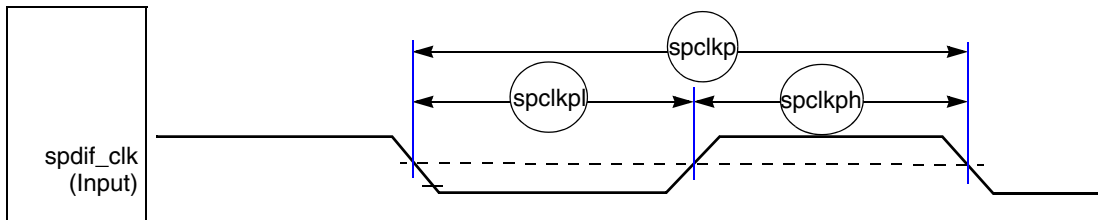


Figure 35. spdif_clk Timing

3.5.14 Synchronous Serial Port (SSP) AC Timing

This section describes the electrical information of the SSP, which includes SD/MMC4.3 (Single Data Rate) timing, MMC4.4 (Dual Data Rate) timing, MS (Memory Stick) timing, and SPI timing.

3.5.14.1 SD/MMC4.3 (Single Data Rate) AC Timing

Figure 36 depicts the timing of SD/MMC4.3, and Table 57 lists the SD/MMC4.3 timing characteristics.

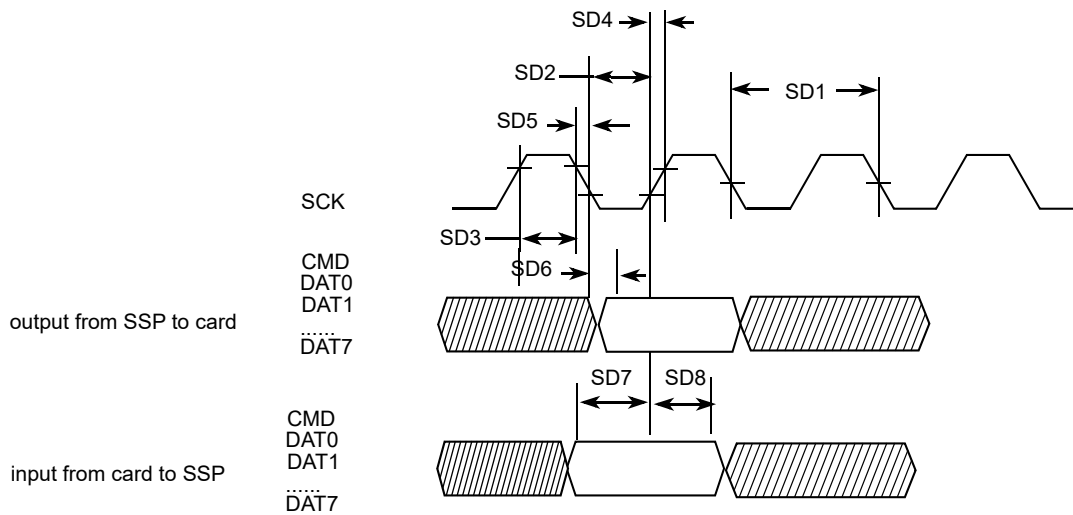


Figure 36. SD/MMC4.3 Timing

Table 57. SD/MMC4.3 Interface Timing Specification

| ID | Parameter | Symbols | Min | Max | Unit |
|---|---|------------|-----|-------|------|
| Card Input Clock | | | | | |
| SD1 | Clock Frequency (Low Speed) | f_{PP}^1 | 0 | 400 | kHz |
| | Clock Frequency (SD/SDIO Full Speed/High Speed) | f_{PP}^2 | 0 | 25/50 | MHz |
| | Clock Frequency (MMC Full Speed/High Speed) | f_{PP}^3 | 0 | 20/52 | MHz |
| | Clock Frequency (Identification Mode) | f_{OD} | 100 | 400 | kHz |
| SD2 | Clock Low Time | t_{WL} | 7 | — | ns |
| SD3 | Clock High Time | t_{WH} | 7 | — | ns |
| SD4 | Clock Rise Time | t_{TLH} | — | 3 | ns |
| SD5 | Clock Fall Time | t_{THL} | — | 3 | ns |
| SSP Output / Card Inputs CMD, DAT (Reference to CLK) | | | | | |
| SD6 | SSP Output Delay | t_{OD} | -5 | 5 | ns |
| SSP Input / Card Outputs CMD, DAT (Reference to CLK) | | | | | |
| SD7 | SSP Input Setup Time | t_{ISU} | 2.5 | — | ns |
| SD8 | SSP Input Hold Time | t_{IH}^4 | 2.5 | — | ns |

¹ In low speed mode, the card clock must be lower than 400 kHz, and the voltage ranges from 2.7 to 3.6 V.

² In normal speed mode for the SD/SDIO card, clock frequency can be any value between 0 ~ 25 MHz. In high speed mode, clock frequency can be any value between 0 ~ 50 MHz.

³ In normal speed mode for MMC card, clock frequency can be any value between 0 ~ 20 MHz. In high speed mode, clock frequency can be any value between 0 ~ 52MHz.

⁴ To satisfy hold timing, the delay difference between clock input and cmd/data input must not exceed 2ns.

3.5.14.2 MMC4.4 (Dual Data Rate) AC Timing

Figure 37 depicts the timing of MMC4.4, and Table 58 lists the MMC4.4 timing characteristics. Be aware that only DATA0–DATA7 are sampled on both edges of the clock (not applicable to CMD).

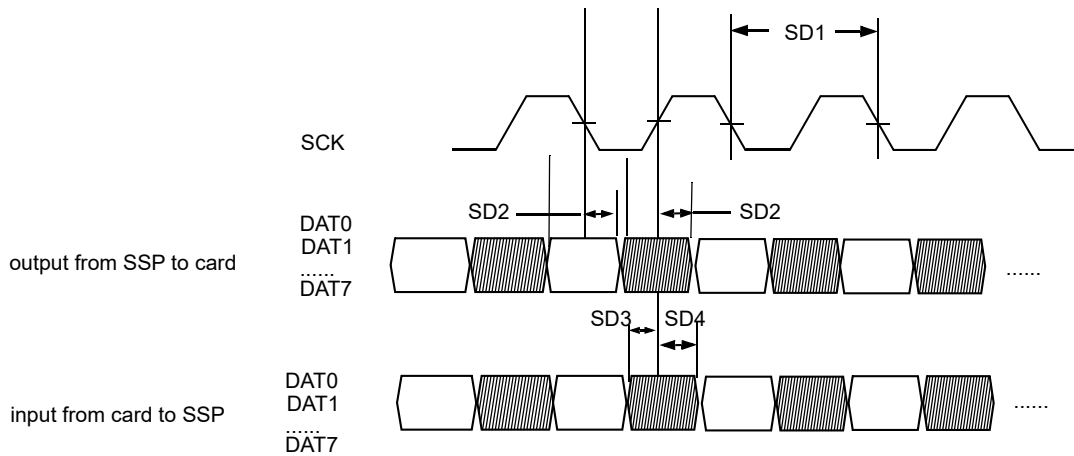


Figure 37. MMC4.4 Timing

Table 58. MMC4.4 Interface Timing Specification

| ID | Parameter | Symbols | Min | Max | Unit |
|---|---|-----------|-----|-----|------|
| Card Input Clock | | | | | |
| SD1 | Clock Frequency (MMC Full Speed/High Speed) | f_{PP} | 0 | 52 | MHz |
| SSP Output / Card Inputs CMD, DAT (Reference to CLK) | | | | | |
| SD2 | SSP Output Delay | t_{OD} | -5 | 5 | ns |
| SSP Input / Card Outputs CMD, DAT (Reference to CLK) | | | | | |
| SD3 | SSP Input Setup Time | t_{ISU} | 2.5 | — | ns |
| SD4 | SSP Input Hold Time | t_{IH} | 2.5 | — | ns |

3.5.14.3 MS (Memory Stick) AC Timing

The SSP module, which also has the function of a memory stick host controller, is compatible with the Sony Memory Stick version 1.x and Memory Stick PRO.

Figure 38, Figure 39 and Table 40 show the timing of the Memory Stick. Table 59 and Table 60 list the Memory Stick timing characteristics.

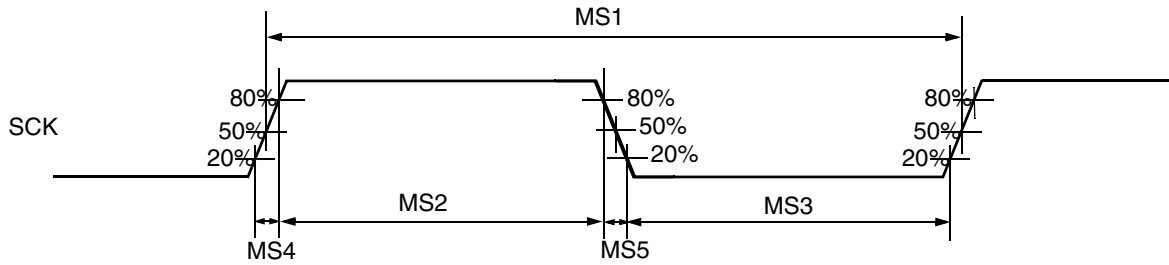


Figure 38. MS Clock Time Waveforms

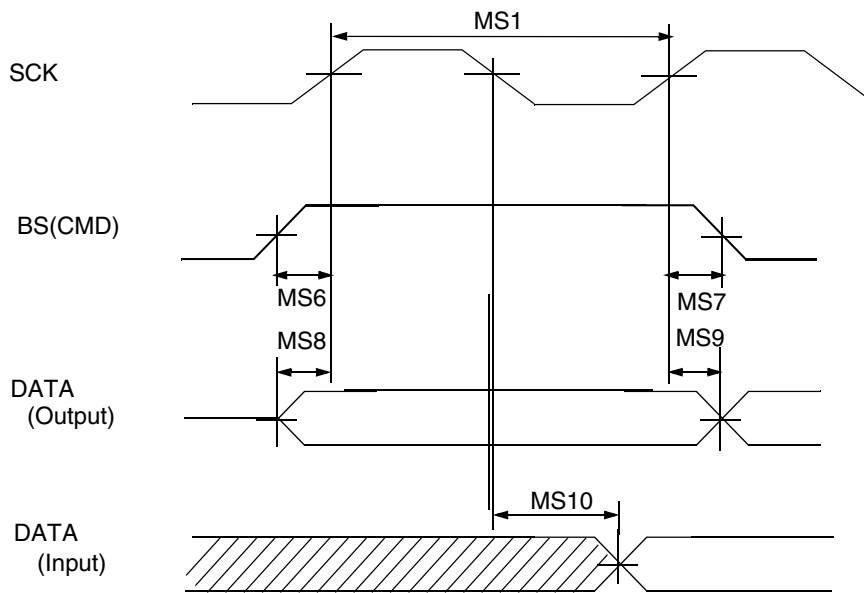


Figure 39. MS Serial Transfer Mode Timing Diagram

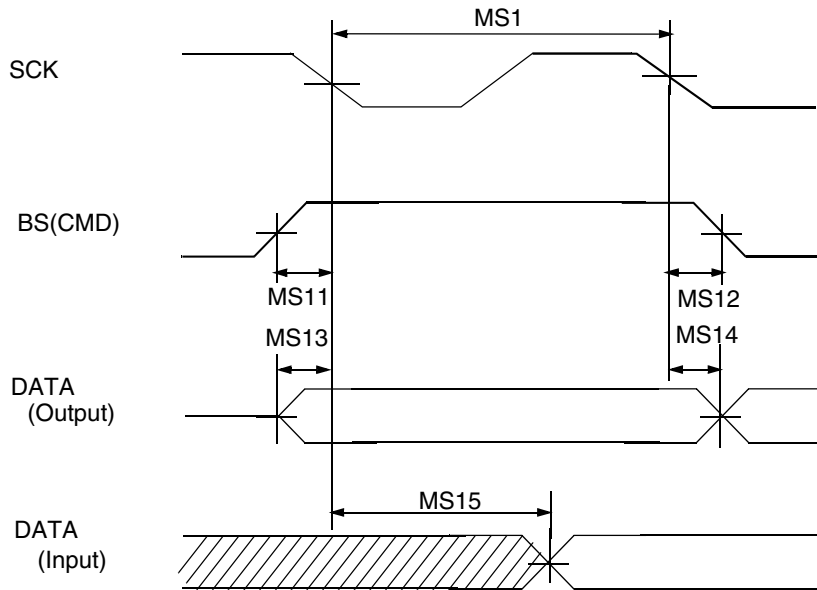


Figure 40. MS Parallel Transfer Mode Timing Diagram

Table 59. MS Serial Transfer Timing Parameters

| ID | Parameter | Symbol | Min | Max | Unit |
|------|-----------------------|--------|-----|-----|------|
| MS1 | SCK Cycle Time | tCLKc | 50 | — | ns |
| MS2 | SCK High Pulse Time | tCLKwh | 15 | — | ns |
| MS3 | SCK Low Pulse Time | tCLKwl | 15 | — | ns |
| MS4 | SCK Rise Time | tCLKr | — | 10 | ns |
| MS5 | SCK Fall Time | tCLKf | — | 10 | ns |
| MS6 | BS Setup Time | tBSsu | 5 | — | ns |
| MS7 | BS Hold Time | tBSsh | 5 | — | ns |
| MS8 | DATA Setup Time | tDsu | 5 | — | ns |
| MS9 | DATA Hold Time | tDh | 5 | — | ns |
| MS10 | DATA Input Delay Time | tDd | — | 15 | ns |

Table 60. MS Parallel Transfer Timing Parameters

| ID | Parameter | Symbol | Min | Max | Unit |
|-----|---------------------|--------|-----|-----|------|
| MS1 | SCK Cycle Time | tCLKc | 25 | — | ns |
| MS2 | SCK High Pulse Time | tCLKwh | 5 | — | ns |
| MS3 | SCK Low Pulse Time | tCLKwl | 5 | — | ns |
| MS4 | SCK Rise Time | tCLKr | — | 10 | ns |
| MS5 | SCK Fall Time | tCLKf | — | 10 | ns |

Table 60. MS Parallel Transfer Timing Parameters (continued)

| ID | Parameter | Symbol | Min | Max | Unit |
|------|-----------------------|--------|-----|-----|------|
| MS11 | BS Setup Time | tBSsu | 8 | — | ns |
| MS12 | BS Hold Time | tBSH | 1 | — | ns |
| MS13 | DATA Setup Time | tDsu | 8 | — | ns |
| MS14 | DATA Hold Time | tDh | 1 | — | ns |
| MS15 | DATA Input Delay Time | tDd | — | 15 | ns |

3.5.14.4 SPI AC Timing

Figure 41 depicts the master mode and slave mode timings of the SPI, and Table 61 lists the timing parameters.

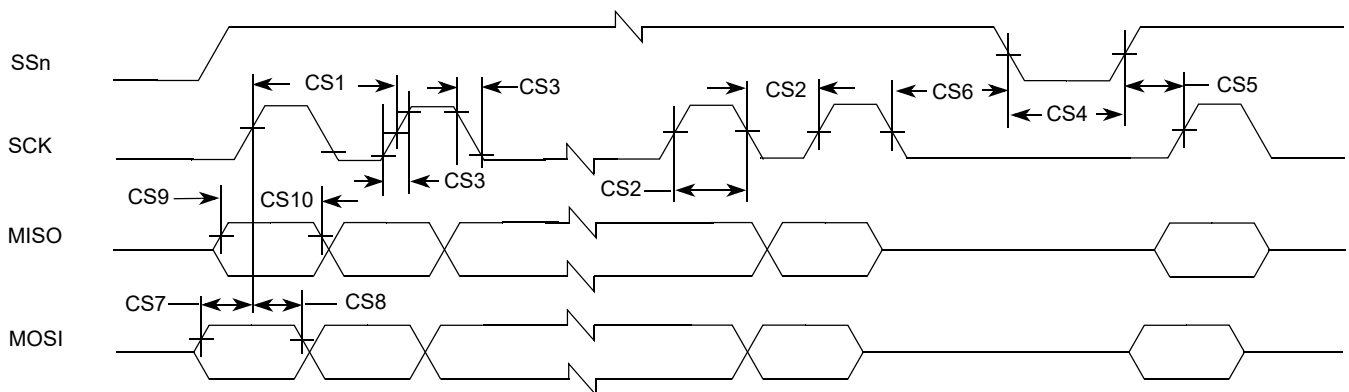


Figure 41. SPI Interface Timing Diagram

Table 61. SPI Interface Timing Parameters

| ID | Parameter | Symbol | Min | Max | Unit |
|------|--|-----------------|-----|-----|------|
| CS1 | SCK cycle time | t_{clk} | 50 | — | ns |
| CS2 | SCK high or low time | t_{SW} | 25 | — | ns |
| CS3 | SCK rise or fall | $t_{RISE/FALL}$ | — | 7.6 | ns |
| CS4 | \overline{SSn} pulse width | t_{CSLH} | 25 | — | ns |
| CS5 | \overline{SSn} lead time (CS setup time) | t_{SCS} | 25 | — | ns |
| CS6 | \overline{SSn} lag time (CS hold time) | t_{HCS} | 25 | — | ns |
| CS7 | MOSI setup time | t_{Smosi} | 5 | — | ns |
| CS8 | MOSI hold time | t_{Hmosi} | 5 | — | ns |
| CS9 | MISO setup time | t_{Smiso} | 5 | — | ns |
| CS10 | MISO hold time | t_{Hmiso} | 5 | — | ns |

3.5.15 UART (UARTAPP and DebugUART) AC Timing

This section describes the UART module AC timing which is applicable to both UARTAPP and DebugUART.

3.5.15.1 UART Transmit Timing

Figure 39 shows the UART transmit timing, showing only eight data bits and one stop bit. Table 62 describes the timing parameter (UA1) shown in the figure.

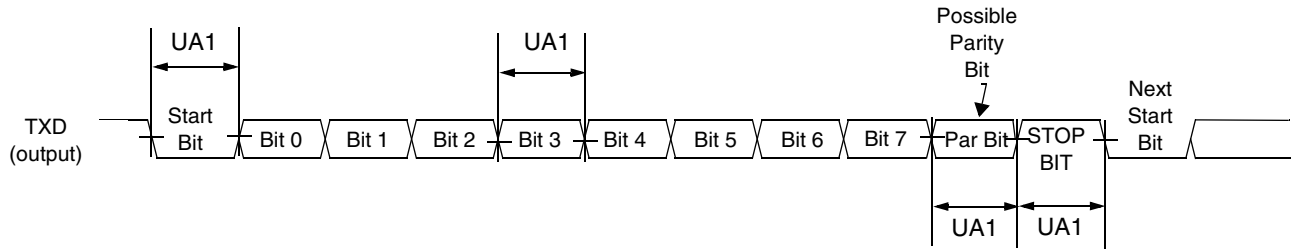


Figure 42. UART Transmit Timing Diagram

Table 62. UART Transmit Timing Parameters

| ID | Parameter | Symbol | Min | Max | Unit |
|-----|-------------------|------------|---------------------------------------|-----------------------------------|------|
| UA1 | Transmit Bit Time | t_{Tbit} | $1/F_{baud_rate}^1 - T_{ref_clk}^2$ | $1/F_{baud_rate} + T_{ref_clk}$ | — |

¹ F_{baud_rate} : Baud rate frequency. The maximum baud rate the UARTAPP can support is 3.25 Mbps. The maximum baud rate of DebugUART is 115.2 kbps.

² T_{ref_clk} : The period of UART reference clock ref_clk (which is APBX clock = 24 MHz).

3.5.15.2 UART Receive Timing

Figure 43 shows the UART receive timing, showing only eight data bits and one stop bit. Table 63 describes the timing parameter (UA2) shown in the figure.

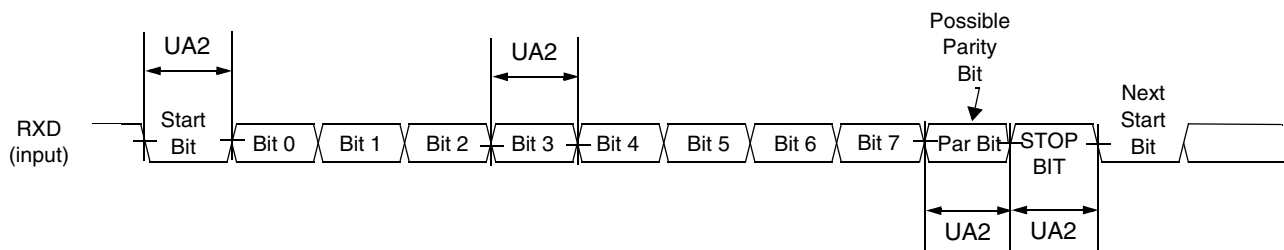


Figure 43. UART Receive Timing Diagram

Table 63. UART Receive Timing Parameters

| ID | Parameter | Symbol | Min | Max | Unit |
|-----|-------------------------------|------------|---|---|------|
| UA2 | Receive bit time ¹ | t_{Rbit} | $1/F_{baud_rate}^2 - 1/(16 \times F_{baud_rate})$ | $1/F_{baud_rate} + 1/(16 \times F_{baud_rate})$ | — |

¹ The UART receiver can tolerate $1/(16 \times F_{baud_rate})$ tolerance in each bit. But accumulation tolerance in one frame must not exceed $3/(16 \times F_{baud_rate})$.

² F_{baud_rate} : Baud rate frequency. The maximum baud rate the UARTAPP can support is 3.25 Mbps. The maximum baud rate of DebugUART is 115 kbps.

4 Package Information and Contact Assignments

4.1 Case MAPBGA-289, 14 x 14 mm, 0.8 mm Pitch

The following notes apply to [Figure 44](#):

- All dimensions are in millimeters.
- Dimensioning and tolerancing per ASME Y14.5M-1994.
- Maximum solder bump diameter measured parallel to datum A.
- Datum A, the seating plane, is determined by the spherical crowns of the solder bumps.
- Parallelism measurement excludes any effect of mark on top surface of package.

Figure 44 shows the i.MX28 production package.

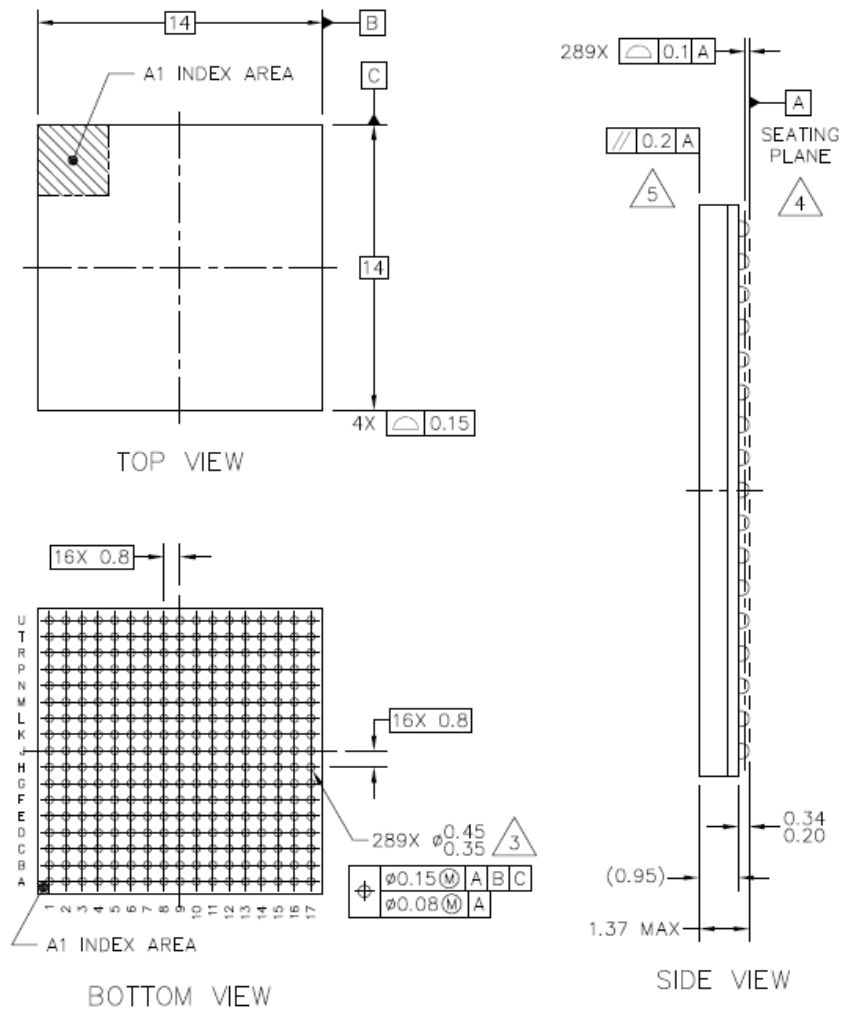


Figure 44. i.MX28 Production Package

4.2 Ground, Power, Sense, and Reference Contact Assignments

Table 64 shows power and ground contact assignments for the MAPBGA package.

Table 64. MAPBGA Power and Ground Contact Assignments

| Contact Name | Contact Assignment |
|--------------|---|
| VDDA1 | C13 |
| VDDD | G12,G11,F10,F11,K12,F12,G10 |
| VDDIO18 | G8,F9,F8,G9 |
| VDDIO33 | H8,J8,N3,G3,E6,J9,J10,A7,E16 |
| VDDIO33_EMI | N17 |
| VDDIO_EMI | P11,R13,N13,N15,G17,M12,M10,G13,M11,L13,G15 |

Table 64. MAPBGA Power and Ground Contact Assignments (continued)

| Contact Name | Contact Assignment |
|--------------|--|
| VDDIO_EMIQ | K15,J13,R15 |
| VDDXTAL | C12 |
| VSS | E15,L11,A1,K10,K11,J11,M14,H11,U1,H9,H12,H3,K9,C16,L10,H16,J12,H10,B7,E5,J15,A9,N4 |
| VSSA1 | B13 |
| VSSA2 | B11 |
| VSSIO_EMI | F16,R10,H14,M16,F14,L12,P16,U17,T14,P14,R12 |

4.3 Signal Contact Assignments

Table 65 lists the i.MX287 MAPBGA package signal contact assignments.

Table 65. i.MX287 MAPBGA Contact Assignments

| Signal Name | Contact Assignment | Signal Name | Contact Assignment | Signal Name | Contact Assignment |
|-------------|--------------------|--------------|--------------------|-------------|--------------------|
| AUART0_CTS | J6 | EMI_DQS1N | J16 | LCD_D17 | R3 |
| AUART0_RTS | J7 | EMI_ODT0 | R17 | LCD_D18 | U4 |
| AUART0_RX | G5 | EMI_ODT1 | T17 | LCD_D19 | T4 |
| AUART0_TX | H5 | EMI_RASN | R16 | LCD_D20 | R4 |
| AUART1_CTS | K5 | EMI_VREF0 | R14 | LCD_D21 | U5 |
| AUART1_RTS | J5 | EMI_VREF1 | K13 | LCD_D22 | T5 |
| AUART1_RX | L4 | EMI_WEN | T15 | LCD_D23 | R5 |
| AUART1_TX | K4 | ENET0_COL | J4 | LCD_DOTCLK | N1 |
| AUART2_CTS | H6 | ENET0_CRS | J3 | LCD_ENABLE | N5 |
| AUART2_RTS | H7 | ENET0_MDC | G4 | LCD_HSYNC | M1 |
| AUART2_RX | F6 | ENET0_MDIO | H4 | LCD_RD_E | P4 |
| AUART2_TX | F5 | ENET0_RXD0 | H1 | LCD_RESET | M6 |
| AUART3_CTS | L6 | ENET0_RXD1 | H2 | LCD_RS | M4 |
| AUART3_RTS | K6 | ENET0_RXD2 | J1 | LCD_VSYNC | L1 |
| AUART3_RX | M5 | ENET0_RXD3 | J2 | LCD_WR_RWN | K1 |
| AUART3_TX | L5 | ENET0_RX_CLK | F3 | LRADC0 | C15 |
| BATTERY | A15 | ENET0_RX_EN | E4 | LRADC1 | C9 |
| DCDC_BATT | B15 | ENET0_TXD0 | F1 | LRADC2 | C8 |
| DCDC_GND | A17 | ENET0_TXD1 | F2 | LRADC3 | D9 |
| DCDC_LN1 | B17 | ENET0_TXD2 | G1 | LRADC4 | D13 |
| DCDC_LP | A16 | ENET0_TXD3 | G2 | LRADC5 | D15 |

Table 65. i.MX287 MAPBGA Contact Assignments (continued)

| Signal Name | Contact Assignment | Signal Name | Contact Assignment | Signal Name | Contact Assignment |
|-------------|--------------------|--------------|--------------------|--------------|--------------------|
| DCDC_VDDA | B16 | ENET0_TX_CLK | E3 | LRADC6 | C14 |
| DCDC_VDDD | D17 | ENET0_TX_EN | F4 | PSWITCH | A11 |
| DCDC_VDDIO | C17 | ENET_CLK | E2 | PWM0 | K7 |
| DEBUG | B9 | GPMI_ALE | P6 | PWM1 | L7 |
| EMI_A00 | U15 | GPMI_CE0N | N7 | PWM2 | K8 |
| EMI_A01 | U12 | GPMI_CE1N | N9 | PWM3 | E9 |
| EMI_A02 | U14 | GPMI_CE2N | M7 | PWM4 | E10 |
| EMI_A03 | T11 | GPMI_CE3N | M9 | RESETN | A14 |
| EMI_A04 | U10 | GPMI_CLE | P7 | RTC_XTALI | D11 |
| EMI_A05 | R11 | GPMI_D00 | U8 | RTC_XTALO | C11 |
| EMI_A06 | R9 | GPMI_D01 | T8 | SAIF0_BITCLK | F7 |
| EMI_A07 | N11 | GPMI_D02 | R8 | SAIF0_LRCLK | G6 |
| EMI_A08 | U9 | GPMI_D03 | U7 | SAIF0_MCLK | G7 |
| EMI_A09 | P10 | GPMI_D04 | T7 | SAIF0_SDATA0 | E7 |
| EMI_A10 | U13 | GPMI_D05 | R7 | SAIF1_SDATA0 | E8 |
| EMI_A11 | T10 | GPMI_D06 | U6 | SPDIF | D7 |
| EMI_A12 | U11 | GPMI_D07 | T6 | SSP0_CMD | A4 |
| EMI_A13 | T9 | GPMI_RDN | R6 | SSP0_DATA0 | B6 |
| EMI_A14 | N10 | GPMI_RDY0 | N6 | SSP0_DATA1 | C6 |
| EMI_BA0 | T16 | GPMI_RDY1 | N8 | SSP0_DATA2 | D6 |
| EMI_BA1 | T12 | GPMI_RDY2 | M8 | SSP0_DATA3 | A5 |
| EMI_BA2 | N12 | GPMI_RDY3 | L8 | SSP0_DATA4 | B5 |
| EMI_CASN | U16 | GPMI_RESETN | L9 | SSP0_DATA5 | C5 |
| EMI_CE0N | P12 | GPMI_WRN | P8 | SSP0_DATA6 | D5 |
| EMI_CE1N | P9 | HSADC0 | B14 | SSP0_DATA7 | B4 |
| EMI_CKE | T13 | I2C0_SCL | C7 | SSP0_DETECT | D10 |
| EMI_CLK | L17 | I2C0_SDA | D8 | SSP0_SCK | A6 |
| EMI_CLKN | L16 | JTAG_RTCK | E14 | SSP1_CMD | C1 |
| EMI_D00 | N16 | JTAG_TCK | E11 | SSP1_DATA0 | D1 |
| EMI_D01 | M13 | JTAG_TDI | E12 | SSP1_DATA3 | E1 |
| EMI_D02 | P15 | JTAG_TDO | E13 | SSP1_SCK | B1 |
| EMI_D03 | N14 | JTAG_TMS | D12 | SSP2_MISO | B3 |

Table 65. i.MX287 MAPBGA Contact Assignments (continued)

| Signal Name | Contact Assignment | Signal Name | Contact Assignment | Signal Name | Contact Assignment |
|---------------------|--------------------|-------------|--------------------|-------------|--------------------|
| EMI_D04 | P13 | JTAG_TRST | D14 | SSP2_MOSI | C3 |
| EMI_D05 | P17 | LCD_CS | P5 | SSP2_SCK | A3 |
| EMI_D06 | L14 | LCD_D00 | K2 | SSP2_SS0 | C4 |
| EMI_D07 | M17 | LCD_D01 | K3 | SSP2_SS1 | D3 |
| EMI_D08 | G16 | LCD_D02 | L2 | SSP2_SS2 | D4 |
| EMI_D09 | H15 | LCD_D03 | L3 | SSP3_MISO | B2 |
| EMI_D10 | G14 | LCD_D04 | M2 | SSP3_MOSI | C2 |
| EMI_D11 | J14 | LCD_D05 | M3 | SSP3_SCK | A2 |
| EMI_D12 | H13 | LCD_D06 | N2 | SSP3_SS0 | D2 |
| EMI_D13 | H17 | LCD_D07 | P1 | TESTMODE | C10 |
| EMI_D14 | F13 | LCD_D08 | P2 | USB0DM | A10 |
| EMI_D15 | F17 | LCD_D09 | P3 | USB0DP | B10 |
| EMI_DDR_OPE N | K14 | LCD_D10 | R1 | USB1DM | B8 |
| EMI_DDR_OPE N_FB | L15 | LCD_D11 | R2 | USB1DP | A8 |
| EMI_DQM0 | M15 | LCD_D12 | T1 | VDD1P5 | D16 |
| EMI_DQM1 | F15 | LCD_D13 | T2 | VDD4P2 | A13 |
| EMI_DQS0 | K17 | LCD_D14 | U2 | VDD5V | E17 |
| EMI_DQS0N | K16 | LCD_D15 | U3 | XTALI | A12 |
| EMI_DQS1 | J17 | LCD_D16 | T3 | XTALO | B12 |

4.4 i.MX280 Ball Map

Table 66 shows the i.MX280 MAPBGA ball map.

Table 66. 289-Pin i.MX280 MAPBGA Ball Map

| | | | | | | | | | | | | | | | | | | |
|---|-----|----|----------|----------|------------|----------|---------|--------|-----|--------|---------|-------|--------|--------|---------|---------|----------|---|
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | |
| A | VSS | NC | SSP2_SCK | SSP0_CMD | SSP0_DATA3 | SSP0_SCK | VDDIO33 | USB1DP | VSS | USB0DM | PSWITCH | XTALI | VDD4P2 | RESETN | BATTERY | DCDC_LP | DCDC_GND | A |

Table 66. 289-Pin i.MX280 MAPBGA Ball Map (continued)

| K | J | H | G | F | E | D | C | B |
|--------------|------------|------------|-------------|--------------|--------------|-------------|------------|------------|
| ETM_TCLK | NC | ENET0_RXD0 | NC | ENET0_TXD0 | NC | NC | NC | NC |
| ETM_DA0 | NC | ENET0_RXD1 | NC | ENET0_TXD1 | ENET_CLK | NC | NC | NC |
| ETM_DA1 | NC | VSS | VDDIO33 | NC | NC | SSP2_SS1 | SSP2_MOSI | SSP2_MISO |
| AUART1_TX | NC | ENET0_MDIO | ENET0_MDC | ENET0_TX_EN | ENET0_RX_EN | SSP2_SS2 | SSP2_SS0 | SSP0_DATA7 |
| NC | NC | AUART0_TX | AUART0_RX | NC | VSS | SSP0_DATA6 | SSP0_DATA5 | SSP0_DATA4 |
| NC | AUART0_CTS | NC | SAIF0_LRCLK | NC | VDDIO33 | SSP0_DATA2 | SSP0_DATA1 | SSP0_DATA0 |
| PWM0 | AUART0_RTS | NC | SAIF0_MCLK | SAIF0_BITCLK | SAIF0_SDATA0 | NC | I2C0_SCL | VSS |
| PWM2 | VDDIO33 | VDDIO33 | VDDIO18 | VDDIO18 | SAIF1_SDATA0 | I2C0_SDA | LRADC2 | USB1DM |
| VSS | VDDIO33 | VSS | VDDIO18 | VDDIO18 | PWM3 | LRADC3 | LRADC1 | DEBUG |
| VSS | VDDIO33 | VSS | VDDD | VDDD | PWM4 | SSP0_DETECT | TESTMODE | USB0DP |
| VSS | VSS | VSS | VDDD | VDDD | JTAG_TCK | RTC_XTALI | RTC_XTALO | VSSA2 |
| VDDD | VSS | VSS | VDDD | VDDD | JTAG_TDI | JTAG_TMS | VDDXTAL | XTALO |
| EMI_VREF1 | VDDIO_EMIQ | EMI_D12 | VDDIO_EMI | EMI_D14 | JTAG_TDO | LRADC4 | VDDA1 | VSSA1 |
| EMI_DDR_OPEN | EMI_D11 | VSSIO_EMI | EMI_D10 | VSSIO_EMI | JTAG_RTCK | JTAG_TRST | LRADC6 | HSADC0 |
| VDDIO_EMIQ | VSS | EMI_D09 | VDDIO_EMI | EMI_DQM1 | VSS | LRADC5 | LRADC0 | DCDC_BATT |
| EMI_DQS0N | EMI_DQS1N | VSS | EMI_D08 | VSSIO_EMI | VDDIO33 | VDD1P5 | VSS | DCDC_VDDA |
| EMI_DQS0 | EMI_DQS1 | EMI_D13 | VDDIO_EMI | EMI_D15 | VDD5V | DCDC_VDDD | DCDC_VDDIO | DCDC_LN1 |
| K | J | H | G | F | E | D | C | B |

Table 66. 289-Pin i.MX280 MAPBGA Ball Map (continued)

| | U | T | R | P | N | M | L |
|----|-----------|-----------|------------|-----------|-------------|------------|-----------------|
| 1 | VSS | NC | NC | ETM_DA7 | NC | NC | NC |
| 2 | NC | NC | NC | NC | ETM_DA6 | ETM_DA4 | ETM_DA2 |
| 3 | NC | NC | NC | NC | VDDIO33 | ETM_DA5 | ETM_DA3 |
| 4 | NC | NC | NC | ETM_TCTL | VSS | GPIO_B1P26 | AUART1_RX |
| 5 | NC | NC | NC | NC | NC | NC | NC |
| 6 | GPMI_D06 | GPMI_D07 | GPMI_RDN | GPMI_ALE | GPMI_RDY0 | NC | NC |
| 7 | GPMI_D03 | GPMI_D04 | GPMI_D05 | GPMI_CLE | GPMI_CE0N | NC | PWM1 |
| 8 | GPMI_D00 | GPMI_D01 | GPMI_D02 | GPMI_WRN | GPMI_RDY1 | NC | NC |
| 9 | EMI_A08 | EMI_A13 | EMI_A06 | EMI_CE1N | GPMI_CE1N | NC | GPMI_RESETN |
| 10 | EMI_A04 | EMI_A11 | VSSIO_EMI | EMI_A09 | EMI_A14 | VDDIO_EMI | VSS |
| 11 | EMI_A12 | EMI_A03 | EMI_A05 | VDDIO_EMI | EMI_A07 | VDDIO_EMI | VSS |
| 12 | EMI_A01 | EMI_BA1 | VSSIO_EMI | EMI_CE0N | EMI_BA2 | VDDIO_EMI | VSSIO_EMI |
| 13 | EMI_A10 | EMI_CKE | VDDIO_EMI | EMI_D04 | VDDIO_EMI | EMI_D01 | VDDIO_EMI |
| 14 | EMI_A02 | VSSIO_EMI | EMI_VREF0 | VSSIO_EMI | EMI_D03 | VSS | EMI_D06 |
| 15 | EMI_A00 | EMI_WEN | VDDIO_EMIQ | EMI_D02 | VDDIO_EMI | EMI_DQM0 | EMI_DDR_OPEN_FB |
| 16 | EMI_CASN | EMI_BA0 | EMI_RASN | VSSIO_EMI | EMI_D00 | VSSIO_EMI | EMI_CLKN |
| 17 | VSSIO_EMI | EMI_ODT1 | EMI_ODT0 | EMI_D05 | VDDIO33_EMI | EMI_D07 | EMI_CLK |
| | U | T | R | P | N | M | L |

4.5 i.MX283 Ball Map

Table 67 shows the i.MX283 MAPBGA ball map.

Table 67. 289-Pin i.MX283 MAPBGA Ball Map

| | | | | | | | | | | | | | | | | | | |
|---|-----|----|----------|----------|------------|----------|---------|--------|-----|--------|---------|-------|--------|--------|---------|---------|----------|---|
| A | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | A |
| | VSS | NC | SSP2_SCK | SSP0_CMD | SSP0_DATA3 | SSP0_SCK | VDDIO33 | USB1DP | VSS | USB0DM | PSWITCH | XTALI | VDD4P2 | RESETN | BATTERY | DCDC_LP | DCDC_GND | |

Table 67. 289-Pin i.MX283 MAPBGA Ball Map (continued)

| K | J | H | G | F | E | D | C | B |
|--------------|------------|------------|-------------|--------------|--------------|-------------|------------|------------|
| LCD_WR_RWN | NC | ENET0_RXD0 | NC | ENET0_TXD0 | NC | NC | NC | NC |
| LCD_D00 | NC | ENET0_RXD1 | NC | ENET0_TXD1 | ENET_CLK | NC | NC | NC |
| LCD_D01 | NC | VSS | VDDIO33 | NC | NC | SSP2_SS1 | SSP2_MOSI | SSP2_MISO |
| AUART1_TX | NC | ENET0_MDIO | ENET0_MDC | ENET0_TX_EN | ENET0_RX_EN | SSP2_SS2 | SSP2_SS0 | SSP0_DATA7 |
| NC | NC | AUART0_TX | AUART0_RX | NC | VSS | SSP0_DATA6 | SSP0_DATA5 | SSP0_DATA4 |
| NC | AUART0_CTS | NC | SAIF0_LRCLK | NC | VDDIO33 | SSP0_DATA2 | SSP0_DATA1 | SSP0_DATA0 |
| PWM0 | AUART0_RTS | NC | SAIF0_MCLK | SAIF0_BITCLK | SAIF0_SDATA0 | NC | I2C0_SCL | VSS |
| PWM2 | VDDIO33 | VDDIO33 | VDDIO18 | VDDIO18 | SAIF1_SDATA0 | I2C0_SDA | LRADC2 | USB1DM |
| VSS | VDDIO33 | VSS | VDDIO18 | VDDIO18 | PWM3 | LRADC3 | LRADC1 | DEBUG |
| VSS | VDDIO33 | VSS | VDDD | VDDD | PWM4 | SSP0_DETECT | TESTMODE | USB0DP |
| VSS | VSS | VSS | VDDD | VDDD | JTAG_TCK | RTC_XTALI | RTC_XTALO | VSSA2 |
| VDDD | VSS | VSS | VDDD | VDDD | JTAG_TDI | JTAG_TMS | VDDXTAL | XTALO |
| EMI_VREF1 | VDDIO_EMIQ | EMI_D12 | VDDIO_EMI | EMI_D14 | JTAG_TDO | LRADC4 | VDDA1 | VSSA1 |
| EMI_DDR_OPEN | EMI_D11 | VSSIO_EMI | EMI_D10 | VSSIO_EMI | JTAG_RTCK | JTAG_TRST | LRADC6 | HSADC0 |
| VDDIO_EMIQ | VSS | EMI_D09 | VDDIO_EMI | EMI_DQM1 | VSS | LRADC5 | LRADC0 | DCDC_BATT |
| EMI_DQS0N | EMI_DQS1N | VSS | EMI_D08 | VSSIO_EMI | VDDIO33 | VDD1P5 | VSS | DCDC_VDDA |
| EMI_DQS0 | EMI_DQS1 | EMI_D13 | VDDIO_EMI | EMI_D15 | VDD5V | DCDC_VDDD | DCDC_VDDIO | DCDC_LN1 |
| K | J | H | G | F | E | D | C | B |

Table 67. 289-Pin i.MX283 MAPBGA Ball Map (continued)

| | U | T | R | P | N | M | L |
|----|-----------|-----------|------------|-----------|-------------|-----------|-----------------|
| 1 | VSS | LCD_D12 | LCD_D10 | LCD_D07 | NC | NC | NC |
| 2 | LCD_D14 | LCD_D13 | LCD_D11 | LCD_D08 | LCD_D06 | LCD_D04 | LCD_D02 |
| 3 | LCD_D15 | LCD_D16 | LCD_D17 | LCD_D09 | VDDIO33 | LCD_D05 | LCD_D03 |
| 4 | LCD_D18 | LCD_D19 | LCD_D20 | LCD_RD_E | VSS | LCD_RS | AUART1_RX |
| 5 | LCD_D21 | LCD_D22 | LCD_D23 | LCD_CS | NC | NC | NC |
| 6 | GPMI_D06 | GPMI_D07 | GPMI_RDN | GPMI_ALE | GPMI_RDY0 | LCD_RESET | NC |
| 7 | GPMI_D03 | GPMI_D04 | GPMI_D05 | GPMI_CLE | GPMI_CEO0 | NC | PWM1 |
| 8 | GPMI_D00 | GPMI_D01 | GPMI_D02 | GPMI_WRN | GPMI_RDY1 | NC | NC |
| 9 | EMI_A08 | EMI_A13 | EMI_A06 | EMI_CE1N | GPMI_CE1N | NC | GPMI_RESETN |
| 10 | EMI_A04 | EMI_A11 | VSSIO_EMI | EMI_A09 | EMI_A14 | VDDIO_EMI | VSS |
| 11 | EMI_A12 | EMI_A03 | EMI_A05 | VDDIO_EMI | EMI_A07 | VDDIO_EMI | VSS |
| 12 | EMI_A01 | EMI_BA1 | VSSIO_EMI | EMI_CE0N | EMI_BA2 | VDDIO_EMI | VSSIO_EMI |
| 13 | EMI_A10 | EMI_CKE | VDDIO_EMI | EMI_D04 | VDDIO_EMI | EMI_D01 | VDDIO_EMI |
| 14 | EMI_A02 | VSSIO_EMI | EMI_VREF0 | VSSIO_EMI | EMI_D03 | VSS | EMI_D06 |
| 15 | EMI_A00 | EMI_WEN | VDDIO_EMIQ | EMI_D02 | VDDIO_EMI | EMI_DQM0 | EMI_DDR_OPEN_FB |
| 16 | EMI_CASN | EMI_BA0 | EMI_RASN | VSSIO_EMI | EMI_D00 | VSSIO_EMI | EMI_CLKN |
| 17 | VSSIO_EMI | EMI_ODT1 | EMI_ODT0 | EMI_D05 | VDDIO33_EMI | EMI_D07 | EMI_CLK |
| | U | T | R | P | N | M | L |

4.6 i.MX286 Ball Map

Table 68 shows the i.MX286 MAPBGA ball map.

Table 68. 289-Pin i.MX286 MAPBGA Ball Map

| | | | | | | | | | | | | | | | | | | |
|---|-----|----|----------|----------|------------|----------|---------|--------|-----|--------|---------|-------|--------|--------|---------|---------|----------|---|
| A | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | A |
| | VSS | NC | SSP2_SCK | SSP0_CMD | SSP0_DATA3 | SSP0_SCK | VDDIO33 | USB1DP | VSS | USB0DM | PSWITCH | XTALI | VDD4P2 | RESETN | BATTERY | DCDC_LP | DCDC_GND | |

Table 68. 289-Pin i.MX286 MAPBGA Ball Map (continued)

| K | J | H | G | F | E | D | C | B |
|--------------|------------|------------|-------------|--------------|--------------|-------------|------------|------------|
| LCD_WR_RWN | NC | ENET0_RXD0 | NC | ENET0_TXD0 | NC | NC | NC | NC |
| LCD_D00 | NC | ENET0_RXD1 | NC | ENET0_TXD1 | ENET_CLK | NC | NC | NC |
| LCD_D01 | NC | VSS | VDDIO33 | NC | NC | SSP2_SS1 | SSP2_MOSI | SSP2_MISO |
| AUART1_TX | NC | ENET0_MDIO | ENET0_MDC | ENET0_TX_EN | ENET0_RX_EN | SSP2_SS2 | SSP2_SS0 | SSP0_DATA7 |
| NC | NC | AUART0_TX | AUART0_RX | NC | VSS | SSP0_DATA6 | SSP0_DATA5 | SSP0_DATA4 |
| NC | AUART0_CTS | NC | SAIF0_LRCLK | NC | VDDIO33 | SSP0_DATA2 | SSP0_DATA1 | SSP0_DATA0 |
| PWM0 | AUART0_RTS | NC | SAIF0_MCLK | SAIF0_BITCLK | SAIF0_SDATA0 | SPDIF | I2C0_SCL | VSS |
| PWM2 | VDDIO33 | VDDIO33 | VDDIO18 | VDDIO18 | SAIF1_SDATA0 | I2C0_SDA | LRADC2 | USB1DM |
| VSS | VDDIO33 | VSS | VDDIO18 | VDDIO18 | PWM3 | LRADC3 | LRADC1 | DEBUG |
| VSS | VDDIO33 | VSS | VDDD | VDDD | PWM4 | SSP0_DETECT | TESTMODE | USB0DP |
| VSS | VSS | VSS | VDDD | VDDD | JTAG_TCK | RTC_XTALI | RTC_XTALO | VSSA2 |
| VDDD | VSS | VSS | VDDD | VDDD | JTAG_TDI | JTAG_TMS | VDDXTAL | XTALO |
| EMI_VREF1 | VDDIO_EMIQ | EMI_D12 | VDDIO_EMI | EMI_D14 | JTAG_TDO | LRADC4 | VDDA1 | VSSA1 |
| EMI_DDR_OPEN | EMI_D11 | VSSIO_EMI | EMI_D10 | VSSIO_EMI | JTAG_RTCK | JTAG_TRST | LRADC6 | HSADC0 |
| VDDIO_EMIQ | VSS | EMI_D09 | VDDIO_EMI | EMI_DQM1 | VSS | LRADC5 | LRADC0 | DCDC_BATT |
| EMI_DQS0N | EMI_DQS1N | VSS | EMI_D08 | VSSIO_EMI | VDDIO33 | VDD1P5 | VSS | DCDC_VDDA |
| EMI_DQS0 | EMI_DQS1 | EMI_D13 | VDDIO_EMI | EMI_D15 | VDD5V | DCDC_VDDD | DCDC_VDDIO | DCDC_LN1 |
| K | J | H | G | F | E | D | C | B |

Table 68. 289-Pin i.MX286 MAPBGA Ball Map (continued)

| | U | T | R | P | N | M | L |
|----|-----------|-----------|------------|-----------|-------------|-----------|-----------------|
| 1 | VSS | LCD_D12 | LCD_D10 | LCD_D07 | NC | NC | NC |
| 2 | LCD_D14 | LCD_D13 | LCD_D11 | LCD_D08 | LCD_D06 | LCD_D04 | LCD_D02 |
| 3 | LCD_D15 | LCD_D16 | LCD_D17 | LCD_D09 | VDDIO33 | LCD_D05 | LCD_D03 |
| 4 | LCD_D18 | LCD_D19 | LCD_D20 | LCD_RD_E | VSS | LCD_RS | AUART1_RX |
| 5 | LCD_D21 | LCD_D22 | LCD_D23 | LCD_CS | NC | NC | NC |
| 6 | GPMI_D06 | GPMI_D07 | GPMI_RDN | GPMI_ALE | GPMI_RDY0 | LCD_RESET | NC |
| 7 | GPMI_D03 | GPMI_D04 | GPMI_D05 | GPMI_CLE | GPMI_CE0N | GPMI_CE2N | PWM1 |
| 8 | GPMI_D00 | GPMI_D01 | GPMI_D02 | GPMI_WRN | GPMI_RDY1 | GPMI_RDY2 | GPMI_RDY3 |
| 9 | EMI_A08 | EMI_A13 | EMI_A06 | EMI_CE1N | GPMI_CE1N | GPMI_CE3N | GPMI_RESETN |
| 10 | EMI_A04 | EMI_A11 | VSSIO_EMI | EMI_A09 | EMI_A14 | VDDIO_EMI | VSS |
| 11 | EMI_A12 | EMI_A03 | EMI_A05 | VDDIO_EMI | EMI_A07 | VDDIO_EMI | VSS |
| 12 | EMI_A01 | EMI_BA1 | VSSIO_EMI | EMI_CE0N | EMI_BA2 | VDDIO_EMI | VSSIO_EMI |
| 13 | EMI_A10 | EMI_CKE | VDDIO_EMI | EMI_D04 | VDDIO_EMI | EMI_D01 | VDDIO_EMI |
| 14 | EMI_A02 | VSSIO_EMI | EMI_VREF0 | VSSIO_EMI | EMI_D03 | VSS | EMI_D06 |
| 15 | EMI_A00 | EMI_WEN | VDDIO_EMIQ | EMI_D02 | VDDIO_EMI | EMI_DQM0 | EMI_DDR_OPEN_FB |
| 16 | EMI_CASN | EMI_BA0 | EMI_RASN | VSSIO_EMI | EMI_D00 | VSSIO_EMI | EMI_CLKN |
| 17 | VSSIO_EMI | EMI_ODT1 | EMI_ODT0 | EMI_D05 | VDDIO33_EMI | EMI_D07 | EMI_CLK |
| | U | T | R | P | N | M | L |

4.7 i.MX287 Ball Map

Table 69 shows the i.MX287 MAPBGA Ball Map.

Table 69. 289-Pin i.MX287 MAPBGA Ball Map

| | | | | | | | | | | | | | | | | | | |
|---|-----|----------|----------|----------|------------|----------|---------|--------|-----|--------|---------|-------|--------|--------|---------|---------|----------|---|
| A | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | A |
| | VSS | SSP3_SCK | SSP2_SCK | SSP0_CMD | SSP0_DATA3 | SSP0_SCK | VDDIO33 | USB1DP | VSS | USB0DM | PSWITCH | XTALI | VDD4P2 | RESETN | BATTERY | DCDC_LP | DCDC_GND | |

Table 69. 289-Pin i.MX287 MAPBGA Ball Map (continued)

| K | J | H | G | F | E | D | C | B |
|--------------|------------|------------|-------------|--------------|--------------|-------------|------------|------------|
| LCD_WR_RWN | ENET0_RXD2 | ENET0_RXD0 | ENET0_TXD2 | ENET0_TXD0 | SSP1_DATA3 | SSP1_DATA0 | SSP1_CMD | SSP1_SCK |
| LCD_D00 | ENET0_RXD3 | ENET0_RXD1 | ENET0_TXD3 | ENET0_TXD1 | ENET_CLK | SSP3_SS0 | SSP3_MOSI | SSP3_MISO |
| LCD_D01 | ENET0_CRS | VSS | VDDIO33 | ENET0_RX_CLK | ENET0_TX_CLK | SSP2_SS1 | SSP2_MOSI | SSP2_MISO |
| AUART1_TX | ENET0_COL | ENET0_MDIO | ENET0_MDC | ENET0_TX_EN | ENET0_RX_EN | SSP2_SS2 | SSP2_SS0 | SSP0_DATA7 |
| AUART1_CTS | AUART1_RTS | AUART0_TX | AUART0_RX | AUART2_TX | VSS | SSP0_DATA6 | SSP0_DATA5 | SSP0_DATA4 |
| AUART3_RTS | AUART0_CTS | AUART2_CTS | SAIF0_LRCLK | AUART2_RX | VDDIO33 | SSP0_DATA2 | SSP0_DATA1 | SSP0_DATA0 |
| PWM0 | AUART0_RTS | AUART2_RTS | SAIF0_MCLK | SAIF0_BITCLK | SAIF0_SDATA0 | SPDIF | I2C0_SCL | VSS |
| PWM2 | VDDIO33 | VDDIO33 | VDDIO18 | VDDIO18 | SAIF1_SDATA0 | I2C0_SDA | LRADC2 | USB1DM |
| VSS | VDDIO33 | VSS | VDDIO18 | VDDIO18 | PWM3 | LRADC3 | LRADC1 | DEBUG |
| VSS | VDDIO33 | VSS | VDDD | VDDD | PWM4 | SSP0_DETECT | TESTMODE | USB0DP |
| VSS | VSS | VSS | VDDD | VDDD | JTAG_TCK | RTC_XTALI | RTC_XTALO | VSSA2 |
| VDDD | VSS | VSS | VDDD | VDDD | JTAG_TDI | JTAG_TMS | VDDXTAL | XTALO |
| EMI_VREF1 | VDDIO_EMIQ | EMI_D12 | VDDIO_EMI | EMI_D14 | JTAG_TDO | LRADC4 | VDDA1 | VSSA1 |
| EMI_DDR_OPEN | EMI_D11 | VSSIO_EMI | EMI_D10 | VSSIO_EMI | JTAG_RTCK | JTAG_TRST | LRADC6 | HSADC0 |
| VDDIO_EMIQ | VSS | EMI_D09 | VDDIO_EMI | EMI_DQM1 | VSS | LRADC5 | LRADC0 | DCDC_BATT |
| EMI_DQS0N | EMI_DQS1N | VSS | EMI_D08 | VSSIO_EMI | VDDIO33 | VDD1P5 | VSS | DCDC_VDDA |
| EMI_DQS0 | EMI_DQS1 | EMI_D13 | VDDIO_EMI | EMI_D15 | VDD5V | DCDC_VDDD | DCDC_VDDIO | DCDC_LN1 |
| K | J | H | G | F | E | D | C | B |

Table 69. 289-Pin i.MX287 MAPBGA Ball Map (continued)

| | U | T | R | P | N | M | L |
|----|-----------|-----------|------------|-----------|-------------|-----------|-----------------|
| 1 | VSS | LCD_D12 | LCD_D10 | LCD_D07 | LCD_DOTCLK | LCD_HSYNC | LCD_VSYNC |
| 2 | LCD_D14 | LCD_D13 | LCD_D11 | LCD_D08 | LCD_D06 | LCD_D04 | LCD_D02 |
| 3 | LCD_D15 | LCD_D16 | LCD_D17 | LCD_D09 | VDDIO33 | LCD_D05 | LCD_D03 |
| 4 | LCD_D18 | LCD_D19 | LCD_D20 | LCD_RD_E | VSS | LCD_RS | AUART1_RX |
| 5 | LCD_D21 | LCD_D22 | LCD_D23 | LCD_CS | LCD_ENABLE | AUART3_RX | AUART3_TX |
| 6 | GPMI_D06 | GPMI_D07 | GPMI_RDN | GPMI_ALE | GPMI_RDY0 | LCD_RESET | AUART3_CTS |
| 7 | GPMI_D03 | GPMI_D04 | GPMI_D05 | GPMI_CLE | GPMI_CE0N | GPMI_CE2N | PWM1 |
| 8 | GPMI_D00 | GPMI_D01 | GPMI_D02 | GPMI_WRN | GPMI_RDY1 | GPMI_RDY2 | GPMI_RDY3 |
| 9 | EMI_A08 | EMI_A13 | EMI_A06 | EMI_CE1N | GPMI_CE1N | GPMI_CE3N | GPMI_RESETN |
| 10 | EMI_A04 | EMI_A11 | VSSIO_EMI | EMI_A09 | EMI_A14 | VDDIO_EMI | VSS |
| 11 | EMI_A12 | EMI_A03 | EMI_A05 | VDDIO_EMI | EMI_A07 | VDDIO_EMI | VSS |
| 12 | EMI_A01 | EMI_BA1 | VSSIO_EMI | EMI_CE0N | EMI_BA2 | VDDIO_EMI | VSSIO_EMI |
| 13 | EMI_A10 | EMI_CKE | VDDIO_EMI | EMI_D04 | VDDIO_EMI | EMI_D01 | VDDIO_EMI |
| 14 | EMI_A02 | VSSIO_EMI | EMI_VREF0 | VSSIO_EMI | EMI_D03 | VSS | EMI_D06 |
| 15 | EMI_A00 | EMI_WEN | VDDIO_EMIQ | EMI_D02 | VDDIO_EMI | EMI_DQM0 | EMI_DDR_OPEN_FB |
| 16 | EMI_CASN | EMI_BA0 | EMI_RASN | VSSIO_EMI | EMI_D00 | VSSIO_EMI | EMI_CLKN |
| 17 | VSSIO_EMI | EMI_ODT1 | EMI_ODT0 | EMI_D05 | VDDIO33_EMI | EMI_D07 | EMI_CLK |
| | U | T | R | P | N | M | L |

5 Revision History

Table 70 summarizes revisions to this document.

Table 70. Document Revision History

| Rev. Number | Date | Substantive Change(s) |
|-------------|---------|---|
| Rev. 4 | 10/2018 | <ul style="list-style-type: none"> • Table 1, "Ordering Information," on page 3: Added "C" suffix part numbers. • Table 37, "LPDDR1 Input AC Timing," on page 33: Corrected table title from "DDR2" to "LPDDR1" Input AC Timing. |
| Rev. 3 | 07/2012 | <ul style="list-style-type: none"> • Removed the Power Consumption table, and added Table 12, "Run IDD Test Case," on page 14. • Updated Table 23, "ON Impedance of EMI Drivers for Different Drive Strengths," on page 20. |
| Rev. 2 | 03/2012 | <ul style="list-style-type: none"> • In Section 1.1, "Device Features:" <ul style="list-style-type: none"> —Updated synchronous serial ports (SSP) support for the i.MX28 —Updated Ethernet support for the i.MX28 —Updated Low-Resolution A/D Converter (LRADC) support for the i.MX28 • Updated Table 2, "i.MX28 Functional Differences," on page 4. • In Table 6, "DC Absolute Maximum Ratings," on page 12, removed the PSWITCH parameter as this parameter is explained in detail in Table 11. • In Table 8, "Recommended Power Supply Operating Conditions," on page 12: <ul style="list-style-type: none"> —Updated two parameters: "VDD5V Supply Voltage" and "Offstate Current" —Updated the third footnote • In Table 9, "Operating Temperature Conditions," on page 13, added a new footnote in the "Parameter" column. • In Table 13, "Power Supply Characteristics," on page 15, updated the "VDD4P2 Output Current Limit Accuracy" parameter. • In Section 3.1.2.1, "Recommended Operating Conditions for Specific Clock Targets:" <ul style="list-style-type: none"> —Removed the "System Clocks" table —Updated two TBD values in the first row of Table 14 —Removed the first row in Table 15 —Removed the first row in Table 16 • In Table 20, "Power Mode Settings," on page 17, changed the second column name from "Deep Sleep" to "Offstate." • Updated Table 22, "EMI Digital Pin DC Characteristics," on page 19. • In Table 30, "LRADC Electrical Specifications," on page 27, updated the "DC Electrical Specification" section. • In Table 31, "HSADC Electrical Specification," on page 27, updated the "DC Electrical Specification" section. • In Section 3.5.5, "Coresight ETM9 AC Interface Timing," updated the first paragraph. • In Section 3.5.5.1, "TRACECLK Timing," corrected the title of Table 43. • In Section 3.5.5.2, "Trace Data Signal Timing," corrected the titles of Figure 15 and Table 44. |

Table 70. Document Revision History (continued)

| Rev. Number | Date | Substantive Change(s) |
|-------------|---------|---|
| Rev. 1 | 04/2011 | <ul style="list-style-type: none"> • Updated Section 1.1, "Device Features." • Added Section 3.2, "Thermal Characteristics." • In Table 1, "Ordering Information," on page 3, added two rows. • Updated Table 2, "i.MX28 Functional Differences," on page 4. • Updated Table 4, "i.MX28 Digital and Analog Modules," on page 7. • In Table 8, "Recommended Power Supply Operating Conditions," on page 12, updated BATT row. • Updated Table 9, "Operating Temperature Conditions," on page 13. • Replaced the term "DC Characteristics" with "Power Consumption" in the title and introduction of the Power Consumption table. Also changed Dissipation to Consumption in first row. • Updated Table 25, "Digital Pin DC Characteristics for GPIO in 3.3-V Mode," on page 21. • Updated Table 26, "Digital Pin DC Characteristics for GPIO in 1.8 V Mode," on page 22. • Updated and added a footnote to Table 33, "Ethernet PLL Specifications," on page 29. • Updated DDR1 row of Table 34, "EMI Command/Address AC Timing," on page 30. • Added Section 4.4, "i.MX280 Ball Map." • In Section 4.5, "i.MX283 Ball Map," updated Figure 67. |
| Rev. 0 | 09/2010 | Initial release. |

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