Industrial DDR3 1333 SO-DIMM Information

Part Number	Capacity	Organization	Rank	Height	DIMM type	Note
TS256MSK64V3N-I	2GB	256Mx8	1	30.00mm	SO-DIMM	anti-sulfur

Features

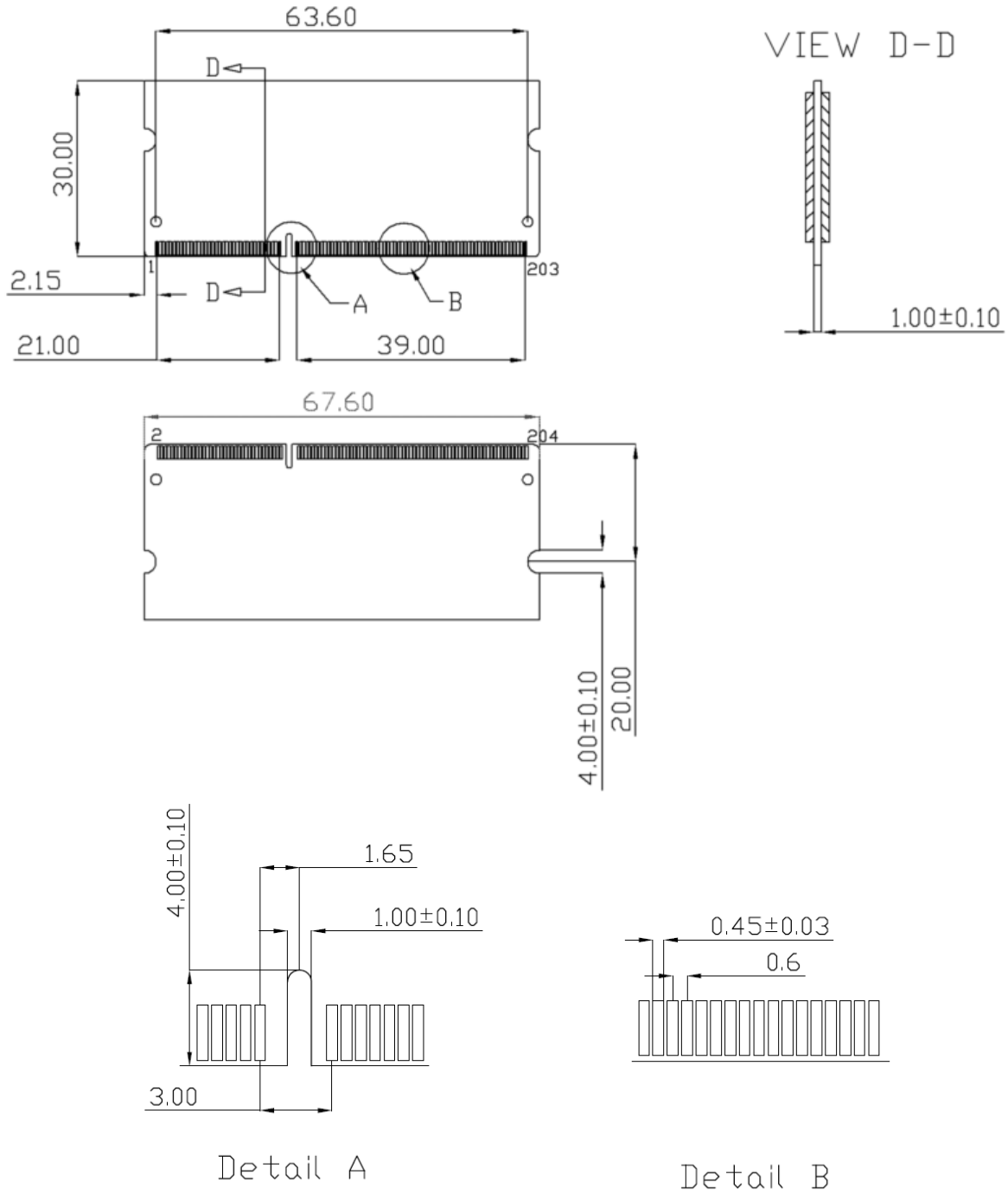
1. Operating Temperature : -40°C to +85°C
2. RoHS compliant products.
3. JEDEC standard 1.5V ± 0.075V Power supply
4. VDDQ=1.5V ± 0.075V
5. Clock Freq: 667MHZ for 1333Mb/s/Pin.
6. Programmable CAS Latency: 5, 6, 7, 8, 9
7. Programmable Additive Latency (Posted /CAS): 0,CL-2 or CL-1 clock
8. Programmable /CAS Write Latency (CWL) = 7(DDR3-1333)
9. 8 bit pre-fetch
10. Burst Length: 4, 8
11. Bi-directional Differential Data-Strobe
12. Internal calibration through ZQ pin
13. On Die Termination with ODT pin
14. Serial presence detect with EEPROM
15. Asynchronous reset

Pin Description

Pin Name	Description
A0~A14, BA0~BA2	Address/Bank input
DQ0~DQ63	Data Input / Output
DQS0~DQS7	Data strobes
/DQS0~/DQS7	Differential Data strobes
CK0, /CK0, CK1, /CK1	Clock Input. (Differential pair)
CKE0, CKE1	Clock Enable Input.
ODT0, ODT1	On-die termination control line
/CS0, /CS1	DIMM Rank Select Lines.
/RAS	Row Address Strobe
/CAS	Column Address Strobe
/WE	Write Enable
DM0~DM7	Data masks/high data strobes
VDD	Voltage power supply
VREFDQ/ VREFCA	Power Supply for Reference
VDDSPD	SPD EEPROM Power Supply
SA0~SA2	I2C serial bus address select for EEPROM
SCL	I2C serial bus clock for EEPROM
SDA	I2C serial bus data for EEPROM
VSS	Ground
/RESET	Set DRAMs Known State
VTT	SDRAM I/O termination supply
NC	No Connection

Dimensions (Unit: millimeter):

TS256MSK64V3N-I



Note:

1. Tolerances on all dimensions +/-0.15mm unless otherwise specified.

Pin Assignments

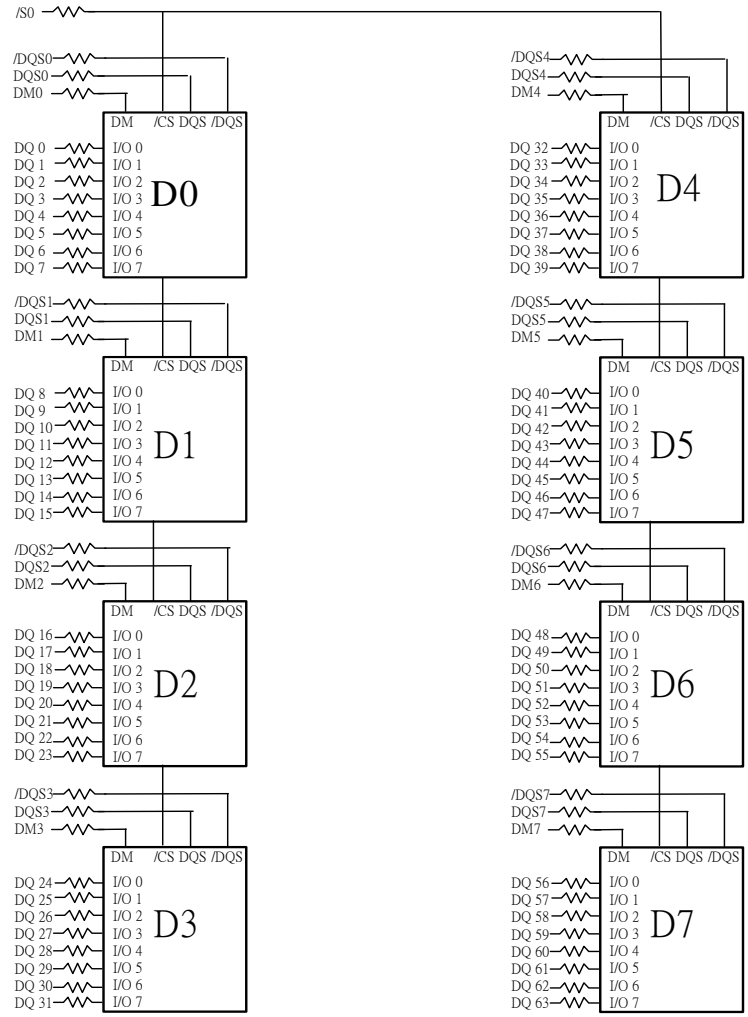
TS256MSK64V3N-I

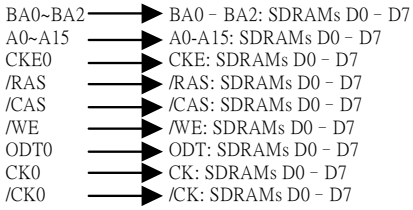
Front Side		Back Side		Front Side		Back Side		Front Side		Back Side	
No.	Name	No.	Name	No.	Name	No.	Name	No.	Name	No.	Name
1	VREFDQ	2	VSS	69	DQ27	70	DQ31	137	DQS4	138	VSS
3	VSS	4	DQ4	71	VSS	72	VSS	139	VSS	140	DQ38
5	DQ0	6	DQ5	73	CKE0	74	CKE1,NC	141	DQ34	142	DQ39
7	DQ1	8	VSS	75	VDD	76	VDD	143	DQ35	144	VSS
9	VSS	10	/DQS0	77	NC	78	A15,NC	145	VSS	146	DQ44
11	DM0	12	DQS0	79	BA2	80	A14	147	DQ40	148	DQ45
13	VSS	14	VSS	81	VDD	82	VDD	149	DQ41	150	VSS
15	DQ2	16	DQ6	83	A12,/BC	84	A11	151	VSS	152	/DQS5
17	DQ3	18	DQ7	85	A9	86	A7	153	DM5	154	DQS5
19	VSS	20	VSS	87	VDD	88	VDD	155	VSS	156	VSS
21	DQ8	22	DQ12	89	A8	90	A6	157	DQ42	158	DQ46
23	DQ9	24	DQ13	91	A5	92	A4	159	DQ43	160	DQ47
25	VSS	26	VSS	93	VDD	94	VDD	161	VSS	162	VSS
27	/DQS1	28	DM1	95	A3	96	A2	163	DQ48	164	DQ52
29	DQS1	30	/RESET	97	A1	98	A0	165	DQ49	166	DQ53
31	VSS	32	VSS	99	VDD	100	VDD	167	VSS	168	VSS
33	DQ10	34	DQ14	101	CK0	102	CK1	169	/DQS6	170	DM6
35	DQ11	36	DQ15	103	/CK0	104	/CK1	171	DQS6	172	VSS
37	VSS	38	VSS	105	VDD	106	VDD	173	VSS	174	DQ54
39	DQ16	40	DQ20	107	A10/AP	108	BA1	175	DQ50	176	DQ55
41	DQ17	42	DQ21	109	BA0	110	/RAS	177	DQ51	178	VSS
43	VSS	44	VSS	111	VDD	112	VDD	179	VSS	180	DQ60
45	/DQS2	46	DM2	113	/WE	114	/CS0	181	DQ56	182	DQ61
47	DQS2	48	VSS	115	/CAS	116	ODT0	183	DQ57	184	VSS
49	VSS	50	DQ22	117	VDD	118	VDD	185	VSS	186	/DQS7
51	DQ18	52	DQ23	119	A13	120	ODT1,NC	187	DM7	188	DQS7
53	DQ19	54	VSS	121	/S1,NC	122	NC	189	VSS	190	VSS
55	VSS	56	DQ28	123	VDD	124	VDD	191	DQ58	192	DQ62
57	DQ24	58	DQ29	125	TEST	126	VREFCA	193	DQ59	194	DQ63
59	DQ25	60	VSS	127	VSS	128	VSS	195	VSS	196	VSS
61	VSS	62	/DQS3	129	DQ32	130	DQ36	197	SA0	198	/EVENT
63	DM3	64	DQS3	131	DQ33	132	DQ37	199	VDDSPD	200	SDA
65	VSS	66	VSS	133	VSS	134	VSS	201	SA1	202	SCL
67	DQ26	68	DQ30	135	/DQS4	136	DM4	203	VTT	204	VTT

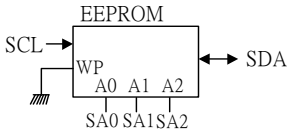
CK1 and /CK1: Used for dual-rank SO-DIMMs; not used on single-rank SO-DIMMs but terminated.
S1, ODT1, CKE1: Used for dual-rank SO-DIMMs; NC on single-rank SO-DIMMs.
A15: NC on some Raw Cards.
TEST: Reserved for bus analysis probes and is NC on normal memory modules.

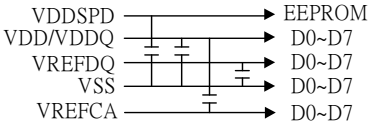
Block Diagram

2GB, 256Mx64 Module(1 Rank x8) TS256MSK64V3N-I









NOTE:

1. DQ-to-I/O wiring is shown as recommended but may be changed.
2. DQ,DQS,/DQS,ODT,DM,CKE,/S relationships must be maintained as shown.
3. DQ,DM,DQS,/DQS resistors: Refer to associated topology diagram.

This technical information is based on industry standard data and tests believed to be reliable. However, Transcend makes no warranties, either expressed or implied, as to its accuracy and assume no liability in connection with the use of this product. Transcend reserves the right to make changes in specifications at any time without prior notice.

Operating Temperature Condition

Part Number	Symbol	Rating	Unit	Note
TS256MSK64V3N-I	T_{OPER}	-40 to 85	°C	1,2

Note:
1. Operating Temperature is the ambient temperature.
2. At -40 ~ 85°C, operation temperature range are the temperature which all DRAM specification will be supported.

Absolute Maximum DC Ratings

Parameter	Symbol	Value	Unit	Note
Voltage on V_{DD} relative to Vss	VDD	-0.4 ~ 1.8	V	1
Voltage on V_{DDQ} pin relative to Vss	VDDQ	-0.4 ~ 1.8	V	1
Voltage on any pin relative to Vss	VIN, VOUT	-0.4 ~ 1.8	V	1
Storage temperature	T_{STG}	-55~+100	°C	1,2

Note:
1. Stress greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.

AC & DC Operating Conditions

Recommended DC operating conditions

Parameter	Symbol	DDR3-1066/1333/1600		DDR3-1866		Unit	Note
		Min	Max	Min	Max		
Supply voltage	VDD	1.425	1.575	1.425	1.575	V	1, 2
Supply voltage for Output	VDDQ	1.425	1.575	1.425	1.575	V	1, 2
I/O Reference Voltage (DQ)	$VREF_{DQ}$(DC)	0.49*VDD	0.51*VDD	0.49*VDD	0.51*VDD	V	3
AC Input Logic High	VIH(AC)	VREF+0.150	-	-	-	V	
AC Input Logic Low	VIL(AC)	-	VREF-0.150	-	-	V	
DC Input Logic High	VIH(DC)	VREF+0.1	VDD	VREF+0.1	VDD	V	
DC Input Logic Low	VIL(DC)	VSS	VREF-0.1	VSS	VREF-0.1	V	

Note:
1. Under all conditions VDDQ must be less than or equal to VDD.
2. VDDQ tracks with VDD, AC parameters are measured with VDD and VDDQ tied together.
3. Peak to peak AC noise on VREF may not allow deviate from VREF(DC) by more than +/-1% VDD.

AC Input Level for Differential Signals

Parameter	Symbol	Value		Unit	Note
Differential Input Logical High	V_{IHdiff}	+200	-	mV	
Differential Input Logical Low	V_{ILdiff}	-	-200		

IDD Specification parameters Definition

(IDD values are for full operating range of Voltage and Temperature)

2GB, 256Mx64 Module(1 Rank x8)

Parameter	Symbol	TS256MSK64V3N-I	Unit
		IDD Max.	
Operating One bank Active-Precharge current; tCK = tCK(IDD), tRC = tRC(IDD), tRAS = tRASmin(IDD); CKE is HIGH, /CS is HIGH between valid commands;Address bus inputs are SWITCHING; Data bus inputs are SWITCHING	IDD0	264	mA
Operating One bank Active-read-Precharge current; IOUT = 0mA; BL = 8, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRC = tRC (IDD), tRAS = tRASmin(IDD), tRCD = tRCD(IDD); CKE is HIGH, /CS is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W	IDD1	376	mA
Precharge power-down current; All banks idle; tCK = tCK(IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	IDD2P	96	mA
Precharge quiet standby current; All banks idle; tCK = tCK(IDD); CKE is HIGH, /CS is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	IDD2Q	120	mA
Precharge standby current; All banks idle; tCK = tCK(IDD); CKE is HIGH, /CS is HIGH; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	IDD2N	136	mA
Active power - down current; All banks open; tCK = tCK(IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	IDD3P	120	mA
Active standby current; All banks open; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, /CS is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	IDD3N	184	mA
Operating burst read current; All banks open, Continuous burst reads, IOUT = 0mA; BL = 4, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, /CS is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W	IDD4R	400	mA
Operating burst write current; All banks open, Continuous burst writes; BL = 8, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, /CS is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING IDD4R	IDD4W	656	mA
Burst refresh current; tCK = tCK(IDD); Refresh command at every tRFC(IDD) interval; CKE is HIGH, /CS is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	IDD5	1360	mA
Self refresh current; CK and /CK at 0V; CKE ≒ 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING	IDD6	96	mA
Operating bank interleave read current; All bank interleaving reads, IOUT = 0mA; BL = 8, CL = CL(IDD), AL = tRCD(IDD)-1*tCK(IDD); tCK = tCK(IDD), Trc = tRC(IDD), tRRD = tRRD(IDD), tRCD = 1*tCK(IDD); CKE is HIGH, CS is HIGH between valid commands;Address bus inputs are STABLE during DESELECTs; Data pattern is same as IDD4R;	IDD7	1120	mA

Note: Module IDD was calculated on the specific brand DRAM component IDD and can be differently measured according to DQ loading capacitor.

Timing Parameters & Specifications

Speed		DDR3-1066		DDR3-1333		DDR3-1600		DDR3-1866		Units
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Average Clock Period	tCK(avg)	1.875	<2.5	1.5	<1.875	1.25	<1.5	1.071	<1.25	ns
Average high pulse width	tCH(avg)	0.47	0.53	0.47	0.53	0.47	0.53	0.47	0.53	tCK(avg)
Average low pulse width	tCL(avg)	0.47	0.53	0.47	0.53	0.47	0.53	0.47	0.53	tCK(avg)
Absolute clock HIGH pulse width	tCH(abs)	0.43	-	0.43	-	0.43	-	0.43	-	tCK(avg)
Absolute clock Low pulse width	tCL(abs)	0.43	-	0.43	-	0.43	-	0.43	-	tCK(avg)
DQS,DQS to DQ skew, per group, per access	tDQSQ	-	150	-	125	-	100	-	85	ps
DQ output hold time from DQS, DQS	tQH	0.38	-	0.38	-	0.38	-	0.38	-	tCK(avg)
DQ low-impedance time from CK, CK	tLZ(DQ)	-600	300	-500	250	-450	225	-390	195	ps
DQ high-impedance time from CK, CK	tHZ(DQ)	-	300	-	250	-	225	-	195	ps
Data setup time to DQS, DQS referenced to VIH(AC)VIL(AC) levels	tDS	75	-	30	-	10	-	-	-	ps
Data hold time from DQS, DQS referenced to VIH(DC)VIL(DC) levels	tDH	100	-	65	-	45	-	20	-	ps
DQ and DM Input pulse width for each input	tDIPW	490	-	400	-	360	-	320	-	ps
DQS, DQS differential READ Preamble	tRPRE	0.9	-	0.9	-	0.9	-	0.9	-	tCK(avg)
DQS, DQS differential READ Postamble	tRPST	0.3	-	0.3	-	0.3	-	0.3	-	tCK(avg)
DQS, DQS differential output high time	tQSH	0.38	-	0.4	-	0.4	-	0.4	-	tCK(avg)
DQS, DQS differential output low time	tQSL	0.38	-	0.4	-	0.4	-	0.4	-	tCK(avg)
DQS, DQS differential WRITE Preamble	tWPRE	0.9	-	0.9	-	0.9	-	0.9	-	tCK(avg)
DQS, DQS differential WRITE Postamble	tWPST	0.3	-	0.3	-	0.3	-	0.3	-	tCK(avg)
DQS, DQS rising edge output access time from rising CK, CK	tDQSCK	-300	300	-255	255	-225	225	-195	195	ps
DQS, DQS low-impedance time (Referenced from RL-1)	tLZ(DQS)	-600	300	-500	250	-450	225	-390	195	ps
DQS, DQS high-impedance time (Referenced from RL+BL/2)	tHZ(DQS)	-	300	-	250	-	225	-	195	ps

Speed		DDR3-1066		DDR3-1333		DDR3-1600		DDR3-1866		Units
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
DQS, DQS differential input low pulse width	tDQSL	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	tCK(avg)
DQS, DQS differential input high pulse width	tDQSH	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	tCK(avg)
DQS, DQS rising edge to CK, CK rising edge	tDQSS	-0.25	0.25	-0.25	0.25	-0.27	0.27	-0.27	0.27	tCK(avg)
DQS,DQS falling edge setup time to CK, CK rising edge	tDSS	0.2	-	0.2	-	0.18	-	0.18	-	tCK(avg)
DQS,DQS falling edge hold time to CK, CK rising edge	tDSH	0.2	-	0.2	-	0.18	-	0.18	-	tCK(avg)
DLL locking time	tDLLK	512	-	512	-	512	-	512	-	nCK
internal READ Command to PRECHARGE Command delay	tRTP	max (4nCK,7.5ns)	-	max (4nCK,7.5ns)	-	max (4nCK,7.5ns)	-	max (4nCK,7.5ns)	-	
Delay from start of internal write transaction to internal read command	tWTR	max (4nCK,7.5ns)	-	max (4nCK,7.5ns)	-	max (4nCK,7.5ns)	-	max (4nCK,7.5ns)	-	
WRITE recovery time	tWR	15	-	15	-	15	-	15	-	ns
Mode Register Set command cycle time	tMRD	4	-	4	-	4	-	4	-	nCK
Mode Register Set command update delay	tMOD	max (12nCK,15ns)	-	max (12nCK, 15ns)	-	max (12nCK,15ns)	-	max (12nCK,15ns)	-	
Average Clock Period	tCK(avg)	1.875	<2.5	1.5	<1.875	1.25	<1.5	1.071	<1.25	ns
Average high pulse width	tCH(avg)	0.47	0.53	0.47	0.53	0.47	0.53	0.47	0.53	tCK(avg)
Average low pulse width	tCL(avg)	0.47	0.53	0.47	0.53	0.47	0.53	0.47	0.53	tCK(avg)
Absolute clock HIGH pulse width	tCH(abs)	0.43	-	0.43	-	0.43	-	0.43	-	tCK(avg)
Absolute clock Low pulse width	tCL(abs)	0.43	-	0.43	-	0.43	-	0.43	-	tCK(avg)
DQS,DQS to DQ skew, per group, per access	tDQSQ	-	150	-	125	-	100	-	85	ps
DQ output hold time from DQS, DQS	tQH	0.38	-	0.38	-	0.38	-	0.38	-	tCK(avg)
DQ low-impedance time from CK, CK	tLZ(DQ)	-600	300	-500	250	-450	225	-390	195	ps
DQ high-impedance time from CK, CK	tHZ(DQ)	-	300	-	250	-	225	-	195	ps
Data setup time to DQS, DQS referenced to VIH(AC)VIL(AC) levels	tDS	75	-	30	-	10	-	-	-	ps

Speed		DDR3-1066		DDR3-1333		DDR3-1600		DDR3-1866		Units
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Data hold time from DQS, DQS referenced to VIH(DC)VIL(DC) levels	tDH	100	-	65	-	45	-	20	-	ps
DQ and DM Input pulse width for each input	tDIPW	490	-	400	-	360	-	320	-	ps
DQS, DQS differential READ Preamble	tRPRE	0.9	-	0.9	-	0.9	-	0.9	-	tCK(avg)
DQS, DQS differential READ Postamble	tRPST	0.3	-	0.3	-	0.3	-	0.3	-	tCK(avg)
DQS, DQS differential output high time	tQSH	0.38	-	0.4	-	0.4	-	0.4	-	tCK(avg)
DQS, DQS differential output low time	tQSL	0.38	-	0.4	-	0.4	-	0.4	-	tCK(avg)
DQS, DQS differential WRITE Preamble	tWPRE	0.9	-	0.9	-	0.9	-	0.9	-	tCK(avg)
DQS, DQS differential WRITE Postamble	tWPST	0.3	-	0.3	-	0.3	-	0.3	-	tCK(avg)
DQS, DQS rising edge output access time from rising CK, CK	tDQSCK	-300	300	-255	255	-225	225	-195	195	ps
DQS, DQS low-impedance time (Referenced from RL- 1)	tLZ(DQS)	-600	300	-500	250	-450	225	-390	195	ps
DQS, DQS high-impedance time (Referenced from RL+BL/2)	tHZ(DQS)	-	300	-	250	-	225	-	195	ps
DQS, DQS differential input low pulse width	tDQSL	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	tCK(avg)
DQS, DQS differential input high pulse width	tDQSH	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	tCK(avg)
DQS, DQS rising edge to CK, CK rising edge	tDQSS	-0.25	0.25	-0.25	0.25	-0.27	0.27	-0.27	0.27	tCK(avg)
DQS,DQS falling edge setup time to CK, CK rising edge	tDSS	0.2	-	0.2	-	0.18	-	0.18	-	tCK(avg)
DQS,DQS falling edge hold time to CK, CK rising edge	tDSH	0.2	-	0.2	-	0.18	-	0.18	-	tCK(avg)
DLL locking time	tDLLK	512	-	512	-	512	-	512	-	nCK
internal READ Command to PRECHARGE Command delay	tRTP	max(4nCK,7.5ns)	-	max(4nCK,7.5ns)	-	max(4nCK,7.5ns)	-	max(4nCK,7.5ns)	-	
Delay from start of internal write transaction to internal read command	tWTR	max(4nCK,7.5ns)	-	max(4nCK,7.5ns)	-	max (4nCK,7.5ns)	-	max (4nCK,7.5ns)	-	
WRITE recovery time	tWR	15	-	15	-	15	-	15	-	ns
Mode Register Set command cycle time	tMRD	4	-	4	-	4	-	4	-	nCK
Mode Register Set command update delay	tMOD	max(12nCK,15ns)	-	max(12nCK,15ns)	-	max(12nCK,15ns)	-	max(12nCK,15ns)	-	

SERIAL PRESENCE DETECT SPECIFICATION

TS128MSK64V3U-I Serial Presence Detect			
Byte No.	**Description**	**Value**	**Hex Value**
0	Number of SPD Bytes written / SPD device size / CRC coverage during module production	CRC: 0-116 bytes SPD bytes used: 176 bytes SPD bytes total: 256 bytes	92
1	SPD Revision	Version 1.0	10
2	Key Byte / DRAM Device Type	DDR3 SDRAM	0B
3	Key Byte / Module Type	SO-DIMM	03
4	SDRAM Density and Banks	2Gb 8banks	03
5	SDRAM Addressing	ROW:15, Column:10	19
6	Module Nominal Voltage, VDD	1.5V	00
7	Module Organization	1 Rank / x8	01
8	Module Memory Bus Width	Non ECC, 64 bits	03
9	Fine Timebase Dividend and Divisor	2.5 ps	52
10-11	Medium Timebase Dividend and Divisor	0.125 ns	01, 08
12	SDRAM Minimum Cycle Time (tCKmin)	1.5 ns	0C
13	Reserved	-	00
14-15	CAS Latencies Supported	5, 6, 7, 8, 9	3E, 00
16	Minimum CAS Latency Time (tAAmin)	13.125 ns	69
17	Minimum Write Recovery Time (tWRmin)	15 ns	78
18	Minimum /RAS to /CAS Delay Time (tRCDmin)	13.125 ns	69
19	Minimum Row Active to Row Active Delay Time (tRRDmin)	6 ns	30
20	Minimum Row Precharge Time (tRPmin)	13.125 ns	69
21	Upper Nibble for tRAS and tRC	See byte 22, 23	11
22	Minimum Active to Precharge Time (tRASmin)	36 ns	20
23	Minimum Active to Active/Refresh Time (tRCmin)	49.125 ns	89
24-25	Minimum Refresh Recovery Time (tRFCmin)	160 ns	00, 05
26	Minimum Internal Write to Read Command Delay Time (tWTmin)	7.5 ns	3C
27	Minimum Internal Read to Precharge Command Delay Time (tRTPmin)	7.5 ns	3C
28-29	Minimum Four Active Window Delay Time (tFAWmin)	30 ns	00, F0
30	SDRAM Optional Features	DLL-Off Mode, RZQ/6, RZQ/7	83
31	SDRAM Thermal and Refresh Options	No ODTS, No ASR	01
32	Module thermal sensor	Not support TS	00
33	SDRAM device type	Standard	00
34	Fine Offset for Minimum Cycle Time(tCKmin)	0 ps	00
35	Fine Offset for Minimum CAS Latency Time (tAAmin)	0 ps	00
36	Fine Offset for Minimum RAS# to CAS# Delay Time (tRCDmin)	0 ps	00
37	Minimum Row Precharge Delay Time (tRPmin)	0 ps	00
38	Fine Offset for Minimum Active to Active/Refresh Delay Time (tRCmin)	0 ps	00

Byte No.	Description	Value	Hex Value
39-40	Reserved	-	00
41	SDRAM Maximum Active Count (MAC) Value	200 K	86
42-59	Reserved	-	00
60	Module Nominal Height	29 < Height ≤ 30 mm	0F
61	Module Max Thickness	Planar Double Sides	11
62	Reference Raw Card Used	Revision 1, R/C B	21
63	Address Mapping from Edge Connector to DRAM	Standard	00
64-116	Reserved	-	00
117-118	Module Manufacturer ID Code	Transcend Information	01, 4F
119	Module Manufacturing Location	Taipei	54
120-121	Module Manufacturing Date	Year, Week	Variable
122-125	Module Serial Number	By Manufacturer	Variable
126-127	Cyclical Redundancy Code	Cyclical Redundancy Code	91, 7C
128-145	Module Part Number	TS256MSK64V3N-I	54 53 32 35 36 4D 53 4B 36 34 56 33 4E 2D 49 20 20 20
146-147	Revision Code	-	00
148-149	DRAM Manufacturer ID Code	By Manufacturer	Variable
150-175	Manufacturer Specific Data	By Manufacturer	Variable
176-255	Open for customer use	By Manufacturer	Variable