Low Noise Micro PMU, 3 A Buck Regulator with 3 A LDO

Data Sheet **ADP5003**

FEATURES

- Low noise, dc power supply system
  - High efficiency buck for first stage conversion
  - High PSRR, low noise LDO regulator to remove switching ripple
  - Adaptive LDO regulator headroom control option for optimal efficiency and PSRR across full load range
- 3 A, low noise, buck regulator
  - Wide input voltage range: 4.2 V to 15 V
  - Programmable output voltage range: 0.6 V to 5.0 V
  - 0.3 MHz to 2.5 MHz internal oscillator
  - 0.3 MHz to 2.5 MHz SYNC frequency range
- 3 A, low noise, NFET LDO regulator (active filter)
  - Wide input voltage range: 0.65 V to 5 V
  - Programmable output voltage range: 0.6 V to 3.3 V
  - Differential point of load remote sensing
  - 3 µV rms output noise (independent of output voltage)
  - PSRR > 50 dB (to 100 kHz) with 400 mV headroom at 3 A
  - Ultrafast transient response
  - Power-good output
- Precision enable inputs for both the buck regulator and LDO
- −40°C to +125°C operating junction temperature range
- 32-lead, 5 mm × 5 mm, LFCSP

APPLICATIONS

- Low noise power for high speed analog-to-digital converter (ADC) and digital-to-analog converter (DAC) designs
- Powering RF transceivers and clocking ICs

FUNCTIONAL BLOCK DIAGRAM

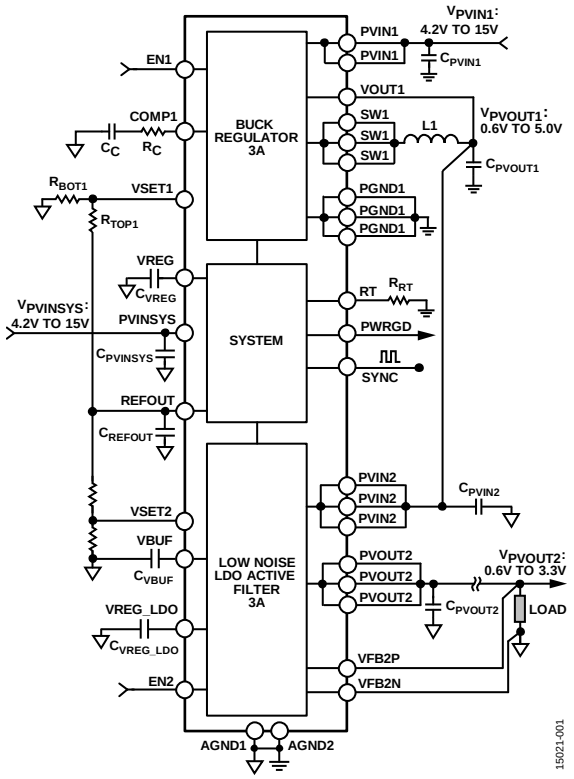

Figure 1.

GENERAL DESCRIPTION

The ADP5003 integrates a high voltage buck regulator and an ultralow noise low dropout (LDO) regulator in a small, 5 mm × 5 mm, 32-lead LFCSP package to provide highly efficient and quiet regulated supplies.

The buck regulator is optimized to operate at high output currents up to 3 A. The LDO is capable of a maximum output current of 3 A and operates efficiently with low headroom voltage while maintaining high power supply rejection.

The ADP5003 can operate in one of two modes. Adaptive mode allows the LDO to operate with an optimized headroom by adjusting the buck output voltage internally in response to the LDO load current. Alternatively, the ADP5003 can operate in independent mode, where both regulators operate separately from each other, and where the output voltages are programmed using resistor dividers.

The LDO regulator output can be accurately controlled at the point of load (POL) using remote sensing that compensates for the printed circuit board (PCB) trace impedance while delivering high output currents.

Each regulator is activated via a dedicated precision enable input. The buck switching frequency can be synchronized to an external signal, or programmed with an external resistor.

Safety features in the ADP5003 include thermal shutdown (TSD), input undervoltage lockout (UVLO) and independent current limits for each regulator. The ADP5003 is rated for a −40°C to +125°C operating junction temperature range.

Rev. A Document Feedback

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700
Technical Support www.analog.com

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11/2017—Revision 0: Initial Version

SPECIFICATIONS

V_{PVIN1} = $V_{PVINSYS}$ = 4.2 V to 15 V, V_{PVIN2} = 0.65 V to 5 V, T_J = −40°C to +125°C for minimum/maximum specifications, and T_A = 25°C for typical specifications, unless otherwise noted.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
INPUT VOLTAGE RANGE	V_{PVIN1}, $V_{PVINSYS}$	4.2		15	V	
	V_{PVIN2}	0.65		5	V	
THERMAL SHUTDOWN						
Threshold	T_{SD}		155		°C	T_J rising
Hysteresis	T_{SD-HYS}		15		°C	
SYNC INPUT						
Input Logic						
High	V_{IH}	1.1			V	
Low	V_{IL}			0.4	V	
Input Leakage Current	$V_{I-LEAKAGE}$			1	µA	
ADAPTIVE MODE INPUT (VSET1)						
Input Rising Threshold	V_{ADPR}		2.5		V	
Input Hysteresis	V_{ADPH}		16		mV	
PRECISION ENABLING						
High Level Threshold	V_{TH_H}	1.125	1.15	1.175	V	
Low Level Threshold	V_{TH_L}	1.025	1.05	1.075	V	
Shutdown Mode	V_{TH_S}			0.4	V	
EN1, EN2 Pull-Down Resistance	R_{ENPD}		1.5		MΩ	
INPUT CURRENT						
Both Channels Enabled	$I_{STBY-NOSW}$		0.5	1	mA	No load, not switching
Both Channels Disabled	$I_{SHUTDOWN}$		5	10	µA	T_J = −40°C to +125°C
REFOUT CHARACTERISTICS						
Output Voltage	V_{REFOUT}		2.0		V	
Accuracy		−0.5		+0.5	%	
VREG AND VREG_LDO CHARACTERISTICS						
Output Voltage	V_{REG}, V_{REG_LDO}		5		V	
Accuracy		−2		+2	%	
Current Limit[1]		10			mA	
POWER-GOOD PIN (PWRGD)						
Power Good Threshold	$PWRGD_F$	80	85	90	%	Applies to VOUT1 and VFB2P to VFB2N
Hysteresis	$PWRGD_{FH}$		2.5		%	
Output Voltage Level	V_{OL}		25	50	mV	PWRGD pin sink current = 1 mA
Deglitch Time	t_{PWRGDD}		60		µs	
PVINSYS UNDERVOLTAGE LOCKOUT (UVLO)						
Input Voltage						
Rising	$UVLO_{PVINSYSRISE}$			4.2	V	
Falling	$UVLO_{PVINSYSFALL}$	3.9			V	

[1] Do not use VREG and VREG_LDO to supply the external loads. This current limit protects against a pin short to ground.

BUCK REGULATOR SPECIFICATIONS

$V_{PVIN1} = V_{PVINSYS} = 4.2$ V to 15 V, $V_{PVIN2} = 0.65$ V to 5 V, $T_J = -40°C$ to $+125°C$ for minimum/maximum specifications, and $T_A = 25°C$ for typical specifications, unless otherwise noted.

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
OUTPUT CHARACTERISTICS						
Programmable Output Voltage Range[1]	V_{PVOUT1}	0.6		5.0	V	
Buck Regulator Gain	A_{BUCK}		2.5			V_{PVOUT1}/V_{VSET1}
Error Amplifier Transconductance	g_{m1}	509	600	661	µS	
Buck Output Voltage Accuracy[2]		−1		+1	%	VOUT1 load current (I_{LOAD1}) = 10 mA
Regulation						
Line	$(\Delta V_{PVOUT1}/V_{PVOUT1})/\Delta V_{PVIN1}$		0.004		%/V	I_{LOAD1} = 10 mA
Load	$(\Delta V_{PVOUT1}/V_{PVOUT1})/\Delta I_{LOAD1}$		0.04		%/A	0 mA ≤ I_{LOAD1} ≤ 3 A, V_{PVIN1} = 12 V
Total Output Voltage Accuracy			±1.5		%	4.2 V ≤ V_{PVIN1} ≤ 15 V, 1 mA ≤ I_{LOAD1} ≤ 3 A
OPERATING SUPPLY CURRENT	I_{IN}		3.8		mA	I_{LOAD1} = 0 mA, LDO disabled, buck switching
SW1 CHARACTERISTICS						
SW1 On Resistance	R_{PFET}		130	200	mΩ	V_{PVIN1} = 15 V (PVIN1 to SW1)
	R_{NFET}		60	100	mΩ	V_{PVIN1} = 15 V (SW1 to PGND1)
Current Limit Threshold	I_{LIMIT1}	3.5			A	Negative channel field effect transistor (NFET) switch valley current limit
				−1	A	Negative current limit
Slew Rate	$SLEW_{SW1}$		1.6		V/ns	V_{PVIN1} = 15 V, I_{LOAD1} = 1 A
Minimum On Time[3]	t_{MIN_ON}		35		ns	
Minimum Off Time	t_{MIN_OFF}		100	128	ns	
BUCK REGULATOR ACTIVE PULL DOWN	R_{PDWN-B}		90		Ω	Channel disabled
BUCK REGULATOR SOFT START (SS)	t_{SSBUCK}		2		ms	
HICCUP TIME	t_{HICCUP}		33		ms	
VSETx ADJUSTABLE INPUT BIAS CURRENT	I_{VSET1}, I_{VSET2}		10	150	nA	
OSCILLATOR						
Internal Switching Frequency 1	f_{SW1}	2.25	2.5	2.75	MHz	R_{RT} ≤ 71.2 kΩ
Internal Switching Frequency 2	f_{SW2}	0.26	0.3	0.34	MHz	R_{RT} = 600 kΩ
SYNC						
Frequency Range	f_{SYNC}	0.3		2.5	MHz	
Minimum Pulse Width						
Positive		20			ns	
Negative		10			ns	

[1] The switching frequency, minimum on time, and minimum off time may limit the output voltage range.
[2] The buck output voltage accuracy is relative to the nominal output voltage and accounts for reference voltage, gain, and offset error.
[3] The minimum on time indicates the minimum high-side turn on time to ensure fixed frequency switching.

LDO SPECIFICATIONS

V_{PVIN1} = $V_{PVINSYS}$ = 4.2 V to 15 V, V_{PVIN2} = 0.65 V to 5 V, LDO headroom voltage (V_{HR}) = 300 mV, T_J = −40°C to +125°C for minimum/maximum specifications, and T_A = 25°C for typical specifications, unless otherwise noted.

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
OUTPUT CHARACTERISTICS						
Programmable Output Voltage Range[1]	V_{LDO}	0.6		3.3	V	$V_{VFB2P-VFB2N}$
LDO Gain	A_{LDO}		1.65			V_{LDO}/V_{VSET2}
Output Voltage Accuracy[2]		−1		+1	%	VOUT2 load current (I_{LOAD2}) = 150 mA
Regulation						
Line	$(\Delta V_{LDO}/V_{LDO})/\Delta V_{PVIN2}$		0.007		%/V	$(V_{PVOUT2} + V_{HR}) \le V_{PVIN2} \le 6$ V, I_{LOAD2} = 100 mA
Load	$(\Delta V_{LDO}/V_{LDO})/\Delta I_{LOAD2}$		0.08		%/A	10 mA ≤ I_{LOAD2} ≤ 3 A
Total Output Voltage Accuracy			±1.5		%	$(V_{PVOUT2} + V_{HR}) \le V_{PVIN2} \le 6$ V, 10 mA ≤ I_{LOAD2} ≤ 3 A
OPERATING SUPPLY CURRENT	I_{GND}		1.8	2.5	mA	I_{LOAD2} = 0 µA
			2.3		mA	I_{LOAD2} = 3 A
MINIMUM VOLTAGE REQUIREMENTS						I_{LOAD2} = 3 A
PVINSYS to PVOUT2[3]	$V_{PVINSYS-PVOUT2}$		1.5		V	
VREG_LDO to PVOUT2[4]	$V_{VREG\_LDO-PVOUT2}$		1.35		V	Required to drive NFET
Dropout[5]	$V_{DROPOUT}$		100		mV	
CURRENT-LIMIT THRESHOLD[6]	I_{LIMIT2}	3.1		4.5	A	
LDO SOFT START (SS) TIME	t_{SSLDO}		400		µs	
LDO ACTIVE PULL-DOWN	$R_{PDWNLDO}$		300		Ω	Channel disabled
OUTPUT NOISE	N_{PVOUT2}		3		µV rms	10 Hz to 100 kHz, I_{LOAD2} = 1 A
LDO POWER SUPPLY REJECTION RATIO	$PSRR_{LDO}$					$V_{PVIN2} = V_{PVOUT2}$ + 0.3 V, I_{LOAD2} = 1A
V_{PVOUT2} = 1.3 V			87		dB	1 kHz
			82		dB	10 kHz
			61		dB	100 kHz
			38		dB	1000 kHz
V_{PVOUT2} = 3.3 V			89		dB	1 kHz
			83		dB	10 kHz
			61		dB	100 kHz
			37		dB	1000 kHz

[1] Limited by minimum PVINSYS to PVOUT2 and VREG_LDO to PVOUT2 voltage.
[2] The LDO output voltage accuracy is relative to the nominal output voltage and accounts for reference voltage, gain, and offset error.
[3] PVINSYS must be higher than PVOUT2 by at least $V_{PVINSYS-PVOUT2}$ to keep the LDO regulating.
[4] PVOUT2 must be lower than VREG_LDO by at least $V_{VREG\_LDO-PVOUT2}$ to keep the LDO regulating.
[5] The dropout voltage is the input to output voltage differential when the input voltage is set to the nominal output voltage.
[6] The current-limit threshold is the current at which the output voltage drops to 90% of the specified typical value. For example, the current limit for a 1.0 V output voltage is the current that causes the output voltage to drop to 90% of 1.0 V or 0.9 V.

ADAPTIVE HEADROOM CONTROLLER SPECIFICATIONS

V_{PVIN1} = $V_{PVINSYS}$ = 4.2 V to 15 V, V_{PVIN2} = 0.65 V to 5 V, T_J = −40°C to +125°C for minimum/maximum specifications, and T_A = 25°C for typical specifications, unless otherwise noted.

Table 4.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
HEADROOM VOLTAGE (PVIN2 – PVOUT2)	V_{HR}		160		mV	I_{LOAD2} = 1 mA
			280		mV	I_{LOAD2} = 1.5 A
			400		mV	I_{LOAD2} = 3 A

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
PVIN1/PVINSYS to AGND1/AGND2	−0.3 V to +16 V
PVIN2 to AGND1/AGND2	−0.3 V to +6.0 V
AGND1 to AGND2	−0.3 V to +0.3 V
PGND1 to AGND1/AGND2	−0.3 V to +0.3 V
PVOUT2 to AGND1/AGND2	−0.3 V to the lower of (PVIN2 + 0.3 V) or +6.0 V
VFB2N to AGND1/AGND2/PGND1	−0.3 V to +0.3 V
VOUT1, VFB2P, EN1, EN2, SYNC, RT, REFOUT, VBUF, VSET1, VSET2, COMP1 to AGND1/AGND2	−0.3 V to the lower of (VREG + 0.3 V) or +6.0 V
SW1 to PGND1	−0.3 V to (PVIN1 + 0.3 V)
VREG, VREG_LDO to AGND1/AGND2/PGND1/VFB2N	−0.3 V to the lower of (PVINSYS + 0.3 V) or +6.0 V
VREG to VREG_LDO	−0.3 V to +0.3 V
Storage Temperature Range	−65°C to +150°C
Operating Junction Temperature Range	−40°C to +125°C
Soldering Conditions	JEDEC J-STD-020

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to PCB design and operating environment. Careful attention to PCB thermal design is required.

Table 6. Thermal Resistance

Package Type	θ_{JA}[1]	θ_{JC}[1]	Unit
CP-32-7	46.91	20.95	°C/W

[1] θ_{JA} and θ_{JC} are based on a 4-layer PCB (two signal and two power planes) with nine thermal vias connecting the exposed pad to the ground plane as recommended in the Layout Considerations section.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

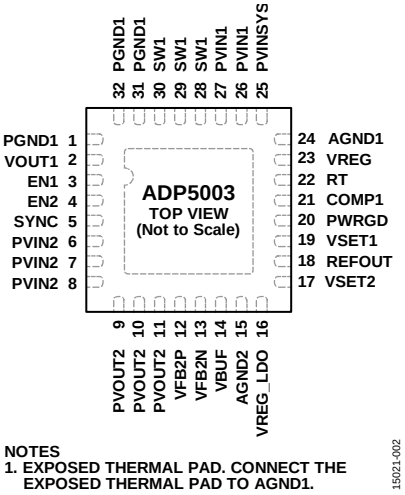


Figure 2. Pin Configuration

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 31, 32	PGND1	Buck Regulator Dedicated Power Ground.
2	VOUT1	Buck Regulator Feedback Input. Connect a short sense trace to the buck output capacitor.
3	EN1	Buck Regulator Precision Enable Pin. Drive the EN1 pin high to turn on the buck regulator, and drive the EN1 pin low to turn off the buck regulator.
4	EN2	LDO Precision Enable Pin. Drive the EN2 pin high to turn on the LDO regulator, and drive the EN2 pin low to turn off the LDO regulator.
5	SYNC	Synchronization Input. To synchronize the switching frequency of the device to an external clock, connect this pin to an external clock with a frequency from 300 kHz to 2.5 MHz.
6 to 8	PVIN2	LDO Regulator Power Input. Connect a 10 µF ceramic capacitor between this pin and AGND2.
9 to 11	PVOUT2	LDO Regulator Power Output. Connect a 10 µF ceramic capacitor between this pin and AGND2.
12	VFB2P	LDO Regulator Positive Sense Feedback Input. Connect a sense trace to the LDO output at the load. Route this pin alongside the VFB2N pin on the PCB.
13	VFB2N	LDO Regulator Ground Sense Feedback Input. Connect a sense trace to ground at the load. Route this pin alongside the VFB2P pin on the PCB.
14	VBUF	Output of the LDO Reference Buffer. Connect a 0.1 µF ceramic capacitor between this pin and VFB2N.
15	AGND2	LDO Dedicated Analog Ground.
16	VREG_LDO	Internal Regulator Output for the LDO. Connect a 1 µF ceramic decoupling capacitor between this pin and AGND2. Do not use this pin to power external devices.
17	VSET2	LDO Regulator Output Voltage Configuration Input.
18	REFOUT	Internal Reference Output Required for Driving the External Resistor Dividers for VSET1 and VSET2. Connect a 0.22 µF ceramic capacitor between this pin and AGND2.
19	VSET1	Buck Regulator Output Voltage Configuration Input. Connect this pin to VREG to enable adaptive headroom control.
20	PWRGD	Power-Good Digital Output (Open-Drain NFET Pull-Down Driver).
21	COMP1	Buck Regulator External Compensation Pin.
22	RT	Resistor Adjustable Frequency Programming Input.
23	VREG	Internal Regulator Output. Connect a 1 µF ceramic decoupling capacitor between this pin and AGND1. Do not use this pin to power external devices.
24	AGND1	Analog Ground.
25	PVINSYS	System Power Supply for the ADP5003. Connect a 10 µF ceramic capacitor between this pin and AGND1.
26, 27	PVIN1	Buck Regulator Power Input. Connect a 10 µF ceramic capacitor between this pin and PGND1.
28 to 30	SW1	Buck Regulator Switching Output.
	EPAD	Exposed Thermal Pad. Connect the exposed thermal pad to AGND1.

TYPICAL PERFORMANCE CHARACTERISTICS

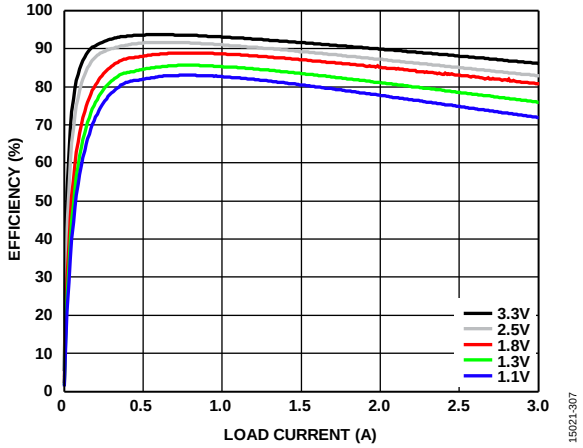


Figure 3. Buck Efficiency vs. Load Current, V_{PVIN1} = 5 V, f_{SW} = 600 kHz at Various Buck Output Voltages

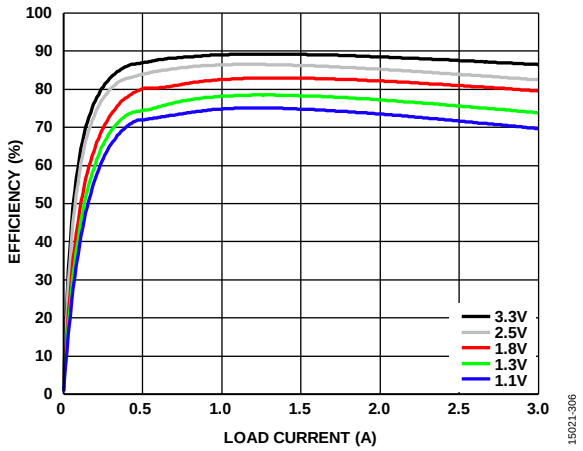


Figure 4. Buck Efficiency vs. Load Current, V_{PVIN1} = 12 V, f_{SW} = 600 kHz at Various Buck Output Voltages

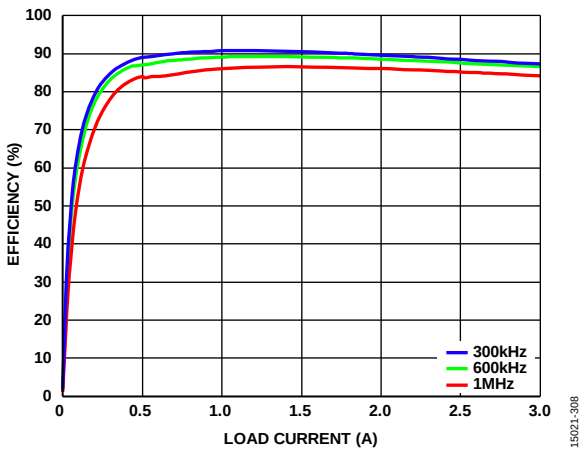


Figure 5. Buck Efficiency vs. Load Current, V_{PVIN1} = 12 V, V_{PVOUT1} = 3.3 V at Various Buck Switching Frequencies

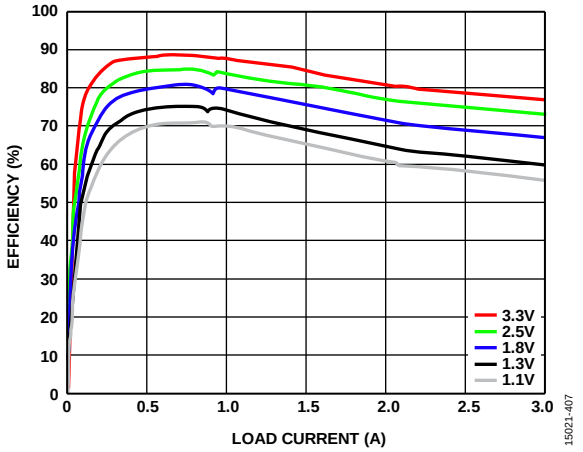


Figure 6. Adaptive Mode Efficiency vs. Load Current, V_{PVIN1} = 5 V, f_{SW} = 600 kHz at Various LDO Output Voltages

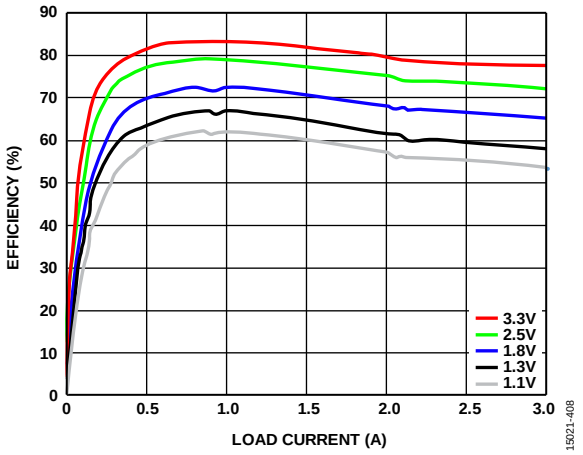


Figure 7. Adaptive Mode Efficiency vs. Load Current, V_{PVIN1} = 12 V, f_{SW} = 600 kHz at Various LDO Output Voltages

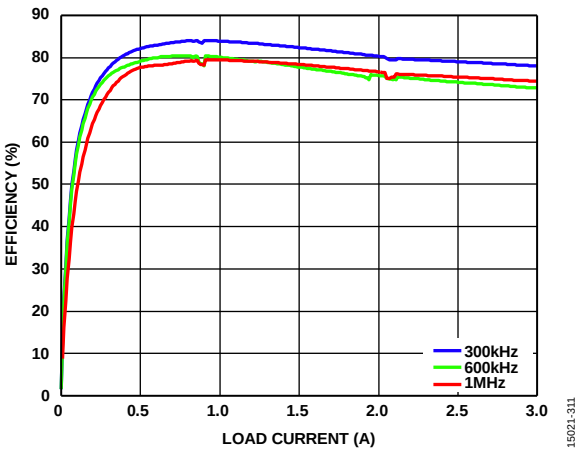


Figure 8. Adaptive Mode Efficiency vs. Load Current, V_{PVIN1} = 12 V, V_{PVOUT2} = 3.3 V at Various Buck Switching Frequencies

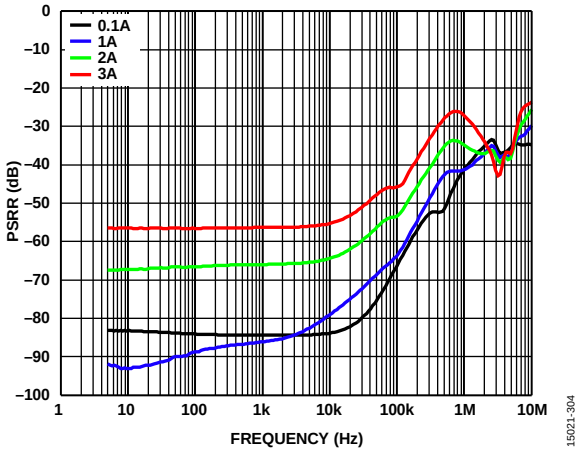


Figure 9. LDO PSRR vs. Frequency, V_{HR} = 0.3 V, V_{PVOUT2} = 1.3 V at Various LDO Load Currents

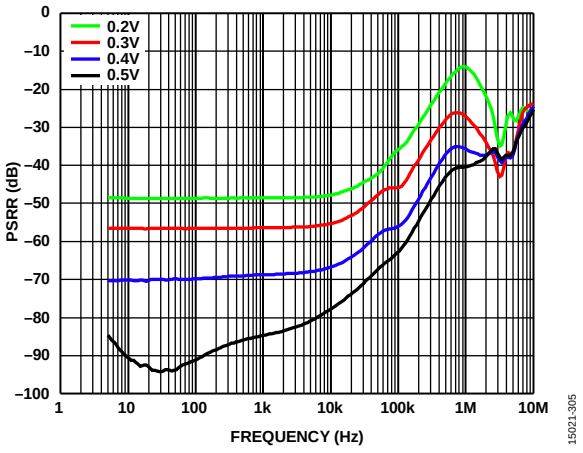


Figure 10. LDO PSRR vs. Frequency, V_{PVOUT2} = 1.3 V, I_{LOAD2} = 1 A at Various LDO Headroom Voltages

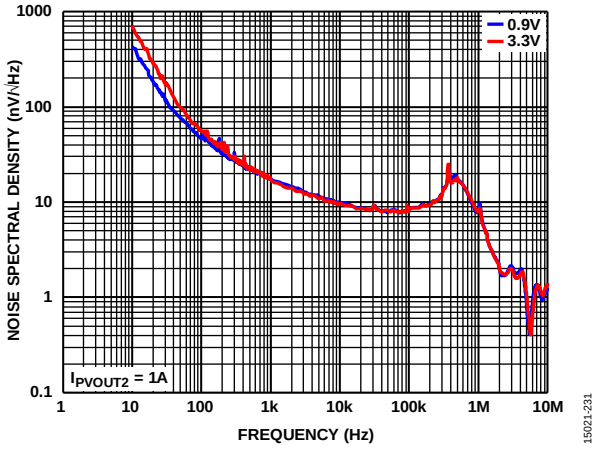


Figure 11. LDO Noise Spectral Density vs. Frequency at Various LDO Output Voltages

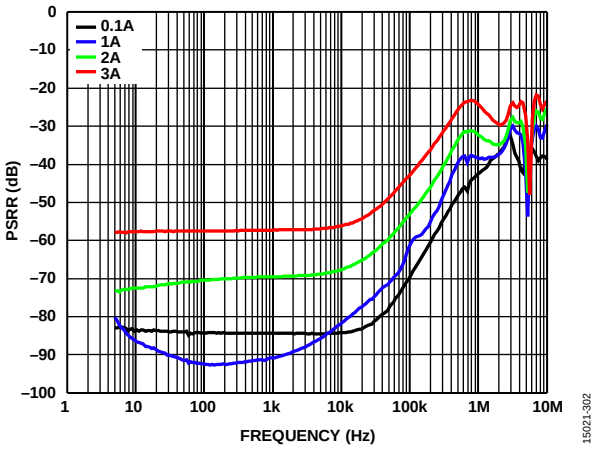


Figure 12. LDO PSRR vs. Frequency, V_{HR} = 0.3 V, V_{PVOUT2} = 3.3 V at Various LDO Load Currents

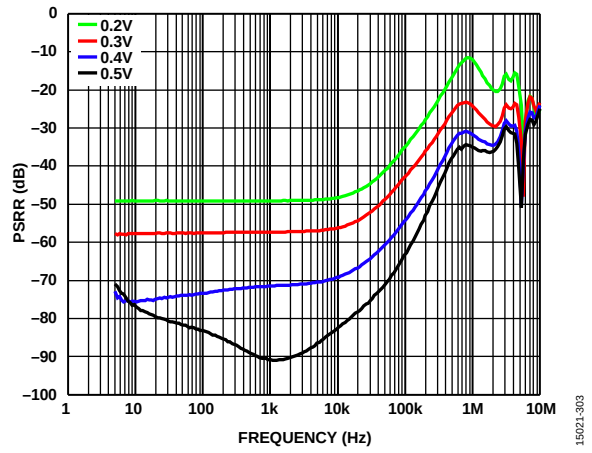


Figure 13. LDO PSRR vs. Frequency, V_{PVOUT2} = 3.3 V, I_{LOAD2} = 1 A at Various LDO Headroom Voltages

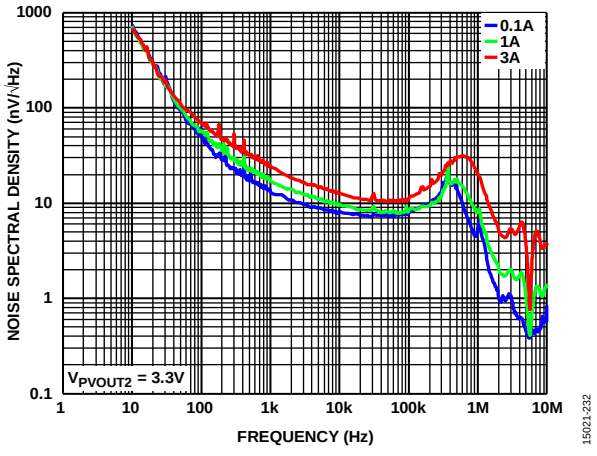


Figure 14. LDO Noise Spectral Density vs. Frequency, V_{PVOUT2} = 3.3 V at Various LDO Load Currents

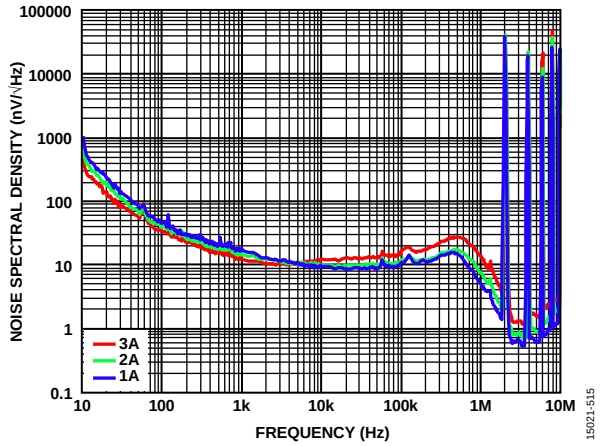


Figure 15. Adaptive Mode Noise Spectral Density vs. Frequency at various Load Currents, $V_{PVOUT1} = V_{PVIN2}$ =3.7 V, V_{PVOUT2} = 3.3 V, f_{SW} = 2 MHz, L = 1.5 µH, R_C = 23.7 kΩ, C_C = 1 nF, C_{CP} = 10 pF, C_{PVOUT1} = 22 µF

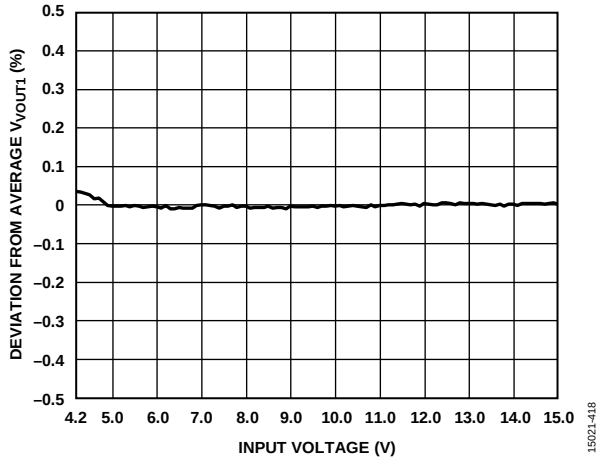


Figure 16. Buck Line Regulation, V_{PVOUT1} = 3.3 V, I_{LOAD1} = 1 A, f_{SW} = 600 kHz

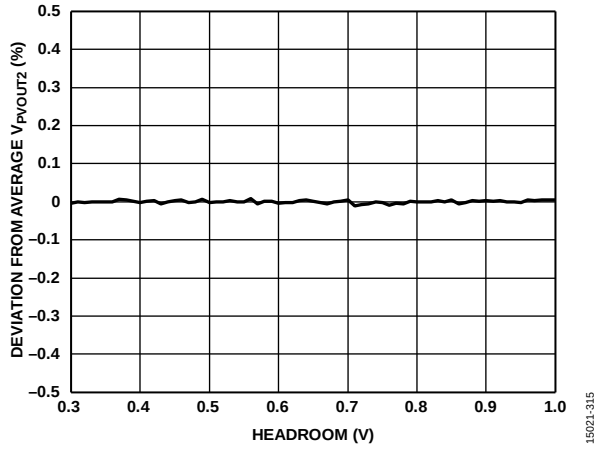


Figure 17. LDO Line Regulation, V_{PVOUT2} = 3.3 V, I_{LOAD2} = 1 A

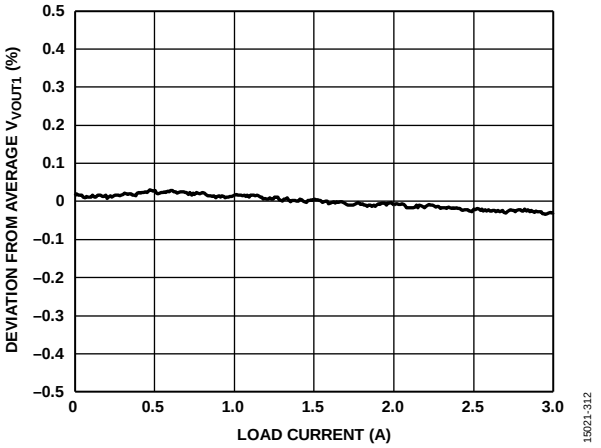


Figure 18. Buck Load Regulation, V_{PVIN1} = 12 V, V_{PVOUT1} = 3.3 V, f_{SW} = 600 kHz

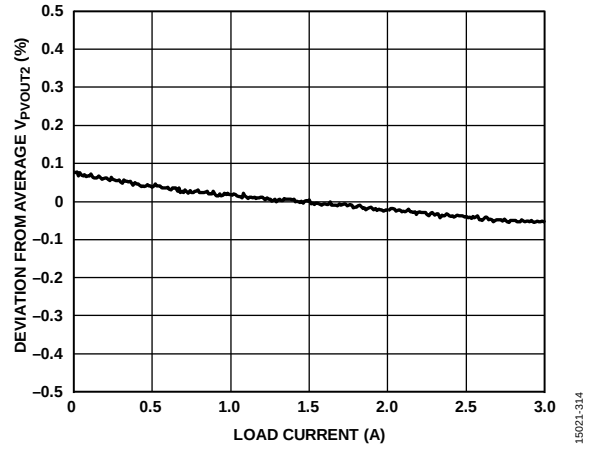


Figure 19. LDO Load Regulation, V_{PVOUT2} = 3.3 V, V_{HR} = 0.3 V

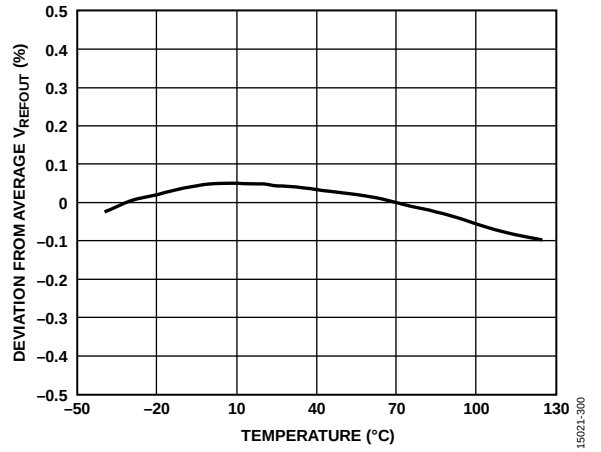


Figure 20. REFOUT Voltage (V_{REFOUT}) vs. Temperature

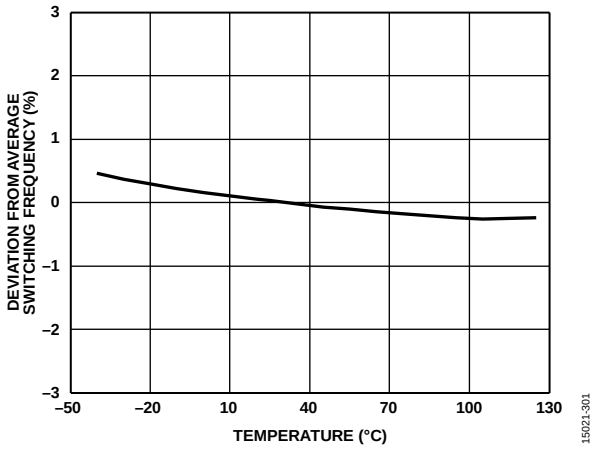


Figure 21. Switching Frequency vs. Temperature

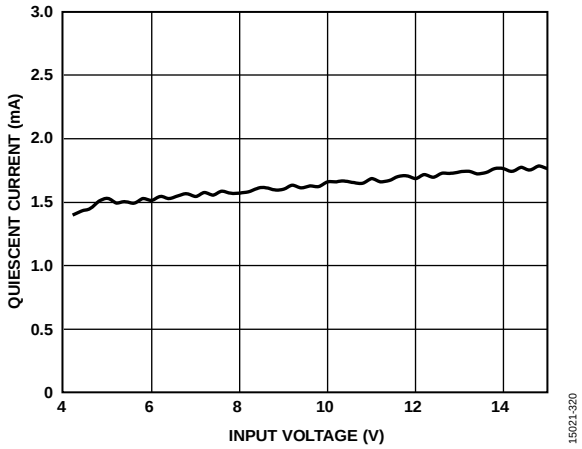


Figure 24. Buck Quiescent Current vs. Input Voltage

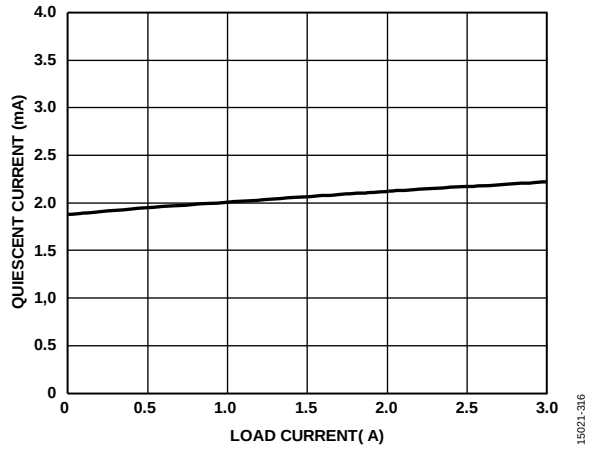


Figure 22. LDO Quiescent Current vs. Load Current

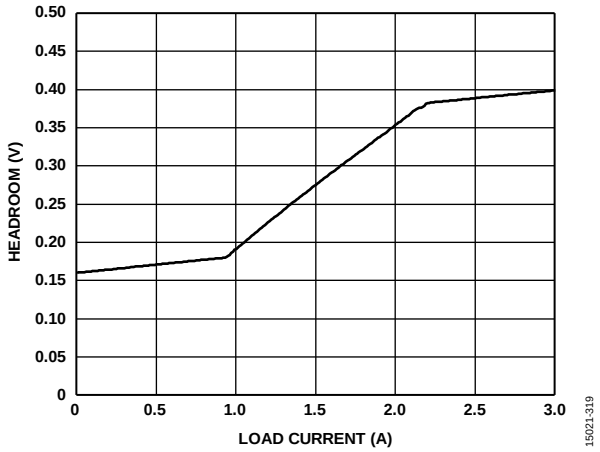


Figure 25. Adaptive Mode Headroom vs. Load Current

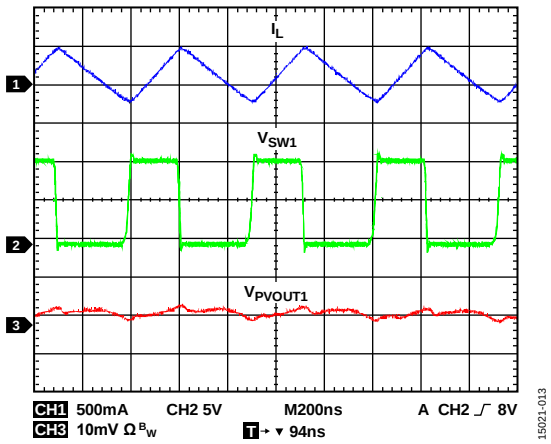


Figure 23 SW1 Waveform, V_{PVOUT1} = 5 V, I_{LOAD1} = 100 mA, f_{SW} = 2 MHz, L = 2.2 µH, R_C = 2.7 kΩ, C_C = 22 nF, C_{CP} = 22 pF, C_{PVOUT1} = 22 µF

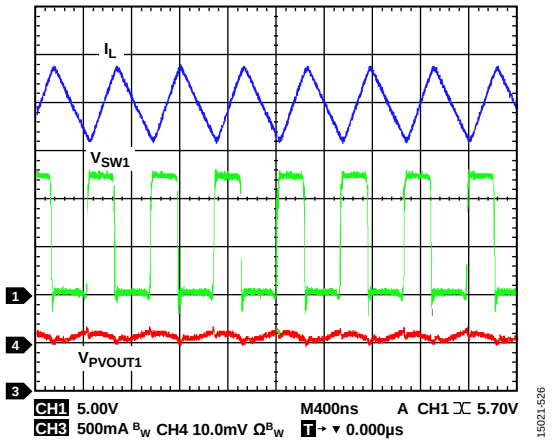


Figure 26. SW1 Waveform, V_{PVOUT1} = 5 V, I_{LOAD1} = 3 A, f_{SW} = 2 MHz, L = 2.2 µH, R_C = 2.7 kΩ, C_C = 22 nF, C_{CP} = 22 pF, C_{PVOUT1} = 22 µF

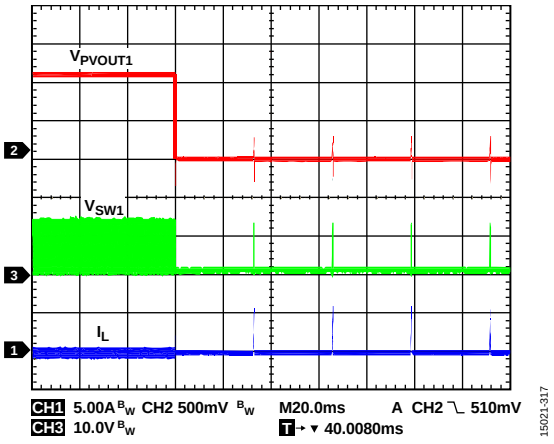


Figure 27. Entering Hiccup Mode
(V_{SW1} is the Voltage of the SW1 Pin, and I_L is Inductor Current)

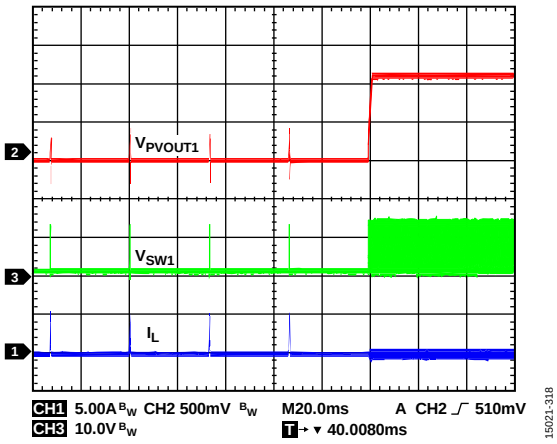


Figure 30. Exiting Hiccup Mode

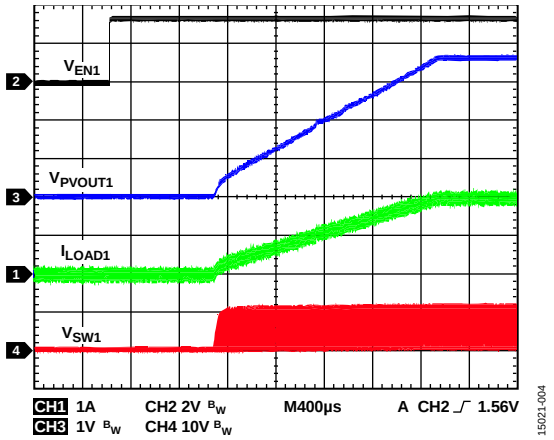


Figure 28. Buck Startup, V_{PVOUT1} = 3.3V, I_{LOAD1} = 3 A
(V_{EN1} is the EN1 voltage.)

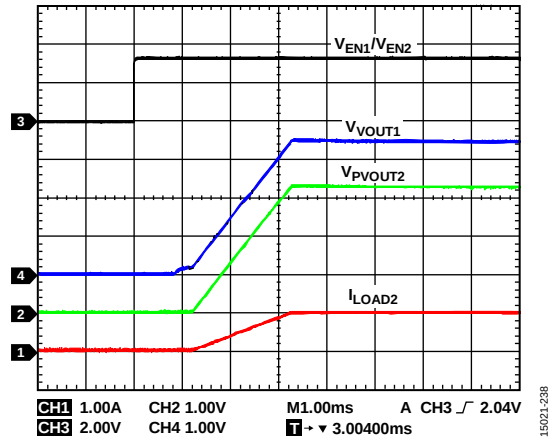


Figure 31. Adaptive Mode Startup, V_{PVOUT2} = 3.3 V, I_{LOAD2} = 1 A
(V_{EN2} is the EN2 voltage.)

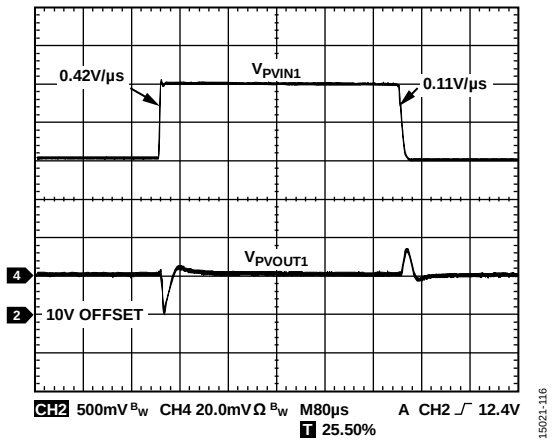


Figure 29. Buck Line Transient, V_{PVIN1} = 12 V to 13 V, V_{PVOUT1} = 1.2 V, I_{LOAD1} = 1A, f_{SW} = 0.6 MHz, L = 2.2 µH, R_C = 3.48 kΩ, C_C = 2 nF, C_{CP} = 22 pF, C_{PVOUT1} = 44 µF

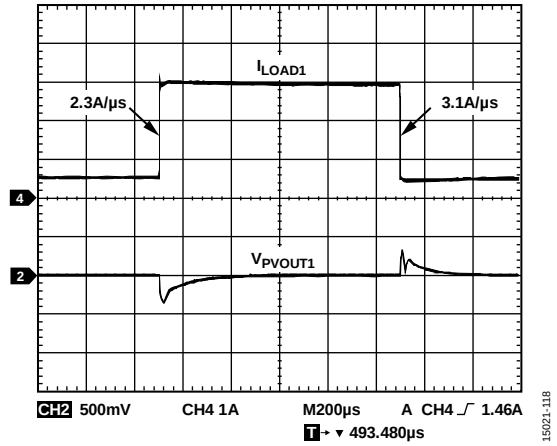


Figure 32. Buck Load Transient, V_{PVIN1} = 12 V, V_{PVOUT1} = 1.2 V, I_{LOAD1} = 0.5 A to 3 A, f_{SW} = 0.6 MHz, L = 2.2 µH, R_C = 3.48 kΩ, C_C = 2 nF, C_{CP} = 22 pF, C_{PVOUT1} = 44 µF

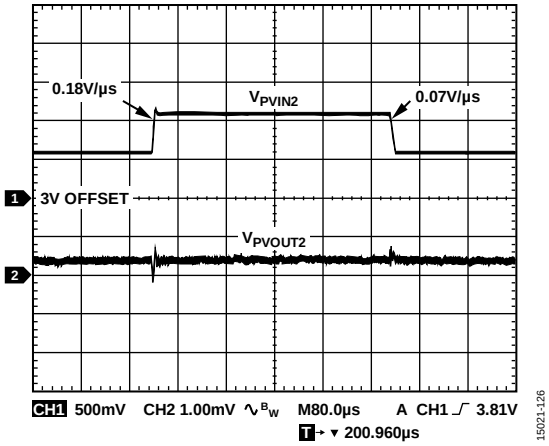


Figure 33. LDO Line Transient, V_{PVIN2} = 3.6 V to 4.1 V, V_{PVOUT2} = 3.3 V, I_{LOAD2} = 1 A

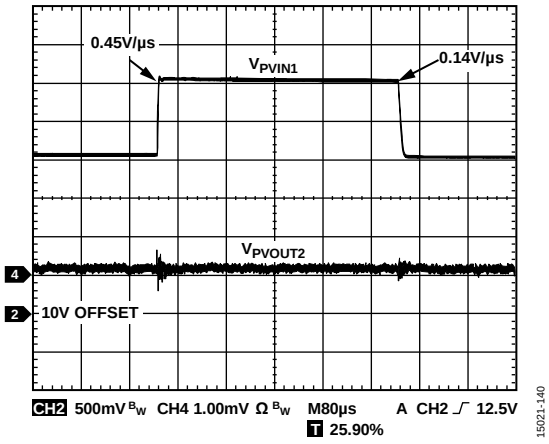


Figure 34. Adaptive Mode Line Transient, V_{PVIN1} = 11 V to 13 V, V_{PVOUT2} = 3.3 V, I_{LOAD2} = 1 A, f_{SW} = 1.5 MHz, L = 2.2 µH, R_C = 3.48 kΩ, C_C = 22 nF, C_{CP} = 22 pF, C_{PVOUT1} = 64 µF

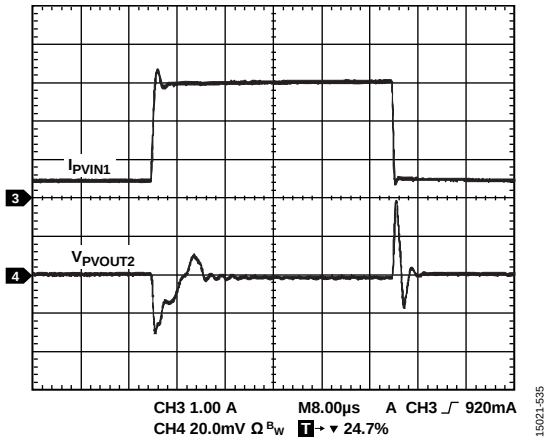


Figure 35. Adaptive Mode Load Transient, V_{PVIN1} = 12 V, V_{PVOUT2} = 3.3 V, I_{LOAD2} = 0.5 A to 3 A, f_{SW} = 1.5 MHz, L = 2.2 µH, R_C = 3.48 kΩ, C_C = 22 nF, C_{CP} = 22 pF, C_{PVOUT1} = 64 µF

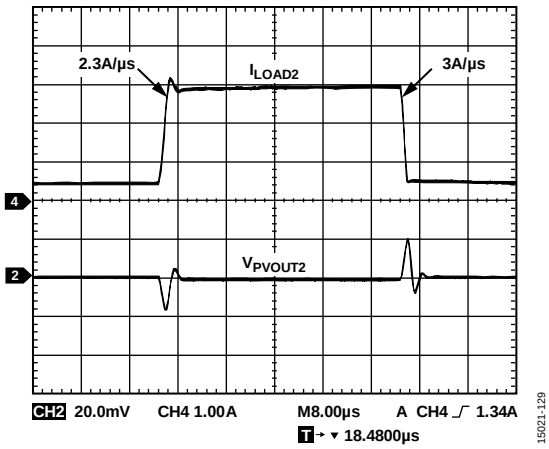


Figure 36. LDO Load Transient, V_{PVIN2} = 3.6 V, V_{PVOUT2} = 3.3 V, I_{LOAD2} = 0.5 A to 3 A

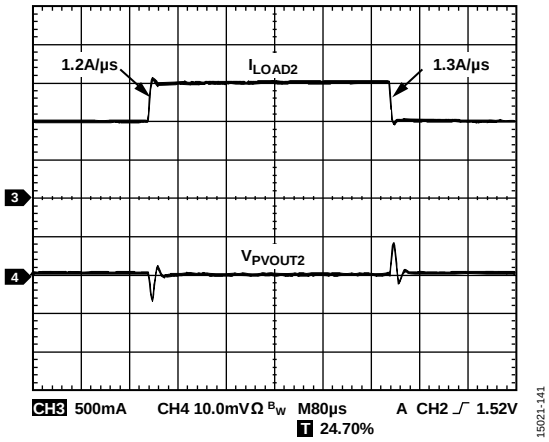


Figure 37. Adaptive Mode Load Transient, V_{PVIN1} = 12 V, V_{PVOUT2} = 3.3 V, I_{LOAD2} = 1 A to 1.5 A, f_{SW} = 1.5 MHz, L = 2.2 µH, R_C = 3.48 kΩ, C_C = 22 nF, C_{CP} = 22 pF, C_{PVOUT1} = 64 µF

THEORY OF OPERATION

POWER MANAGEMENT UNIT

The ADP5003 is a micropower management unit combining a step-down (buck) dc-to-dc converter and an ultralow noise low dropout linear (LDO)regulator. The high switching frequency and 5 mm × 5 mm, 32-lead LFCSP package allow a compact power management solution.

Adaptive Headroom Control

The ADP5003 features a scheme to control the LDO headroom voltage to ensure optimal operating efficiency while maintaining a consistent power supply rejection ratio (PSRR) across the full range of the LDO load current.

The scheme works by varying the headroom voltage across the LDO NFET with respect to the LDO load current. Lower and upper limits prevent the headroom from approaching zero volts at light loads and from increasing more than necessary at high loads.

Precision Enable/Shutdown

The ADP5003 has individual enable pins (EN1 and EN2) to control the regulators.

The precision enable function allows a precise turn on point for the regulators to allow the possibility of external sequencing. A voltage level higher than V_{TH_H} applied to the EN1 or EN2 pin activates a regulator, whereas a level below V_{TH_L} turns off a regulator. The buck is controlled by EN1, and the LDO is controlled by the EN2 pin. When both EN1 and EN2 fall below V_{TH_S}, the ADP5003 enters shutdown mode.

Undervoltage Lockout (UVLO)

To protect against the input voltage being too low, UVLO circuitry is integrated into the system. If the input voltage on PVINSYS drops to less than the $UVLO_{PVINSYSFALL}$ threshold, all channels shut down.

The device is enabled again when the voltage on PVINSYS rises to more than the $UVLO_{PVINSYSRISE}$ threshold, provided the enable pins remain active.

Thermal Shutdown (TSD)

In the event that the junction temperature rises above T_{SD}, the thermal shutdown circuit turns off both regulators. Extreme junction temperatures can be the result of high current operation, poor circuit board design, or a high ambient temperature. A hysteresis value of $T_{SD\text{-}HYS}$ is included so that when thermal shutdown occurs, the regulators do not return to operation until the on-chip temperature drops below $T_{SD} - T_{SD\text{-}HYS}$. When emerging from thermal shutdown, both regulators restart with soft start control.

Active Pull Down

Both regulators have active pull-down resistors discharging the respective output capacitors when the regulators are disabled. The pull-down resistors are connected between VOUT1 to AGND1 and PVOUT2 to AGND2. Active pull-down resistors are disabled when the regulators are turned on.

When the enable pins are asserted low, or a TSD or UVLO event occurs, the active pull-down resistors enable to quickly discharge the output capacitors. The pull-down resistors remain engaged until the enable pins are asserted high, the fault event is no longer present, or the VREG supply voltage falls to less than the voltage required (approximately 1 V) to guarantee that the pull-down resistor remains enabled.

Soft Start (SS)

Both regulators have an internal soft start function that ramps the output voltage in a controlled manner on startup, thereby limiting the inrush current. The soft start function reduces the risk of noise spikes and voltage drops on the upstream supplies.

Power-Good

The ADP5003 has a dedicated power-good, open-drain, output (PWRGD). PWRGD indicates whether one or more regulators are outside the voltage limits specified by the power-good lower limit ($PWRGD_F$) and the power-good upper limit ($PWRGD_F$ + $PWRGD_{FH}$). When either one or both of the regulator outputs are outside the power-good limits, the PWRGD output pulls low. PWRGD will continue to pull low, provided the VREG supply voltage remains above approximately 1 V.

When in adaptive mode, PWRGD only monitors the LDO output, and when in standalone mode, PWRGD only monitors the regulator/regulators that are enabled.

BUCK REGULATOR

Control Scheme

The buck regulator operates with a fixed frequency, emulated peak current mode, pulse-width modulation (PWM) control architecture, where the duty cycle of the integrated switches is adjusted and regulates the output voltage. At the start of each oscillator cycle, the positive channel field effect transistor (PFET) switch is turned on, sending a positive voltage across the inductor. Current in the inductor increases until the emulated current sense signal crosses the peak inductor current threshold, which turns off the PFET switch and turns on the NFET synchronous rectifier. Turning on the NFET synchronous rectifier creates a negative voltage across the inductor, which causes the inductor current to decrease. The synchronous rectifier stays on for the remainder of the cycle. By adjusting the peak inductor current threshold, the buck regulator can regulate the output voltage.

The emulated inductor current scheme senses the current in the inductor during the off phase of the cycle, when the NFET is conducting, and uses this inductor current to generate the emulated current sense signal during the on time of the cycle. This scheme allows the low duty cycles necessary for high input voltage, V_{IN}, to output voltage, V_{OUT}, conversion ratios.

Oscillator Frequency Control

The ADP5003 buck regulator oscillator frequency is controlled by using the RT pin or the SYNC pin. To define the buck regulator internal switching frequency, connect the RT pin via a resistor to AGND1. Figure 38 shows the relationship of the buck oscillator frequency and the RT resistor value.

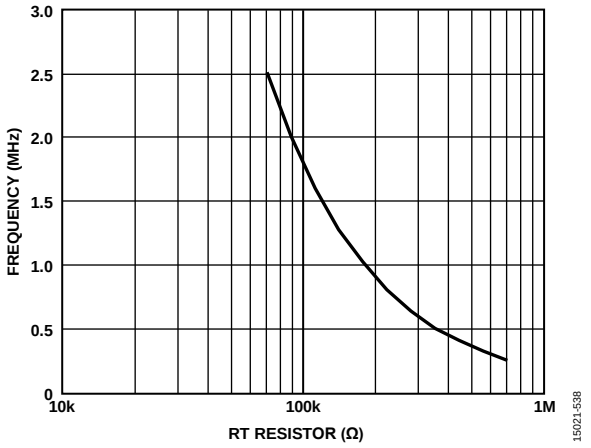


Figure 38. Buck Oscillator Frequency vs. RT Resistor (R_{RT})

To determine the oscillator frequency (f_{SW}), use the following equation:

$$f_{SW} = (1.78 \times 10^{11})/R_{RT} \quad (1)$$

An upper limit prevents out of range frequencies when the RT pin is shorted to ground or connected with a resistor value less than 70 kΩ.

External Oscillator Synchronization

The SYNC pin is dedicated for oscillator synchronization and allows the ADP5003 to lock to an external clock.

When an applied external clock signal is present at the SYNC pin, the buck regulator operates in sync with this signal.

When alternating between external clocks and the internal oscillator, the presence of an external frequency causes a multiplexer to switch between the internal oscillator and the external SYNC frequency. The output of this multiplexer acts as the frequency reference to an internal phase-locked loop (PLL), which ensures that changing between the two modes of operation results in a smooth transition between the different frequencies.

Buck Startup

The buck regulator turns on with a controlled soft start ramp to limit inrush current. The reference of the buck is ramped during t_{SSBUCK}, which is typically 2 ms (see Figure 39).

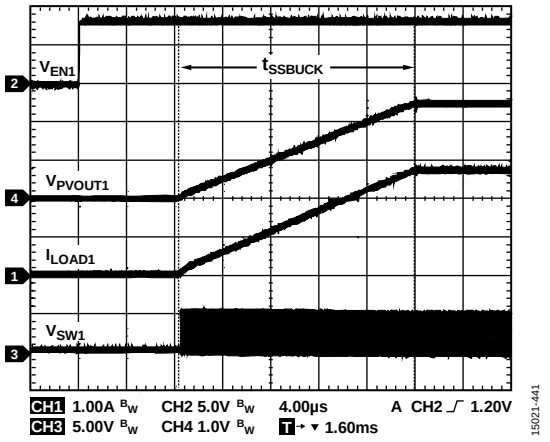


Figure 39. Buck Startup

Current-Limit and Short-Circuit Protection

The buck regulator includes current-limit protection circuitry to limit the amount of forward current through the field effect transistor (FET) switches. When the valley inductor current exceeds the overcurrent limit threshold for a number of clock cycles during an overload or short-circuit condition, the regulator enters hiccup mode. The regulator stops switching and then restarts with a new soft start cycle after the hiccup time, t_{HICCUP}, and repeats until the over-current condition is removed. If the buck regulator output voltage falls below 50% of the nominal output voltage, the regulator immediately enters hiccup mode. When the valley inductor current falls below the negative current-limit threshold, the NFET turns off and the PFET remains off allowing the inductor current to be discharged via the PFET body diode. The PFET turns on again with the next clock edge after the inductor current no longer exceeds the negative current-limit threshold.

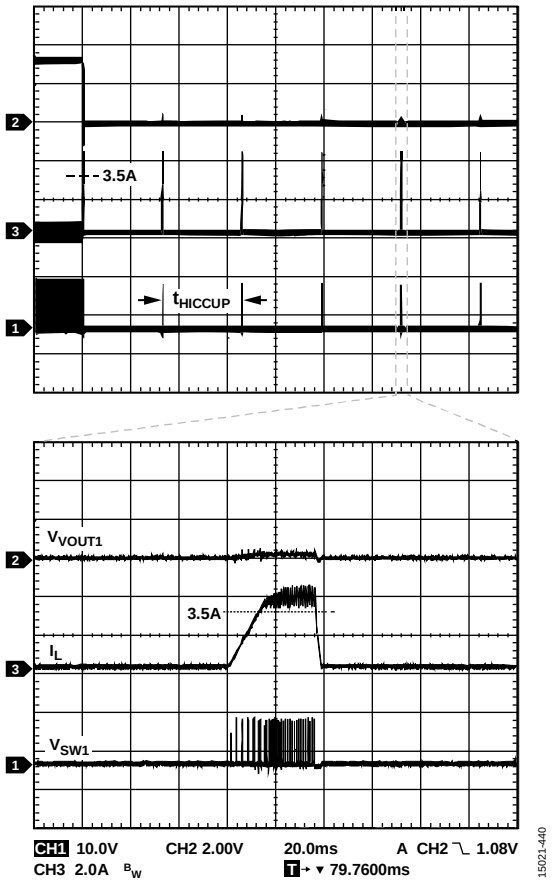


Figure 40. Short-Circuit Response (Current Limit and Hiccup Mode)

LDO REGULATOR

The ADP5003 contains a single low noise, low dropout (LDO) linear regulator that uses an NFET pass device to provide high PSRR with low headroom voltage and an output current up to 3 A.

The LDO regulator can operate with an input voltage of 0.65 V to 5 V while providing excellent line and load transient response using 10 µF ceramic input and output capacitors.

LDO Startup

The LDO regulator turns on with a controlled soft start ramp to limit inrush current. This soft start ramp is dictated by t_{SSLDO}, which is typically 400 µs.

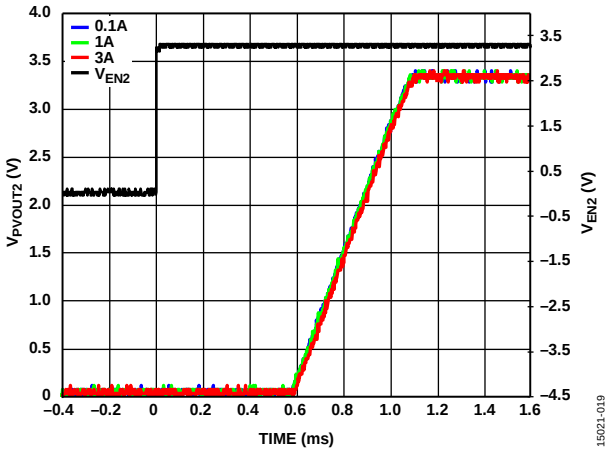


Figure 41. LDO Startup

Current Limit

The LDO operates in current limit when the output load exceeds I_{LIMIT2}. When in current limit operation, the output voltage reduces to maintain a constant output current.

Differential Remote Sensing

The LDO can sense at the point of load by using VFB2P and VFB2N as shown in Figure 42. Differential remote sensing compensates for both the source drop and the return drop to provide a more precise supply scheme at the point of load.

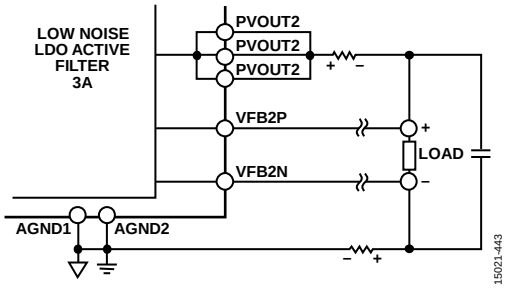


Figure 42. Differential Remote Sensing

POWER-GOOD

An external pull-up resistor is necessary to drive the PWRGD output high (see Figure 43). Through the value of the pull-up resistor is not critical, it is recommended to use a 10 kΩ to 300 kΩ resistor. The resistor must be pulled to a voltage level no greater than 5.5 V.

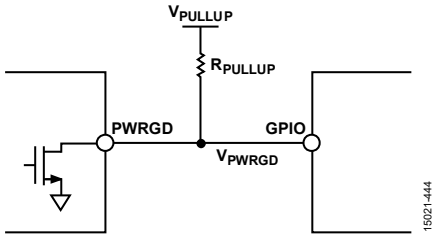


Figure 43. Power-Good Setup

OUTPUT VOLTAGE OF THE BUCK REGULATOR

The output voltage on the buck regulator is adjustable through an external resistor divider. When using adaptive mode, the ADP5003 controls the buck output voltage.

The adjustable output voltage configuration is shown in Figure 44.

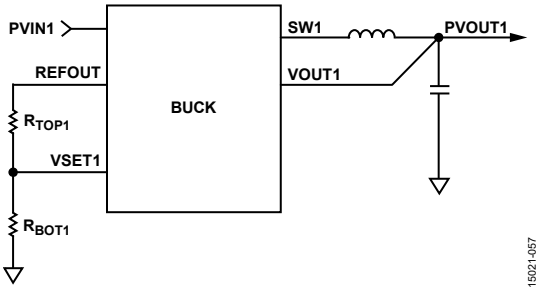


Figure 44. Buck Regulator Adjustable Output Voltage

To calculate the buck output voltage, use the following equation:

$$V_{PVOUT1} = V_{REFOUT} A_{BUCK} \left(\frac{R_{BOT1}}{R_{TOP1} + R_{BOT1}} \right) \quad (2)$$

where:
V_{REFOUT} is the REFOUT output voltage.
A_{BUCK} is the buck regulator gain.
R_{BOT1} is the bottom divider resistor.
R_{TOP1} is the top divider resistor.

OUTPUT VOLTAGE OF THE LDO REGULATOR

The output voltage on the LDO regulator is adjustable through an external resistor divider. The LDO adjustable output voltage configuration is shown in Figure 45.

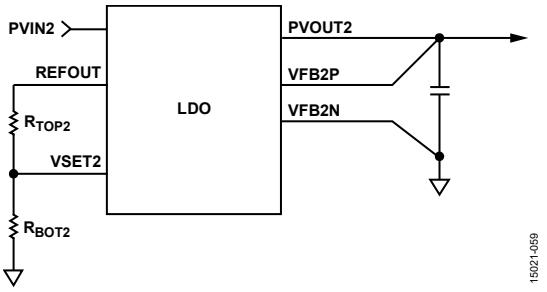


Figure 45. LDO Adjustable Output Voltage Configuration

To calculate the LDO output voltage, use the following equation:

$$V_{PVOUT2} = V_{REFOUT} A_{LDO} \left(\frac{R_{BOT2}}{R_{TOP2} + R_{BOT2}} \right) \quad (3)$$

where:
A_{LDO} is the LDO gain.
R_{BOT2} is the bottom divider resistor.
R_{TOP2} is the top divider resistor.

VOLTAGE CONVERSION LIMITATIONS

For a given input voltage and switching frequency, an upper and lower limitation on the output voltage exists due to the minimum on time and minimum off time. The minimum on time limits the minimum output voltage for a given input voltage and switching frequency.

If the minimum on time is exceeded, the ADP5003 may not switch at a fixed frequency because the device can switch at an effective zero on time, resulting in unpredictable switching frequencies and unwanted noise.

To calculate the minimum output voltage for a given input voltage and fixed switching frequency, use the following equation:

$$V_{OUT\_MIN} = V_{PVIN1} \times t_{MIN\_ON} \times f_{SW} - (R_{PFET} - R_{NFET}) \times I_{OUT\_MIN} \times t_{MIN\_ON} \times f_{SW} - (R_{NFET} + R_L) \times I_{OUT\_MIN} \quad (4)$$

where:
V_{OUT_MIN} is the minimum output voltage.
V_{PVIN1} is the input voltage.
t_{MIN_ON} is the minimum on time.
f_{SW} is the switching frequency.
R_{PFET} is the high-side PFET on resistance.
R_{NFET} is the low-side NFET on resistance.
I_{OUT_MIN} is the minimum output current.
R_L is the resistance of the output inductor.

The minimum off time limits the maximum duty cycle which in turn limits the maximum output voltage for a given input voltage and switching frequency. Calculate the maximum output voltage for a given input voltage and switching frequency by using the following equation:

$$V_{OUT\_MAX} = V_{PVIN1} \times (1 - t_{MIN\_OFF} \times f_{SW}) - (R_{PFET} - R_{NFET}) \times I_{OUT\_MAX} \times (1 - t_{MIN\_OFF} \times f_{SW}) - (R_{NFET} + R_L) \times I_{OUT\_MAX} \quad (5)$$

where:
V_{OUT_MAX} is the maximum output voltage.
I_{OUT_MAX} is the maximum output current.
t_{MIN_OFF} is the minimum off time.

As shown in Equation 4 and Equation 5, reducing the switching frequency eases the minimum on time and minimum off time limitations.

COMPONENT SELECTION

Output Capacitors

Higher output capacitor values reduce the output voltage ripple and improve the load transient response.

Ceramic capacitors are manufactured with a variety of dielectrics, each with a different behavior over temperature and applied voltage. Capacitors must have a dielectric adequate to ensure the minimum capacitance over the necessary temperature range and dc bias conditions. X5R or X7R dielectrics with a voltage rating of 25 V are recommended for best performance. Y5V and Z5U dielectrics are not recommended for use with any dc-to-dc converter because of their poor temperature and dc bias characteristics.

Use the following equation to calculate the worst case capacitance, accounting for capacitor variation over temperature, component tolerance, and voltage:

$$C_{EFFECTIVE} = C_{NOMINAL} \times (1 - TEMPCO) \times (1 - DCBIASCO) \times (1 - Tolerance) \quad (6)$$

where:
$C_{EFFECTIVE}$ is the effective capacitance at the operating voltage.
$C_{NOMINAL}$ is the nominal data sheet capacitance.
TEMPCO is the worst case capacitor temperature coefficient.
DCBIASCO is the dc bias derating at the output voltage.
Tolerance is the worst case component tolerance.

To guarantee the performance of the device, it is imperative to evaluate the dc bias effects, temperature, and tolerances on the behavior of the capacitors for each application.

Capacitors with lower effective series resistance (ESR) and effective series inductance (ESL) are preferred to minimize output voltage ripple.

Use the following equation to calculate the minimum capacitance needed for a specific output voltage ripple:

$$C_{OUT\_MIN} \cong \frac{\Delta I_L}{8 \times f_{SW} \times (V_{RIPPLE} - \Delta I_L \times R_{ESR})} \quad (7)$$

where:
ΔI_L is the current ripple.
f_{SW} is the switching frequency.
V_{RIPPLE} is the allowed peak-to-peak voltage ripple.
R_{ESR} is the effective series resistance of the capacitor.

The minimum capacitance needed for stability considering temperature and dc bias effects is 22 µF.

The minimum capacitance recommended for the LDO is 10 µF.

Table 8. Recommended Output Capacitors

Vendor	Part No.	Value (µF)	Type	Voltage Rating (V)	Case
Wurth	885 012 207 026	10	X7R	10	0805
	885 012 209 006	22	X7R	10	1210
	885 012 109 012	47	X5R	25	1210
	885 012 109 004	100	X5R	6.3	1210
Murata	GRM21BR71A106KE51	10	X7R	10	0805
	GRM32ER71C226KEA8	22	X7R	16	1210
	GRM32ER71A476KE15	47	X7R	10	1210

Input Capacitor

The input current to the buck converter steps from zero to a positive value that is dependent on inductor value, switching frequency, and load current (typically between 1 A and 4 A) and then drops quickly to zero again every switching cycle. Because these current pulses occur at relatively high frequencies (0.3 MHz to 2.5 MHz), the input bypass capacitor provides most of the high frequency current while the input power source supplies only the average current. Higher value input capacitors reduce the input voltage ripple and improve transient response.

To minimize supply noise, it is recommended to place a low ESR capacitor as close as possible to the relevant supply pin.

Inductor

The high switching frequency of the ADP5003 buck allows the selection of small chip inductors. A small inductor leads to larger inductor current ripple that provides improved transient response but degrades efficiency. The sizing of the inductor is a trade-off between efficiency and transient response. As a guideline, the inductor peak-to-peak current ripple is typically set to 1/3 of the maximum load current for optimal transient response and efficiency.

To calculate the inductor value, L, use the following equation:

$$L = ((V_{PVIN1} - V_{PVOUT1}) \times D)/(\Delta I_L \times f_{SW}) \quad (8)$$

where:
V_{PVIN1} is the input voltage.
V_{PVOUT1} is the output voltage.
D is the duty cycle ($D = V_{VOUT1}/V_{PVIN1}$).
ΔI_L is the inductor ripple current.
f_{SW} is the switching frequency.

The minimum dc current rating of the inductor must be greater than the inductor peak current. Use the following equation to calculate the inductor peak current:

$$I_{PEAK} = I_{LOAD1} + (\Delta I_L/2) \quad (9)$$

where:
I_{LOAD1} is the output current.
ΔI_L is the inductor ripple current.

Inductor conduction losses are minimized by using larger sized inductors that have smaller dc resistance; this in turn improves efficiency at the cost of solution size. Due to the high switching frequency of the ADP5003, shielded ferrite core material is recommended for its low core losses and low electromagnetic interference (EMI).

Table 9. Recommended Inductors

Vendor	Part No.	Value (µH)	Saturation Current, I_{SAT} (A)	RMS Current, I_{RMS} (A)	DC Resistance (mΩ)	Size (mm)
Coilcraft	XAL4020-102	1	8.7	6.7	13.25	4 × 4
	XAL4020-122	1.2	7.9	6.6	17.75	4 × 4
	XAL4020-152	1.5	7.1	5.2	21.45	4 × 4
	XAL4020-222	2.2	5.6	4	35.2	4 × 4
	XAL5030-102	1	14	8.7	8.5	5 × 5
	XAL5030-122	1.2	12.5	7.9	11.4	5 × 5
	XAL5030-222	2.2	9.2	7.2	13.2	5 × 5
	XAL5030-332	3.3	8.7	5.9	21.2	5 × 5
	XAL5050-562	5.6	6.3	5.3	23.45	5 × 5
	XAL5050-682	6.8	6	4.7	26.75	5 × 5
	XEL6030-102	1	18	12	6.32	6 × 6
	XEL6030-152	1.5	15	10	9.57	6 × 6
	XEL6030-222	2.2	13	7	12.7	6 × 6
	XEL6030-332	3.3	10.5	6	19.92	6 × 6
	XEL6060-472	4.7	11.4	9	13.65	6 × 6
	XAL6060-562	5.6	9.9	7.5	14.46	6 × 6
	XEL6060-682	6.8	7.9	7.3	20.82	6 × 6
	XEL6060-822	8.2	7.6	7	22.71	6 × 6
	XAL6060-103	10	7.6	5	27	6 × 6
Wurth	744 383 570 10	1	9.6	7.4	11.6	4 × 4
	744 383 570 12	1.2	8.8	7	13.4	4 × 4
	744 383 570 15	1.5	8.5	6.2	17.1	4 × 4
	744 383 570 18	1.8	8	5.8	18	4 × 4
	744 383 570 22	2.2	7	5.2	22	4 × 4

COMPENSATION COMPONENTS DESIGN

For the peak current mode control architecture, the power stage can be simplified as a voltage controlled current source that supplies current to the output capacitor and load resistor. The simplified loop is composed of one dominant pole and a zero contributed by the output capacitor ESR.

The ADP5003 uses a transconductance amplifier as the error amplifier to compensate the system. Figure 46 shows the simplified peak current mode control, small signal circuit.

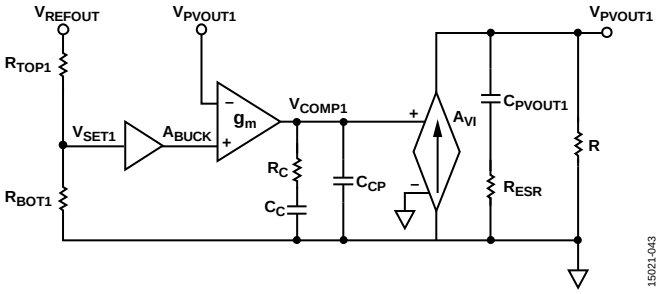


Figure 46. Simplified Peak Current Mode Control, Small Signal Circuit

The compensation components, R_C and C_C, contribute a zero, and the optional C_{CP} and R_C contribute an optional pole.

The following procedure shows how to select the compensation components (R_C, C_C, and C_{CP}) for ceramic output capacitor applications:

1. Determine the cross frequency (f_C). Generally, f_C is between $f_{SW}/12$ and $f_{SW}/6$.
2. Use the following equation to calculate R_C:

$$R_C = \frac{2 \times \pi \times C_{PVOUT1} \times A_{BUCK}}{g_m \times A_{VI}} \quad (10)$$

   where:
   C_{PVOUT1} is the output capacitance.
   A_{VI} = 7 A/V.

3. Place the compensation zero at the domain pole (f_P). Determine C_C as follows:

$$C_C = ((R + R_{ESR}) \times C_{PVOUT1})/R_C \quad (11)$$

   where:
   R_{ESR} is the equivalent series resistance of the output capacitor.

4. C_{CP} is optional. It can cancel the zero caused by the ESR of the output capacitor. Determine C_{CP} as follows:

$$C_{CP} = (R_{ESR} \times C_{PVOUT1})/R_C \quad (12)$$

JUNCTION TEMPERATURE

In cases where the ambient temperature (T_A) is known, the thermal resistance parameter (θ_{JA}) can estimate the junction temperature rise (T_J). T_J is calculated with T_A and the power dissipation (P_D) using the following formula:

$$T_J = T_A + (P_D \times \theta_{JA}) \quad (13)$$

The typical θ_{JA} value for the 32-lead, 5 mm × 5 mm LFCSP is 46.91°C/W. An important factor to consider is that θ_{JA} is based on a 4-layer, 4 inches × 3 inches, 2.5 ounces copper PCB, as per the JEDEC standard, and applications may use different sizes and layers. It is important to maximize the copper used to remove the heat from the device. Copper exposed to air dissipates heat better than copper used in the inner layers. Connect the exposed pad to the ground plane with several vias.

If the case temperature can be measured, the junction temperature is calculated by

$$T_J = T_C + (P_D \times \theta_{JC}) \quad (14)$$

where:
T_C is the case temperature.
θ_{JC} is the junction to case thermal resistance provided in Table 6.

To achieve reliable operation of the buck converter and LDO regulator, the estimated die junction temperature of the ADP5003 must be less than 125°C. Reliability and mean time between failures (MTBF) is highly affected by increasing the junction temperature. Additional information about product reliability can be found in the Analog Devices, Inc., *Reliability Handbook* at www.analog.com/reliability_handbook.

The total power dissipation in the ADP5003 simplifies to

$$P_D = P_{DBUCK} + P_{DLDO} \quad (15)$$

where:
$P_{DBUCK} = (V_{PVIN1} \times I_{PVIN1}) - (V_{PVOUT1} \times I_{LOAD1})$.
$P_{DLDO} = ((V_{PVIN2} - V_{PVOUT2}) \times I_{LOAD2}) + (V_{PVIN2} \times I_{GND})$.

BUCK REGULATOR DESIGN EXAMPLE

This section provides an example of the step by step design procedures and the external components required for the buck regulator. Table 10 lists the design requirements for this example.

Table 10. Example Design Requirements for the Buck Regulator

Parameter	Specification
Input Voltage	V_{PVIN1} = 12 V
Output Voltage	V_{PVOUT1} = 2.5 V
Output Current	I_{LOAD1} = 3 A
Output Ripple	ΔV_{OUT1_RIPPLE} = 25 mV
Load Transient	±5% at 20% to 80% load transient

SETTING THE SWITCHING FREQUENCY FOR THE BUCK REGULATOR

The first step is to determine the switching frequency for the ADP5003 design. In general, higher switching frequencies produce a smaller solution size due to the lower component values required, whereas lower switching frequencies result in higher conversion efficiency due to lower switching losses.

The switching frequency of the ADP5003 can be set from 0.3 MHz to 2.5 MHz by connecting a resistor from the RT pin to ground. The selected resistor allows the user to make decisions based on the trade-off between efficiency and solution size. (For more information, see the Oscillator Frequency Control section.) However, the highest supported switching frequency must be assessed by checking the voltage conversion limitations enforced by the minimum on time and the minimum off time (see the Voltage Conversion Limitations section).

In this design example, a switching frequency of 600 kHz is used to achieve an ideal combination of small solution size and high conversion efficiency. To set the switching frequency to 600 kHz, use Equation 1 to calculate the resistor value, R_{RT}. This gives a standard resistor value of R_T = 294 kΩ.

SETTING THE OUTPUT VOLTAGE FOR THE BUCK REGULATOR

Select a value for the top resistor (R_{TOP1}) and then calculate the bottom feedback (R_{BOT1}) resistor by using the following equation:

$$R_{BOT1} = (R_{TOP1} \times V_{PVOUT1})/((V_{REFOUT} \times A_{BUCK}) - V_{PVOUT1}) \quad (16)$$

where:
V_{PVOUT1} is the buck output voltage.
V_{REFOUT} is 2 V.
A_{BUCK} is the buck regulator gain.

To set the output voltage to 2.5 V, R_{TOP1} is set to 100 kΩ, giving an R_{BOT1} value of 100 kΩ.

SELECTING THE INDUCTOR FOR THE BUCK REGULATOR

The peak-to-peak inductor ripple current, ΔI_L, is set to 35% of the maximum output current. Use Equation 8 to estimate the value of the inductor:

$$L = ((V_{PVIN1} - V_{PVOUT1}) \times D)/(\Delta I_L \times f_{SW})$$

where:
V_{PVIN1} = 12 V.
V_{PVOUT1} = 2.5 V.
D is the duty cycle ($D = V_{PVOUT1}/V_{PVIN1}$).
ΔI_L = 35% × 3 A = 1.05 A.
f_{SW} = 600 kHz.

The resulting value for L is 3.14 µH. The selected standard inductor value is 3.3 µH; therefore, ΔI_L is 1 A.

To calculate the peak inductor current (I_{PEAK}), use Equation 9:

$$I_{PEAK} = I_{LOAD1} + (\Delta I_L/2)$$

The calculated peak current for the inductor is 3.5 A.

SELECTING THE OUTPUT CAPACITOR FOR THE BUCK REGULATOR

The output capacitor must meet the output voltage ripple, load transient requirements and stability requirements. To meet the output voltage ripple requirement, use Equation 7 to calculate the capacitance:

$$C_{OUT\_MIN} \cong \frac{\Delta I_L}{8 \times f_{SW} \times (V_{RIPPLE} - \Delta I_L \times R_{ESR})}$$

The calculated capacitance, C_{OUT_MIN}, is 8.7 µF.

To meet the ±5% overshoot and undershoot requirements, use the following equations to calculate the capacitance:

$$C_{OUT\_UV} = \frac{K_{UV} \times \Delta I_{STEP}{}^2 \times L}{2 \times (V_{PVIN1} - V_{PVOUT1}) \times \Delta V_{OUT\_UV}} \quad (17)$$

$$C_{OUT\_OV} = \frac{K_{OV} \times \Delta I_{STEP}{}^2 \times L}{(V_{PVOUT1} + \Delta V_{OUT\_OV})^2 - V_{PVOUT1}{}^2} \quad (18)$$

where:
K_{UV} and K_{OV} are factors (typically set to 2).
ΔI_{STEP} is the load step.
ΔV_{OUT_UV} is the allowable undershoot on the output voltage.
ΔV_{OUT_OV} is the allowable overshoot on the output voltage.

For estimation purposes, use $K_{OV} = K_{UV} = 2$; therefore, C_{OUT_OV} = 33.4 µF and C_{OUT_UV} = 9 µF.

It is recommended to use two 22 µF ceramic capacitors.

DESIGNING THE COMPENSATION NETWORK FOR THE BUCK REGULATOR

For better load transient and stability performance, set the cross frequency, f_C, to $f_{SW}/10$. In this example, f_{SW} is set to 600 kHz; therefore, f_C is set to 60 kHz.

$$R_C = \frac{2 \times \pi \times 44\ \mu F \times 60\ kHz \times 2.5}{600\ \mu S \times 7\ A/V} = 9.87\ k\Omega$$

$$C_C = \frac{(0.833\ \Omega + 0.001\ \Omega) \times 44\ \mu F}{7.18\ k\Omega} = 3.72\ nF$$

$$C_{CP} = \frac{0.001\ \Omega \times 44\ \mu F}{7.18\ k\Omega} = 4.46\ pF$$

Choose standard components: R_C = 9.76 kΩ, C_C = 4.7 nF, C_{CP} = 4.7 pF.

Figure 47 shows the load transient waveform.

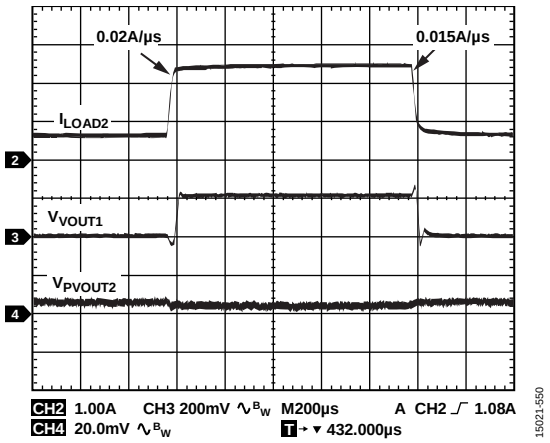


Figure 47. 0.6 A to 2.4 A Load Transient for 2.5 V Output, f_{SW} = 0.6 MHz, L = 3.3 µH, R_C = 9.76 kΩ, C_C = 4.7 nF, C_{CP} = 4.7 pF, C_{PVOUT1} = 44 µF

SELECTING THE INPUT CAPACITOR FOR THE BUCK REGULATOR

For the input capacitor, select a ceramic capacitor with a minimum capacitance of 10 µF. Place the input capacitor close to the PVIN1 pin. In this example, one 10 µF, X5R, 25 V ceramic capacitor is recommended.

ADAPTIVE HEADROOM CONTROL DESIGN EXAMPLE

This section provides an example of the step by step design procedures and the external components required for the buck regulator using adaptive headroom control. Table 11 lists the design requirements for this example.

Table 11. Example Design Requirements for the Buck Regulator Using Adaptive Headroom Control

Parameter	Specification
Input Voltage	V_{PVIN1} = 12 V
Output Voltage	V_{PVOUT2} = 1.3 V
Output Current	$I_{LOAD1} = I_{LOAD2}$ = 3 A
Buck Load Transient	±100 mV at 20% to 80% load transient

SETTING THE SWITCHING FREQUENCY FOR THE BUCK REGULATOR USING ADAPTIVE HEADROOM CONTROL

Similar to the buck design example, a switching frequency of 600 kHz is used to achieve a good combination of small solution size and high conversion efficiency. To set the switching frequency to 600 kHz, use Equation 1 to calculate the resistor value, R_{RT}:

$$R_{RT}\ (\text{k}\Omega) = 1.78 \times 10^{11}/f_{SW}\ (\text{kHz})$$

Therefore, select standard resistor R_T = 294 kΩ.

SETTING THE OUTPUT VOLTAGE FOR THE LDO REGULATOR USING ADAPTIVE HEADROOM CONTROL

Select a value for the top feedback resistor (R_{TOP2}) and then calculate the bottom resistor (R_{BOT2}) by using the following equation:

$$R_{BOT2} = (R_{TOP2} \times V_{PVOUT2})/((V_{REFOUT} \times A_{LDO}) - V_{PVOUT2}) \quad (19)$$

where:
V_{PVOUT2} is the LDO output voltage.
V_{REFOUT} is 2 V.
A_{LDO} is the LDO regulator gain.

To set the output voltage to 1.3 V, R_{TOP2} is set to 100 kΩ giving an R_{BOT2} value of 65 kΩ.

SELECTING THE INDUCTOR FOR THE BUCK REGULATOR USING ADAPTIVE HEADROOM CONTROL

The peak-to-peak inductor ripple current, ΔI_L, is set to 35% of the maximum output current. Use the Equation 8 to estimate the value of the inductor:

$$L = ((V_{PVIN1} - V_{PVOUT1}) \times D)/(\Delta I_L \times f_{SW})$$

where:
V_{PVIN1} = 12 V.
$V_{PVOUT1} = V_{PVOUT2} + V_{HR}$ = 1.7 V.
V_{PVOUT2} = 1.3 V.
V_{HR} is the adaptive headroom voltage at steady state current. See Table 4 and Figure 25 for the approximate values of V_{HR} vs. load current. For this example, use V_{HR} equal to 0.4 V for steady state load current of 3 A.
D is the duty cycle ($D = V_{VOUT1}/V_{PVIN1}$).
ΔI_L = 35% × 3 A = 1.05 A.
f_{SW} = 600 kHz.

The resulting value for L is 2.32 µH. The selected standard inductor value is 2.2 µH; therefore, ΔI_L is 1.1 A.

To calculate the peak inductor current (I_{PEAK}), use Equation 9:

$$I_{PEAK} = I_{LOAD1} + (\Delta I_L/2)$$

The calculated peak current for the inductor is 3.55 A.

SELECTING THE OUTPUT CAPACITORS FOR THE BUCK REGULATOR USING ADAPTIVE HEADROOM CONTROL

To ensure that the LDO regulator does not track the buck output, the undershoot voltage must be set to a value less than the minimum adaptive headroom voltage. Use Equation 17 and Equation 18 to calculate the capacitance.

For estimation purposes, use $K_{OV} = K_{UV} = 2$; therefore, C_{OUT_OV} = 40.7 µF and C_{OUT_UV} = 6.92 µF.

It is recommended to use a single 47 µF ceramic capacitor for the output of the buck and a single 10 µF for the output of the LDO.

DESIGNING THE COMPENSATION NETWORK FOR THE BUCK REGULATOR USING ADAPTIVE HEADROOM CONTROL

Due to the addition of the adaptive headroom scheme in the feedback loop, a lower bandwidth is required. Set the crossover frequency, f_C, to $f_{SW}/60$. In this example, f_{SW} is set to 600 kHz; therefore, f_C is set to 10 kHz.

$$R_C = \frac{2 \times \pi \times 47\ \mu F \times 10\ kHz \times 2.5}{600\ \mu S \times 7\ A/V} = 1.76\ k\Omega$$

$$C_C = \frac{(0.433\ \Omega + 0.001\ \Omega) \times 47\ \mu F}{1.76\ k\Omega} = 15.2\ nF$$

$$C_{CP} = \frac{0.001\ \Omega \times 47\ \mu F}{1.76\ k\Omega} = 26.7\ pF$$

Choose standard components: R_C = 1.74 kΩ, C_C = 22 nF, C_{CP} = 22 pF.

Figure 48 shows the load transient waveform.

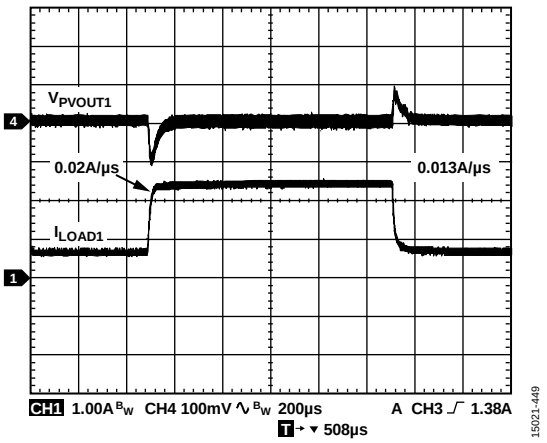


Figure 48. 0.6 A to 2.4 A Load Transient for 2.5 V Output, f_{SW} = 600 kHz, L = 2.2 µH, R_C = 1.74 kΩ, C_C = 22 nF, C_{CP} = 22 pF, C_{PVOUT1} = 47µF

SELECTING THE INPUT CAPACITOR FOR THE BUCK REGULATOR USING ADAPTIVE HEADROOM CONTROL

For the input capacitor, select a ceramic capacitor with a minimum value of 10 µF. Place the input capacitor close to the PVIN1 pin. In this example, one 10 µF, X5R, 25 V ceramic capacitor is recommended.

RECOMMENDED EXTERNAL COMPONENTS FOR THE BUCK REGULATOR

Table 12 lists the recommended external components for buck applications up to 3 A operation (±5% tolerance at an ~60% step transient), and Table 13 lists the recommended buck external components for adaptive headroom applications up to 3 A operation (V_{PVOUT2} ± 100 mV at an ~60% step transient).

Table 12. Recommended External Components for Buck Applications up to 3 A Operation (±5% Tolerance at an ~60% Step Transient)

f_{SW} (kHz)	V_{IN} (V)	V_{OUT} (V)	L (µH)	C_{OUT} (µF)	R_{TOP1} (kΩ)	R_{BOT1} (kΩ)	R_C (kΩ)	C_C (nF)	C_{CP} (pF)
300	12	1	3.3	210	200	49.9	23.7	3.3	10
	12	1.2	4.7	204.7	150	47.5	23.2	3.3	10
	12	1.5	4.7	147	174	75	16.5	4.7	10
	12	1.8	5.6	110	150	84.5	12.4	4.7	10
	12	2.5	6.8	69	100	100	7.68	6.8	10
	12	3.3	8.2	47	49.9	97.6	5.23	10	10
	12	5	10	26.7	0	open	3.01	15	10
	5	1	3.3	210	200	49.9	23.7	3.3	10
	5	1.2	3.3	147	150	47.5	16.5	3.3	10
	5	1.5	4.7	132	174	75	14.7	4.7	10
	5	1.8	4.7	94	150	84.5	10.5	4.7	10
	5	2.5	4.7	47	100	100	5.23	6.8	10
	5	3.3	4.7	51.7	49.9	97.6	5.76	10	10
600	12	1.5	2.2	69	150	84.5	15.4	2.2	4.7
	12	1.8	3.3	69	150	84.5	15.4	2.2	4.7
	12	2.5	3.3	32	100	100	7.15	3.3	4.7
	12	3.3	4.7	26.7	49.9	97.6	6.04	4.7	4.7
	12	5	5.6	22	0	Open	4.99	6.8	4.7
	5	1	1.5	94	200	49.9	21	1.5	4.7
	5	1.2	1.8	147	150	47.5	33.2	1.5	4.7
	5	1.5	1.8	49.2	174	75	11	2.2	4.7
	5	1.8	2.2	47	150	84.5	10.5	2.2	4.7
	5	2.5	2.2	23	100	100	5.11	3.3	4.7
	5	3.3	2.2	24.2	49.9	97.6	5.49	4.7	4.7
1000	12	2.5	2.2	22	100	100	8.25	2.2	2.2
	12	3.3	3.3	22	49.9	97.6	8.25	3.3	2.2
	12	5	3.3	22	0	Open	8.25	4.7	2.2
	5	1	1	69	200	49.9	25.5	1	2.2
	5	1.2	1	47	150	47.5	17.4	1	2.2
	5	1.5	1.2	32	174	75	12.1	1.5	2.2
	5	1.8	1.2	23	150	84.5	8.66	1.5	2.2
	5	2.5	1.5	22	100	100	8.25	2.2	2.2
	5	3.3	1.2	22	49.9	97.6	8.25	3.3	2.2

Table 13. Recommended Buck External Components for Adaptive Headroom Applications up to 3 A Operation (V_{PVOUT2} ± 100 mV at an ~60% Step Transient)

f_{SW} (kHz)	V_{IN} (V)	V_{OUT2} (V)	L (µH)	C_{OUT1} (µF)	R_C (kΩ)	C_C (nF)	C_{CP} (pF)	R_{TOP2} (kΩ)	R_{BOT2} (kΩ)	C_{OUT2} (µF)
600	12	3.3	4.7	47	1.74	33	22	Short	Open	10
	12	2.5	3.3	44	1.65	22	22	37.4	118	10
	12	1.8	3.3	57	2.15	22	22	100	121	10
	12	1.3	2.2	47	1.74	22	22	100	64.9	10
	12	1.1	1.8	47	1.74	10	22	100	49.9	10
	5	3.3	1.5	44	1.65	33	22	Short	Open	10
	5	2.5	1.8	32	1.21	22	22	37.4	118	10
	5	1.8	1.8	32	1.21	22	22	100	121	10
	5	1.3	1.8	44	1.65	22	22	100	64.9	10
	5	1.1	1.5	44	1.65	10	22	100	49.9	10

BUCK CONFIGURATIONS

INDEPENDENT

The buck and LDO regulators can operate independently of each other (see Figure 50) to provide two voltage rails from a single supply. In this way, the buck regulator can provide an intermediate supply rail for the LDO regulator with a fixed headroom voltage between the buck output voltage and the LDO output voltage. The LDO regulator acts to filter the voltage ripple and switching noise generated by the buck regulator for noise sensitive supplies. Where additional filtering is required, a second stage LC filter can be added between the buck output and the LDO input. Because the regulators are independently operated to provide a single voltage rail, the PSRR and efficiency can be configured as required by the application by either setting a lower headroom voltage for greater efficiency or a higher headroom voltage for greater PSRR.

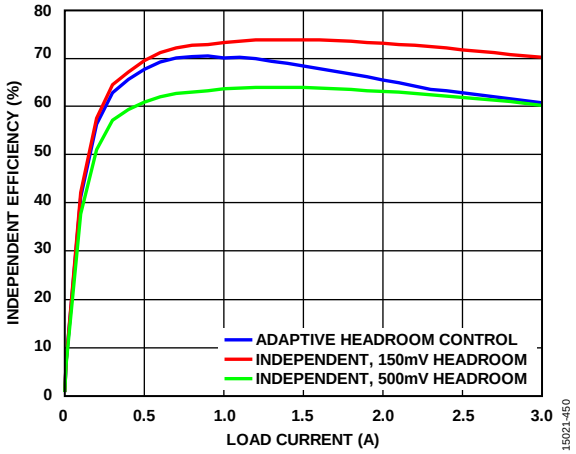


Figure 49. Efficiency vs. Load Current for Different Operating Modes

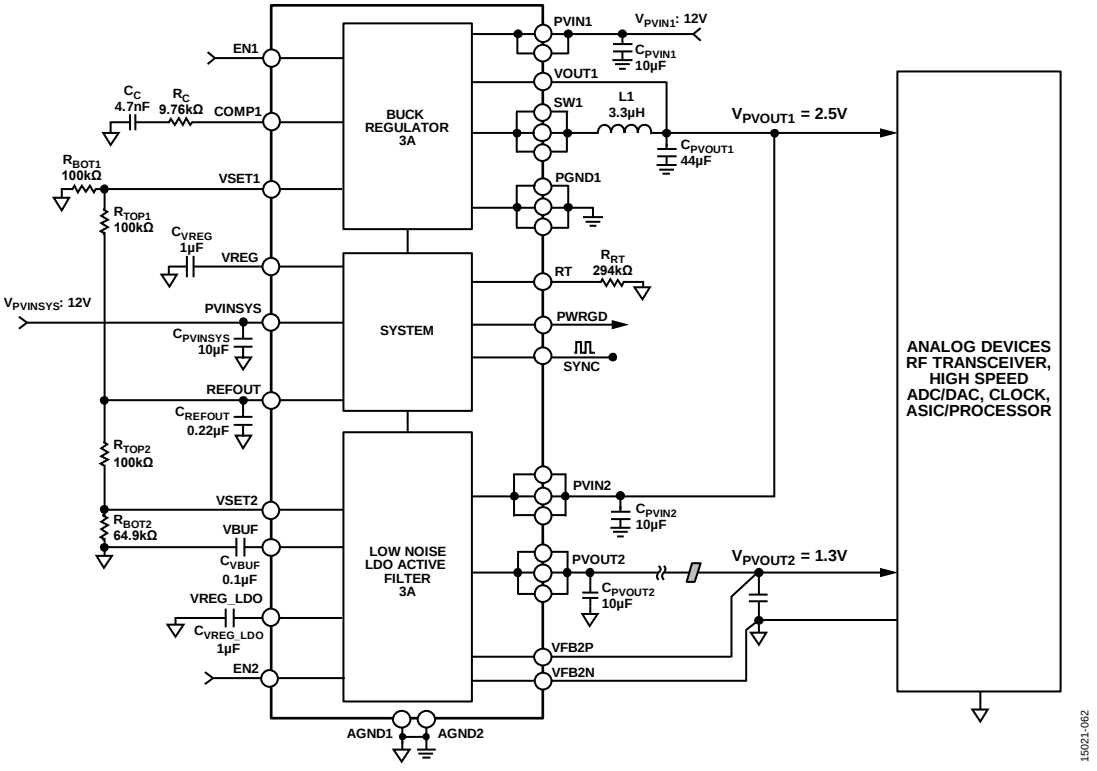


Figure 50. Independent Configuration (Dual Output)

ADAPTIVE HEADROOM

The ADP5003 features a scheme to control the buck regulator output voltage and thus the LDO headroom voltage to provide better efficiency with the same noise performance of a standalone LDO regulator. When the buck regulator uses the adaptive headroom control configuration, the ADP5003 manages the buck regulator output voltage vs. the LDO load current (see Figure 25). The adaptive headroom control also optimizes the LDO headroom when the remote sense feedback corrects any output voltage drop due to additional filtering or high trace impedance under high load conditions. The headroom profile of the adaptive headroom control is set to deliver a consistent PSRR across the load range while optimizing efficiency of the overall system (see Figure 51). To enable adaptive headroom control, connect VSET1 to VREG (see Figure 52).

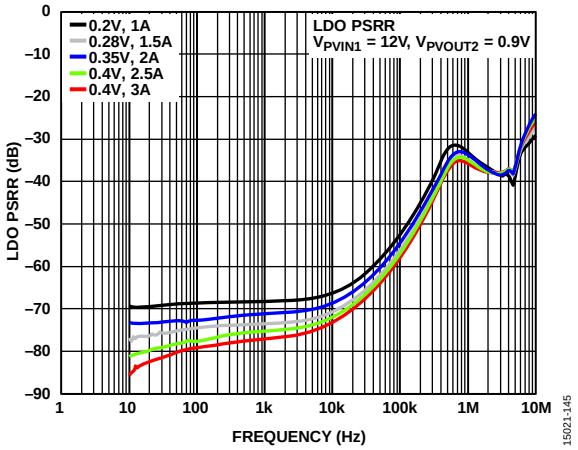


Figure 51. LDO PSRR vs. Frequency

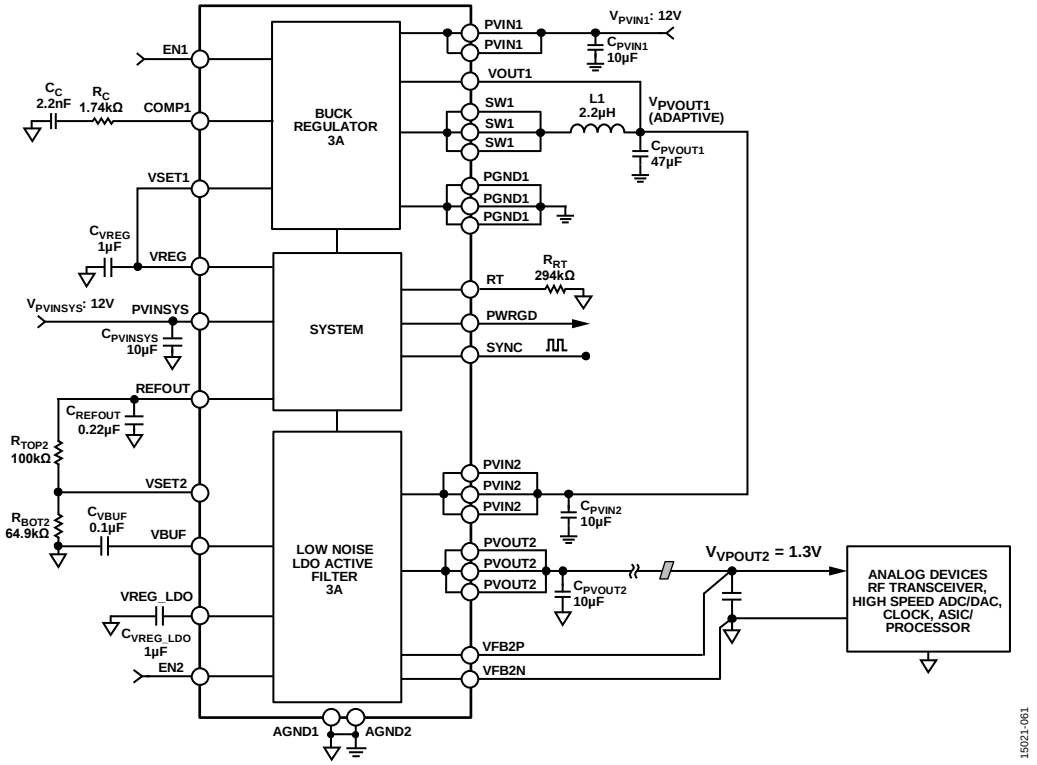


Figure 52. Adaptive Headroom Configuration

LAYOUT CONSIDERATIONS

Layout is important for all switching regulators but is particularly important for regulators with high switching frequencies. To achieve high efficiency, proper regulation, stability, and low noise, a well designed PCB layout is required. Follow these guidelines when designing PCBs:

- Keep high current loops as short and wide as possible.
  - Keep the input bypass capacitors close to the PVIN1, PVIN2, and PVINSYS pins.
  - Keep the inductor and output capacitor close to SW1 and PGND1.
- Route the VFB2P and VFB2N LDO sense traces side by side connecting them each as close as possible to the point of load. Keep them as short as possible and away from noise sources.
- Place the frequency setting resistor close to the RT pin. Keep AGND1 and PGND1 separate on the top layer of the board. This separation avoids pollution of AGND1 with switching noise. Do not connect PGND1 to the EPAD on the top layer of the layout. Connect both AGND1 and PGND1 to the board ground plane with vias. Ideally, connect PGND1 to the plane at a point between the input and output capacitors.
- Connect the negative terminal of C_{VBUF} to the VFB2N pin.

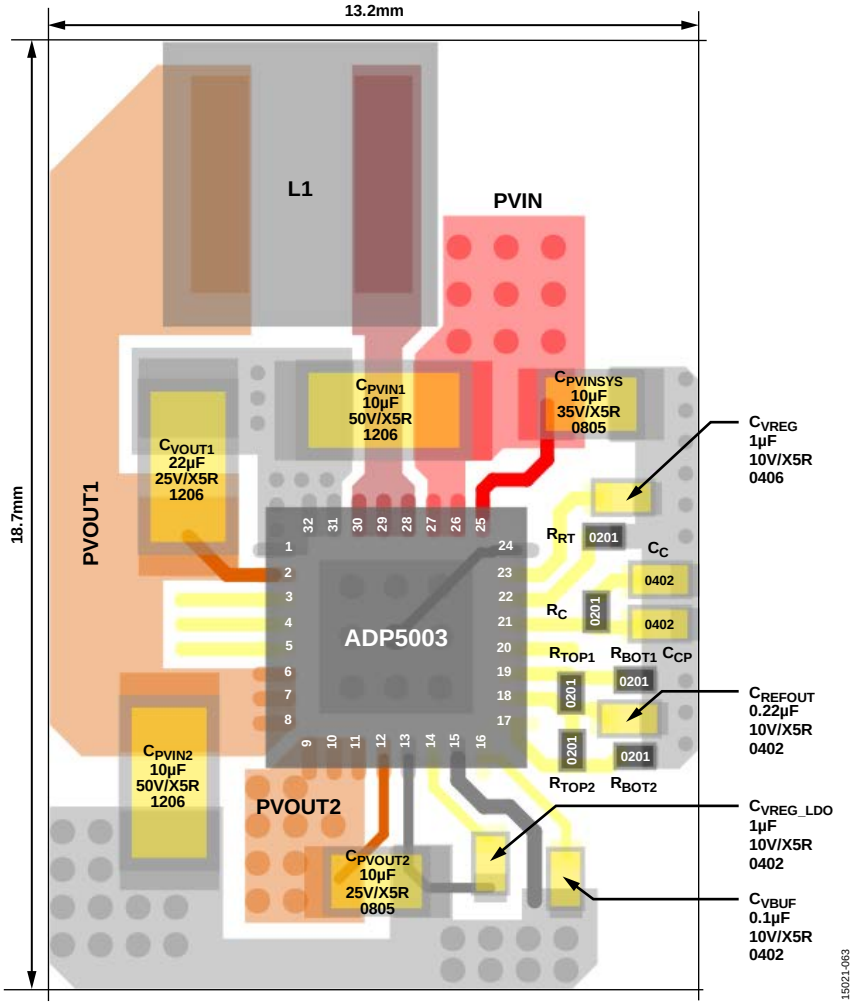
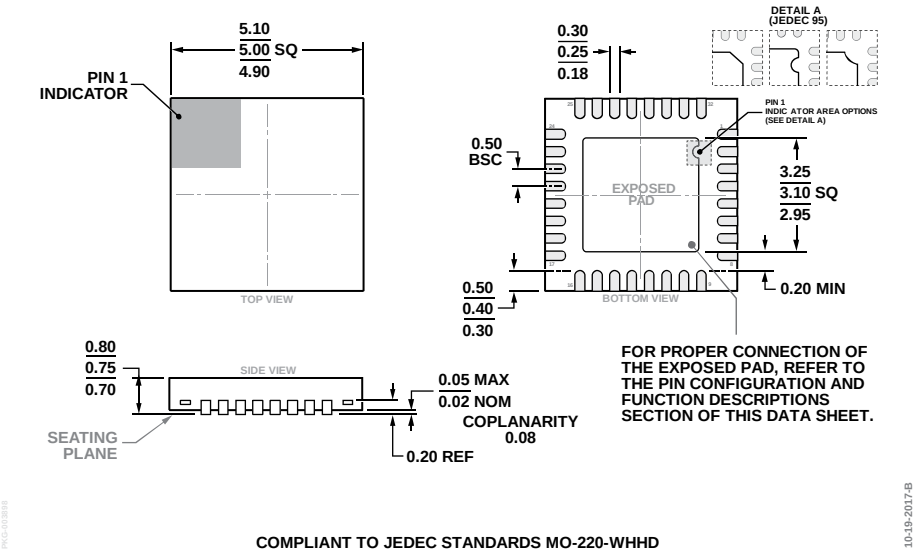


Figure 53. Example Outline Layout

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WHHD

Figure 54. 32-Lead Lead Frame Chip Scale Package [LFCSP]
5 mm × 5 mm Body and 0.75 mm Package Height
(CP-32-7)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADP5003ACPZ-R7	−40°C to +125°C	32-Lead Lead Frame Chip Scale Package [LFCSP]	CP-32-7
ADP5003CP-EVALZ		Evaluation Board	

[1] Z = RoHS Compliant Part.

D15021-0-3/19(A)

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ADP5003CP-EVALZ ADP5003ACPZ-R7