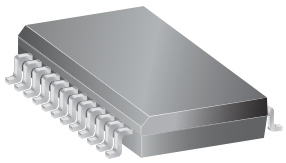
A3967

Microstepping Driver with Translator

FEATURES AND BENEFITS

- ±750 mA, 30 V output rating
- Satlington® sink drivers
- Automatic current-decay mode detection/selection
- 3.0 to 5.5 V logic supply voltage range
- Mixed, fast, and slow current-decay modes
- Internal UVLO and thermal shutdown circuitry
- Crossover-current protection

PACKAGE: 24-pin SOIC with internally fused pins (suffix LB)



Not to scale

DESCRIPTION

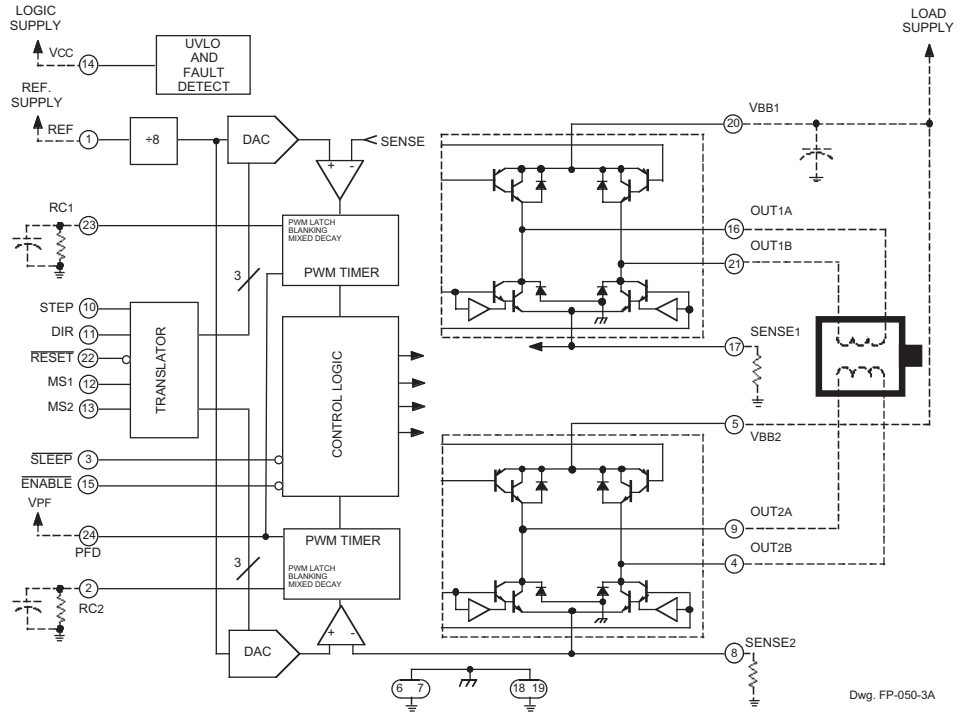
The A3967 is a complete microstepping motor driver with built-in translator. It is designed to operate bipolar stepper motors in full-, half-, quarter-, and eighth-step modes, with output drive capability of 30 V and ±750 mA. The A3967 includes a fixed off-time current regulator that has the ability to operate in slow, fast, or mixed current-decay modes. This current-decay control scheme results in reduced audible motor noise, increased step accuracy, and reduced power dissipation.

The translator is the key to the easy implementation of the A3967. By simply inputting one pulse on the STEP input the motor will take one step (full, half, quarter, or eighth depending on two logic inputs). There are no phase-sequence tables, high-frequency control lines, or complex interfaces to program. The A3967 interface is an ideal fit for applications where a complex µP is unavailable or overburdened.

Internal circuit protection includes thermal shutdown with hysteresis, undervoltage lockout (UVLO) and crossover-current protection. Special power-up sequencing is not required.

The A3967 is supplied in a 24-pin SOIC, which is lead (Pb) free with 100% matte tin leadframe plating. Four pins are fused internally for enhanced thermal dissipation. The pins are at ground potential and need no insulation.

Functional Block Diagram



SELECTION GUIDE

Part Number	Packing	Package
A3967SLBTR-T	24-pin SOIC with internally fused pins	1000 per reel

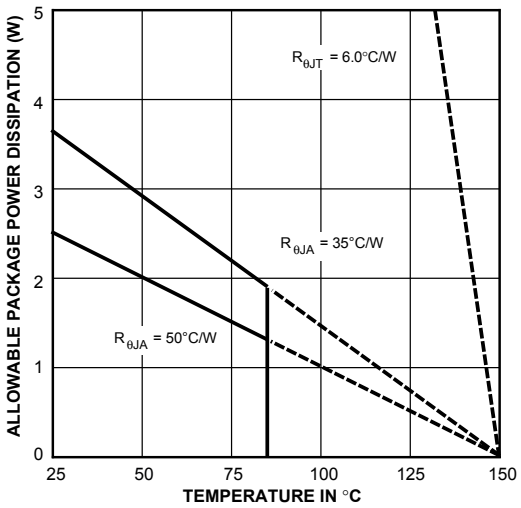
ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Notes		Rating	Units
Load Supply Voltage	V_{BB}			30	V
Logic Supply Voltage	V_{CC}			7.0	V
Logic Input Voltage Range	V_{IN}	t_w > 30 ns		–0.3 to 7.0	V
		t_w < 30 ns		–1 to 7.0	V
Sense Voltage	V_{SENSE}			0.68	V
Reference Voltage	V_{REF}			V_{CC}	mA
Output Current	I_{OUT}	Output current rating may be limited by duty cycle, ambient temperature, and heat sinking. Under any set of conditions, do not exceed the specified current rating or a junction temperature of 150°C.	Continuous	±750	mA
			Peak	±850	mA
Package Power Dissipation	P_D	See graph		–	–
Operating Ambient Temperature	T_A	Range S		–20 to 85	°C
Maximum Junction Temperature	T_J(max)	Fault conditions that produce excessive junction temperature will activate the device's thermal shutdown circuitry. These conditions can be tolerated but should be avoided.		150	°C
Storage Temperature	T_{stg}			–55 to 150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Test Conditions*	Value	Units
Package Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	2-layer PCB, 1.3 in² 2-oz. exposed copper	50	°C/W
		4-layer PCB, based on JEDEC standard	35	°C/W

*Additional thermal information available on Allegro website.



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ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{BB} = 30 V, V_{CC} = 3.0 V to 5.5V (unless otherwise noted)

Characteristic	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Output Drivers						
Load Supply Voltage Range	V_{BB}	Operating	4.75	–	30	V
		During sleep mode	0	–	30	V
Output Leakage Current	I_{CEX}	V_{OUT} = V_{BB}	–	<1.0	20	µA
		V_{OUT} = 0 V	–	<-1.0	-20	µA
Output Saturation Voltage	$V_{CE(sat)}$	Source driver, I_{OUT} = -750 mA	–	1.9	2.1	V
		Source driver, I_{OUT} = -400 mA	–	1.7	2.0	V
		Sink driver, I_{OUT} = 750 mA	–	0.65	1.3	V
		Sink driver, I_{OUT} = 400 mA	–	0.21	0.5	V
Clamp Diode Forward Voltage	V_F	I_F = 750 mA	–	1.4	1.6	V
		I_F = 400 mA	–	1.1	1.4	V
Motor Supply Current	I_{BB}	Outputs enabled	–	–	5.0	mA
		RESET high	–	–	200	µA
		Sleep mode	–	–	20	µA
Control Logic						
Logic Supply Voltage Range	V_{CC}	Operating	3.0	5.0	5.5	V
Logic Input Voltage	$V_{IN(1)}$		0.7V_{CC}	–	–	V
	$V_{IN(0)}$		–	–	0.3V_{CC}	V
Logic Input Current	$I_{IN(1)}$	V_{IN} = 0.7V_{CC}	-20	<1.0	20	µA
	$I_{IN(0)}$	V_{IN} = 0.3V_{CC}	-20	<1.0	20	µA
Maximum STEP Frequency	f_{STEP}		500*	–	–	kHz
Blank Time	t_{BLANK}	R_t = 56 kΩ, C_t = 680 pF	700	950	1200	ns
Fixed Off Time	t_{off}	R_t = 56 kΩ, C_t = 680 pF	30	38	46	µs

continued next page …

Table 1. Microstep Resolution Truth Table

MS1	MS2	Resolution
L	L	Full step (2 phase)
H	L	Half step
L	H	Quarter step
H	H	Eighth step

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ELECTRICAL CHARACTERISTICS (continued) at T_A = +25°C, V_{BB} = 30 V, V_{CC} = 3.0 V to 5.5V (unless otherwise noted)

Characteristic	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Control Logic (cont'd)						
Mixed Decay Trip Point	PFDH		–	$0.6V_{CC}$	–	V
	PFDL		–	$0.21V_{CC}$	–	V
Ref. Input Voltage Range	V_{REF}	Operating	1.0	–	V_{CC}	V
Reference Input Impedance	Z_{REF}		120	160	200	kΩ
Gain (G_m) Error (note 3)	E_G	V_{REF} = 2 V, Phase Current = 38.37% †	–	–	±10	%
		V_{REF} = 2 V, Phase Current = 70.71% †	–	–	±5.0	%
		V_{REF} = 2 V, Phase Current = 100.00% †	–	–	±5.0	%
Thermal Shutdown Temp.	T_J		–	165	–	°C
Thermal Shutdown Hysteresis	ΔT_J		–	15	–	°C
UVLO Enable Threshold	V_{UVLO}	Increasing V_{CC}	2.45	2.7	2.95	V
UVLO Hysteresis	ΔV_{UVLO}		0.05	0.10	–	V
Logic Supply Current	I_{CC}	Outputs enabled	–	50	65	mA
		Outputs off	–	–	9.0	mA
		Sleep mode	–	–	20	µA

* Operation at a step frequency greater than the specified minimum value is possible but not warranteed.
† 8 microstep/step operation.

NOTES: 1. Typical Data is for design information only.
2. Negative current is defined as coming out of (sourcing) the specified device terminal.
3. $E_G = ([V_{REF}/8] – V_{SENSE})/(V_{REF}/8)$

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FUNCTIONAL DESCRIPTION

Device Operation. The A3967 is a complete microstepping motor driver with built in translator for easy operation with minimal control lines. It is designed to operate bipolar stepper motors in full-, half-, quarter- and eighth-step modes. The current in each of the two output full bridges is regulated with fixed off time pulse-width modulated (PWM) control circuitry. The full-bridge current at each step is set by the value of an external current sense resistor (R_S), a reference voltage (V_{REF}), and the DACs output voltage controlled by the output of the translator.

At power up, or reset, the translator sets the DACs and phase current polarity to initial home state (see figures for home-state conditions), and sets the current regulator for both phases to mixed-decay mode. When a step command signal occurs on the STEP input the translator automatically sequences the DACs to the next level (see table 2 for the current level sequence and current polarity). The microstep resolution is set by inputs MS_1 and MS_2 as shown in table 1. If the new DAC output level is lower than the previous level the decay mode for that full bridge will be set by the PFD input (fast, slow or mixed decay). If the new DAC level is higher or equal to the previous level then the decay mode for that Full bridge will be slow decay. This automatic current-decay selection will improve microstepping performance by reducing the distortion of the current waveform due to the motor BEMF.

Reset Input ($\overline{\text{RESET}}$). The RESET input (active low) sets the translator to a predefined home state (see figures for home state conditions) and turns off all of the outputs. STEP inputs are ignored until the RESET input goes high.

Step Input (STEP). A low-to-high transition on the STEP input sequences the translator and advances the motor one increment. The translator controls the input to the DACs and the direction of current flow in each winding. The size of the increment is determined by the state of inputs MS_1 and MS_2 (see table 1).

Microstep Select (MS_1 and MS_2). Input terminals MS1 and MS_2 select the microstepping format per table 1. Changes to these inputs do not take effect until the STEP command (see figure).

Direction Input (DIR). The state of the DIRECTION input will determine the direction of rotation of the motor.

Internal PWM Current Control. Each full bridge is controlled by a fixed off-time PWM current-control circuit that limits the load current to a desired value (I_{TRIP}). Initially, a diagonal pair of source and sink outputs are enabled and current flows through the motor winding and R_S. When the voltage across the current-sense resistor equals the DAC output voltage, the current-sense comparator resets the PWM latch, which turns off the source driver (slow-decay mode) or the sink and source drivers (fast- or mixed-decay modes).

The maximum value of current limiting is set by the selection of R_S and the voltage at the V_{REF} input with a transconductance function approximated by:

$$I_{TRIP}max = V_{REF}/8R_S$$

The DAC output reduces the V_{REF} output to the current-sense comparator in precise steps (see table 2 for % I_{TRIP}-max at each step).

$$I_{TRIP} = (\%\ I_{TRIP}max/100) \times I_{TRIP}max$$

Fixed Off-Time. The internal PWM current-control circuitry uses a one shot to control the time the driver(s) remain(s) off. The one shot off-time, t_{off}, is determined by the selection of an external resistor (R_T) and capacitor (C_T) connected from the RC timing terminal to ground. The off time, over a range of values of C_T = 470 pF to 1500 pF and R_T = 12 kΩ to 100 kΩ is approximated by:

$$t_{off} = R_T C_T$$

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FUNCTIONAL DESCRIPTION (continued)

RC Blanking. In addition to the fixed off-time of the PWM control circuit, the C_T component sets the comparator blanking time. This function blanks the output of the current-sense comparator when the outputs are switched by the internal current-control circuitry. The comparator output is blanked to prevent false overcurrent detection due to reverse recovery currents of the clamp diodes, and/or switching transients related to the capacitance of the load. The blank time t_{BLANK} can be approximated by:

$$t_{BLANK} = 1400C_T$$

Enable Input ($\overline{\text{ENABLE}}$). This active-low input enables all of the outputs. When logic high the outputs are disabled. Inputs to the translator (STEP, DIRECTION, MS_1, MS_2) are all active independent of the ENABLE input state.

Shutdown. In the event of a fault (excessive junction temperature) the outputs of the device are disabled until the fault condition is removed. At power up, and in the event of low V_{CC}, the under-voltage lockout (UVLO) circuit disables the drivers and resets the translator to the home state.

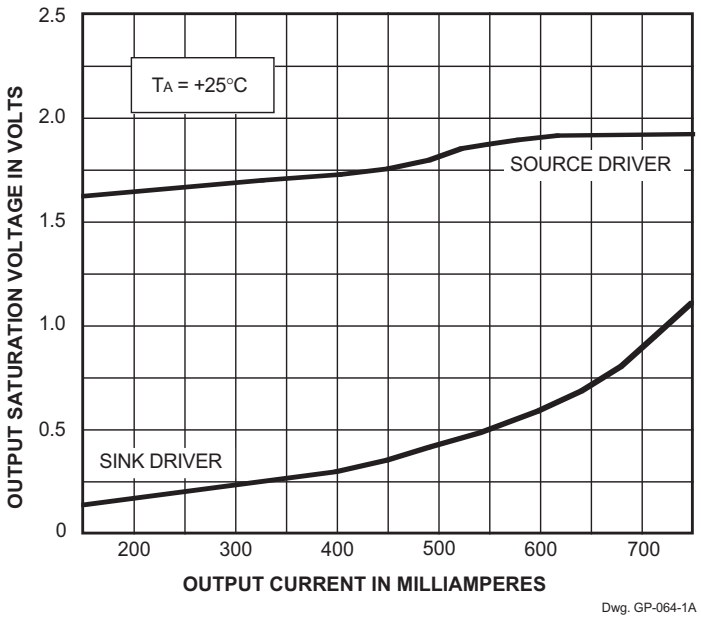
Sleep Mode ($\overline{\text{SLEEP}}$). An active-low control input used to minimize power consumption when not in use. This disables much of the internal circuitry including the outputs. A logic high allows normal operation and startup of the device in the home position.

Percent Fast Decay Input (PFD). When a STEP input signal commands a lower output current from the previous step, it switches the output current decay to either slow-, fast-, or mixed-decay depending on the voltage level at the PFD input. If the voltage at the PFD input is greater than $0.6V_{CC}$ then slow-decay mode is selected. If the voltage on the PFD input is less than $0.21V_{CC}$ then fast-decay mode is selected. Mixed decay is between these two levels.

Mixed Decay Operation. If the voltage on the PFD input is between $0.6V_{CC}$ and $0.21V_{CC}$, the bridge will operate in mixed-decay mode depending on the step sequence (see figures). As the trip point is reached, the device will go into fast-decay mode until the voltage on the RC terminal decays to the voltage applied to the PFD terminal. The time that the device operates in fast decay is approximated by:

$$t_{FD} = R_T C_T \ln (0.6V_{CC}/V_{PFD})$$

After this fast decay portion, t_{FD}, the device will switch to slow-decay mode for the remainder of the fixed off-time period.



Typical output saturation voltages showing Satlington sink-driver operation.

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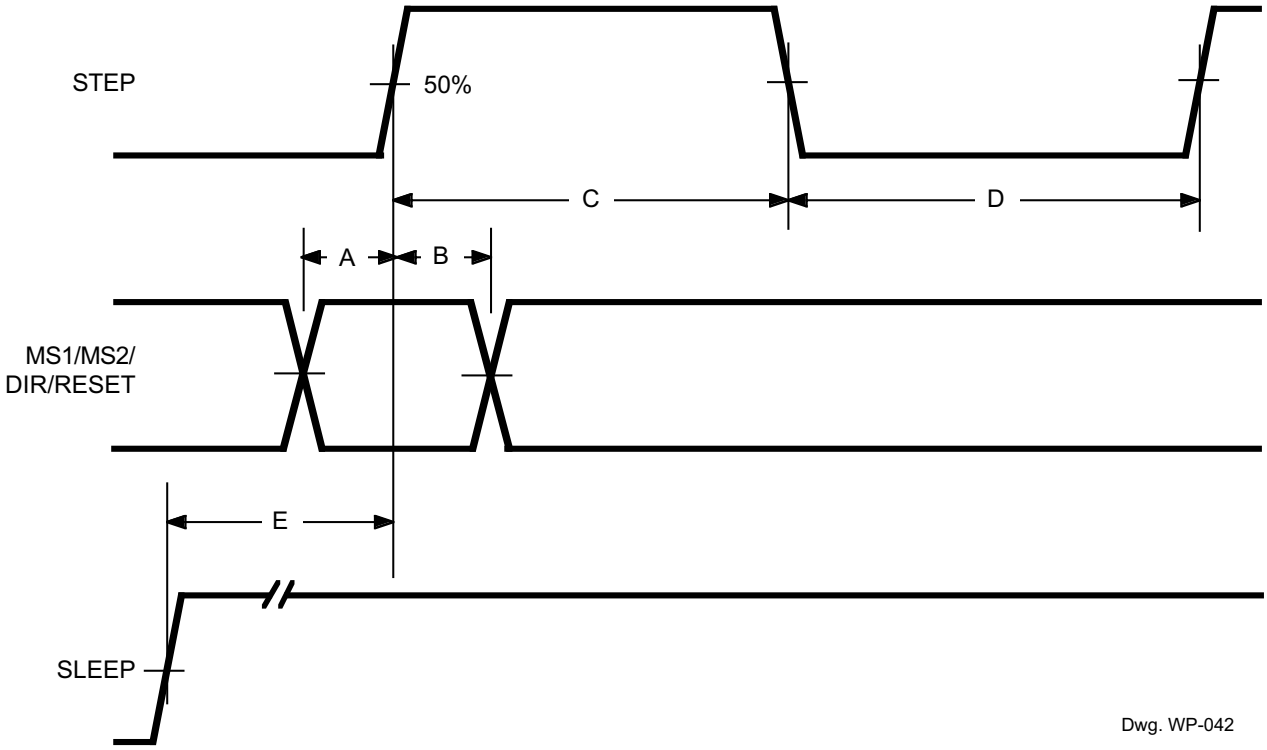
Timing Requirements
(T_A = +25°C, V_{CC} = 5 V, Logic Levels are V_{CC} and Ground)



A. Minimum Command Active Time
Before Step Pulse (Data Set-Up Time) ..... 200 ns

B. Minimum Command Active Time
After Step Pulse (Data Hold Time) ..... 200 ns

C. Minimum STEP Pulse Width ..... 1.0 µs

D. Minimum STEP Low Time ..... 1.0 µs

E. Maximum Wake-Up Time ..... 1.0 ms

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APPLICATIONS INFORMATION

Layout. The printed wiring board should use a heavy ground plane.

For optimum electrical and thermal performance, the driver should be soldered directly onto the board.

The load supply terminal, V_{BB}, should be decoupled with an electrolytic capacitor (>47 µF is recommended) placed as close to the device as possible.

To avoid problems due to capacitive coupling of the high dv/dt switching transients, route the bridge-output traces away from the sensitive logic-input traces. Always drive the logic inputs with a low source impedance to increase noise immunity.

Grounding. A star ground system located close to the driver is recommended.

The 24-lead SOIC has the analog ground and the power ground internally bonded to the power tabs of the package (leads 6, 7, 18, and 19).

Current Sensing. To minimize inaccuracies caused by ground-trace IR drops in sensing the output current level, the current-sense resistor (R_S) should have an independent ground return to the star ground of the device. This path should be as short as possible. For low-value sense resistors the IR drops in the printed wiring board sense resistor's traces can be significant and should be taken into account. The use of sockets should be avoided as they can introduce variation in R_S due to their contact resistance.

Allegro MicroSystems recommends a value of R_S given by

$$R_S = 0.5/I_{TRIP}max$$

Thermal protection. Circuitry turns off all drivers when the junction temperature reaches 165°C, typically. It is intended only to protect the device from failures due to excessive junction temperatures and should not imply that output short circuits are permitted. Thermal shutdown has a hysteresis of approximately 15°C.

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Table 2. Step Sequencing

Home State = 45º Step Angle, DIR = H

Full Step	Half Step	¼ Step	⅛ Step	Phase 1 Current ($\%I_{trip}$max) (%)	Phase 2 Current ($\%I_{trip}$max) (%)	Step Angle (º)
	1	1	1	100.00	0.00	0.0
			2	98.08	19.51	11.3
		2	3	92.39	38.27	22.5
			4	83.15	55.56	33.8
1	2	3	5	70.71	70.71	45.0
			6	55.56	83.15	56.3
		4	7	38.27	92.39	67.5
			8	19.51	98.08	78.8
	3	5	9	0.00	100.00	90.0
			10	–19.51	98.08	101.3
		6	11	–38.27	92.39	112.5
			12	–55.56	83.15	123.8
2	4	7	13	–70.71	70.71	135.0
			14	–83.15	55.56	146.3
		8	15	–92.39	38.27	157.5
			16	–98.08	19.51	168.8
	5	9	17	–100.00	0.00	180.0
			18	–98.08	–19.51	191.3
		10	19	–92.39	–38.27	202.5
			20	–83.15	–55.56	213.8
3	6	11	21	–70.71	–70.71	225.0
			22	–55.56	–83.15	236.3
		12	23	–38.27	–92.39	247.5
			24	–19.51	–98.08	258.8
	7	13	25	0.00	–100.00	270.0
			26	19.51	–98.08	281.3
		14	27	38.27	–92.39	292.5
			28	55.56	–83.15	303.8
4	8	15	29	70.71	–70.71	315.0
			30	83.15	–55.56	326.3
		16	31	92.39	–38.27	337.5
			32	98.08	–19.51	348.8

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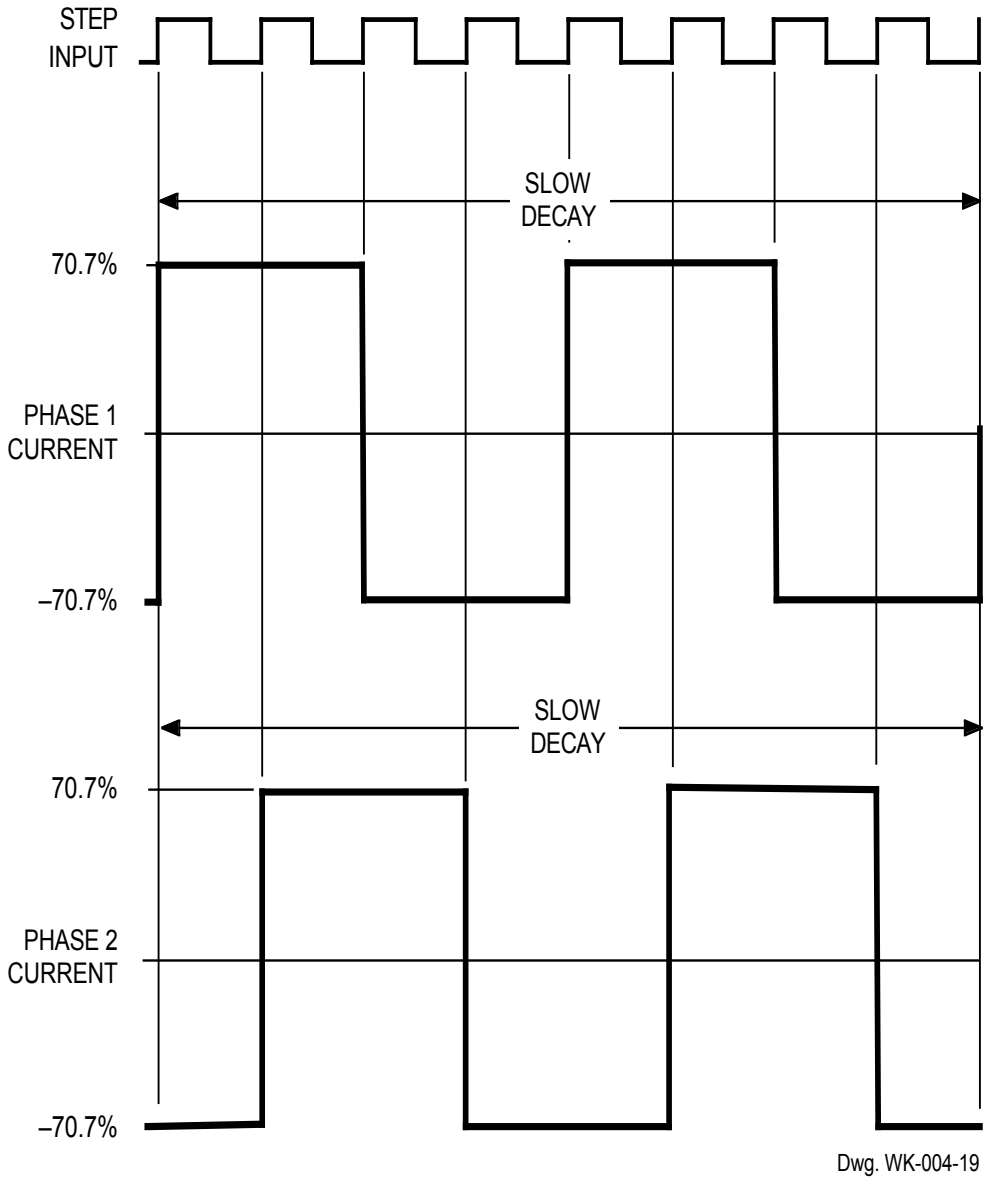
Full Step Operation
$MS_1 = MS_2 = L$, DIR = H



The vector addition of the output currents at any step is 100%.

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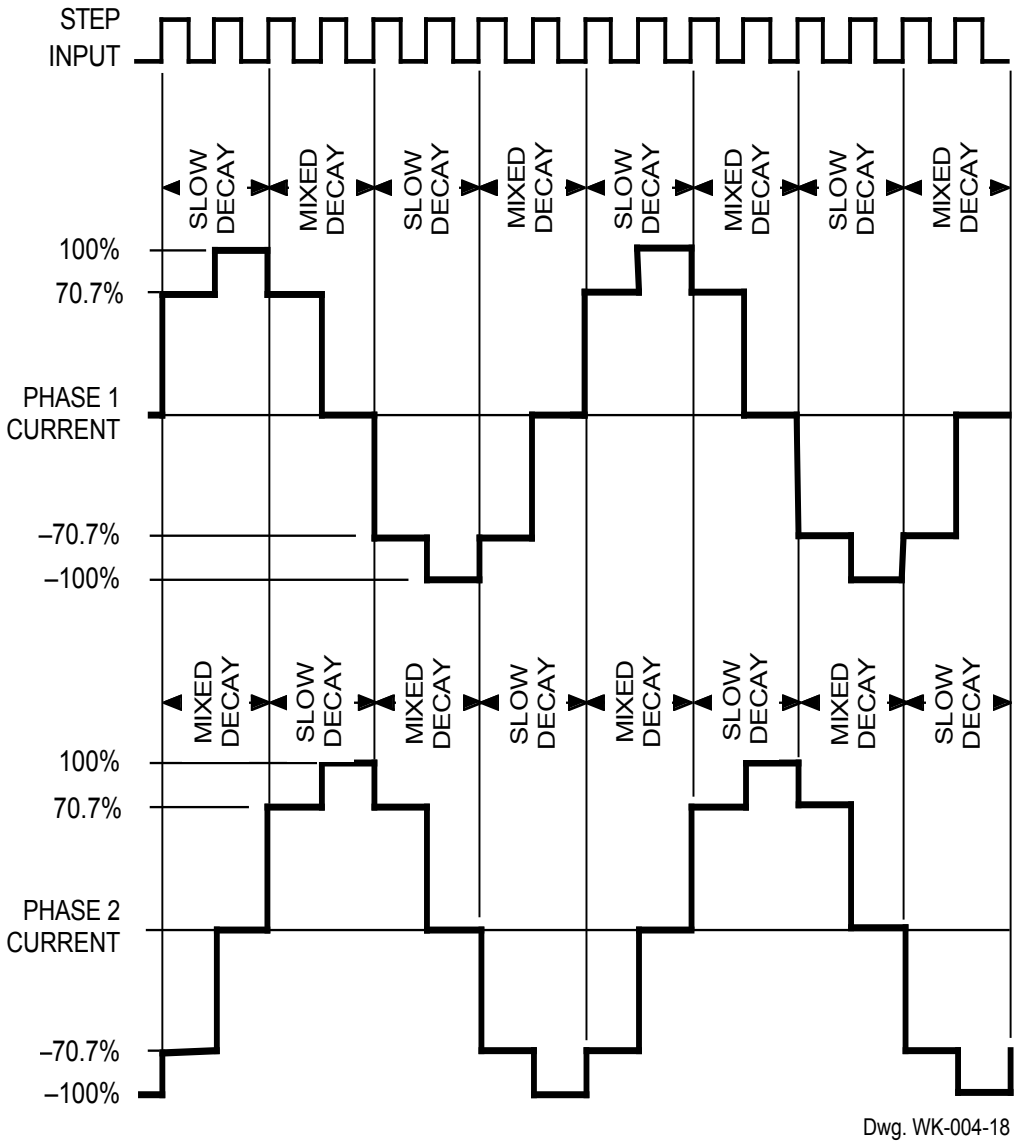
Half Step Operation
MS_1 = H, MS_2 = L, DIR = H



The mixed-decay mode is controlled by the percent fast decay voltage (V_{PFD}). If the voltage at the PFD input is greater than $0.6V_{CC}$ then slow-decay mode is selected. If the voltage on the PFD input is less than $0.21V_{CC}$ then fast-decay mode is selected. Mixed decay is between these two levels.

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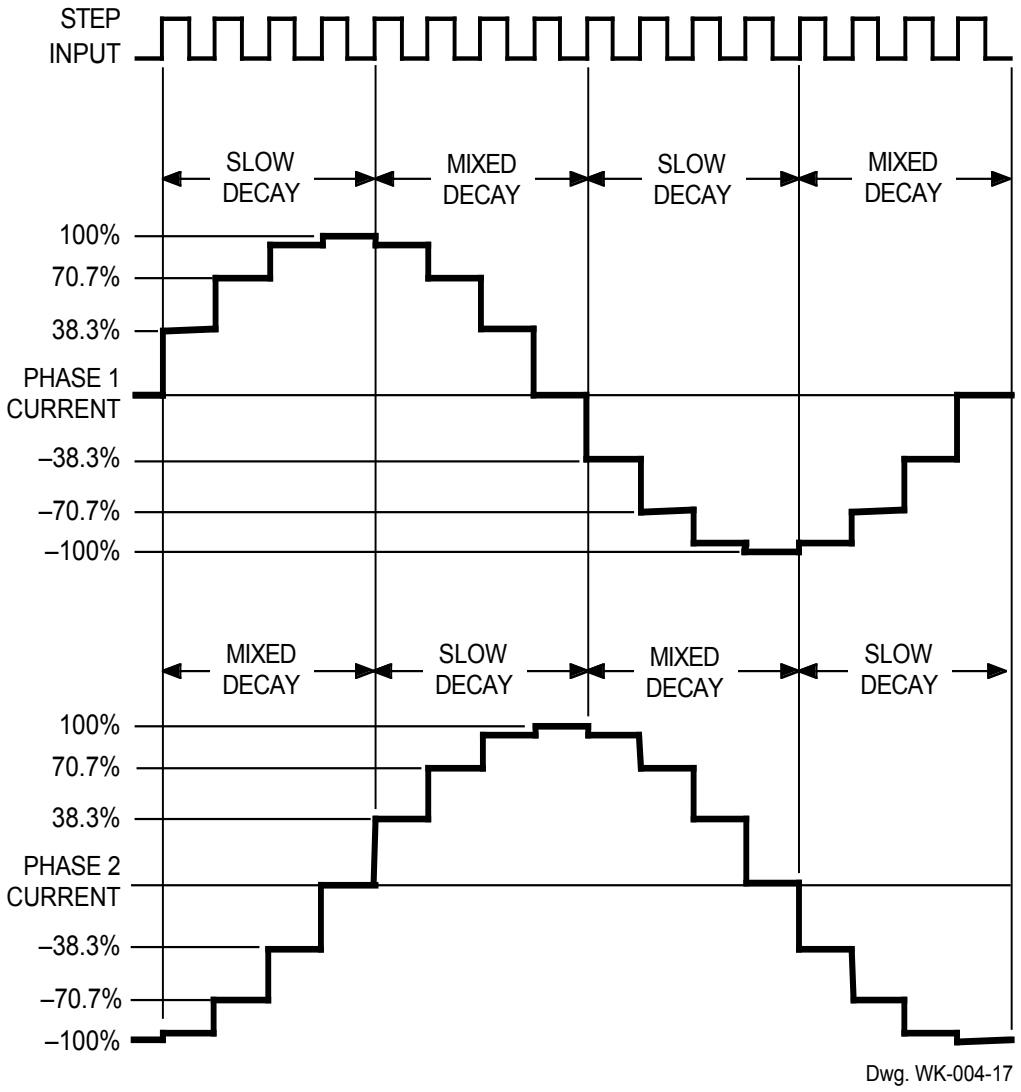
Quarter Step Operation
MS_1 = L, MS_2 = H, DIR = H



The mixed-decay mode is controlled by the percent fast decay voltage (V_{PFD}). If the voltage at the PFD input is greater than $0.6V_{CC}$ then slow-decay mode is selected. If the voltage on the PFD input is less than $0.21V_{CC}$ then fast-decay mode is selected. Mixed decay is between these two levels.

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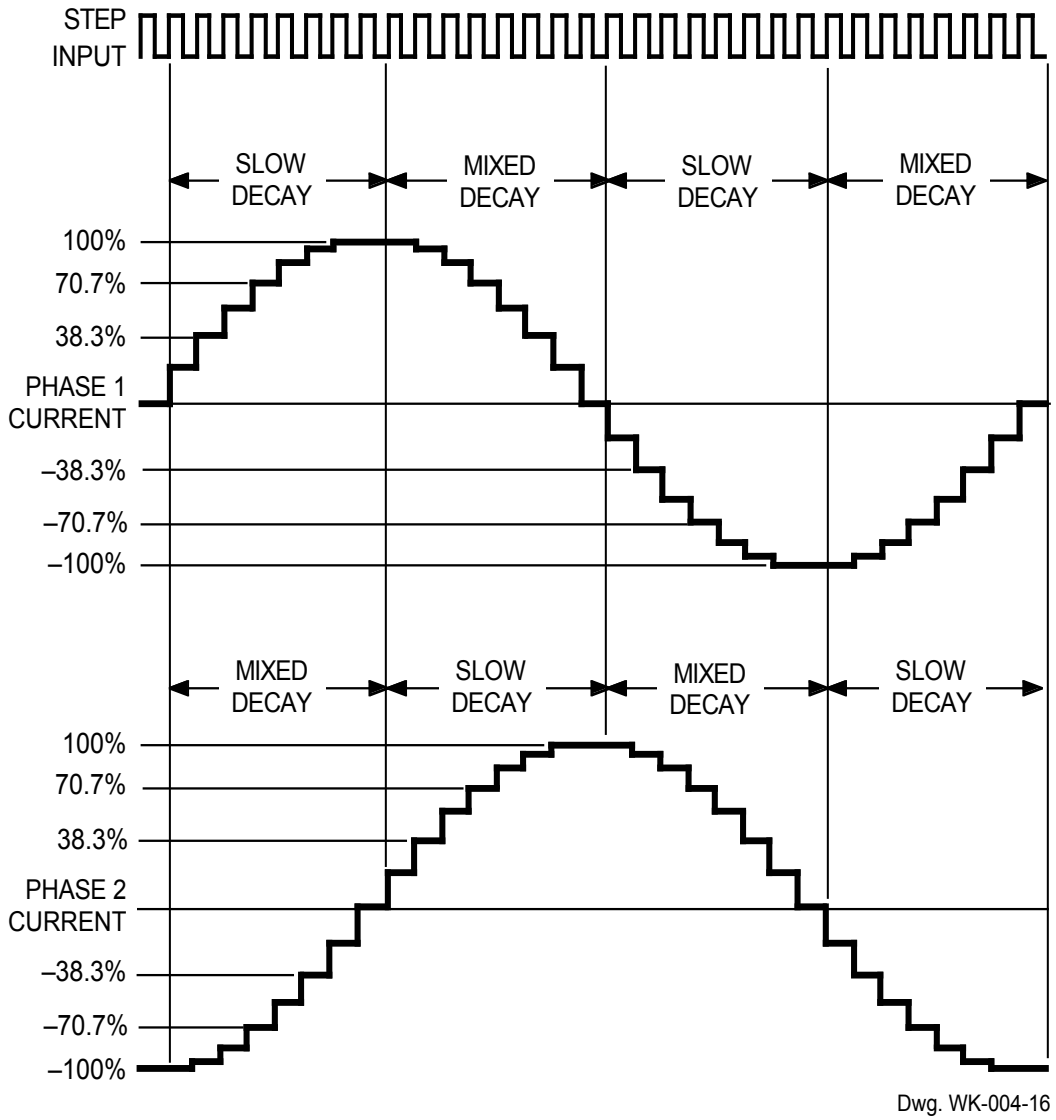
8 Microstep/Step Operation
$MS_1 = MS_2 = H$, DIR = H



The mixed-decay mode is controlled by the percent fast decay voltage (V_{PFD}). If the voltage at the PFD input is greater than $0.6V_{CC}$ then slow-decay mode is selected. If the voltage on the PFD input is less than $0.21V_{CC}$ then fast-decay mode is selected. Mixed decay is between these two levels.

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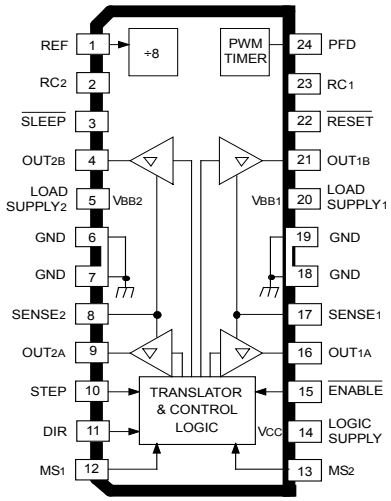
Pinout Diagram



Dwg. PP-075-2

Terminal List

Terminal Name	Terminal Description	Terminal Number
REF	Gm reference input	1
RC2	Analog input for fixed offtime – bridge 2	2
SLEEP	Logic input	3
OUT2B	H bridge 2 output B	4
LOAD SUPPLY2	VBB2, the load supply for bridge 2	5
GND	Analog and power ground	6, 7
SENSE2	Sense resistor for bridge 2	8
OUT2A	H bridge 2 output A	9
STEP	Logic input	10
DIR	Logic Input	11
MS1	Logic input	12
MS2	Logic input	13
LOGIC SUPPLY	VCC, the logic supply voltage	14
ENABLE	Logic input	15
OUT1A	H bridge 1 output A	16
SENSE1	Sense resistor for bridge 1	17
GND	Analog and power ground	18, 19
LOAD SUPPLY1	VBB1, the load supply for bridge 1	20
OUT1B	H bridge 1 output B	21
RESET	Logic input	22
RC1	Analog Input for fixed offtime – bridge 1	23
PFD	Mixed decay setting	24

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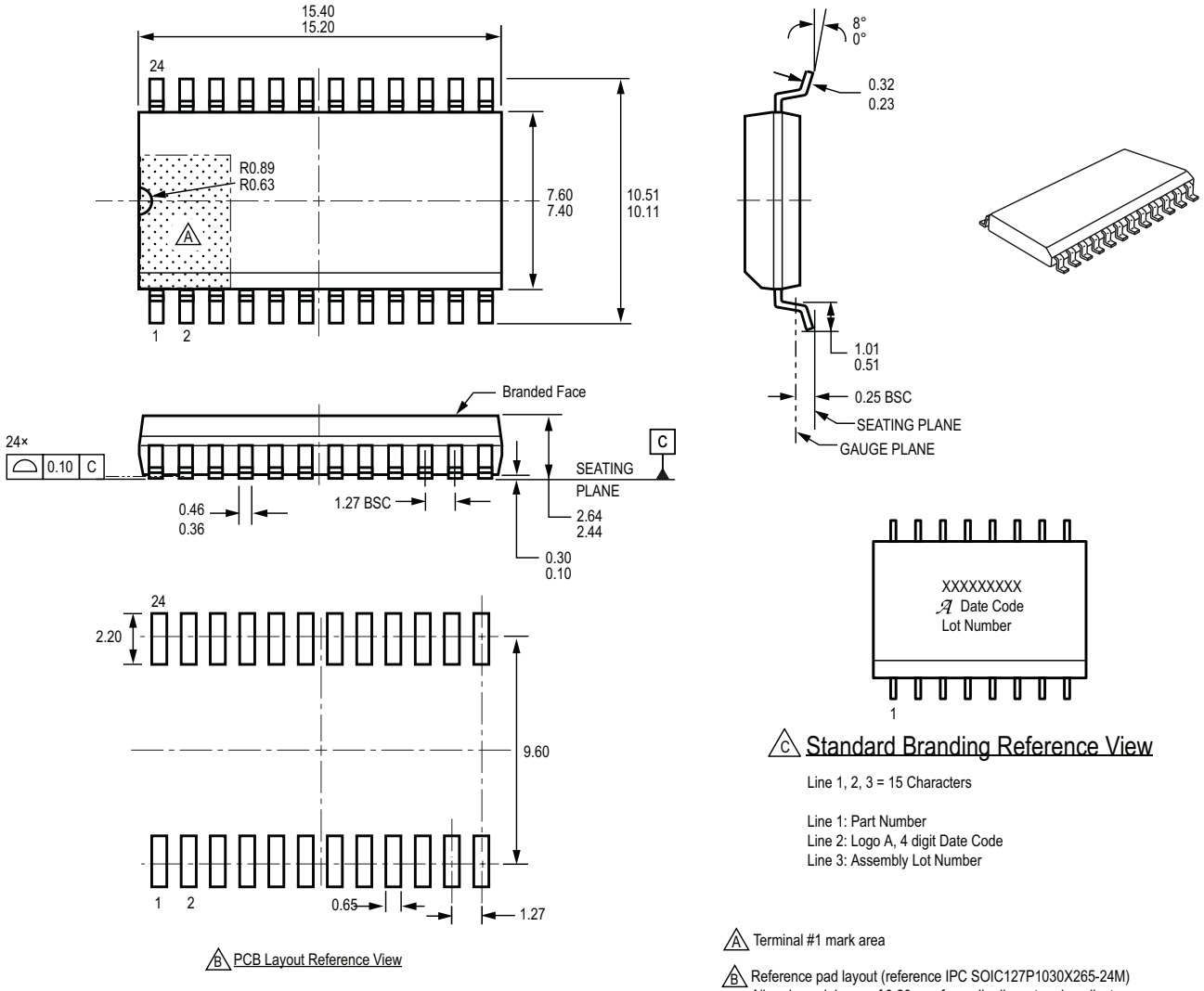
Package LB 24-Pin SOIC

For Reference Only – Not for Tooling Use

(Reference Allegro DWG-0000388, Rev. 1 and JEDEC MS-013AD)
NOT TO SCALE
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown
Internal configuration of fused pins is device-dependent



B PCB Layout Reference View

C Standard Branding Reference View

Line 1, 2, 3 = 15 Characters

Line 1: Part Number
Line 2: Logo A, 4 digit Date Code
Line 3: Assembly Lot Number

A Terminal #1 mark area

B Reference pad layout (reference IPC SOIC127P1030X265-24M)
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances

C Branding scale and appearance at supplier discretion

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REVISION HISTORY

Number	Date	Description
9	November 1, 2019	Minor editorial updates
10	October 21, 2022	Updated package drawing (page 15)

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