REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

Prepared in accordance with ASME Y14.24

Vendor item drawing

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PMIC N/A	**PREPARED BY** RICK OFFICER	**DLA LAND AND MARITIME** **COLUMBUS, OHIO 43218-3990** **https://www.dla.mil/LandandMaritime**
Original date of drawing YY-MM-DD 20-12-15	**CHECKED BY** RAJESH PITHADIA **APPROVED BY** JAMES R. ESCHMEYER	TITLE MICROCIRCUIT,LINEAR, MMIC, pHEMT 0.4 GHz TO 11 GHz LOW NOISE AMPLIFIER, GALLIUM ARSENIDE
	SIZE **A** / **CODE IDENT. NO.** **16236**	**DWG NO.** **V62/21602**
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AMSC N/A

5962-V013-21

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance gallium arsenide (GaAs) monolithic microwave integrated circuit (MMIC), pseudomorphic high electron mobility transistor (pHEMT) 0.4 GHZ to 11 GHz low noise amplifier microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/21602	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	HMC8412TCPZ-EP	GaAs, MMIC, pHEMT 0.4 GHZ to 11 GHz low noise amplifier

1.2.2 Case outline(s). The case outline(s) are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	6	See figure 1	Lead frame chip scale package (LFCSP)

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

1.3 Absolute maximum ratings. 1/

Supply voltage (V_{DD}) ..... +7 V
RF input power ..... 25 dBm
Continuous power dissipation (P_D) :
T_{CASE} = +85°C ..... 0.82 W
T_{CASE} = +125°C ..... 0.46 W
Storage temperature range (T_{STG}) ..... -65°C to +125°C
Peak reflow (moisture sensitivity level 1 (MSL1)) ..... +260°C
Junction temperature (T_J) to maintain 1,000,000 hours mean time to failure (MTTF)..... +175°C
Nominal junction temperature (TA = +125°C, V_{DD} = 5 V, I_{DQ} = 60 mA) ..... +157.8°C
Thermal resistance, junction to case (θ_{JC}) ..... 109.3°C/W
Electrostatic discharge (ESD) rating:
Human body model (HDM) per JEDEC JS-001 ..... ±500 V

1.4 Recommended operating conditions. 2/

Supply voltage (V_{DD}) ..... +5 V
Operating temperature range (T_A) ..... -55°C to +125°C

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

JEDEC JS-001 – Human Body Model Testing of Integrated Circuits
JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at https://www.jedec.org.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Interface schematics. The interface schematic shall be as shown in figures 3, 4, 5, and 6.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Frequency range		0.4 GHz to 3 GHz					
Frequency range			+25°C	01	0.4	3	GHz
Gain			+25°C	01	15.5 typical		dB
					13		
Gain variation over temperature			-55°C to +125°C	01	0.005 typical		dB/°C
Noise figure	NF		+25°C	01	1.4 typical		dB
Return loss							
Input			+25°C	01	14 typical		dB
Output			+25°C	01	13 typical		dB
Output							
Power for 1 dB compression	OP1dB		+25°C	01	18 typical		dBm
					15		
Saturated output power	P_{SAT}		+25°C	01	20.5 typical		dBm
Third order intercept	OIP3	Measurement taken at output power (P_{OUT}) per tone = 0 dBm	+25°C	01	32 typical		dBm
Second order intercept	OIP2	Measurement taken at output power (P_{OUT}) per tone = 0 dBm	+25°C	01	40 typical		dBm
Power added efficiency	PAE	Measure at PSAT	+25°C	01	28 typical		%
Supply							
Supply current	I_{DQ}		+25°C	01	60 typical		mA
Supply voltage	V_{DD}		+25°C	01	5 typical		V
					2	6	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Frequency range		3 GHz to 9 GHz					
Frequency range			+25°C	01	3	9	GHz
Gain			+25°C	01	15 typical		dB
					13		
Gain variation over temperature			-55°C to +125°C	01	0.007 typical		dB/°C
Noise figure	NF		+25°C	01	1.5 typical		dB
Return loss							
Input			+25°C	01	15 typical		dB
Output			+25°C	01	16 typical		dB
Output							
Power for 1 dB compression	OP1dB		+25°C	01	18 typical		dBm
					15.5		
Saturated output power	P_{SAT}		+25°C	01	20.5 typical		dBm
Third order intercept	OIP3	Measurement taken at output power (P_{OUT}) per tone = 0 dBm	+25°C	01	33 typical		dBm
Second order intercept	OIP2	Measurement taken at output power (P_{OUT}) per tone = 0 dBm	+25°C	01	41.5 typical		dBm
Power added efficiency	PAE	Measure at PSAT	+25°C	01	29 typical		%
Supply							
Supply current	I_{DQ}		+25°C	01	60 typical		mA
Supply voltage	V_{DD}		+25°C	01	5 typical		V
					2	6	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Frequency range		9 GHz to 11 GHz					
Frequency range			+25°C	01	9	11	GHz
Gain			+25°C	01	14 typical		dB
					12		
Gain variation over temperature			-55°C to +125°C	01	0.012 typical		dB/°C
Noise figure	NF		+25°C	01	1.8 typical		dB
Return loss							
Input			+25°C	01	14 typical		dB
Output			+25°C	01	10 typical		dB
Output							
Power for 1 dB compression	OP1dB		+25°C	01	14 typical		dBm
					11		
Saturated output power	P_{SAT}		+25°C	01	18 typical		dBm
Third order intercept	OIP3	Measurement taken at output power (P_{OUT}) per tone = 0 dBm	+25°C	01	31 typical		dBm
Second order intercept	OIP2	Measurement taken at output power (P_{OUT}) per tone = 0 dBm	+25°C	01	49.5 typical		dBm
Power added efficiency	PAE	Measure at PSAT	+25°C	01	15.5 typical		%
Supply							
Supply current	I_{DQ}		+25°C	01	60 typical		mA
Supply voltage	V_{DD}		+25°C	01	5 typical		V
					2	6	

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ Unless otherwise specified, V_{DD} = +5 V, supply current (I_{DQ}) = 60 mA, R_{BIAS} = 1.47 kΩ, and T_A = +25°C.

Case X

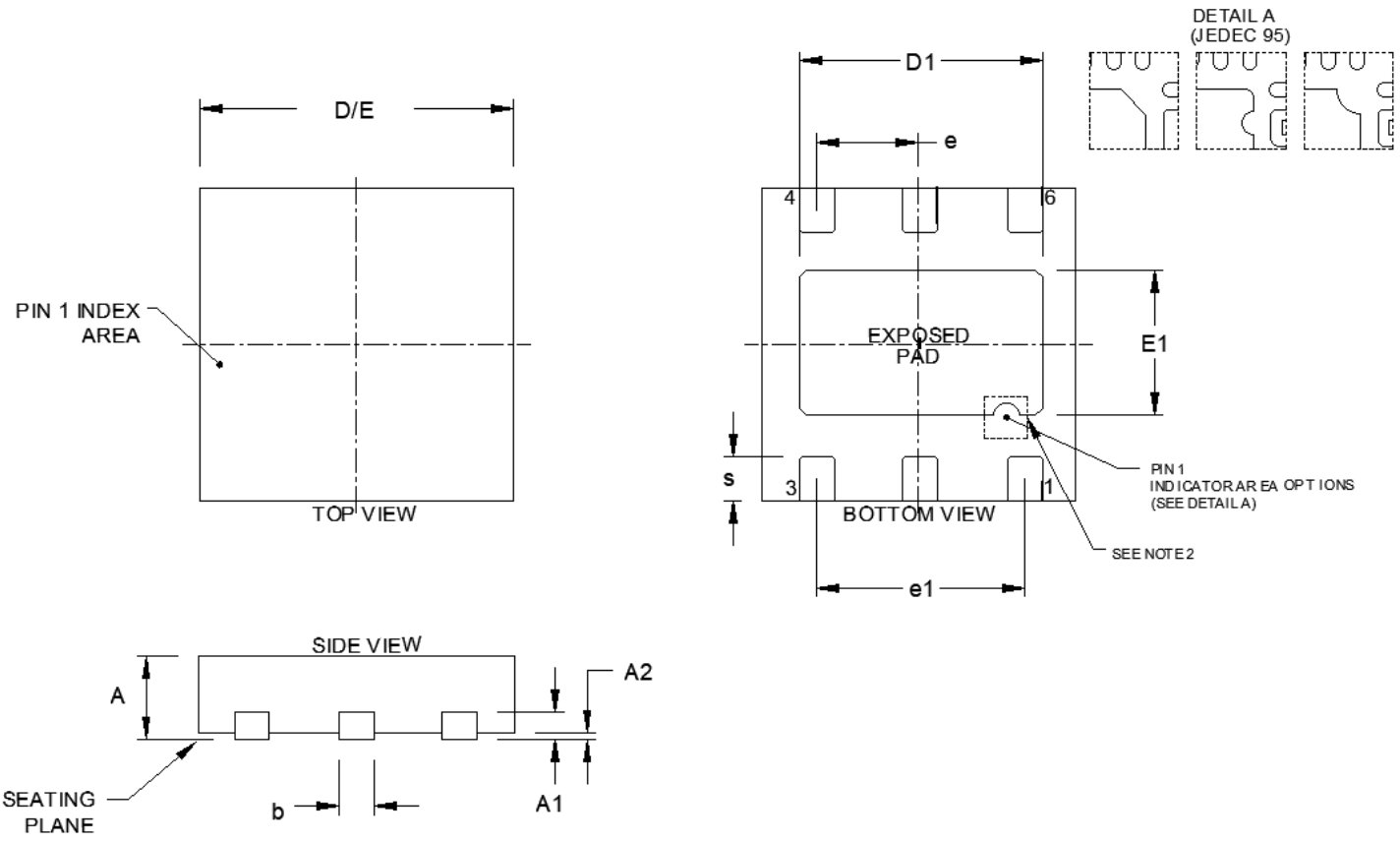

FIGURE 1. Case outline.

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/21602
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Symbol	Dimensions					
	Inches			Millimeters		
	Minimum	Nominal	Maximum	Minimum	Nominal	Maximum
A	.031	.033	.035	0.80	0.85	0.90
A1	.008 REF			0.203 REF		
A2		.001 NOM	.002		0.02 NOM	0.050
b	.009	.012	.014	0.25	0.30	0.35
D/E	.077	.079	.081	1.95	2.00	2.05
D1	.059	.063	.067	1.50	1.60	1.70
E1	.035	.039	.043	0.90	1.00	1.10
e	.025 BSC			0.65 BSC		
e1	.051 REF			1.30 REF		
s	.008	.010	.012	0.20	0.25	0.30

NOTES:
1. Controlling dimensions are millimeter, inch dimensions are given for reference only.
2. For proper connection of the exposed pad, refer to the pin configuration and function descriptions section of the manufacturer's datasheet.

FIGURE 1. Case outline - Continued.

Device type	01	
Case outline	X	
Terminal number	Terminal symbol	Description
1	R_{BIAS}	Current mirror bias resistor. Use the RBIAS pin to set the quiescent current by connecting the external bias resistor. Refer to the manufacturer's data sheet for the bias resistor connection and for recommended bias resistor values. See figure 3 for the interface schematic.
2	GND	Ground. The GND pin must be connected to RF and dc ground. See figure 4 for the interface schematic.
3	RF_{IN}	RF input. The RF_{IN} pin is ac-coupled and matched to 50 Ω. See figure 5 for the interface schematic.
4	RF_{OUT}	RF output. The RFOUT pin is ac-coupled and matched to 50 Ω. See figure 6 for the interface schematic.
5	GND	Ground. The GND pin must be connected to RF and dc ground. See figure 4 for the interface schematic.
6	V_{DD}	Drain supply voltage for the amplifier. See figure 6 for the interface schematic.
	EPAD	Exposed pad. The exposed pad must be connected to the RF and dc ground.

FIGURE 2. Terminal connections.

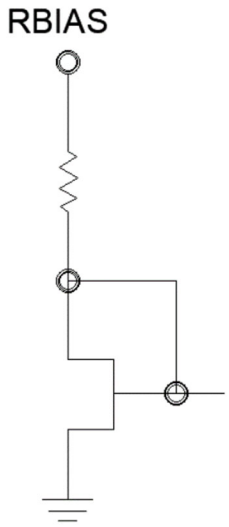

FIGURE 3. R_{BIAS} interface schematic.

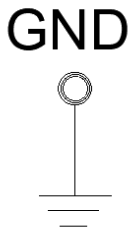

FIGURE 4. GND interface schematic.

FIGURE 5. RF_{IN} interface schematic.

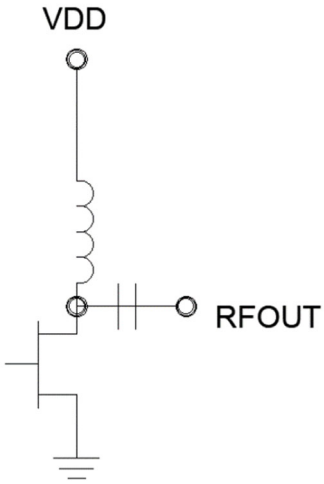

FIGURE 6. V_{DD} and RF_{OUT} interface schematic.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Mode of transportation and quantity	Top side marking	Vendor part number
V62/21602-01XE	24355	Cut tape, 500 or 1 units	Y7X	HMC8412TCPZ-EP-PT
		Reel, 500 units	Y7X	HMC8412TCPZ-EP-R7

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code

24355

Source of supply

Analog Devices
Route 1 Industrial Park
P.O. Box 9106
Norwood, MA 02062
Point of contact: 20 Alpha Road
Chelmsford, MA 01824-4123