

74LVT244A; 74LVTH244A

3.3 V octal buffer/line driver; 3-state

Rev. 6 — 24 August 2020

Product data sheet

1. General description

The 74LVT244A; 74LVTH244A is a high-performance BiCMOS product designed for V_{CC} operation at 3.3 V.

This device is an octal buffer that is ideal for driving bus lines. The device features two output enables ($\overline{1OE}$, $\overline{2OE}$), each controlling four of the 3-state outputs.

2. Features and benefits

- Octal bus interface
- 3-state buffers
- Output capability: +64 mA and -32 mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5 V supply
- Bus hold data inputs eliminate need for external pull-up resistors to hold unused inputs
- Live insertion and extraction permitted
- Power-up 3-state
- No bus current loading when output is tied to 5 V bus
- Latch-up protection
 - JESD78 Class II exceeds 500 mA
- ESD protection:
 - HBM JESD22-A114E exceeds 2000 V
 - MM JESD22-A115-A exceeds 200 V

3. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74LVT244AD	-40 °C to +85 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
74LVTH244AD				
74LVT244ADB	-40 °C to +85 °C	SSOP20	plastic shrink small outline package; 20 leads; body width 5.3 mm	SOT339-1
74LVTH244ADB				
74LVT244APW	-40 °C to +85 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1
74LVTH244APW				
74LVT244ABQ	-40 °C to +85 °C	DHVQFN20	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 × 4.5 × 0.85 mm	SOT764-1
74LVTH244ABQ				

4. Functional diagram

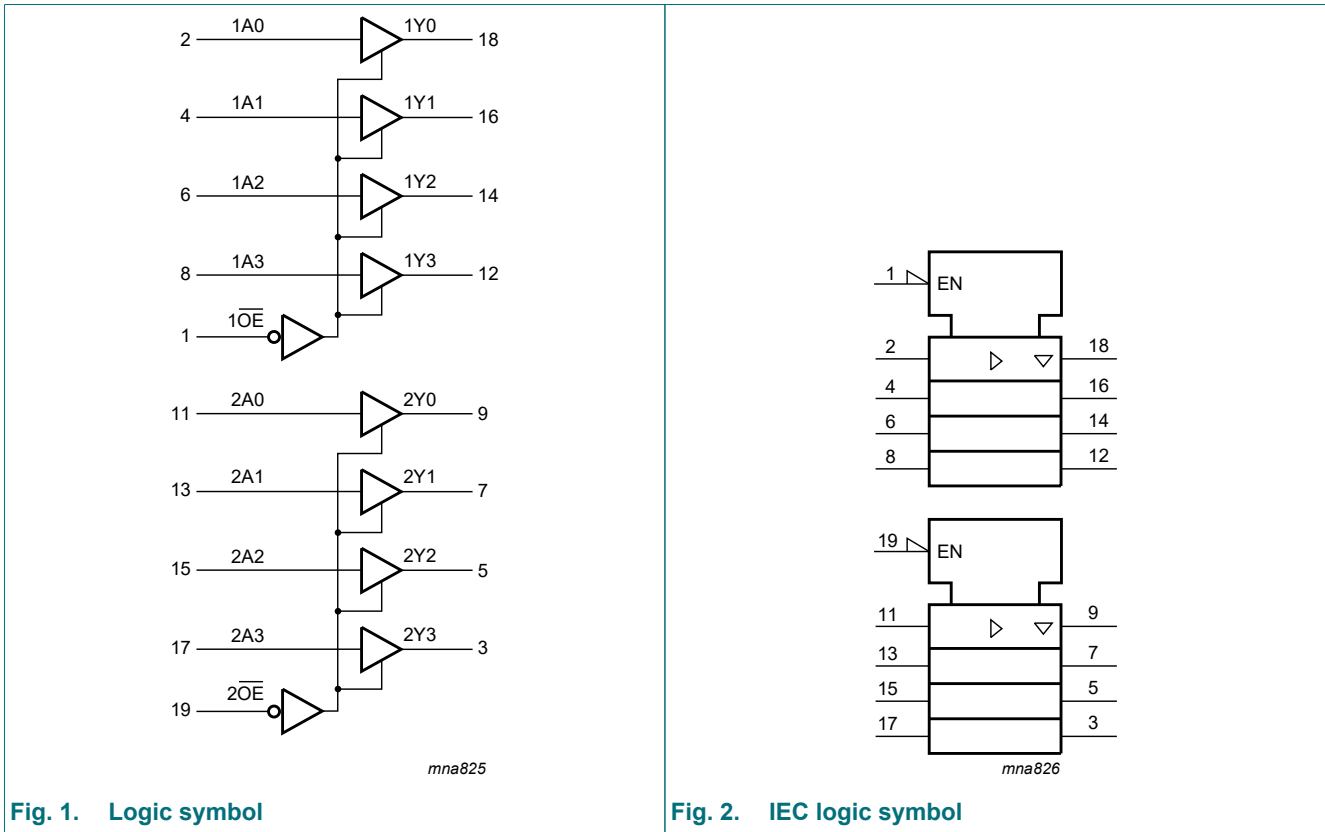
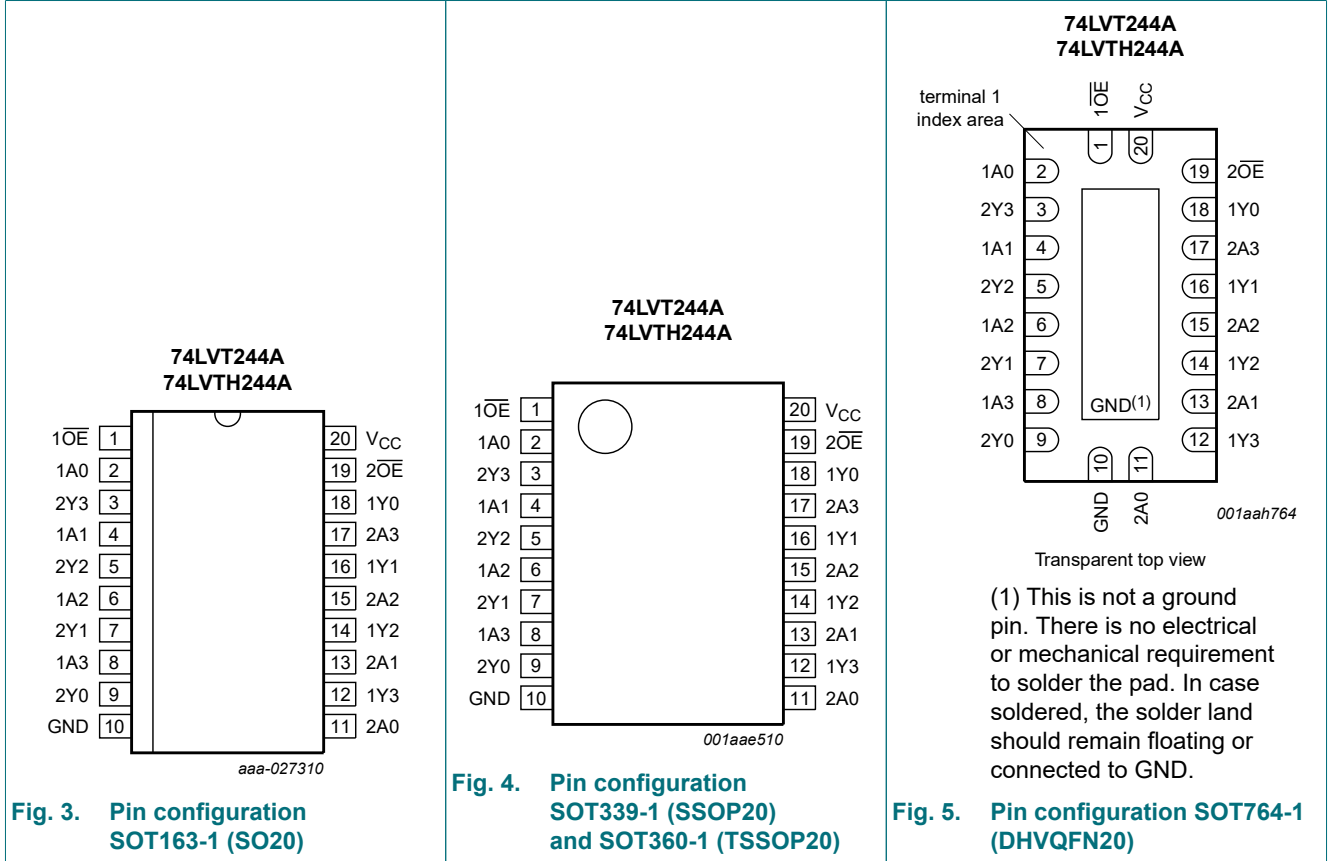


Fig. 1. Logic symbol

Fig. 2. IEC logic symbol

5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
10E, 2OE	1, 19	output enable input (active low)
1A0, 1A1, 1A2, 1A3	2, 4, 6, 8	data input
2Y0, 2Y1, 2Y2, 2Y3	9, 7, 5, 3	data output
GND	10	ground (0 V)
2A0, 2A1, 2A2, 2A3	11, 13, 15, 17	data input
1Y0, 1Y1, 1Y2, 1Y3	18, 16, 14, 12	data output
VCC	20	supply voltage

6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

Control	Input	Output
nOE	nAn	nYn
L	L	L
L	H	H
H	X	Z

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+4.6	V
V _I	input voltage		[1] -0.5	+7.0	V
V _O	output voltage	output in OFF-state or HIGH-state	[1] -0.5	+7.0	V
I _{IK}	input clamping current	V _I < 0 V	-50	-	mA
I _{OK}	output clamping current	V _O < 0 V	-50	-	mA
I _O	output current	output in LOW-state	-	128	mA
		output in HIGH-state	-64	-	mA
T _{stg}	storage temperature		-65	+150	°C
T _j	junction temperature		[2] -	150	°C
P _{tot}	total power dissipation	T _{amb} = -40 to +85 °C	[3] -	500	mW

- [1] The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.
 [2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.
 [3] For SOT163-1 (SO20) package: P_{tot} derates linearly with 12.3 mW/K above 109 °C.
 For SOT339-1 (SSOP20) package: P_{tot} derates linearly with 10.0 mW/K above 100 °C.
 For SOT360-1 (TSSOP20) package: P_{tot} derates linearly with 10.0 mW/K above 100 °C.
 For SOT764-1 (DHVQFN20) package: P_{tot} derates linearly with 12.9 mW/K above 111 °C.

8. Recommended operating conditions

Table 5. Operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{CC}	supply voltage		2.7	-	3.6	V
V _I	input voltage		0	-	5.5	V
I _{OH}	HIGH-level output current		-32	-	-	mA
I _{OL}	LOW-level output current	none	-	-	32	mA
		current duty cycle ≤ 50 %; f _i ≥ 1 kHz	-	-	64	mA
T _{amb}	ambient temperature	in free-air	-40	-	+85	°C
Δt/ΔV	input transition rise and fall rate	outputs enabled	-	-	10	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	T _{amb} = -40 °C to +85 °C			Unit
			Min	Typ[1]	Max	
V _{IK}	input clamping voltage	V _{CC} = 2.7 V; I _{IK} = -18 mA	-1.2	-0.9	-	V
V _{IH}	HIGH-level input voltage		2.0	-	-	V
V _{IL}	LOW-level input voltage		-	-	0.8	V
V _{OH}	HIGH-level output voltage	V _{CC} = 2.7 V to 3.6 V; I _{OH} = -100 μA	V _{CC} - 0.2	V _{CC} - 0.1	-	V
		V _{CC} = 2.7 V to 3.6 V; I _{OH} = -8 mA	2.4	2.5	-	V
		V _{CC} = 3.0 V; I _{OH} = -32 mA	2.0	2.2	-	V
V _{OL}	LOW-level output voltage	V _{CC} = 2.7 V; I _{OL} = 100 μA	-	0.1	0.2	V
		V _{CC} = 2.7 V; I _{OL} = 24 mA	-	0.3	0.5	V
		V _{CC} = 3.0 V; I _{OL} = 16 mA	-	0.25	0.4	V
		V _{CC} = 3.0 V; I _{OL} = 32 mA	-	0.3	0.5	V
		V _{CC} = 3.0 V; I _{OL} = 64 mA	-	0.4	0.55	V
I _I	input leakage current	all input pins				
		V _{CC} = 0 V or 3.6 V; V _I = 5.5 V	-	0.1	10	μA
		control pins				
		V _{CC} = 3.6 V; V _I = V _{CC} or GND	-	±0.1	±1	μA
		data pins [2]				
		V _{CC} = 3.6 V; V _I = V _{CC}	-	0.1	1	μA
		V _{CC} = 3.6 V; V _I = 0 V	-5	-1	-	μA
I _{OFF}	power-off leakage current	V _{CC} = 0 V; V _I or V _O = 0 V to 4.5 V	-	1	±100	μA
I _{BHL}	bus hold LOW current	V _{CC} = 3 V; V _I = 0.8 V	75	150	-	μA
I _{BHH}	bus hold HIGH current	V _{CC} = 3 V; V _I = 2.0 V	-	-150	-75	μA
I _{BHLO}	bus hold LOW overdrive current	nAn input; V _{CC} = 3.6 V; V _I = 0 V to 3.6 V [3]	500	-	-	μA
I _{BHHO}	bus hold HIGH overdrive current	nAn input; V _{CC} = 3.6 V; V _I = 0 V to 3.6 V [3]	-	-	-500	μA
I _{EX}	external current	nYn output in HIGH-state when V _O > V _{CC} ; V _O = 5.5 V; V _{CC} = 3.0 V	-	60	125	μA
I _{O(pu/pd)}	power-up/power-down output current	V _{CC} ≤ 1.2 V; V _O = 0.5 V to V _{CC} ; V _I = GND or V _{CC} ; nOE = don't care [4]	-	±1	±100	μA
I _{OZ}	OFF-state output current	V _{CC} = 3.6 V; V _I = V _{IH} or V _{IL}				
		V _O = 3.0 V	-	1	5	μA
		V _O = 0.5 V	-5	-1	-	μA
I _{CC}	supply current	V _{CC} = 3.6 V; V _I = GND or V _{CC} ; I _O = 0 A				
		output HIGH	-	0.13	0.19	mA
		output LOW	-	3	12	mA
		outputs disabled [5]	-	0.13	0.19	mA
ΔI _{CC}	additional supply current	per input pin; V _{CC} = 3.0 V to 3.6 V; one input at V _{CC} - 0.6 V and other inputs at V _{CC} or GND [6]	-	0.1	0.2	mA
C _I	input capacitance	V _I = 0 V or 3.0 V	-	4	-	pF

Symbol	Parameter	Conditions	T _{amb} = -40 °C to +85 °C			Unit
			Min	Typ[1]	Max	
C _O	output capacitance	outputs disabled; V _O = 0 V or 3.0 V	-	8	-	pF

[1] All typical values are measured at T_{amb} = 25 °C.

[2] Unused pins at V_{CC} or GND.

[3] This is the bus hold overdrive current required to force the input to the opposite logic state.

[4] This parameter is valid for any V_{CC} between 0 V and 1.2 V with a transition time of up to 10 ms.

From V_{CC} = 1.2 V to V_{CC} = 3.3 V ± 0.3 V a transition time of 100 μs is permitted. This parameter is valid for T_{amb} = 25 °C only.

[5] I_{CC} is measured with outputs pulled to V_{CC} or GND.

[6] This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND.

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 8.

Symbol	Parameter	Conditions	T _{amb} = -40 °C to +85 °C			Unit
			Min	Typ[1]	Max	
t _{PLH}	LOW to HIGH propagation delay	nAn to nYn; see Fig. 6				
		V _{CC} = 2.7 V	-	-	5.0	ns
		V _{CC} = 3.0 V to 3.6 V	1	2.5	4.1	ns
t _{PHL}	HIGH to LOW propagation delay	nAn to nYn; see Fig. 6				
		V _{CC} = 2.7 V	-	-	5.1	ns
		V _{CC} = 3.0 V to 3.6 V	1	2.6	4.1	ns
t _{PZH}	OFF-state to HIGH propagation delay	n $\overline{O}E$ to nYn; see Fig. 7				
		V _{CC} = 2.7 V	-	-	6.3	ns
		V _{CC} = 3.0 V to 3.6 V	1	3.2	5.2	ns
t _{PZL}	OFF-state to LOW propagation delay	n $\overline{O}E$ to nYn; see Fig. 7				
		V _{CC} = 2.7 V	-	-	6.7	ns
		V _{CC} = 3.0 V to 3.6 V	1.1	3.1	5.2	ns
t _{PHZ}	HIGH to OFF-state propagation delay	n $\overline{O}E$ to nYn; see Fig. 7				
		V _{CC} = 2.7 V	-	-	6.3	ns
		V _{CC} = 3.0 V to 3.6 V	1.9	3.3	5.6	ns
t _{PLZ}	LOW to OFF-state propagation delay	n $\overline{O}E$ to nYn; see Fig. 7				
		V _{CC} = 2.7 V	-	-	5.6	ns
		V _{CC} = 3.0 V to 3.6 V	1.8	3.3	5.1	ns

[1] All typical values are at V_{CC} = 3.3 V and T_{amb} = 25 °C.

10.1. Waveforms and test circuit

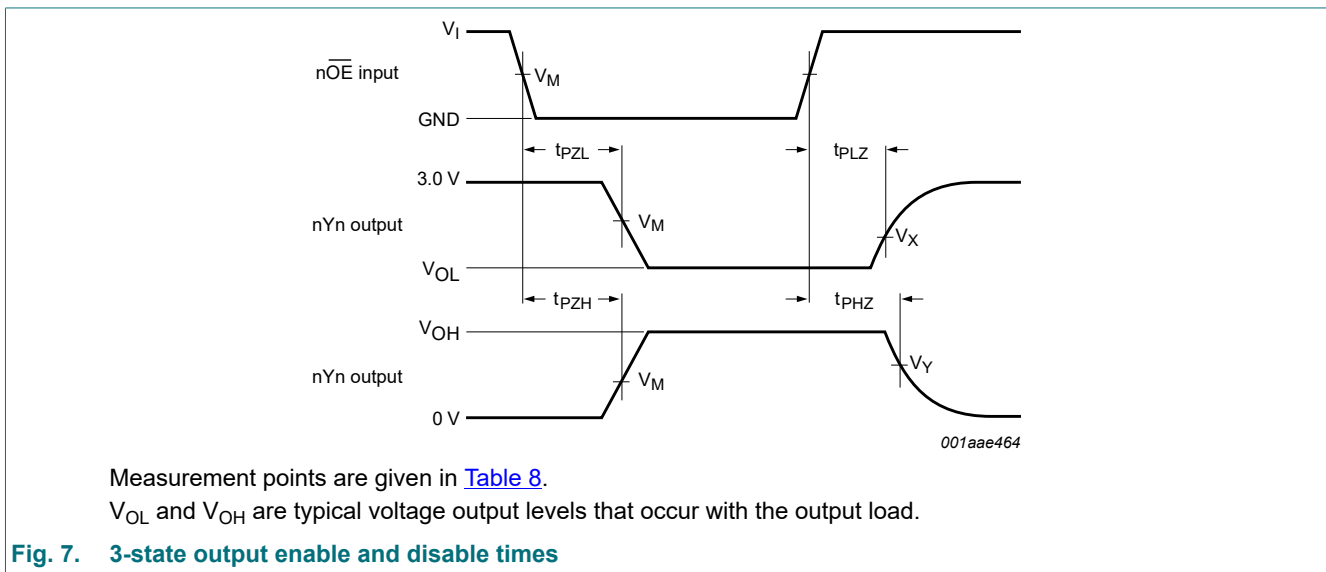
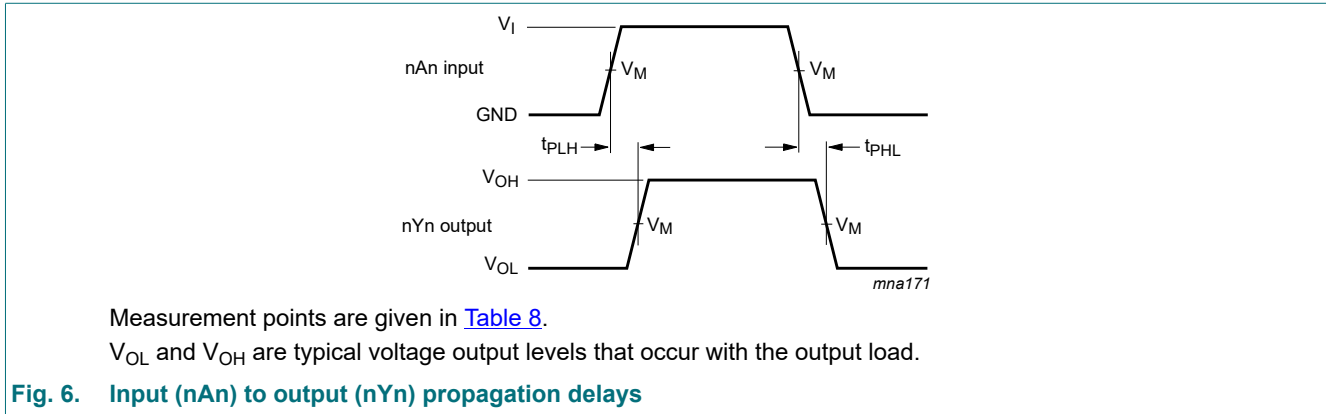
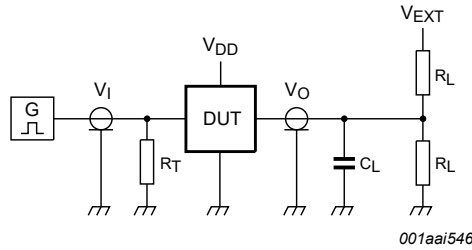
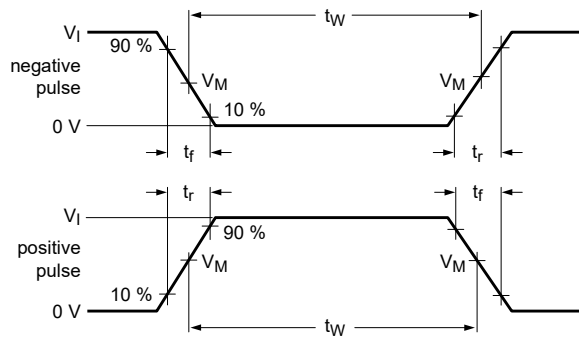


Table 8. Measurement points

Input	Output		
V_M	V_M	V_X	V_Y
1.5 V	1.5 V	$V_{OL} + 0.3 V$	$V_{OH} - 0.3 V$



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Test data is given in [Table 9](#).

Definitions test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

V_{EXT} = Test voltage for switching times.

Fig. 8. Test circuit for measuring switching times

Table 9. Test data

Input				Load		V_{EXT}		
V_I	f_i	t_W	t_r, t_f	C_L	R_L	t_{PHZ}, t_{PZH}	t_{PLZ}, t_{PZL}	t_{PLH}, t_{PHL}
2.7 V	≤ 10 MHz	500 ns	≤ 2.5 ns	50 pF	500 Ω	GND	6 V	open

11. Package outline

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1



Fig. 9. Package outline SOT163-1 (SO20)

SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm

SOT339-1

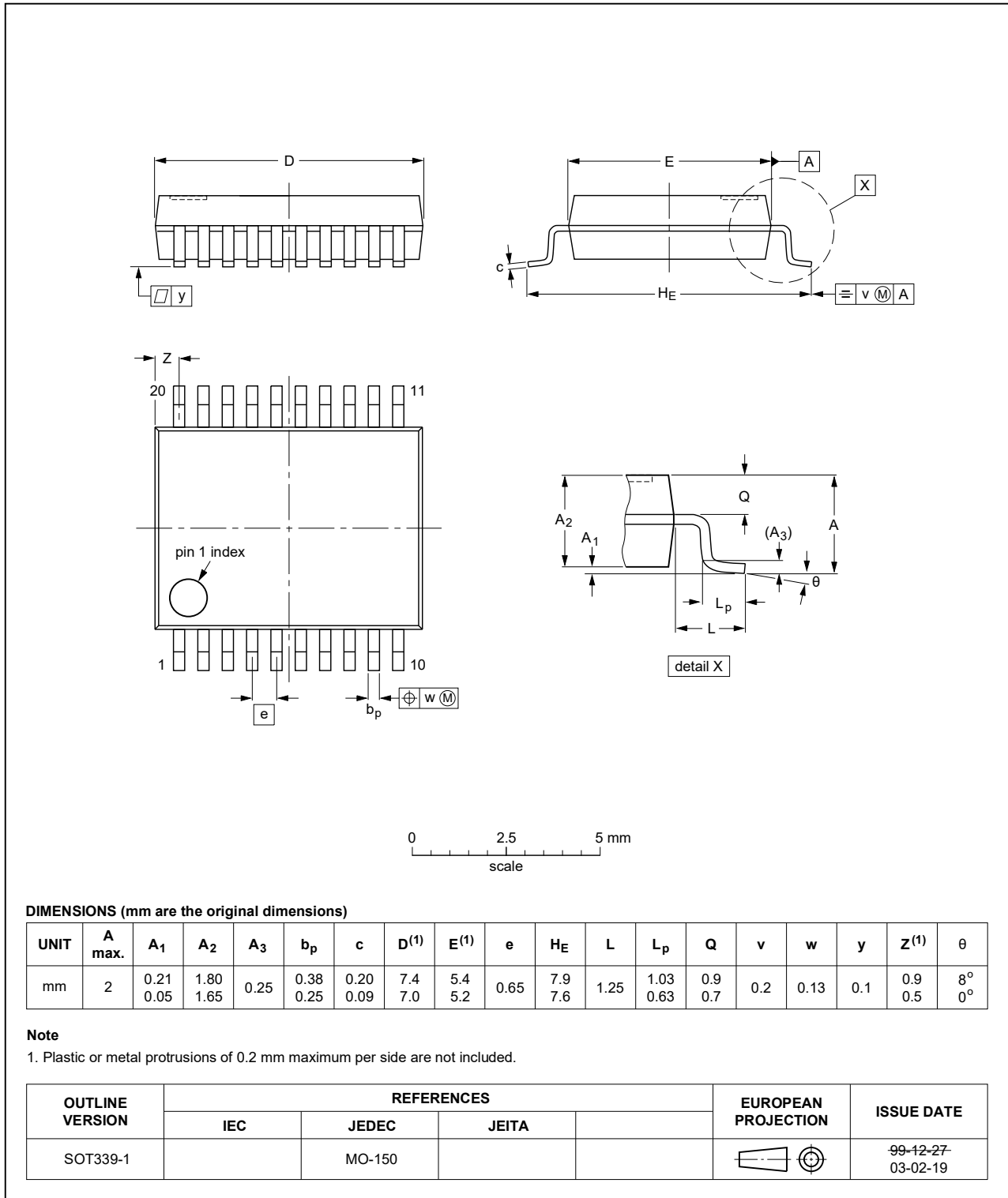


Fig. 10. Package outline SOT339-1 (SSOP20)

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1



Fig. 11. Package outline SOT360-1 (TSSOP20)

12. Abbreviations

Table 10. Abbreviations

Acronym	Description
BiCMOS	Bipolar Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVT_LVTH244A v.6	20200824	Product data sheet	-	74LVT_LVTH244A v.5
Modifications:	<ul style="list-style-type: none"> • Table 4: Derating values for P_{tot} total power dissipation have been updated. 			
74LVT_LVTH244A v.5	20170816	Product data sheet	-	74LVT_LVTH244A v.4
Modifications:	<ul style="list-style-type: none"> • The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate. 			
74LVT_LVTH244A v.4	20080903	Product data sheet	-	74LVT_LVTH244A v.3
Modifications:	<ul style="list-style-type: none"> • The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Section 3 and Section 11 DHVQFN20 package added. 			
74LVT_LVTH244A v.3	20060315	Product specification	-	74LVT244A v.2
74LVT244A v.2	19980219	Product specification	-	74LVT244A v.1

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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