Operational Amplifiers

Low Noise Operational Amplifier

BA15218F

General Description

The BA15218F is low noise operational amplifier with high voltage gain.
They have good performance of input referred noise voltage(1.0μVrms), total harmonic distortion (0.0015%) and operating supply voltage(±2.0V to ±16.0V).
These are suitable for audio applications and active filter.

Features

- High Voltage Gain
- Low Input Referred Noise Voltage
- Low Total Harmonic Distortion
- Wide Operating Supply Voltage

Applications

- Audio Application
- Consumer Equipment
- Active Filter

Key Specifications

- Operating Supply Voltage (split supply): ±2.0V to ±16.0V
- Slew Rate: 3V/μs(Typ)
- Input Referred Noise Voltage: 1.0μVrms(Typ)
- Total Harmonic Distortion: 0.0015%(Typ)
- Temperature Range: -40°C to +85°C

Packages

Packages	W(Typ) x D(Typ) x H(Max)
SOP8	5.00mm x 6.20mm x 1.71mm

Simplified Schematic

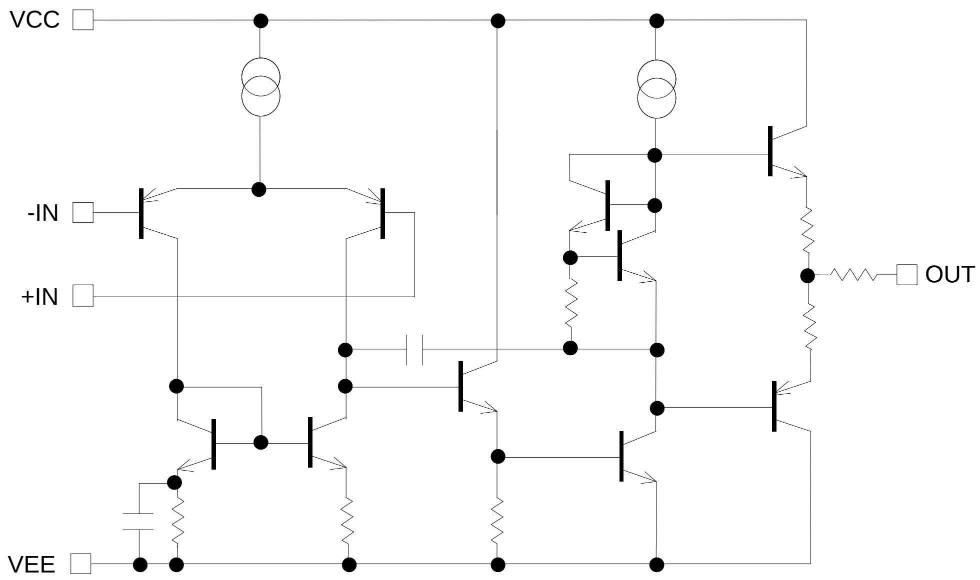
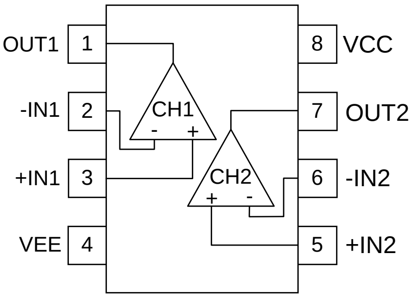


Figure 1. Simplified Schematic

○Product structure：Silicon monolithic integrated circuit　○This product has no designed protection against radioactive rays.

Pin Configuration

BA15218F : SOP8



Pin No.	Pin Name
1	OUT1
2	-IN1
3	+IN1
4	VEE
5	+IN2
6	-IN2
7	OUT2
8	VCC

Package
SOP8
BA15218F

Ordering Information

B A 1 5 2 1 8 F - E2

Part Number
BA15218F

Package
F: SOP8

Packaging and Forming Specification
E2: Embossed tape and reel
(SOP8)

Line-Up

Topr	Operating Supply Voltage (split supply)	Supply Current (Typ)	Slew Rate (Typ)	Package		Orderable Part Number
-40°C to +85°C	±2.0V to ±16.0V	5mA	3V/μs	SOP8	Reel of 2500	BA15218F-E2

Absolute Maximum Ratings (T_A=25°C)

Parameter	Symbol	Rating	Unit
Supply Voltage	VCC-VEE	+36	V
Power Dissipation	P_D	0.55 (Note 1,2)	W
Differential Input Voltage (Note 3)	V_{ID}	VCC - VEE	V
Input Common-Mode Voltage Range	V_{ICM}	VEE - VCC	V
Input Current	I_I	-10 (Note 4)	mA
Operating Supply Voltage	V_{opr}	±2 to ±16 (+4 to +32)	V
Operating Temperature	T_{opr}	-40 to +85	°C
Storage Temperature	T_{stg}	-55 to +125	°C
Output Short Current (Note 5)	I_{OMAX}	±50	mA
Maximum Junction Temperature	T_{Jmax}	+125	°C

(Note 1) To use at temperature above T_A=25°C reduce 5.5mW/°C.
(Note 2) Mounted on a FR4 glass epoxy PCB 70mm×70mm×1.6mm (Copper foil area less than 3%).
(Note 3) The voltage difference between inverting input and non-inverting input is the differential input voltage.
Then input terminal voltage is set to more than VEE.
(Note 4) An excessive input current will flow when input voltages of less than VEE-0.6V are applied.
The input current can be set to less than the rated current by adding a limiting resistor.
(Note 5) This current value is when the output is shorted to VCC or VEE. Please use within the P_D range.
Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Electrical Characteristics

○BA15218F (Unless otherwise specified VCC=+15V, VEE=-15V, T_A=25°C)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
Input Offset Voltage (Note 6)	V_{IO}	-	0.5	5.0	mV	R_S≦10kΩ
Input Offset Current (Note 6)	I_{IO}	-	5	200	nA	-
Input Bias Current (Note 6,7)	I_B	-	50	500	nA	-
Large Signal Voltage Gain	A_V	86	110	-	dB	R_L≧2kΩ, OUT=±10V
Input Common-mode Voltage Range	V_{ICM}	±12	±14	-	V	-
Common-Mode Rejection Ratio	CMRR	70	90	-	dB	R_S≦10kΩ
Power Supply Rejection Ratio	PSRR	76	90	-	dB	R_S≦10kΩ
Supply Current	I_{CC}	-	5.0	8.0	mA	+IN=0V, R_L=∞
Maximum Output Voltage	V_{OM}	±12	±14	-	V	R_L≧10kΩ
		±10	±13	-	V	R_L≧2kΩ
Slew Rate	SR	-	3.0	-	V/μs	A_V=0dB, R_L=2kΩ
Gain Bandwidth	GBW	-	10	-	MHz	f=10kHz
Input Referred Noise Voltage	V_N	-	1.0	-	μVrms	R_S=1kΩ f=20Hz to 30kHz, RIAA
		-	9.5	-	nV/$\sqrt{Hz}$	R_S=100Ω, +IN=0V, f=1kHz
Total Harmonic Distortion + Noise	THD+N	-	0.0015	-	%	A_V=20dB R_L=2kΩ, 80kHz-LPF
Channel Separation	CS	-	120	-	dB	f=1kHz, OUT=0.5Vrms

(Note 6) Absolute value

(Note 7) Current direction: Since first input stage is composed with PNP transistor, input bias current flows out of IC.

Description of Electrical Characteristics

Described below are descriptions of the relevant electrical terms used in this datasheet. Items and symbols used are also shown. Note that item name and symbol and their meaning may differ from those on another manufacturer's document or general document.

1. Absolute maximum ratings

Absolute maximum rating items indicate the condition which must not be exceeded. Application of voltage in excess of absolute maximum rating or use out of absolute maximum rated temperature environment may cause deterioration of characteristics.

(1) Supply Voltage (VCC/VEE)
Indicates the maximum voltage that can be applied between the VCC terminal and VEE terminal without deterioration or destruction of characteristics of internal circuit.

(2) Differential Input Voltage (V_{ID})
Indicates the maximum voltage that can be applied between non-inverting and inverting terminals without damaging the IC.

(3) Input Common-mode Voltage Range (V_{ICM})
Indicates the maximum voltage that can be applied to the non-inverting and inverting terminals without deterioration or destruction of electrical characteristics. Input common-mode voltage range of the maximum ratings does not assure normal operation of IC. For normal operation, use the IC within the input common-mode voltage range characteristics.

(4) Power Dissipation (P_D)
Indicates the power that can be consumed by the IC when mounted on a specific board at the ambient temperature 25°C (normal temperature). As for package product, P_D is determined by the temperature that can be permitted by the IC in the package (maximum junction temperature) and the thermal resistance of the package.

2. Electrical Characteristics Items

(1) Input Offset Voltage (V_{IO})
Indicates the voltage difference between non-inverting terminal and inverting terminals. It can be translated into the input voltage difference required for setting the output voltage at 0 V.

(2) Input Offset Current (I_{IO})
Indicates the difference of input bias current between the non-inverting and inverting terminals.

(3) Input Bias Current (I_B)
Indicates the current that flows into or out of the input terminal. It is defined by the average of input bias currents at the non-inverting and inverting terminals.

(4) Large Signal Voltage Gain (A_V)
Indicates the amplifying rate (gain) of output voltage against the voltage difference between non-inverting terminal and inverting terminal. It is normally the amplifying rate (gain) with reference to DC voltage.
A_V = (Output voltage) / (Differential Input voltage)

(5) Input Common-mode Voltage Range (V_{ICM})
Indicates the input voltage range where IC normally operates.

(6) Common-mode Rejection Ratio (CMRR)
Indicates the ratio of fluctuation of input offset voltage when the input common mode voltage is changed. It is normally the fluctuation of DC.
CMRR = (Change of Input common-mode voltage)/(Input offset fluctuation)

(7) Power Supply Rejection Ratio (PSRR)
Indicates the ratio of fluctuation of input offset voltage when supply voltage is changed.
It is normally the fluctuation of DC.
PSRR= (Change of power supply voltage)/(Input offset fluctuation)

(8) Supply Current (I_{CC})
Indicates the current that flows within the IC under specified no-load conditions.

(9) Maximum Output Voltage (V_{OM})
Signifies the voltage range that can be output under specific output conditions.

(10) Slew Rate (SR)
Indicates the ratio of the change in output voltage with time when a step input signal is applied.

(11) Gain Band Width (GBW)
The product of the open-loop voltage gain and the frequency at which the voltage gain decreases 20dB/decade.

(12) Input Referred Noise Voltage (V_N)
Indicates a noise voltage generated inside the operational amplifier equivalent by ideal voltage source connected in series with input terminal.

(13) Total Harmonic Distortion + Noise (THD+N)
Indicates the fluctuation of input offset voltage or that of output voltage with reference to the change of output voltage of driven channel.

(14) Channel Separation (CS)
Indicates the fluctuation in the output voltage of the driven channel with reference to the change of output voltage of the channel which is not driven.

Typical Performance Curves

○BA15218F

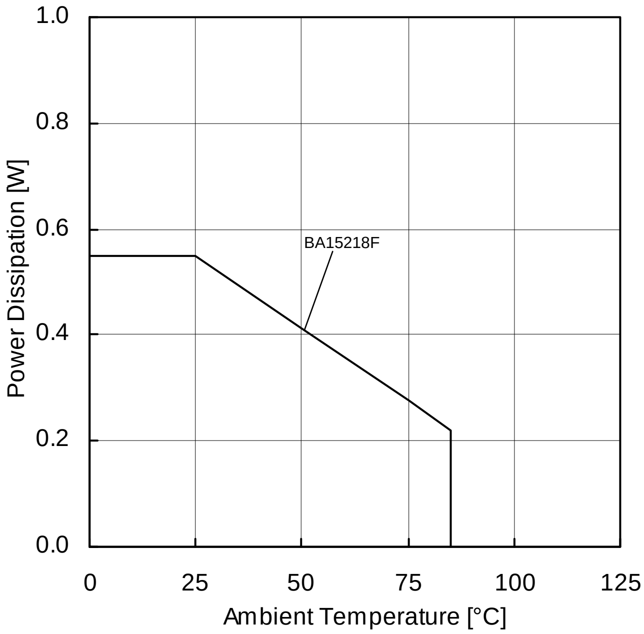


Figure 2.
Power Dissipation vs Ambient Temperature
(Derating Curve)

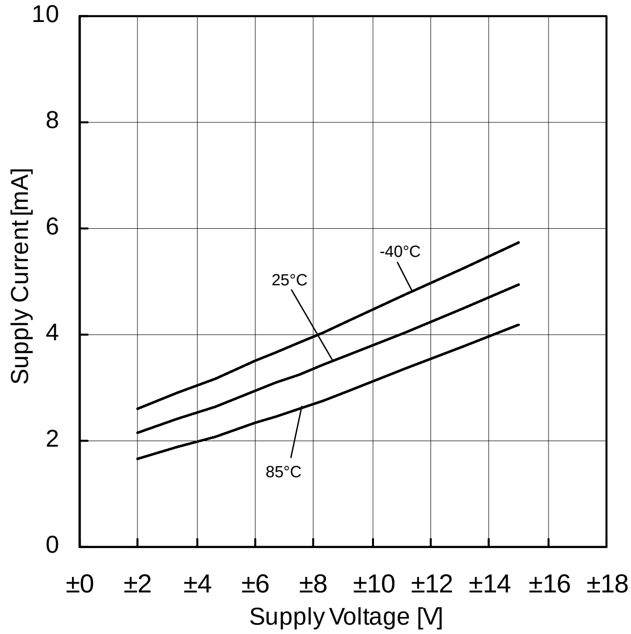


Figure 3.
Supply Current vs Supply Voltage

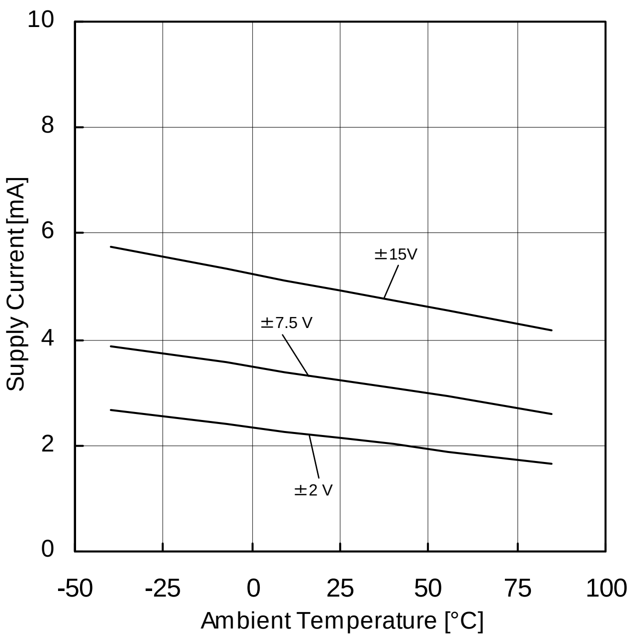


Figure 4.
Supply Current vs Ambient Temperature

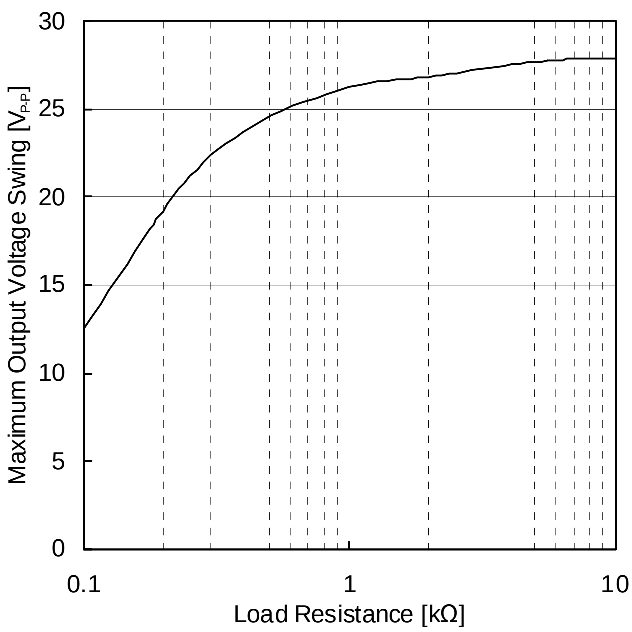


Figure 5.
Maximum Output Voltage Swing vs Load Resistance
(VCC/VEE=+15V/-15V, T_A=25°C)

(*)The above characteristics are measurements of typical sample, they are not guaranteed.

Typical Performance Curves - continued

○BA15218F

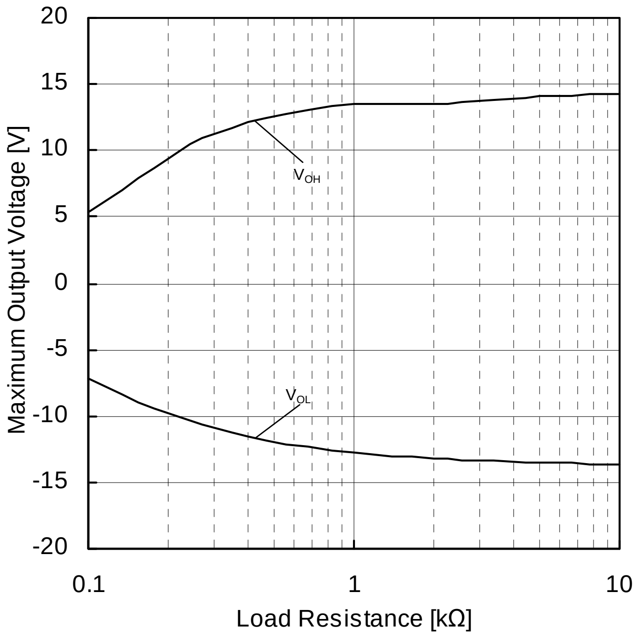


Figure 6.
Maximum Output Voltage vs Load Resistance
(VCC/VEE=+15V/-15V, T_A=25°C)

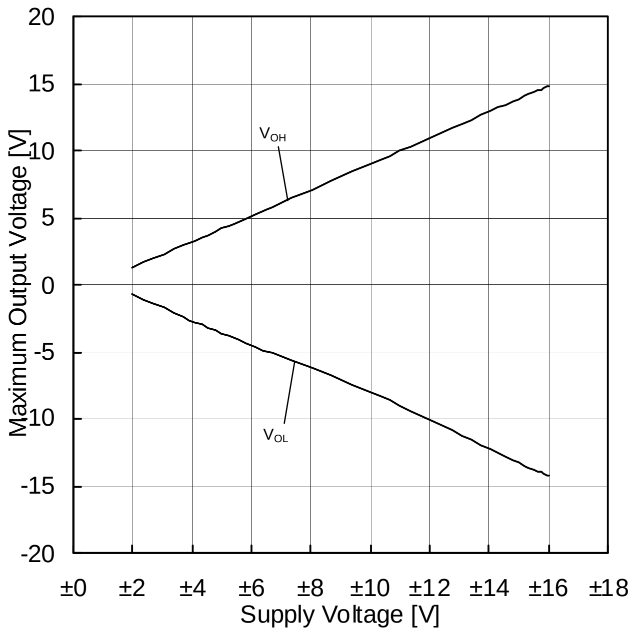


Figure 7.
Maximum Output Voltage vs Supply Voltage
(R_L=2kΩ, T_A=25°C)

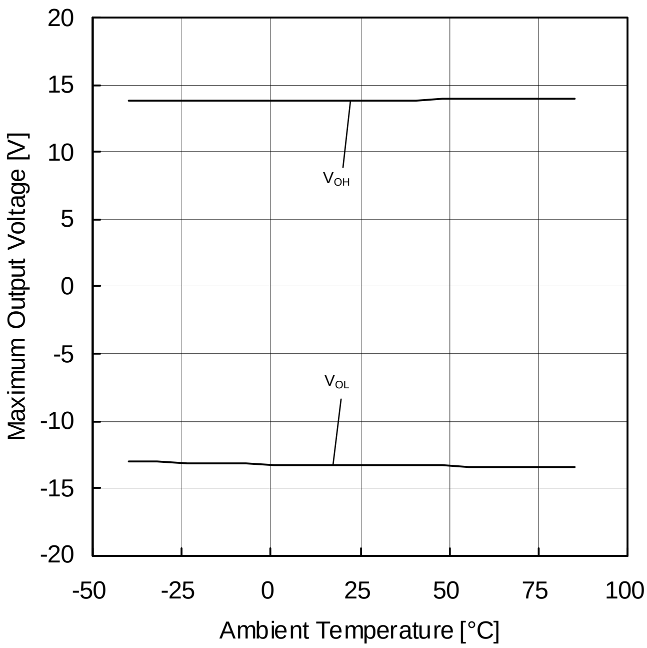


Figure 8.
Maximum Output Voltage vs Ambient Temperature
(VCC/VEE=+15V/-15V, R_L=2kΩ)

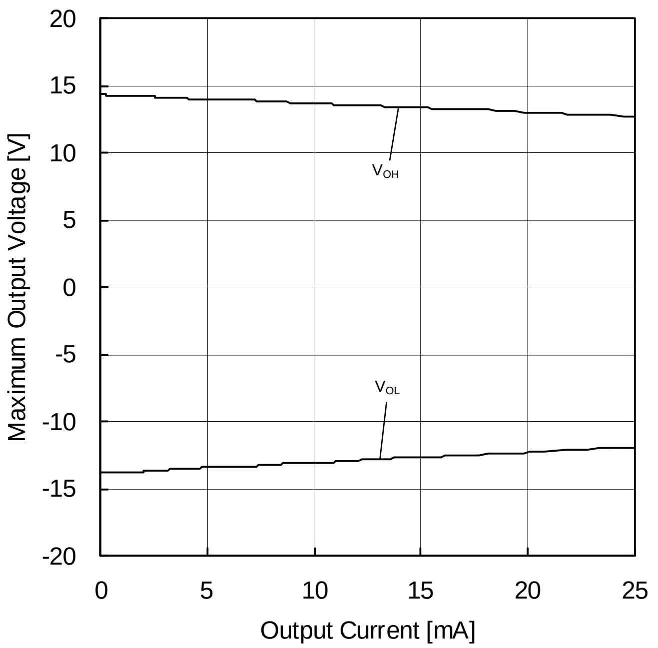


Figure 9.
Maximum Output Voltage vs Output Current
(VCC/VEE=+15V/-15V, T_A=25°C)

(*)The above characteristics are measurements of typical sample, they are not guaranteed.

Typical Performance Curves - continued

○BA15218F

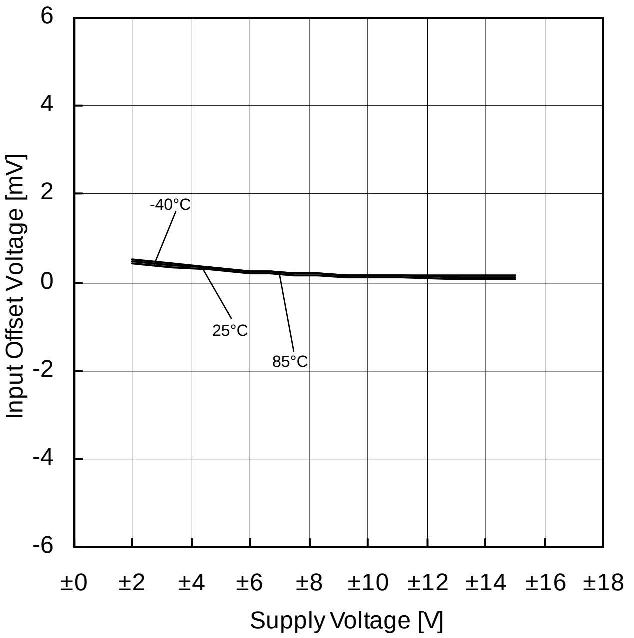


Figure 10.
Input Offset Voltage vs Supply Voltage
(V_{ICM}=0V, E_K=0V)

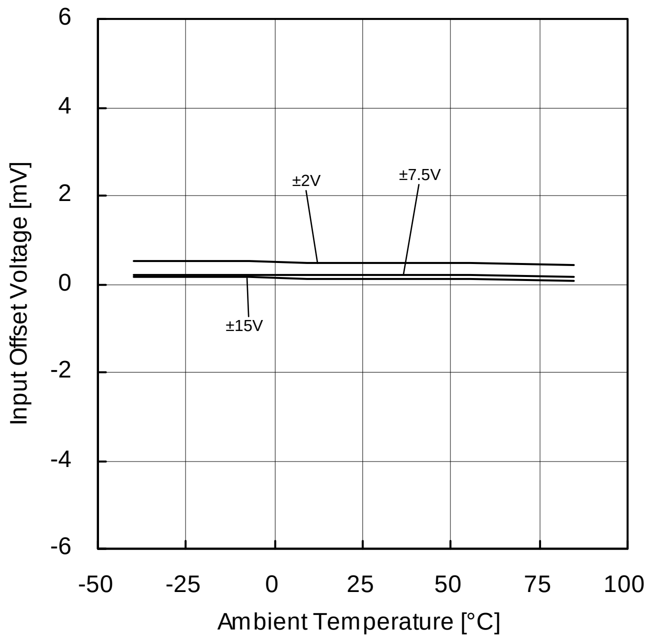


Figure 11.
Input Offset Voltage vs Ambient Temperature
(V_{ICM}=0V, E_K=0V)

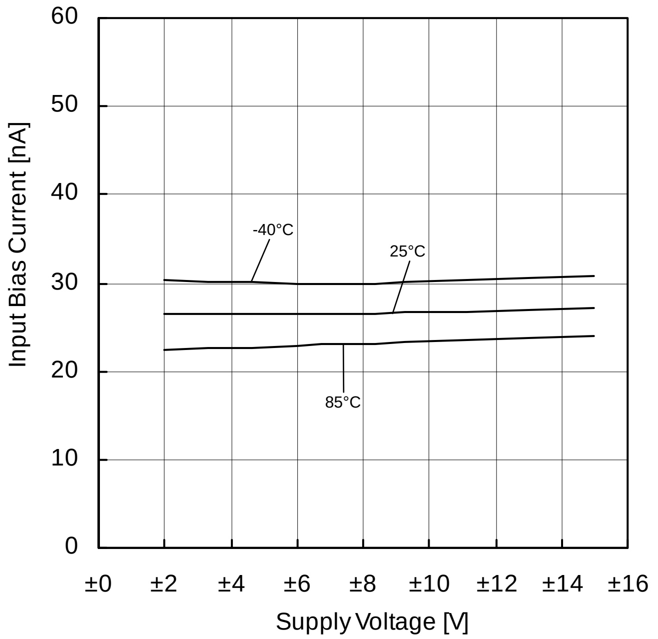


Figure 12.
Input Bias Current vs Supply Voltage
(V_{ICM}=0V, E_K=0V)

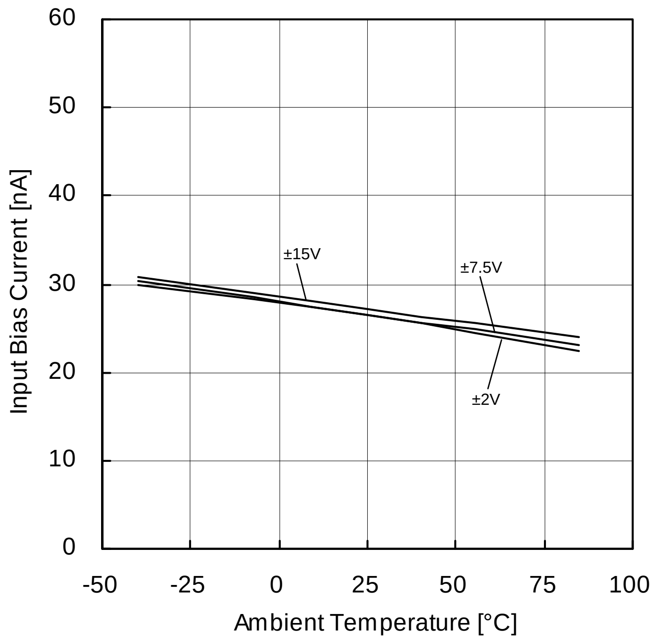


Figure 13.
Input Bias Current vs Ambient Temperature
(V_{ICM}=0V, E_K=0V)

(*)The above characteristics are measurements of typical sample, they are not guaranteed.

Typical Performance Curves - continued

○BA15218F

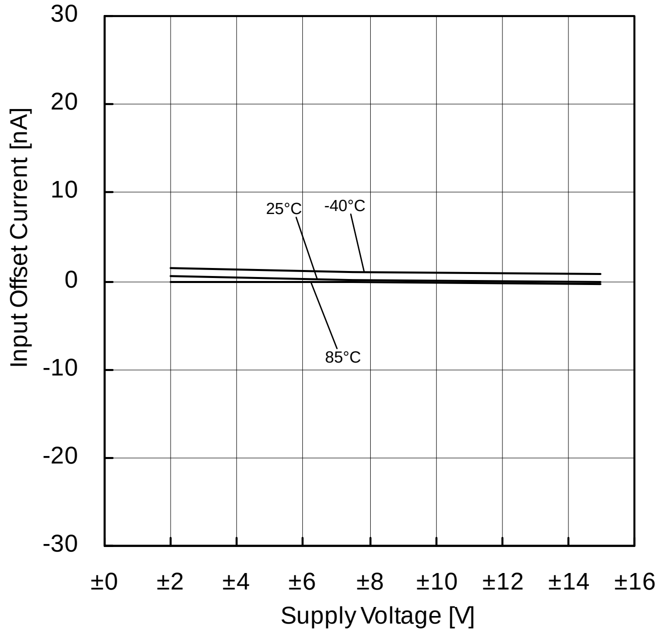


Figure 14.
Input Offset Current vs Supply Voltage
(V_{ICM}=0V, E_K=0V)

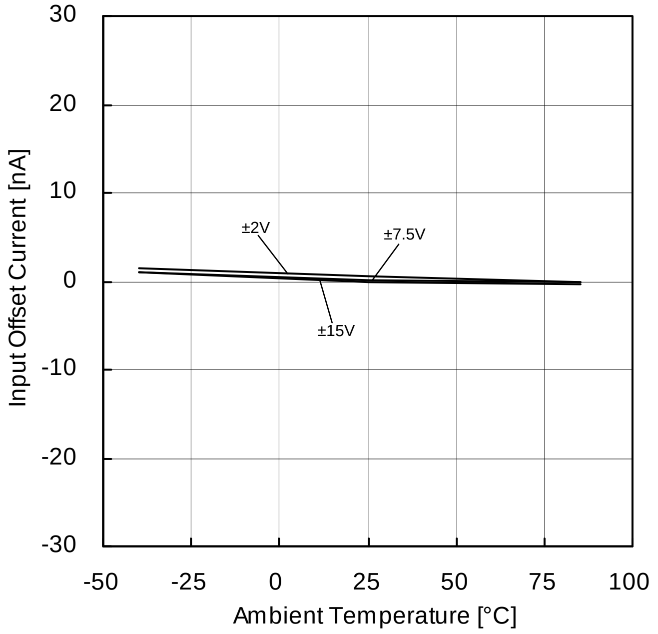


Figure 15.
Input Offset Current vs Ambient Temperature
(V_{ICM}=0V, E_K=0V)

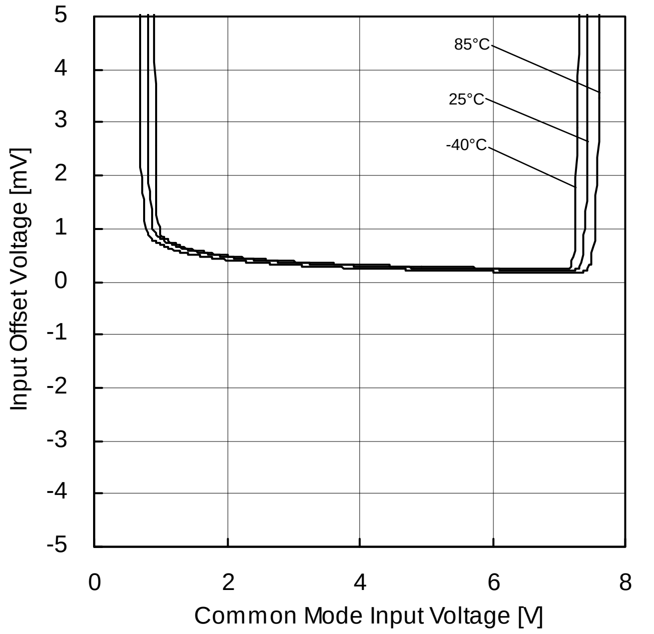


Figure 16.
Input Offset Voltage vs Common Mode Input Voltage
(VCC=8V, E_K=-4V)

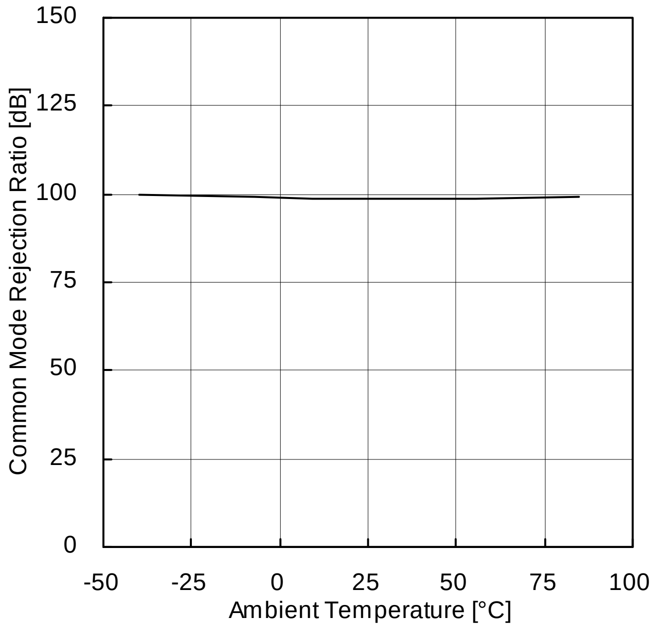


Figure 17.
Common Mode Rejection Ratio vs Ambient Temperature
(VCC/VEE=+15V/-15V, V_{ICM}=-12V to +12V)

(*)The above characteristics are measurements of typical sample, they are not guaranteed.

Typical Performance Curves - continued

○BA15218F

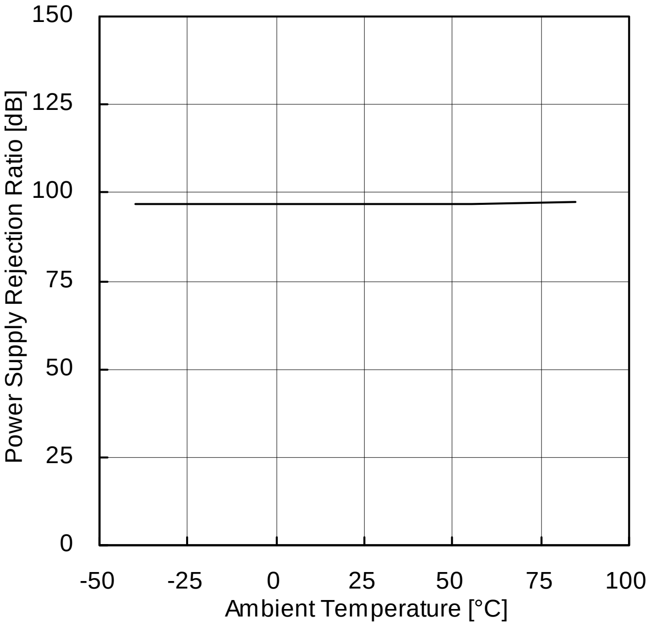


Figure 18.
Power Supply Rejection Ratio vs Ambient Temperature
(VCC/VEE=+2V/-2V to +15V/-15V)

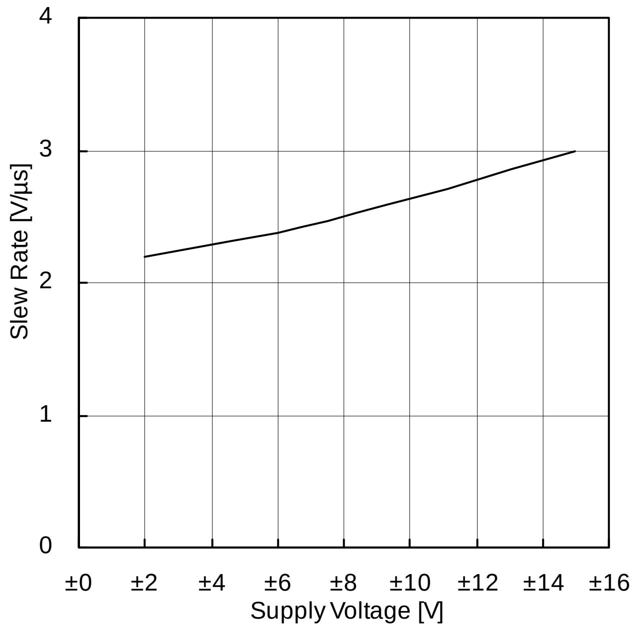


Figure 19.
Slew Rate vs Supply Voltage
(C_L=100pF, R_L=2kΩ, T_A=25°C)

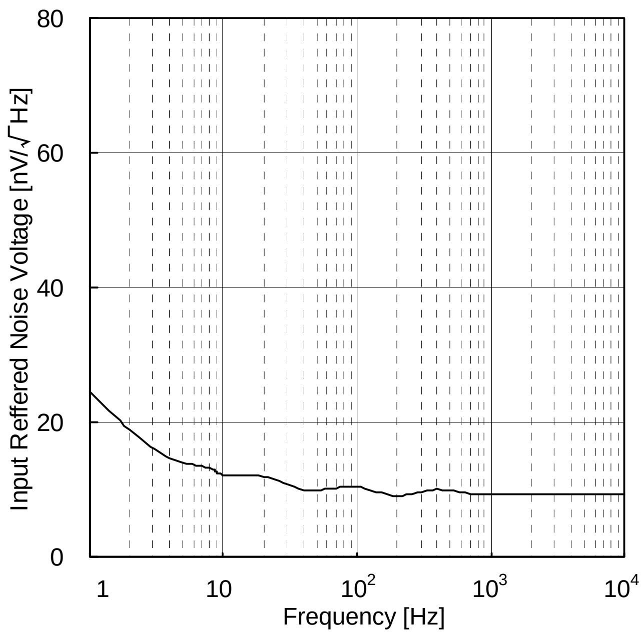


Figure 20.
Equivalent Input Noise Voltage vs Frequency
(VCC/VEE=+15V/-15V, R_S=100Ω, T_A=25°C)

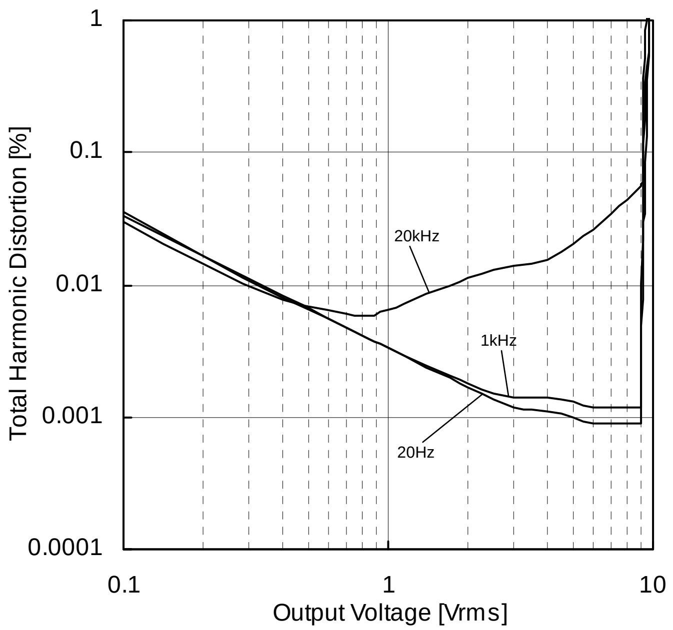


Figure 21.
Total Harmonic Distortion vs Output Voltage
(VCC/VEE=+15V/-15V, A_V=20dB,
R_L=2kΩ, 80kHz-LPF, T_A=25°C)

(*)The above characteristics are measurements of typical sample, they are not guaranteed.

Typical Performance Curves - continued

○BA15218F

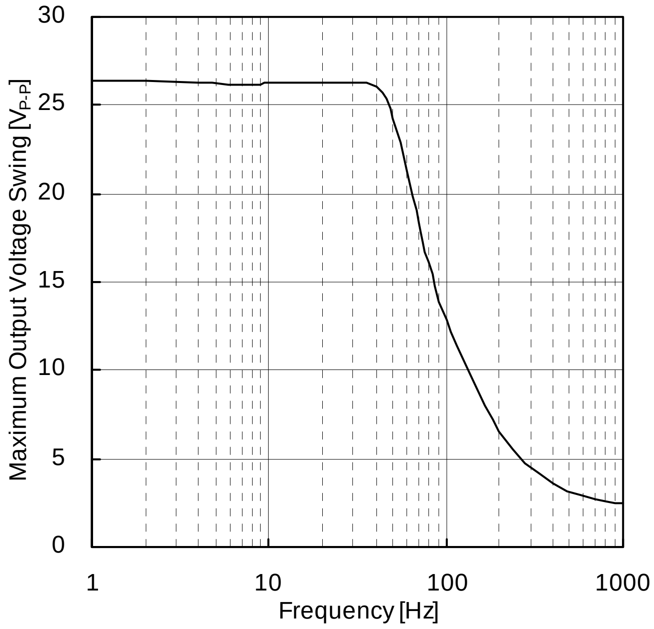


Figure 22.
Maximum Output Voltage Swing vs Frequency
(VCC/VEE=+15V/-15V, R_L=2kΩ, T_A=25°C)

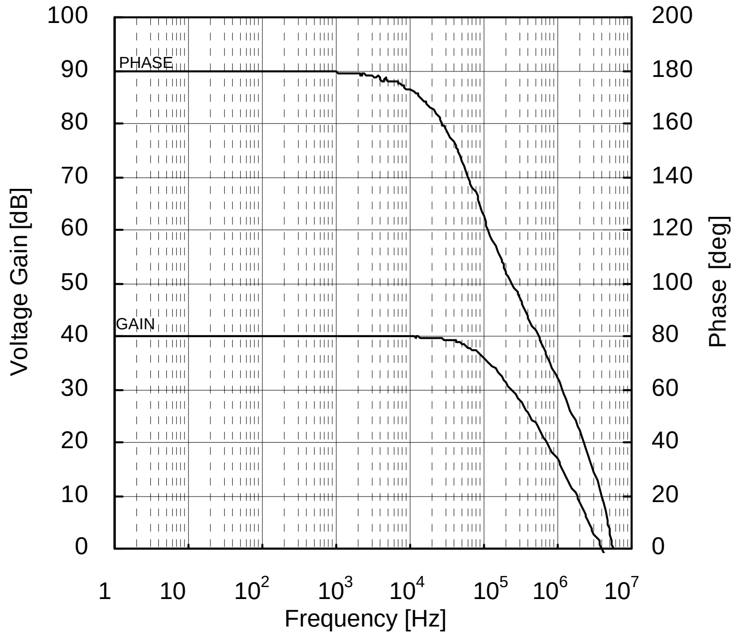


Figure 23.
Voltage Gain・Phase vs Frequency
(VCC/VEE=+15V/-15V, A_V=40dB, R_L=2kΩ, T_A=25°C)

(*)The above characteristics are measurements of typical sample, they are not guaranteed.

Application Information

NULL method condition for Test Circuit 1

VCC, VEE, E_K, V_{ICM} Unit: V

Parameter	V_F	S1	S2	S3	VCC	VEE	E_K	V_{ICM}	calculation
Input Offset Voltage	V_{F1}	ON	ON	OFF	15	-15	0	0	1
Input Offset Current	V_{F2}	OFF	OFF	OFF	15	-15	0	0	2
Input Bias Current	V_{F3}	OFF	ON	OFF	15	-15	0	0	3
	V_{F4}	ON	OFF						
Large Signal Voltage Gain	V_{F5}	ON	ON	ON	15	-15	-10	0	4
	V_{F6}				15	-15	10	0	
Common-Mode Rejection Ratio (Input Common-Mode Voltage Range)	V_{F7}	ON	ON	OFF	3	-27	12	0	5
	V_{F8}				27	-3	-12	0	
Power Supply Rejection Ratio	V_{F9}	ON	ON	OFF	2	-2	0	0	6
	V_{F10}				15	-15	0	0	

- Calculation -

1. Input Offset Voltage (V_{IO})

$$V_{IO} = \frac{|V_{F1}|}{1 + R_F/R_S} \quad [V]$$

2. Input Offset Current (I_{IO})

$$I_{IO} = \frac{|V_{F2} - V_{F1}|}{R_I \times (1 + R_F/R_S)} \quad [A]$$

3. Input Bias Current (I_B)

$$I_B = \frac{|V_{F4} - V_{F3}|}{2 \times R_I \times (1 + R_F/R_S)} \quad [A]$$

4. Large Signal Voltage Gain (A_V)

$$Av = 20Log \frac{\Delta E_K \times (1+R_F/R_S)}{|V_{F6} - V_{F5}|} \quad [dB]$$

5. Common-mode Rejection Ration (CMRR)

$$CMRR = 20Log \frac{\Delta V_{ICM} \times (1+R_F/R_S)}{|V_{F8} - V_{F7}|} \quad [dB]$$

6. Power supply rejection ratio (PSRR)

$$PSRR = 20Log \frac{\Delta VCC \times (1+ R_F/R_S)}{|V_{F10} - V_{F9}|} \quad [dB]$$

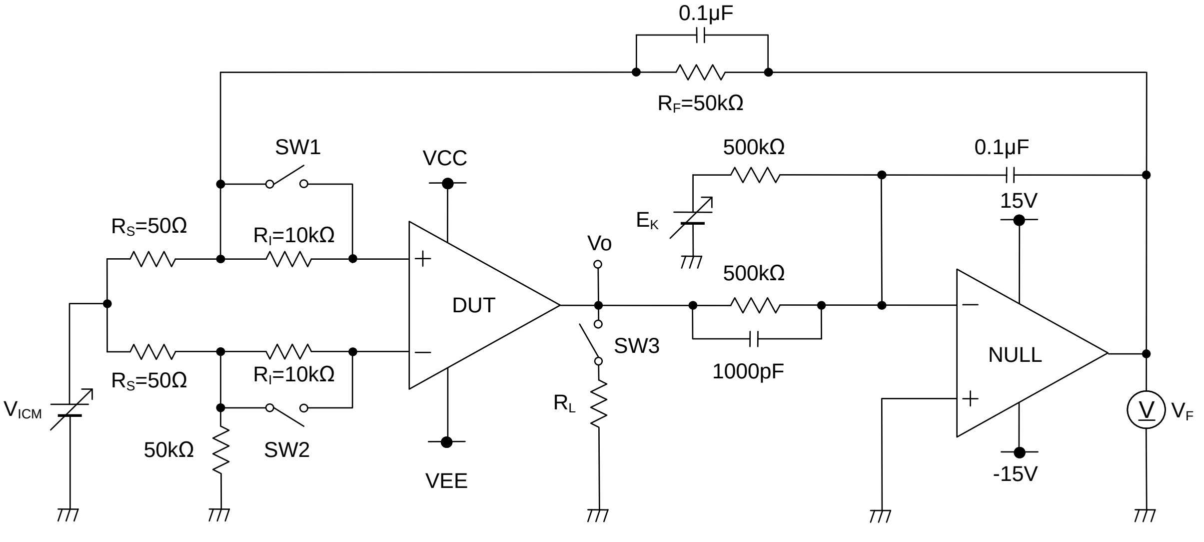


Figure 24. Test Circuit 1 (one channel only)

Switch Condition for Test Circuit 2

SW No.	SW1	SW2	SW3	SW4	SW5	SW6	SW7	SW8	SW9	SW10	SW11	SW12
Supply Current	OFF	OFF	OFF	ON	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF
Maximum Output Voltage	OFF	OFF	ON	OFF	OFF	OFF	ON	OFF	ON	OFF	OFF	ON
Slew Rate	OFF	OFF	OFF	ON	OFF	OFF	OFF	ON	ON	ON	OFF	OFF
Gain Bandwidth	OFF	ON	OFF	OFF	ON	ON	OFF	OFF	ON	ON	ON	OFF
Input Referred Noise Voltage	ON	OFF	OFF	OFF	ON	ON	OFF	OFF	OFF	OFF	ON	OFF

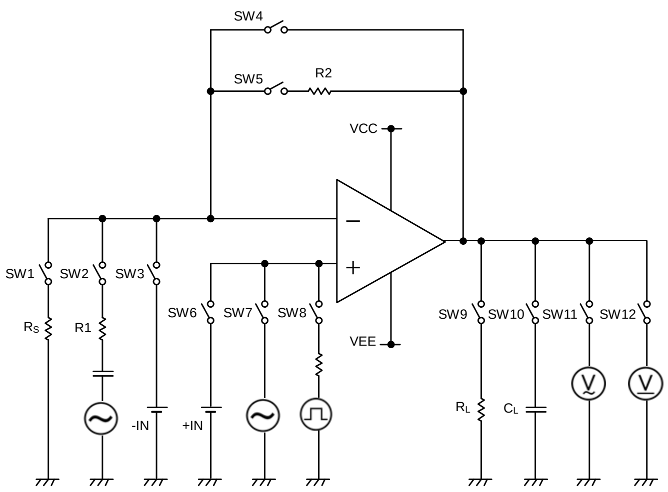


Figure 25. Test Circuit 2 (each channel)

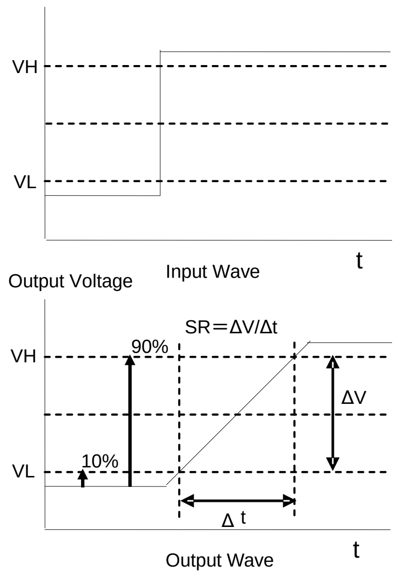


Figure 26. Slew Rate Input Waveform

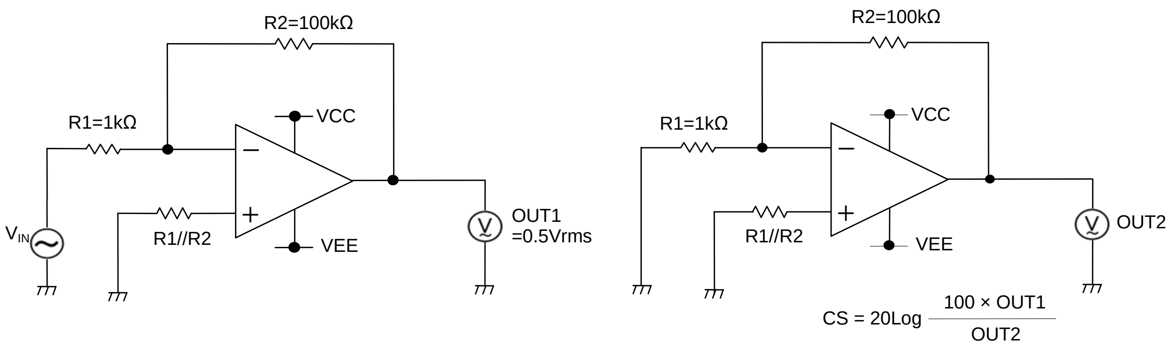


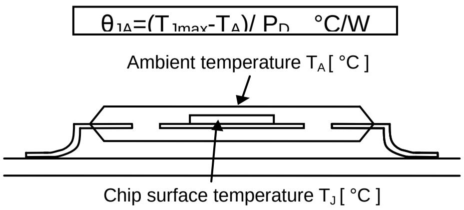
Figure 27. Test Circuit 3 (Channel Separation)

Power Dissipation

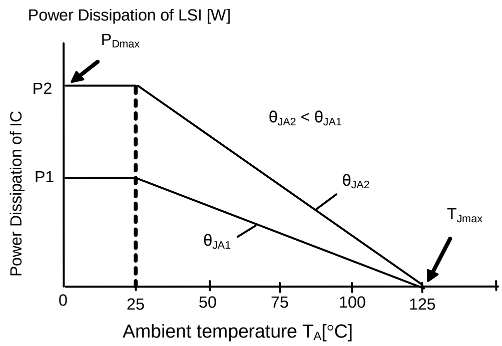
Power dissipation (total loss) indicates the power that the IC can consume at T_A=25°C (normal temperature). As the IC consumes power, it heats up, causing its temperature to be higher than the ambient temperature. The allowable temperature that the IC can accept is limited. This depends on the circuit configuration, manufacturing process, and consumable power.
Power dissipation is determined by the allowable temperature within the IC (maximum junction temperature) and the thermal resistance of the package used (heat dissipation capability). Maximum junction temperature is typically equal to the maximum storage temperature. The heat generated through the consumption of power by the IC radiates from the mold resin or lead frame of the package. Thermal resistance, represented by the symbol θ_{JA}°C/W, indicates this heat dissipation capability. Similarly, the temperature of an IC inside its package can be estimated by thermal resistance.
Figure 28(a) shows the model of the thermal resistance of the package. The equation below shows how to compute for the Thermal resistance (θ_{JA}), given the ambient temperature (T_A), junction temperature (T_{Jmax}), and power dissipation (P_D).

$$\theta_{JA} = (T_{Jmax} - T_A) / P_D \quad °C/W$$

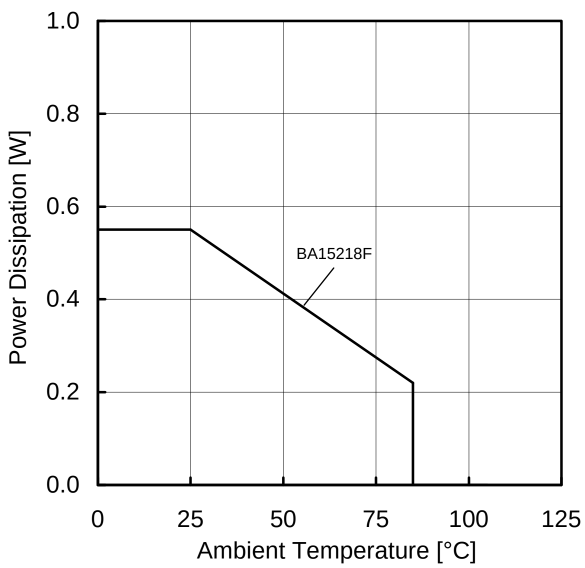
The derating curve in Figure 28(b) indicates the power that the IC can consume with reference to ambient temperature. Power consumption of the IC begins to attenuate at certain temperatures. This gradient is determined by Thermal resistance (θ_{JA}), which depends on the chip size, power consumption, package, ambient temperature, package condition, wind velocity, etc. This may also vary even when the same of package is used. Thermal reduction curve indicates a reference value measured at a specified condition. Figure 28(c) shows an example of the derating curve for BA15218F.



(a) Thermal resistance



(b) Derating curve



(c)BA15218F

5.5	mW/°C

When using the unit above T_A=25°C, subtract the value above per Celsius degree. Permissible dissipation is the value when FR4 glass epoxy board 70mm ×70mm ×1.6mm (copper foil area less than 3%) is mounted.

Figure 28. Thermal Resistance and Derating Curve

Examples of Circuit

○Voltage Follower

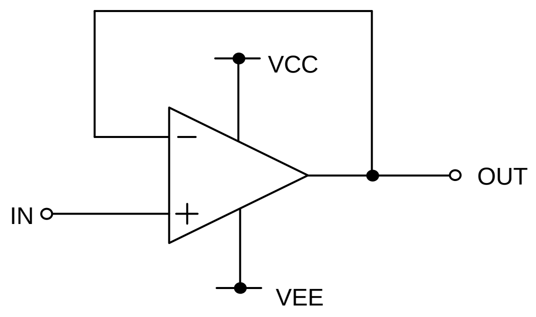


Figure 29. Voltage Follower Circuit

Voltage gain is 0dB.

Using this circuit, the output voltage (OUT) is configured to be equal to the input voltage (IN). This circuit also stabilizes the output voltage (OUT) due to high input impedance and low output impedance. Computation for output voltage (OUT) is shown below.

OUT=IN

○Inverting Amplifier

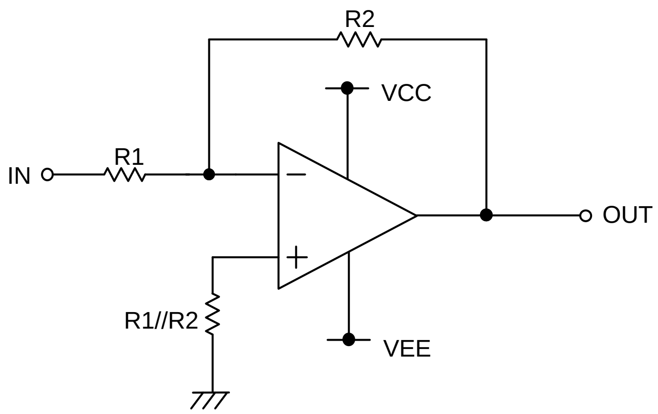


Figure 30. Inverting Amplifier Circuit

For inverting amplifier, input voltage (IN) is amplified by a voltage gain and depends on the ratio of R1 and R2. The out-of-phase output voltage is shown in the next expression

OUT=-(R2/R1)・IN

This circuit has input impedance equal to R1.

○Non-inverting Amplifier

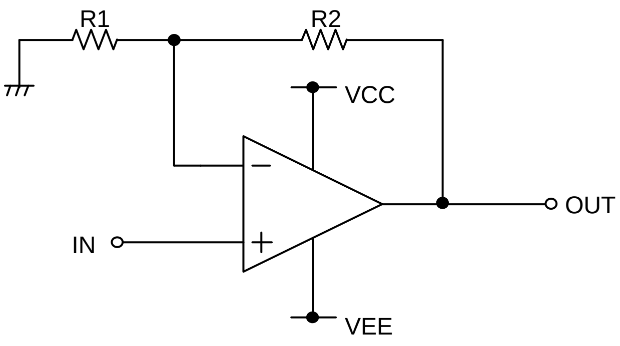


Figure 31. Non-inverting Amplifier Circuit

For non-inverting amplifier, input voltage (IN) is amplified by a voltage gain, which depends on the ratio of R1 and R2. The output voltage (OUT) is in-phase with the input voltage (IN) and is shown in the next expression.

OUT=(1 + R2/R1)・IN

Effectively, this circuit has high input impedance since its input side is the same as that of the operational amplifier.

Operational Notes

1. **Reverse Connection of Power Supply**
Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Thermal Consideration**
Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. The absolute maximum rating of the P_D stated in this specification is when the IC is mounted on a 70mm x 70mm x 1.6mm glass epoxy board. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the P_D rating.

6. **Recommended Operating Conditions**
These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. **Inrush Current**
When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. **Operation Under Strong Electromagnetic Field**
Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. **Testing on Application Boards**
When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. **Inter-pin Short and Mounting Errors**
Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

11. **Regarding the Input Pin of the IC**
This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure 32):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Operational Notes – continued

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

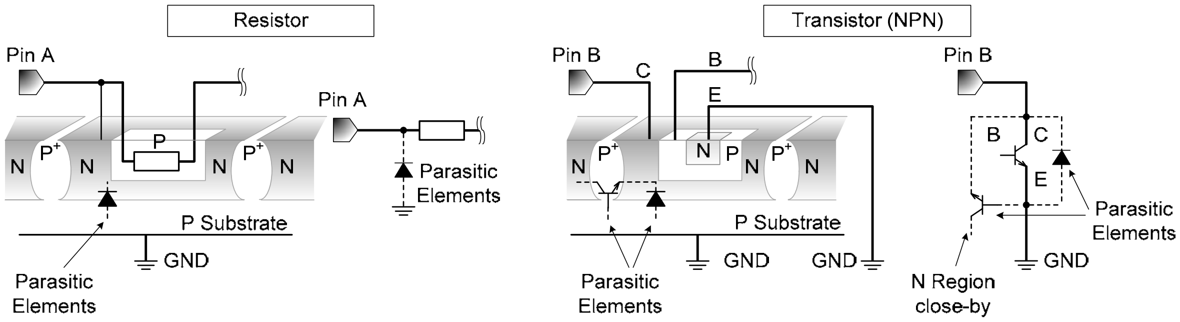


Figure 32. Example of monolithic IC structure

12. Unused circuits
When there are unused op-amps, it is recommended that they are connected as in Figure 33, setting the non-inverting input terminal to a potential within the in-phase input voltage range (V_{ICM}).

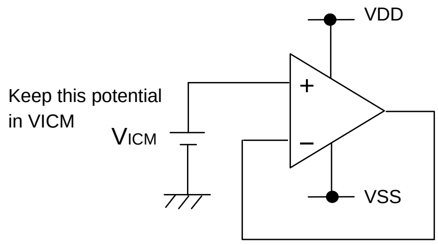


Figure 33. Example of Application Circuit for Unused Op-amp

13. Input Voltage
Applying VEE +36V to the input terminal is possible without causing deterioration of the electrical characteristics or destruction, regardless of the supply voltage. However, this does not ensure normal circuit operation. Please note that the circuit operates normally only when the input voltage is within the common mode input voltage range of the electric characteristics.

14. Power supply(single/dual)
The op-amp operates when the voltage supplied is between VCC and VEE. Therefore, the single supply op-amp can be used as dual supply op-amp as well.

15. Output capacitor
If a large capacitor is connected between the output pin and VEE pin, current from the charged capacitor will flow into the output pin and may destroy the IC when the VCC pin is shorted to ground or pulled down to 0V. Use a capacitor smaller than 0.1uF between output pin and VEE pin.

16. Oscillation by output capacitor
Please pay attention to the oscillation by output capacitor and in designing an application of negative feedback loop circuit with these ICs.

17. Short-circuit of Output Terminal
When output terminal and VCC or VEE terminal are shorted, excessive Output current may flow under some conditions, and heating may destroy IC. It is necessary to connect a resistor as shown in Figure 34, thereby protecting against load shorting.

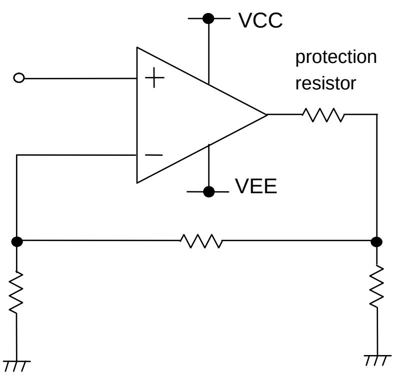
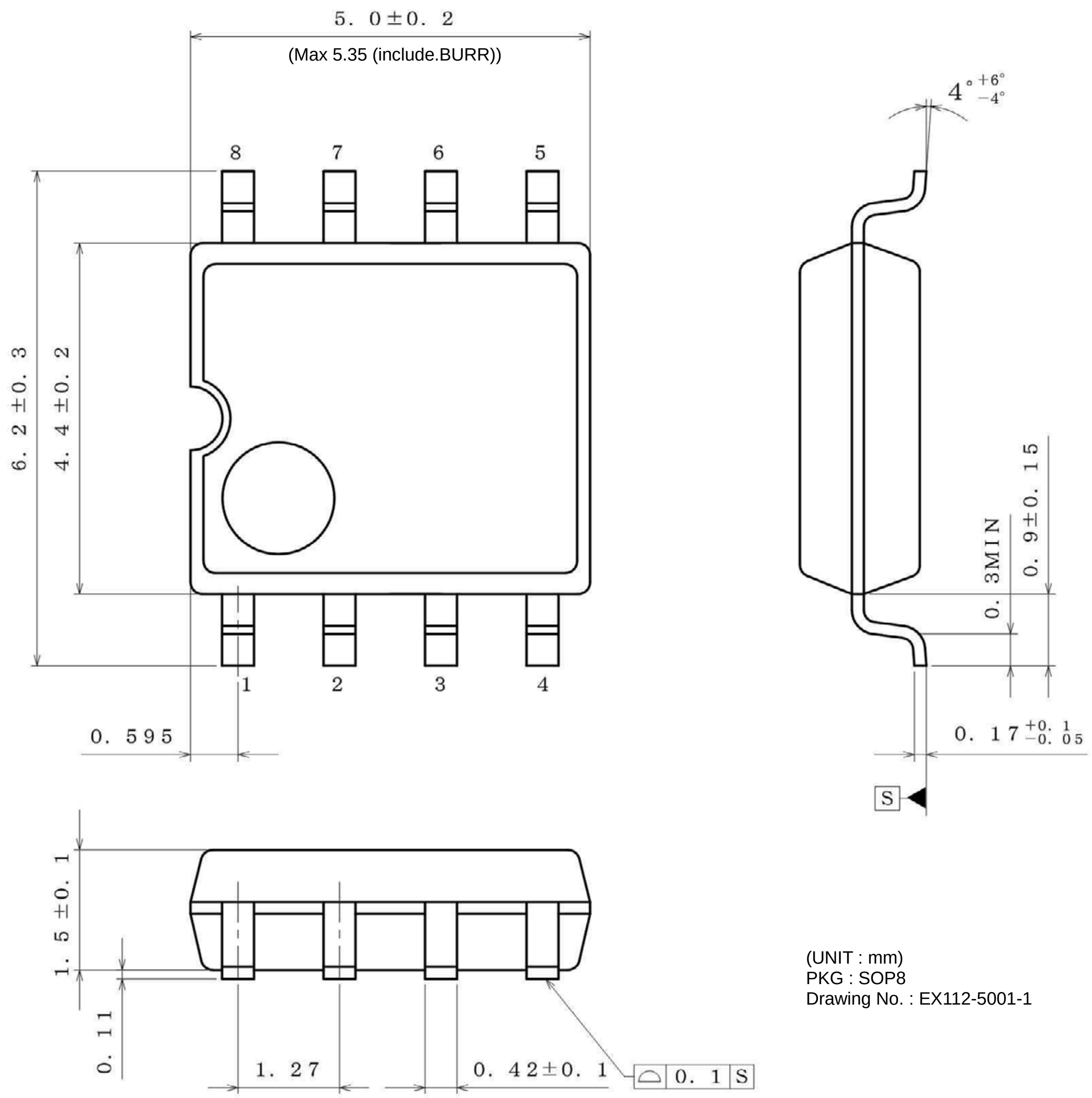


Figure 34. The Example of Output Short Protection

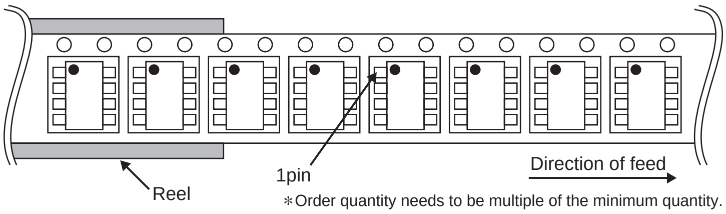
Physical Dimensions Tape and Reel Information

Package Name	SOP8



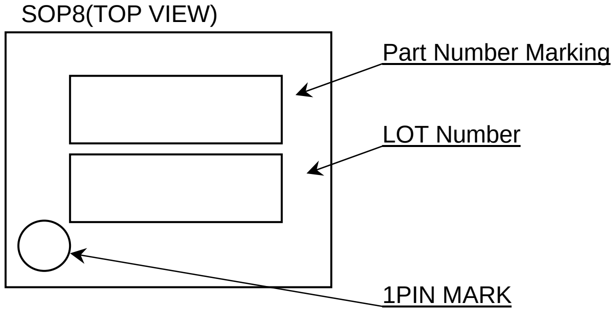
<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

Marking Diagrams

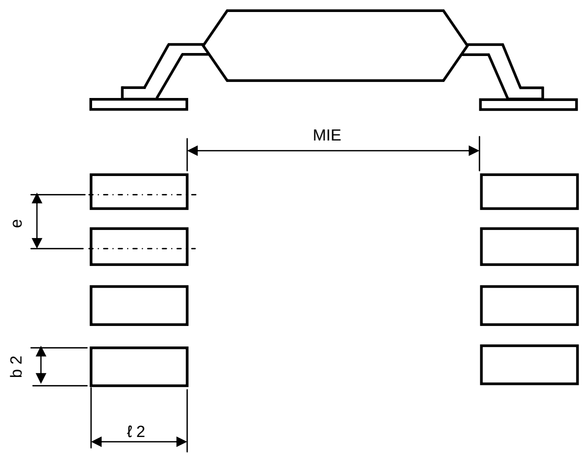


Product Name	Package Type	Marking
BA15218F	SOP8	15218

Land Pattern Data

All dimensions in mm

PKG	Land pitch e	Land space MIE	Land length ≧ℓ2	Land width b2
SOP8	1.27	4.60	1.10	0.76



Revision History

Date	Revision	Changes
10.SEP.2013	001	New Release

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(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation (Pd) depending on Ambient temperature (Ta). When used in sealed area, confirm the actual ambient temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used; if flow soldering method is preferred, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

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1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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