

TOSHIBA Field-Effect Transistor Silicon P-Channel MOS Type (U-MOSVI)

SSM3J56MFV

○ Load Switching Applications

- 1.2 V drive
- Low ON-resistance: $R_{DS(ON)} = 390 \text{ m}\Omega$ (max) (@ $V_{GS} = -4.5 \text{ V}$)
 $R_{DS(ON)} = 480 \text{ m}\Omega$ (max) (@ $V_{GS} = -2.5 \text{ V}$)
 $R_{DS(ON)} = 660 \text{ m}\Omega$ (max) (@ $V_{GS} = -1.8 \text{ V}$)
 $R_{DS(ON)} = 900 \text{ m}\Omega$ (max) (@ $V_{GS} = -1.5 \text{ V}$)
 $R_{DS(ON)} = 4000 \text{ m}\Omega$ (max) (@ $V_{GS} = -1.2 \text{ V}$)

Absolute Maximum Ratings (Ta = 25°C)

Characteristic	Symbol	Rating	Unit
Drain-Source voltage	V_{DSS}	-20	V
Gate-Source voltage	V_{GSS}	± 8	V
Drain current	DC	I_D (Note 1)	-800
	Pulse	I_{DP} (Note 1)	-1600
Power dissipation	P_D (Note 2)	150	mW
	P_D (Note 3)	500	
	$t < 5\text{s}$	800	
Channel temperature	T_{ch}	150	°C
Storage temperature range	T_{stg}	-55 to 150	°C

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: The channel temperature should not exceed 150°C during use.

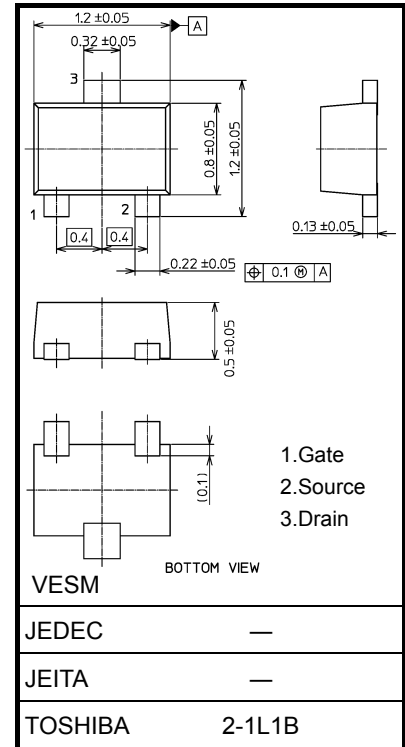
Note 2: Mounted on a FR4 board.

(25.4 mm × 25.4 mm × 1.6 mm, Cu Pad: 0.585 mm²)

Note 3: Mounted on a FR4 board.

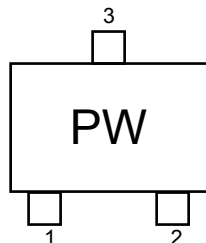
(25.4 mm × 25.4 mm × 1.6 mm, Cu Pad: 645 mm²)

Unit: mm

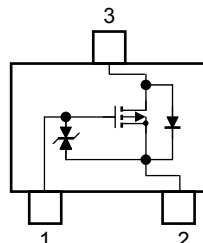


Weight: 1.5mg (typ.)

Marking



Equivalent Circuit (top view)



Handling Precaution

When handling individual devices that are not yet mounted on a circuit board, make sure that the environment is protected against electrostatic discharge. Operators should wear antistatic clothing, and containers and other objects that come into direct contact with devices should be made of antistatic materials.

Thermal resistance $R_{th(ch-a)}$ and Power dissipation P_D vary depending on board material, board area, board thickness and pad area. When using this device, please take heat dissipation into consideration.

Start of commercial production
2011-05

Electrical Characteristics (Ta = 25°C)

Characteristic	Symbol	Test Conditions	Min	Typ.	Max	Unit
Drain-source breakdown voltage	$V_{(BR)DSS}$	$I_D = -1 \text{ mA}, V_{GS} = 0 \text{ V}$	-20	—	—	V
	$V_{(BR)DSX}$	$I_D = -1 \text{ mA}, V_{GS} = 5 \text{ V}$ (Note 5)	-15	—	—	V
Drain cut-off current	I_{DSS}	$V_{DS} = -20 \text{ V}, V_{GS} = 0 \text{ V}$	—	—	-1	μA
Gate leakage current	I_{GSS}	$V_{GS} = \pm 8 \text{ V}, V_{DS} = 0 \text{ V}$	—	—	± 1	μA
Gate threshold voltage	V_{th}	$V_{DS} = -3 \text{ V}, I_D = -1 \text{ mA}$	-0.3	—	-1.0	V
Forward transfer admittance	$ Y_{fs} $	$V_{DS} = -3 \text{ V}, I_D = -100 \text{ mA}$ (Note 4)	0.5	1.0	—	S
Drain-source ON-resistance	$R_{DS(ON)}$	$I_D = -800 \text{ mA}, V_{GS} = -4.5 \text{ V}$ (Note 4)	—	310	390	m Ω
		$I_D = -500 \text{ mA}, V_{GS} = -2.5 \text{ V}$ (Note 4)	—	380	480	
		$I_D = -200 \text{ mA}, V_{GS} = -1.8 \text{ V}$ (Note 4)	—	470	660	
		$I_D = -100 \text{ mA}, V_{GS} = -1.5 \text{ V}$ (Note 4)	—	560	900	
		$I_D = -10 \text{ mA}, V_{GS} = -1.2 \text{ V}$ (Note 4)	—	770	4000	
Input capacitance	C_{iss}	$V_{DS} = -10 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	—	100	—	pF
Output capacitance	C_{oss}		—	16	—	
Reverse transfer capacitance	C_{rss}		—	10	—	
Switching time	Turn-on time	t_{on}	$V_{DD} = -10 \text{ V}, I_D = -200 \text{ mA}$ $V_{GS} = 0 \text{ to } -2.5 \text{ V}, R_G = 50 \Omega$	—	8	ns
	Turn-off time	t_{off}		—	26	
Total gate charge	Q_g	$V_{DD} = -10 \text{ V}, I_D = -800 \text{ mA},$ $V_{GS} = -4.5 \text{ V}$	—	1.6	—	nC
Gate-source charge	Q_{gs1}		—	0.2	—	
Gate-drain charge	Q_{gd}		—	0.4	—	
Drain-source forward voltage	V_{DSF}	$I_D = 800 \text{ mA}, V_{GS} = 0 \text{ V}$ (Note 4)	—	0.9	1.2	V

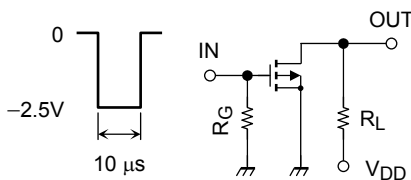
Note 4: Pulse test

Note 5: If a forward bias is applied between gate and source, this device enters $V_{(BR)DSX}$ mode.

Note that the drain-source breakdown voltage is lowered in this mode.

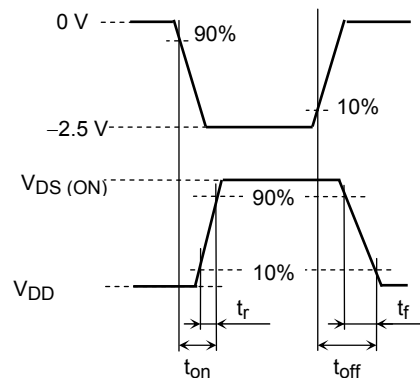
Switching Time Test Circuit

(a) Test Circuit



$V_{DD} = -10 \text{ V}$
 $R_G = 50 \Omega$
 Duty $\leq 1\%$
 V_{IN} : $t_r, t_f < 5 \text{ ns}$
 Common Source
 $T_a = 25^\circ\text{C}$

(b) V_{IN}

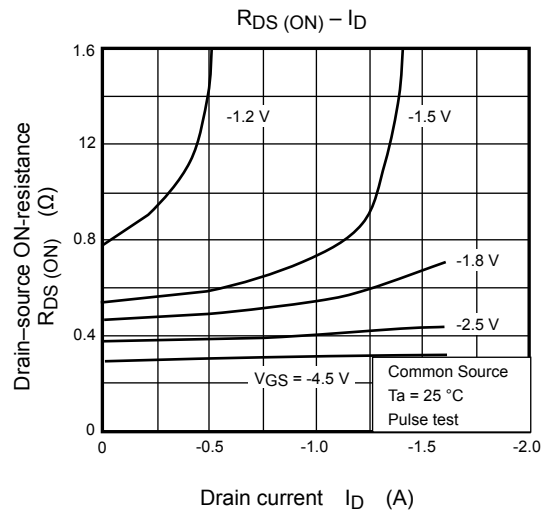
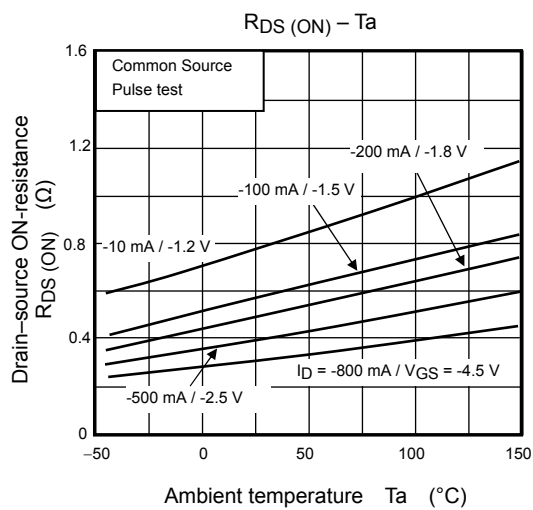
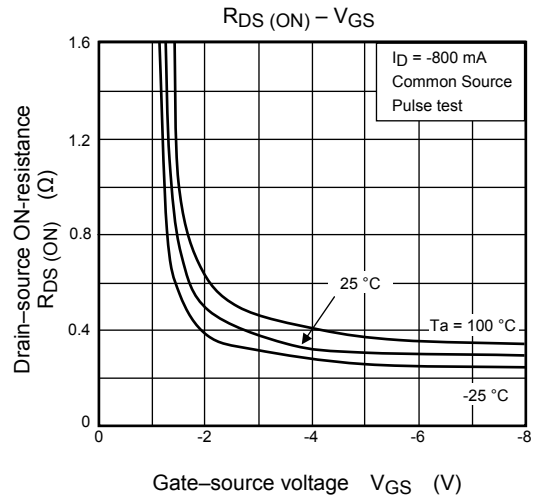
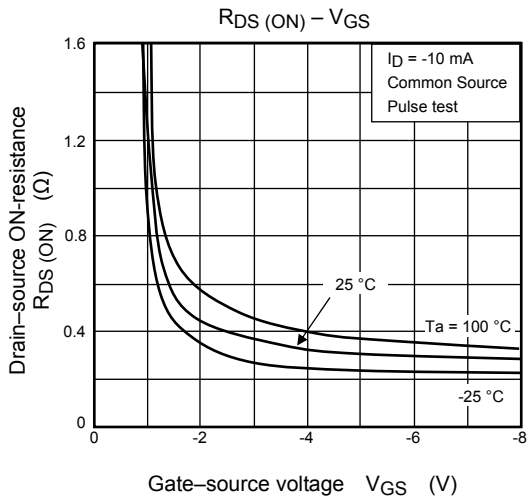
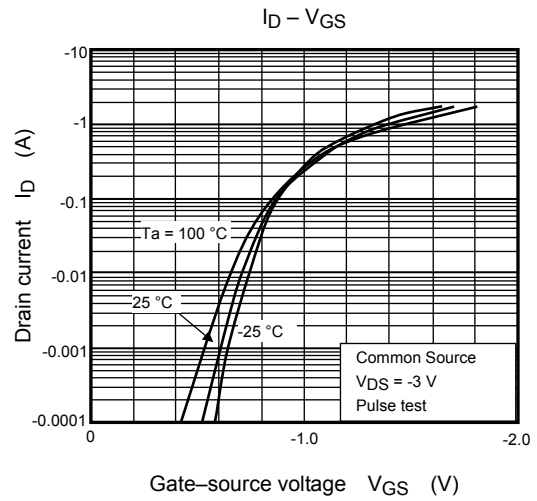
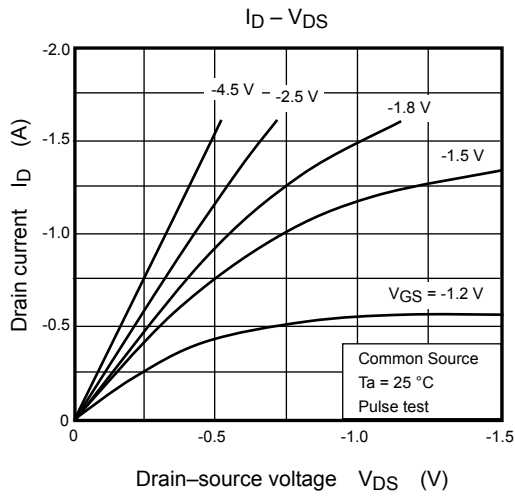


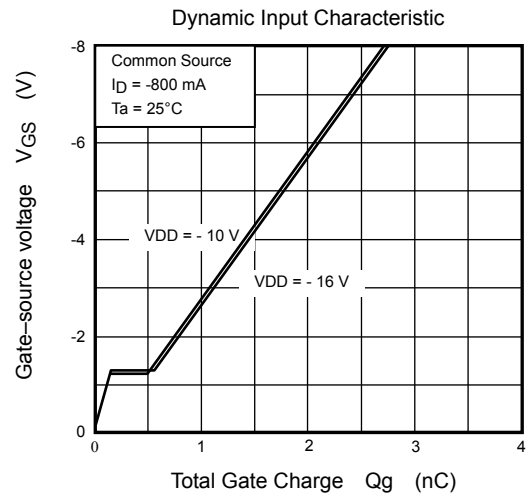
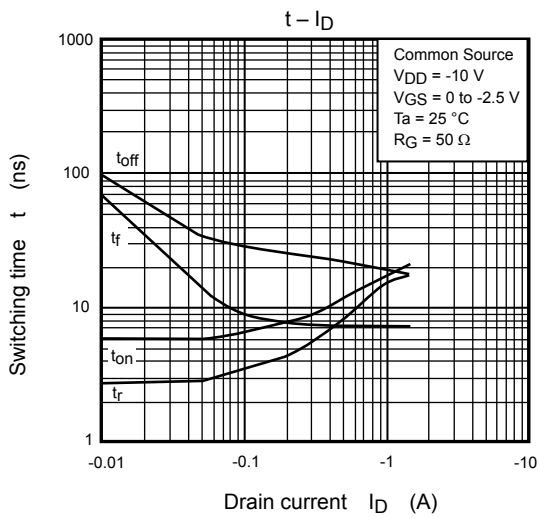
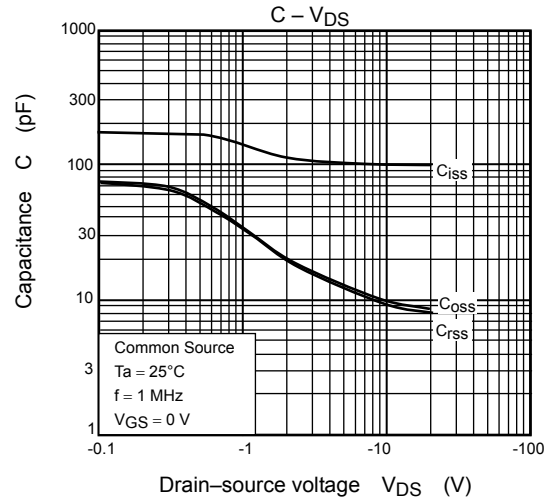
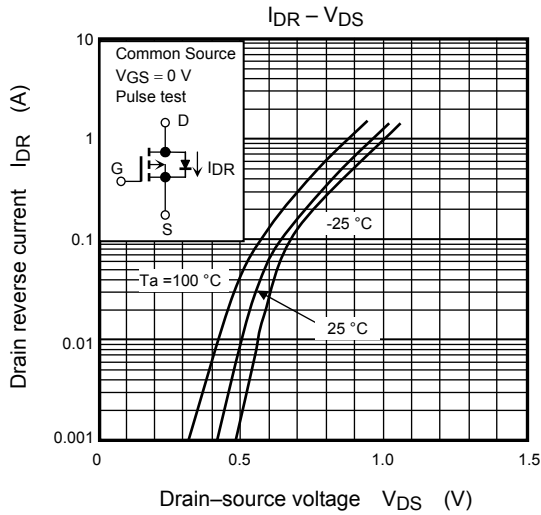
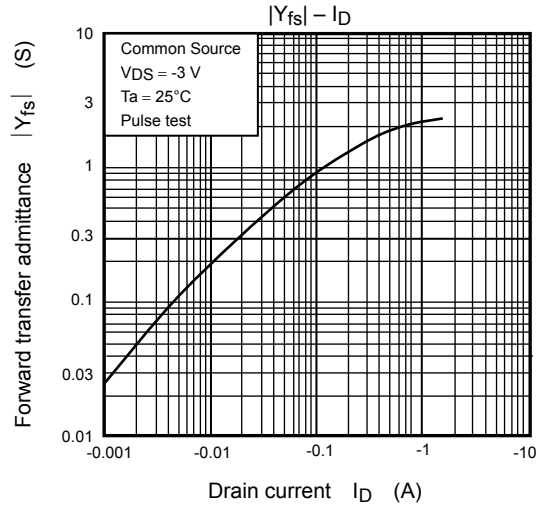
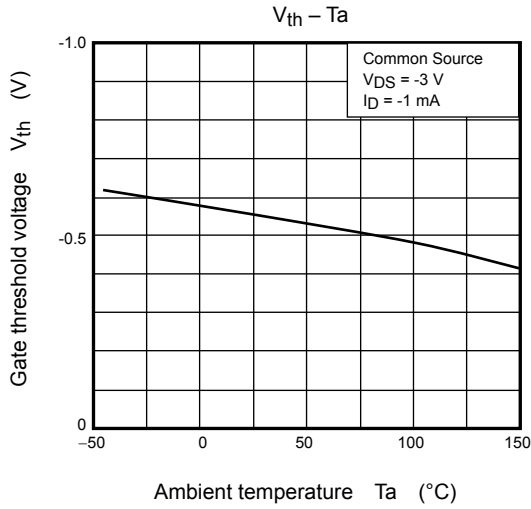
(c) V_{OUT}

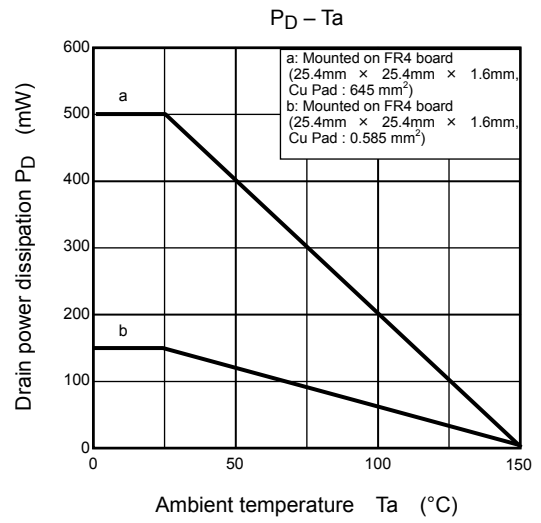
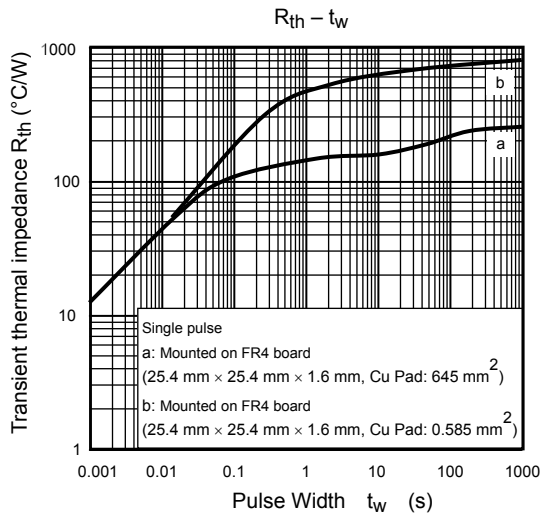
Notice on Usage

V_{th} can be expressed as the voltage between gate and source when the low operating current value is $I_D = -1 \text{ mA}$ for this product. For normal switching operation, $V_{GS(ON)}$ requires a higher voltage than V_{th} and $V_{GS(OFF)}$ requires a lower voltage than V_{th} . (The relationship can be established as follows: $V_{GS(OFF)} < V_{th} < V_{GS(ON)}$.)

Take this into consideration when using the device.







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