

TOSHIBA Field-Effect Transistor Silicon P-Channel MOS Type (U-MOSVI)

## SSM3J334R

### Power Management Switch Applications

- Low ON-resistance:  $R_{DS(ON)} = 71 \text{ m}\Omega$  (max) (@ $V_{GS} = -10 \text{ V}$ )  
 $R_{DS(ON)} = 105 \text{ m}\Omega$  (max) (@ $V_{GS} = -4.5 \text{ V}$ )  
 $R_{DS(ON)} = 136 \text{ m}\Omega$  (max) (@ $V_{GS} = -4.0 \text{ V}$ )

### Absolute Maximum Ratings ( $T_a = 25^\circ\text{C}$ )

Characteristic	Symbol	Rating	Unit
Drain-Source voltage	$V_{DSS}$	-30	V
Gate-Source voltage	$V_{GSS}$	$\pm 20$	V
Drain current	DC	$I_D$ (Note 1)	-4
	Pulse	$I_{DP}$ (Note 1,2)	-16
Power dissipation	$P_D$ (Note 3)		1
		$t < 10\text{s}$	2
Channel temperature	$T_{ch}$	150	$^\circ\text{C}$
Storage temperature range	$T_{stg}$	-55 to 150	$^\circ\text{C}$

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

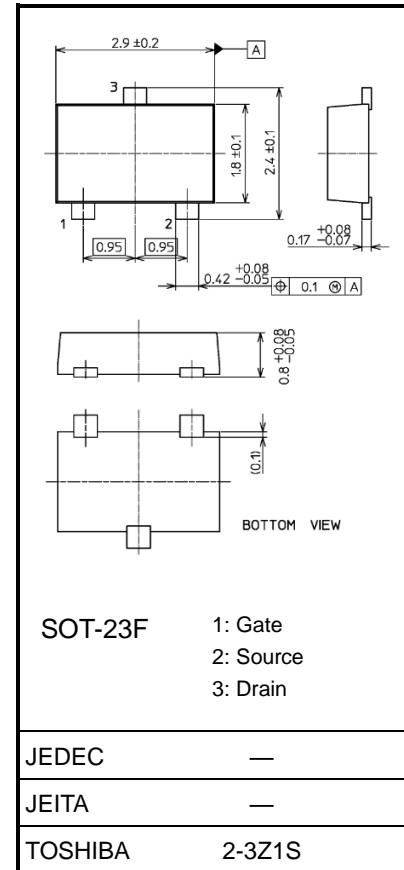
Note 1: The channel temperature should not exceed  $150^\circ\text{C}$  during use.

Note 2:  $PW \leq 1\text{ms}$ , Duty  $\leq 1\%$

Note 3: Mounted on a FR4 board.

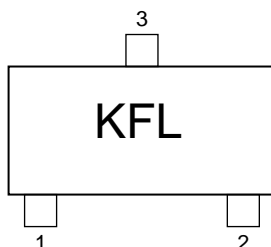
( $25.4 \text{ mm} \times 25.4 \text{ mm} \times 1.6 \text{ mm}$ , Cu Pad:  $645 \text{ mm}^2$ )

Unit: mm

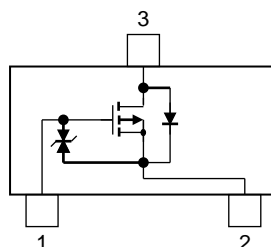


Weight: 11 mg (typ.)

### Marking



### Equivalent Circuit (Top View)



Start of commercial production  
2010-08

## Electrical Characteristics (Ta = 25°C)

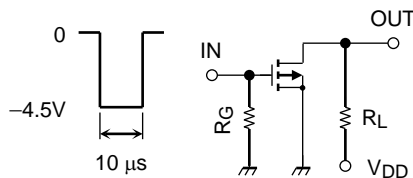
Characteristic	Symbol	Test Conditions	Min	Typ.	Max	Unit
Drain-Source breakdown voltage	V (BR) DSS	ID = -10 mA, VGS = 0 V	-30	—	—	V
	V (BR) DSX	ID = -10 mA, VGS = 10 V (Note 5)	-21	—	—	V
Drain cut-off current	IDSS	VDS = -30 V, VGS = 0 V	—	—	-1	μA
Gate leakage current	IGSS	VGS = ±16 V, VDS = 0 V	—	—	±10	μA
Gate threshold voltage	Vth	VDS = -10 V, ID = -100 μA	-0.8	—	-2.0	V
Forward transfer admittance	Yfs	VDS = -10 V, ID = -1.0 A (Note 4)	2.3	4.6	—	S
Drain-source ON-resistance	RDS (ON)	ID = -3.0 A, VGS = -10 V (Note 4)	—	54	71	mΩ
		ID = -2.0 A, VGS = -4.5 V (Note 4)	—	80	105	
		ID = -1.0 A, VGS = -4.0 V (Note 4)	—	89	136	
Input capacitance	Ciss	VDS = -15 V, VGS = 0 V f = 1 MHz	—	280	—	pF
Output capacitance	Coss		—	55	—	
Reverse transfer capacitance	Crss		—	40	—	
Switching time	Turn-on time	ton	VDD = -15 V, ID = -1.0 A VGS = 0 to -4.5 V, RG = 10 Ω	—	13	ns
	Turn-off time	toff		—	22	
Total Gate Charge	Qg	VDD = -15 V, ID = -4.0 A, VGS = -10 V	—	5.9	—	nC
Gate-Source Charge	Qgs1		—	0.8	—	
Gate-Drain Charge	Qgd		—	1.2	—	
Drain-Source forward voltage	VDSF	ID = 4.0 A, VGS = 0 V (Note 4)	—	0.9	1.2	V

Note4: Pulse test

Note5: If a forward bias is applied between gate and source, this device enters V(BR)DSX mode. Note that the drain-source breakdown voltage is lowered in this mode.

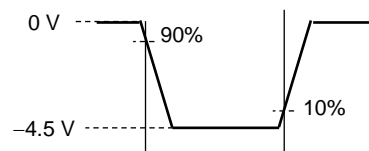
## Switching Time Test Circuit

### (a) Test Circuit

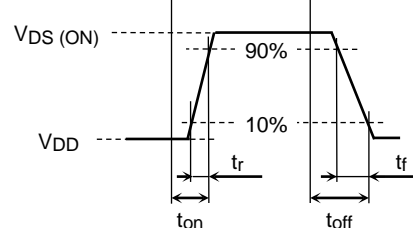


VDD = -15 V  
 RG = 10 Ω  
 Duty ≤ 1%  
 VIN: tr, tf < 5 ns  
 Common Source  
 Ta = 25°C

### (b) VIN



### (c) VOUT



## Notice on Usage

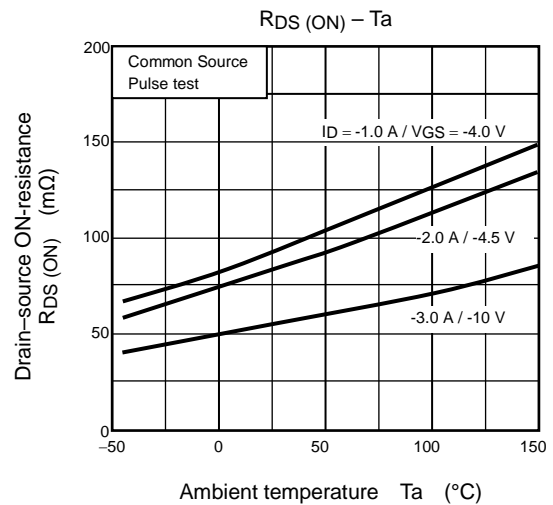
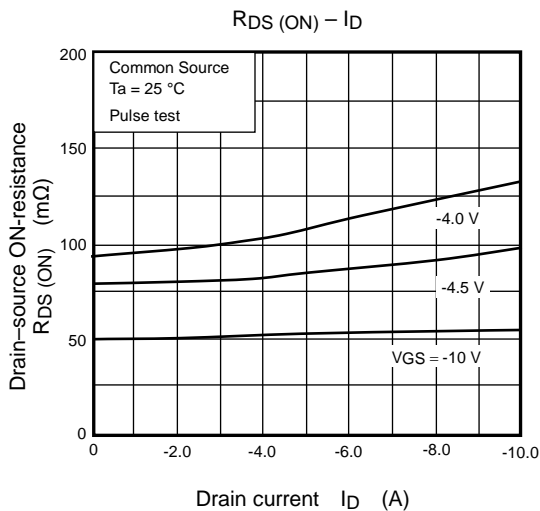
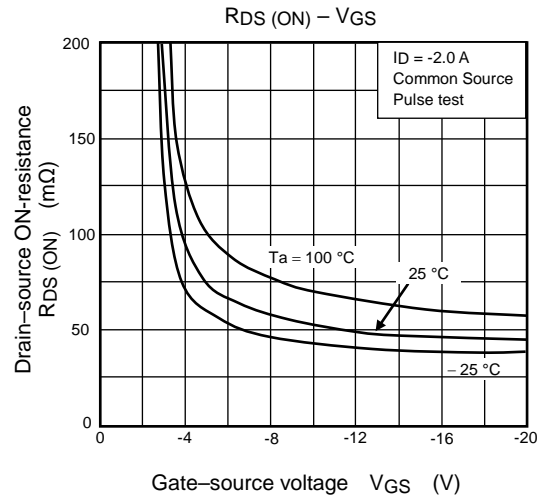
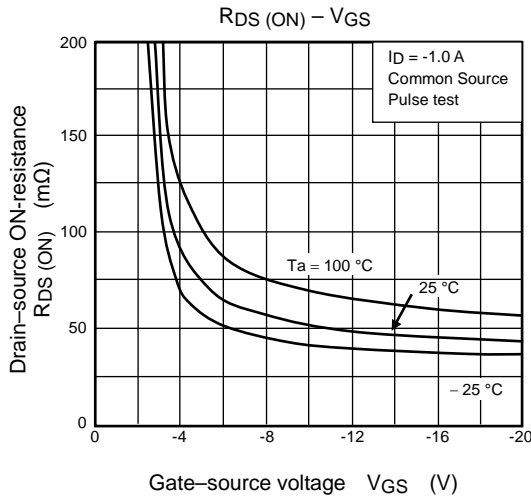
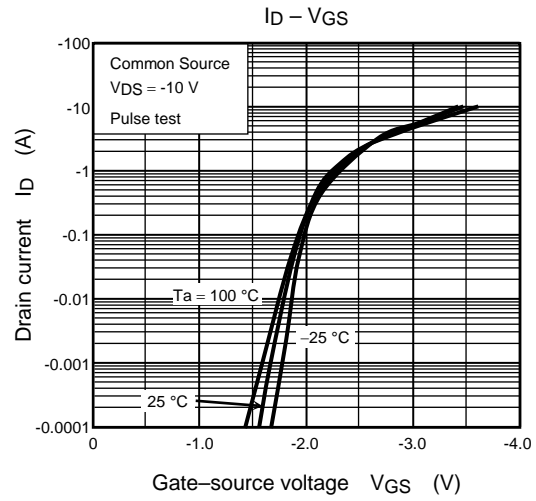
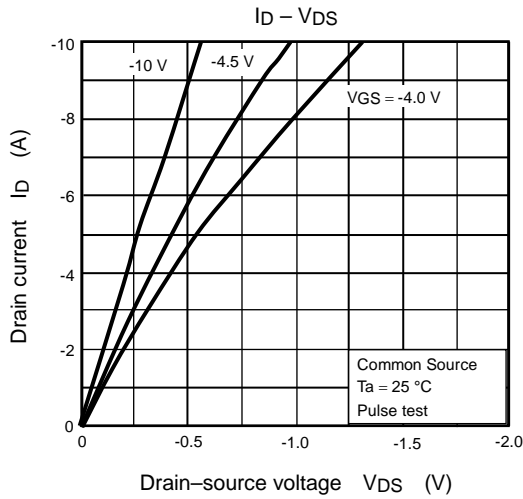
Let Vth be the voltage applied between gate and source that causes the drain current (ID) to be low (-100μA for the SSM3J334R). Then, for normal switching operation, VGS(on) must be higher than Vth, and VGS(off) must be lower than Vth. This relationship can be expressed as: VGS(off) < Vth < VGS(on).

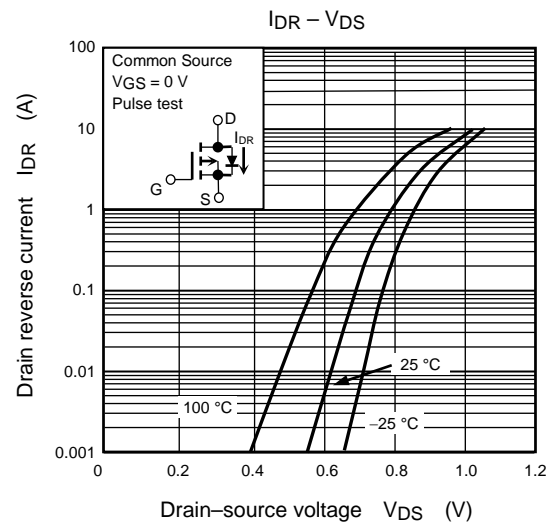
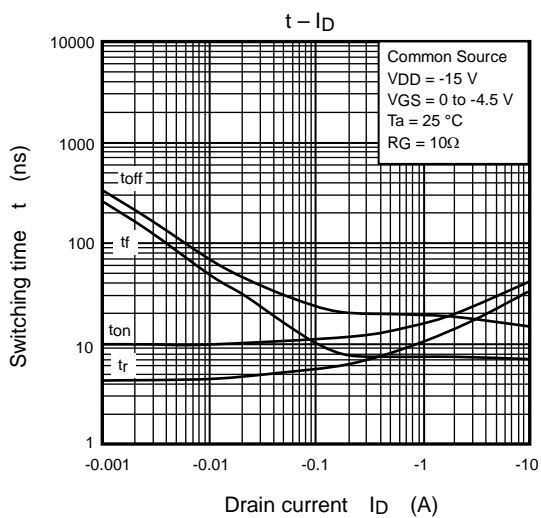
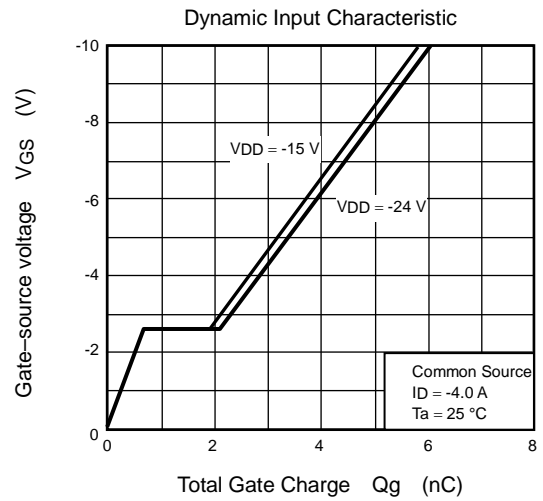
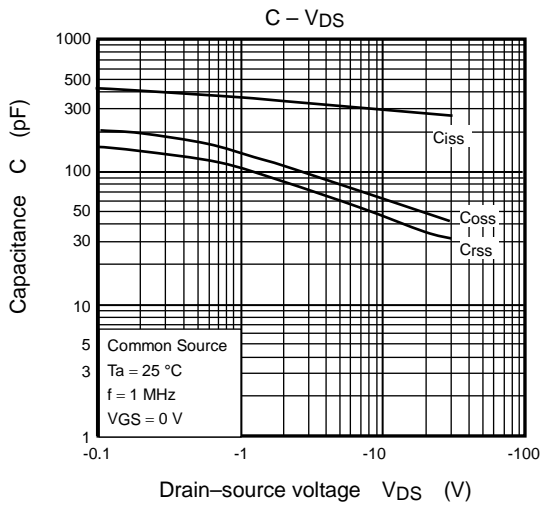
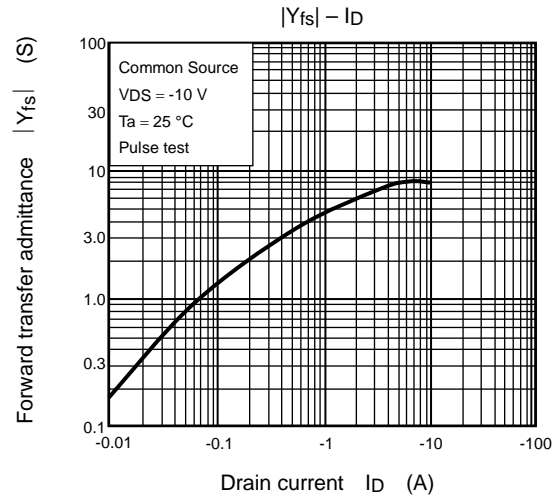
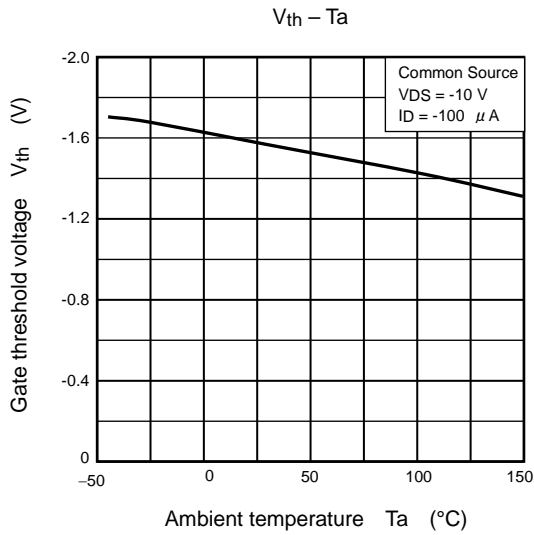
Take this into consideration when using the device.

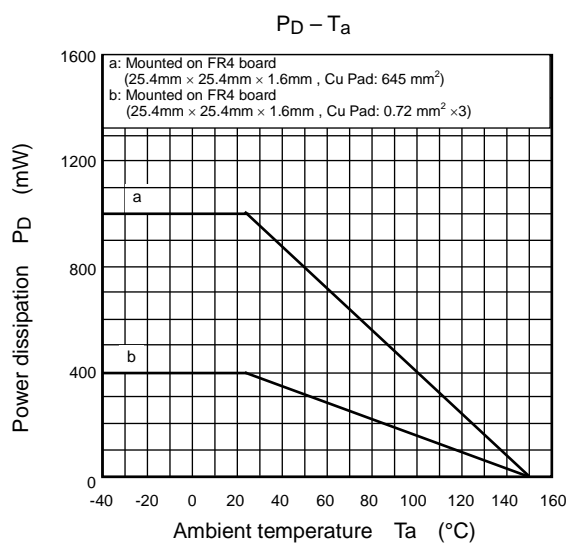
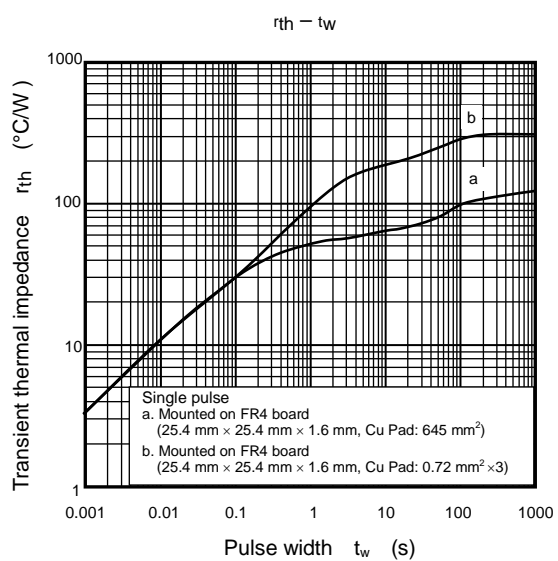
## Handling Precaution

When handling individual devices that are not yet mounted on a circuit board, make sure that the environment is protected against electrostatic discharge. Operators should wear antistatic clothing, and containers and other objects that come into direct contact with devices should be made of antistatic materials.

Thermal resistance Rth(ch-a) and power dissipation PD vary depending on board material, board area, board thickness and pad area. When using this device, please take heat dissipation into consideration







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