SigmaDSP Digital Audio Processor with Flexible Audio Routing Matrix

Data Sheet

ADAU1442/ADAU1445/ADAU1446

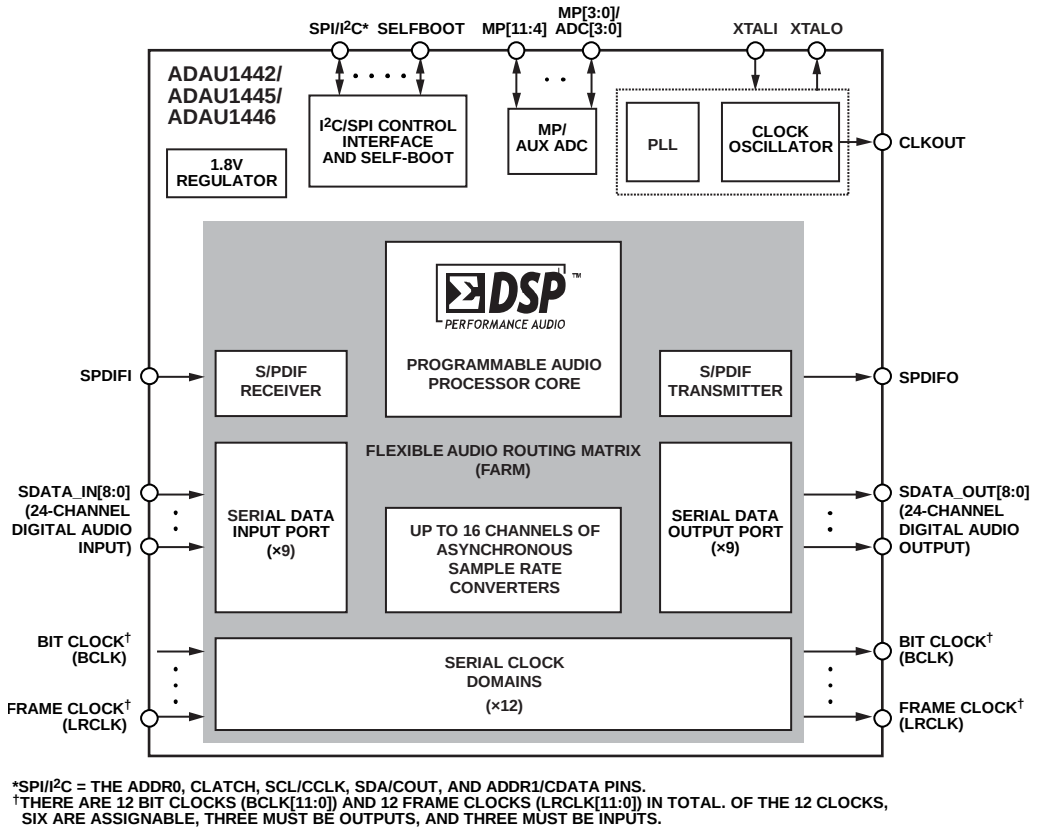
FEATURES

- Fully programmable audio digital signal processor (DSP) for enhanced sound processing
- Features SigmaStudio, a proprietary graphical programming tool for the development of custom signal flows
- 172 MHz SigmaDSP core; 3584 instructions per sample at 48 kHz
- 4k parameter RAM, 8k data RAM
- Flexible audio routing matrix (FARM)
  - 24-channel digital input and output
  - Up to 8 stereo asynchronous sample rate converters (from 1:8 up to 7.75:1 ratio and 139 dB DNR)
  - Stereo S/PDIF input and output
- Supports serial and TDM I/O, up to f_S = 192 kHz
- Multichannel byte-addressable TDM serial port
- Pool of 170 ms digital audio delay (at 48 kHz)
- Clock oscillator for generating master clock from crystal
- PLL for generating core clock from common audio clocks
- I²C and SPI control interfaces
- Standalone operation
  - Self-boot from serial EEPROM
  - 4-channel, 10-bit auxiliary control ADC
  - Multipurpose pins for digital controls and outputs
- Easy implementation of available third-party algorithms
- On-chip regulator for generating 1.8 V from 3.3 V supply
- 100-lead TQFP and LQFP packages
- Temperature range: −40°C to +105°C

APPLICATIONS

- Automotive audio processing
  - Head units
  - Navigation systems
  - Rear-seat entertainment systems
  - DSP amplifiers (sound system amplifiers)
- Commercial audio processing

FUNCTIONAL BLOCK DIAGRAM



*SPI/I²C = THE ADDR0, CLATCH, SCL/CCLK, SDA/COUT, AND ADDR1/CDATA PINS.
†THERE ARE 12 BIT CLOCKS (BCLK[11:0]) AND 12 FRAME CLOCKS (LRCLK[11:0]) IN TOTAL. OF THE 12 CLOCKS, SIX ARE ASSIGNABLE, THREE MUST BE OUTPUTS, AND THREE MUST BE INPUTS.

Figure 1.

Rev. D
Document Feedback

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REVISION HISTORY

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9/10—Rev. B to Rev. C

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Changes to Stereo ASRC[3:0] Lock Status and Mute Register (Address 0xE101), Stereo ASRC[3:0] Mute Ramp Disable Register (Address 0xE103), and Stereo ASRC[7:4] Lock Status and Mute Register (Address 0xE141) Sections 58
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4/10—Rev. A to Rev. B

Added ADAU1442 ..... Universal
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Added Multipurpose Pin Value Registers (Address 0x129A to Address 0x12A5) Section and Table 66; Renumbered Sequentially 68
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4/09—Rev. 0 to Rev. A

Added ADAU1446 ..... Universal
Added LQFP ..... Universal
Added Minimum Digital Current (DVDD) of ADAU1446, Maximum Digital Current (DVDD) of ADAU1446, and AVDD, DVDD, PVDD During Operation of ADAU1446 Parameters, Table 1 5
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Added Table 43; Renumbered Sequentially 61
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1/09—Revision 0: Initial Version

GENERAL DESCRIPTION

The ADAU1442/ADAU1445/ADAU1446 are enhanced audio processors that allow full flexibility in routing all input and output signals. The SigmaDSP® core features full 28-bit processing (56-bit in double-precision mode), synchronous parameter loading for ensuring filter stability, and 100% code efficiency with the SigmaStudio™ tools. This DSP allows system designers to compensate for the real-world limitations of speakers, amplifiers, and listening environments, resulting in a dramatic improvement of the perceived audio quality through speaker equalization, multiband compression, limiting, and third-party branded algorithms.

The flexible audio routing matrix (FARM) allows the user to multiplex inputs from multiple sources running at various sample rates to or from the SigmaDSP core. This drastically reduces the complexity of signal routing and clocking issues in the audio system. FARM includes up to eight stereo asynchronous sample rate converters (depending on the device model), Sony/Philips Digital Interconnect Format (S/PDIF) input and output, and serial (I^2S) and time division multiplexing (TDM) I/Os. Any of these inputs can be routed to the SigmaDSP core or to any of the asynchronous sample rate converters (ASRCs). Similarly, any one of the output signals can be taken from the SigmaDSP core or from any of the ASRC outputs. This routing scheme, which can be modified at any time via control registers, allows for maximum system flexibility.

The ADAU1442, ADAU1445, and ADAU1446 differ only in ASRC functionality and packaging. The ADAU1442/ADAU1445 contain 16 channels of ASRCs and are packaged in TQFP packages, whereas the ADAU1446 contains no ASRCs and is packaged in an LQFP. The ADAU1442 can handle nine clock domains, the ADAU1445 can handle three clock domains, and the ADAU1446 can handle one clock domain.

The ADAU1442/ADAU1445/ADAU1446 can be controlled in one of two operational modes: the settings of the chip can be loaded and dynamically updated through the SPI/I^2C® port, or the DSP can self-boot from an external EEPROM in a system with no microcontroller. There is also a bank of multipurpose (MP) pins that can be used as general-purpose digital I/Os or as inputs to the 4-channel auxiliary control ADC.

The ADAU1442/ADAU1445/ADAU1446 are supported by the SigmaStudio graphical development environment. This software includes audio processing blocks such as FIR and IIR filters, dynamics processors, mixers, low level DSP functions, and third-party algorithms for fast development of custom signal flows.

Table 1.

Device	ASRC Channels	ASRC Clock Domains	Package
ADAU1442	16	8	TQFP
ADAU1445	16	2	TQFP
ADAU1446	0	N/A	LQFP

SPECIFICATIONS

AVDD = 3.3 V, DVDD = 1.8 V, PVDD = 3.3 V, IOVDD = 3.3 V, T_A = 25°C, master clock input = 12.288 MHz, core clock f_{CORE} = 172.032 MHz, I/O pins set to 2 mA drive setting, unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
ANALOG PERFORMANCE					AVDD = 3.3 V ± 10%.
Auxiliary Analog Inputs					
Resolution		10		Bits	
Full-Scale Analog Input		AVDD		V	
Integral Nonlinearity (INL)	−2.3		+2.3	LSB	
Differential Nonlinearity (DNL)	−2.0		+2.0	LSB	
Gain Error	−2.0		+2.0	LSB	
Input Impedance		200		kΩ	
Sample Rate		f_{CORE}/896		kHz	4:1 multiplexed input, each channel at f_{CORE}/3584. For f_{CORE} = 172.032 MHz, each channel is sampled at 48 kHz.
POWER					
Supply Voltage					
Analog Voltage (AVDD)	2.97	3.3	3.63	V	
Digital Voltage (DVDD)	1.62	1.8	1.98	V	
PLL Voltage (PVDD)	2.97	3.3	3.63	V	
IOVDD Voltage (IOVDD)	2.97	3.3	3.63	V	
Supply Current					
Analog Current (AVDD)		2		mA	
PLL Current (PVDD)		10		mA	
I/O Current (IOVDD)		10		mA	Depends greatly on the number of active serial ports, clock pins, and characteristics of external loads.
Digital Current (DVDD)					
ADAU1442					
Typical Program		335		mA	Test program includes 16 channels I/O, 10-band EQ per channel, all ASRCs active.
Minimal Program		115		mA	Test program includes 2 channels I/O, 10-band EQ per channel.
ADAU1445					
Typical Program		270		mA	Test program includes 16 channels I/O, 10-band EQ per channel, all ASRCs active.
Minimal Program		115		mA	Test program includes 2 channels I/O, 10-band EQ per channel.
ADAU1446					
Typical Program		135		mA	Test program includes 16 channels I/O, 10-band EQ per channel, all ASRCs active.
Minimal Program		110			Test program includes 2 channels I/O, 10-band EQ per channel.
ASYNCHRONOUS SAMPLE RATE CONVERTERS[1]					
Dynamic Range		139		dB	A-weighted, 20 Hz to 20 kHz.
I/O Sample Rate	6		192	kHz	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
I/O Sample Rate Ratio	1:8		7.75:1		
THD + N		−133	−120	dB	
CRYSTAL OSCILLATOR					
Transconductance		40		mS	
REGULATOR[2]					
DVDD Voltage	1.65	1.75	1.85	V	Maximum 500 mA load.

[1] To calculate the group delay, refer to the SRC Group Delay section.
[2] Regulator specifications are calculated using an NJT4030P transistor from On Semiconductor in the circuit.

AVDD = 3.3 V ± 10%, DVDD = 1.8 V ± 10%, PVDD = 3.3 V, IOVDD = 3.3 V ± 10%, T_A = −40°C to +105°C, master clock input = 12.288 MHz, core clock f_{CORE} = 172.032 MHz, I/O pins set to 2 mA drive setting, unless otherwise noted.

Table 3.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
ANALOG PERFORMANCE					AVDD = 3.3 V ± 10%.
Auxiliary Analog Inputs					
Resolution		10		Bits	
Full-Scale Analog Input		AVDD		V	
Integral Nonlinearity (INL)	−2.3		+2.3	LSB	
Differential Nonlinearity (DNL)	−2.0		+2.0	LSB	
Gain Error	−2.0		+2.0	LSB	
Input Impedance		200		kΩ	
Sample Rate		f_{CORE}/896		kHz	4:1 multiplexed input, each channel at f_{CORE}/3584. For f_{CORE} = 172.032 MHz, each channel is sampled at 48 kHz.
DIGITAL I/O					
Input Voltage, High (V_{IH})	0.7 × IOVDD			V	Digital input pins except SPDIFI.[1]
Input Voltage, Low (V_{IL})			0.3 × IOVDD	V	Digital input pins except SPDIFI.[1]
Input Leakage, High (I_{IH}) at 3.3 V	−2		+2	µA	Digital input pins except MCLK and SPDIFI.
	−2		+8	µA	MCLK.
	60		140	µA	SPDIFI.
Input Leakage, Low (I_{IL}) at 0 V	−85		−10	µA	All other pins.
	−2		+2	µA	CLKMODEx, RSVD, PLLx, RESET.
	−8		+2	µA	MCLK.
	−140		−60	µA	SPDIFI.
High Level Output Voltage (V_{OH})	0.85 × IOVDD			V	I_{OH} = 1 mA.
Low Level Output Voltage (V_{OL})			0.1 × IOVDD	V	I_{OL} = 1 mA.
Input Capacitance (C_I)		5		pF	Guaranteed by design.
Multipurpose Pins Output Drive		2		mA	These pins are not designed for static current draw and should not drive LEDs directly.
POWER					
Supply Voltage					
Analog Voltage (AVDD)	2.97	3.3	3.63	V	
Digital Voltage (DVDD)	1.62	1.8	1.98	V	
PLL Voltage (PVDD)	2.97	3.3	3.63	V	
IOVDD Voltage (IOVDD)	2.97	3.3	3.63	V	
Supply Current					
Analog Current (AVDD)		2		mA	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
PLL Current (PVDD)		10		mA	
I/O Current (IOVDD)		10		mA	Depends greatly on the number of active serial ports, clock pins, and characteristics of external loads.
Maximum Digital Current (DVDD)					
ADAU1442			460	mA	Test program includes 24 channels I/O, fully utilized program RAM.
ADAU1445			365	mA	Test program includes 24 channels I/O, fully utilized program RAM.
ADAU1446			315	mA	Test program includes 24 channels I/O, fully utilized program RAM.
Power Dissipation					
AVDD, DVDD, PVDD During Operation of ADAU1442			960	mW	All supplies at nominal +10%, IOVDD is not included in measurement.
AVDD, DVDD, PVDD During Operation of ADAU1445			780	mW	All supplies at nominal +10%, IOVDD is not included in measurement.
AVDD, DVDD, PVDD During Operation of ADAU1446			675	mW	All supplies at nominal +10%, IOVDD is not included in measurement.
Reset, All Supplies		94		mW	
ASYNCHRONOUS SAMPLE RATE CONVERTERS[2]					
Dynamic Range		139		dB	A-weighted, 20 Hz to 20 kHz.
I/O Sample Rate	6		192	kHz	
I/O Sample Rate Ratio	1:8		7.75:1		
THD + N		−133	−120	dB	
CRYSTAL OSCILLATOR					
Transconductance		40		mS	
REGULATOR[3]					
DVDD Voltage	1.65	1.75	1.85	V	Maximum 500 mA load.

[1] SPDIFI input voltage range exceeds the requirements of the S/PDIF specification.
[2] To calculate the group delay, refer to the SRC Group Delay section.
[3] Regulator specifications are calculated using an NJT4030P transistor from On Semiconductor in the circuit.

DIGITAL TIMING SPECIFICATIONS

T_A = −40°C to +105°C, DVDD = 1.8 V, IOVDD = 3.3 V.

Table 4.

Parameter[1]	Min	Max	Unit	Description
MASTER CLOCK				
f_{MP}	2.822	24.576	MHz	Master clock (MCLK) frequency. See the Master Clock and PLL section.
t_{MP}	40.69	354.36	ns	Master clock (MCLK) period. See the Master Clock and PLL section.
t_{MD}	25	75	%	Master clock (MCLK) duty cycle.
CLKOUT Jitter		250	ps	Cycle-to-cycle rms average.
CORE CLOCK				
f_{CORE}		172.032	MHz	DSP core clock frequency.
SERIAL PORT				
f_{BCLK}		24.576	MHz	BCLK frequency.
t_{BCLK}	40.69		ns	BCLK period.
t_{BIL}	30		ns	BCLKx low pulse width, slave mode.
t_{BIH}	30		ns	BCLKx high pulse width, slave mode.
t_{LIS}	20		ns	LRCLKx setup to BCLKx input rising edge, slave mode.
t_{LIH}	20		ns	LRCLKx hold from BCLKx input rising edge, slave mode.
t_{SIS}	10		ns	SDATA_INx setup to BCLKx input rising edge.
t_{SIH}	10		ns	SDATA_INx hold from BCLKx input rising edge.
t_{TS}		5	ns	BCLKx output falling edge to LRCLKx output timing skew.
t_{SODS}		30	ns	SDATA_OUTx delay in slave mode from BCLKx output falling edge.
t_{SODM}		30	ns	SDATA_OUTx delay in master mode from BCLKx output falling edge.
SPI PORT				
$f_{CCLK\ write}$		32	MHz	CCLK frequency.[2]
$f_{CCLK\ read}$		16	MHz	CCLK frequency.[2]
t_{CCPL}	20		ns	CCLK pulse width low.
t_{CCPH}	20		ns	CCLK pulse width high.
t_{CLS}	0		ns	CLATCH setup to CCLK rising edge.
t_{CLH}	35		ns	CLATCH hold from CCLK rising edge.
t_{CLPH}	20		ns	CLATCH pulse width high.
t_{CLDLY}	20		ns	Minimum delay between CLATCH low pulses.
t_{CDS}	0		ns	CDATA setup to CCLK rising edge.
t_{CDH}	35		ns	CDATA hold from CCLK rising edge.
t_{COV}		40	ns	COUT valid output delay from CCLK falling edge.
I²C PORT				
f_{SCL}		400	kHz	SCL clock frequency.
t_{SCLH}	0.6		µs	SCL pulse width high.
t_{SCLL}	1.3		µs	SCL pulse width low.
t_{SCS}	0.6		µs	Start and repeated start condition setup time.
t_{SCH}	0.6		µs	Start condition hold time.
t_{DS}	100		ns	Data setup time.
t_{DH}	0.9		µs	Data hold time.
t_{SCLR}		300	ns	SCL rise time.
t_{SCLF}		300	ns	SCL fall time.
t_{SDR}		300	ns	SDA rise time.
t_{SDF}		300	ns	SDA fall time.
t_{BFT}	1.3		µs	Bus-free time between stop and start.
MULTIPURPOSE PINS AND RESET				
f_{MP}		$f_S/2$	Hz	MPx maximum switching rate.
t_{MPIL}		$1.5 \times 1/f_{S,NORMAL}$	µs	MPx pin input latency until high/low value is read by core. Guaranteed by design.
t_{RLPW}	10		ns	$\overline{\text{RESET}}$ low pulse width.

[1] All timing specifications are given for the default (I²S) states of the serial audio input ports and the serial audio output ports (see Table 26 and Table 30).
[2] Maximum SPI CCLK clock frequency is dependent on current drive strength and capacitive loads on the circuit board.

Digital Timing Diagrams

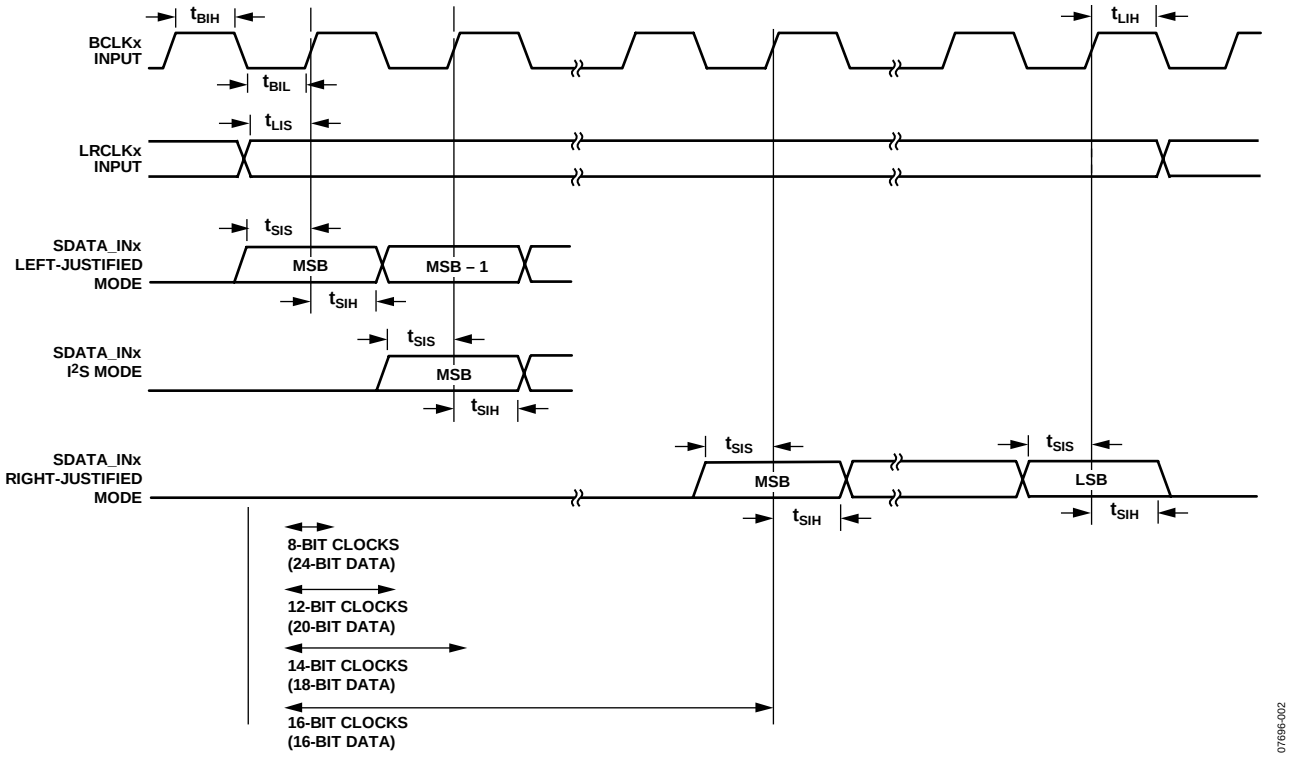


Figure 2. Serial Input Port Timing

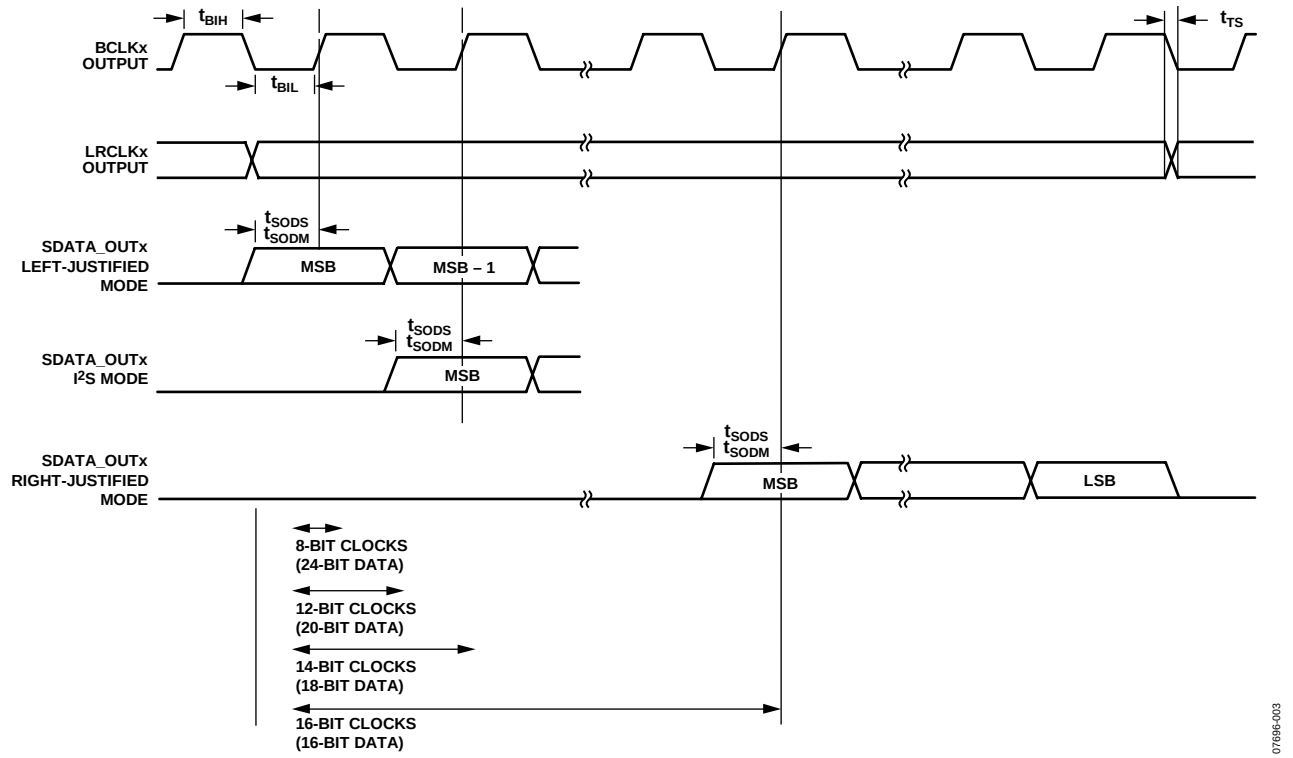


Figure 3. Serial Output Port Timing

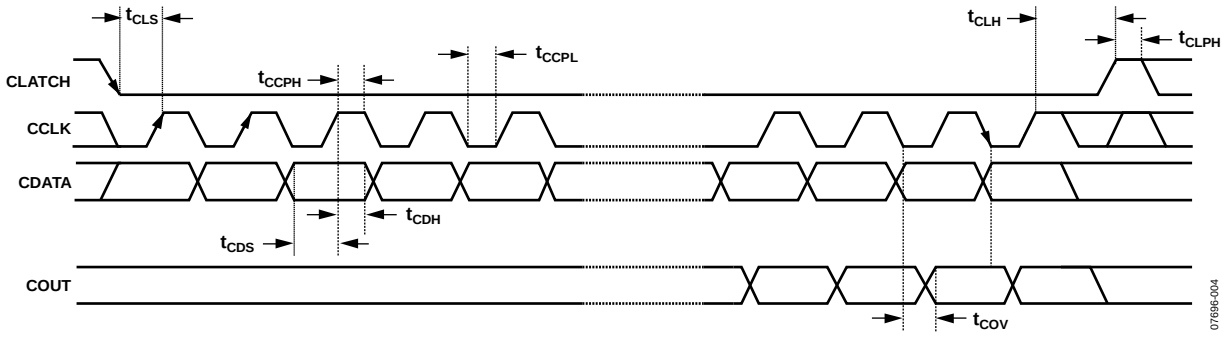


Figure 4. SPI Port Timing

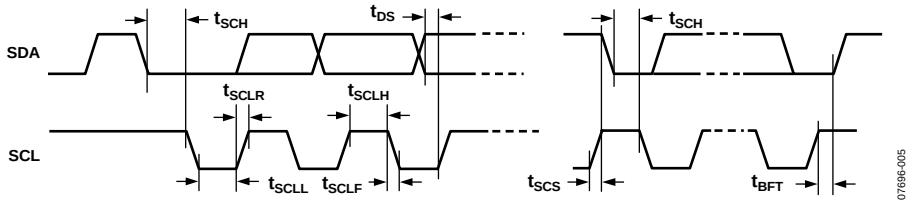


Figure 5. I²C Port Timing

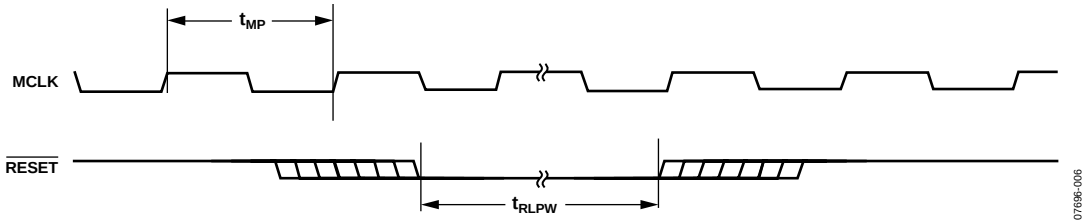


Figure 6. Master Clock and Reset Timing

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
DVDD to Ground	0 V to 2.2 V
AVDD to Ground	0 V to 4.0 V
IOVDD to Ground	0 V to 4.0 V
Digital Inputs	DGND – 0.3 V to IOVDD + 0.3 V
Maximum Ambient Temperature	−40°C to +105°C
Maximum Junction Temperature	150°C
Storage Temperature Range	−65°C to +150°C
Soldering (10 sec)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

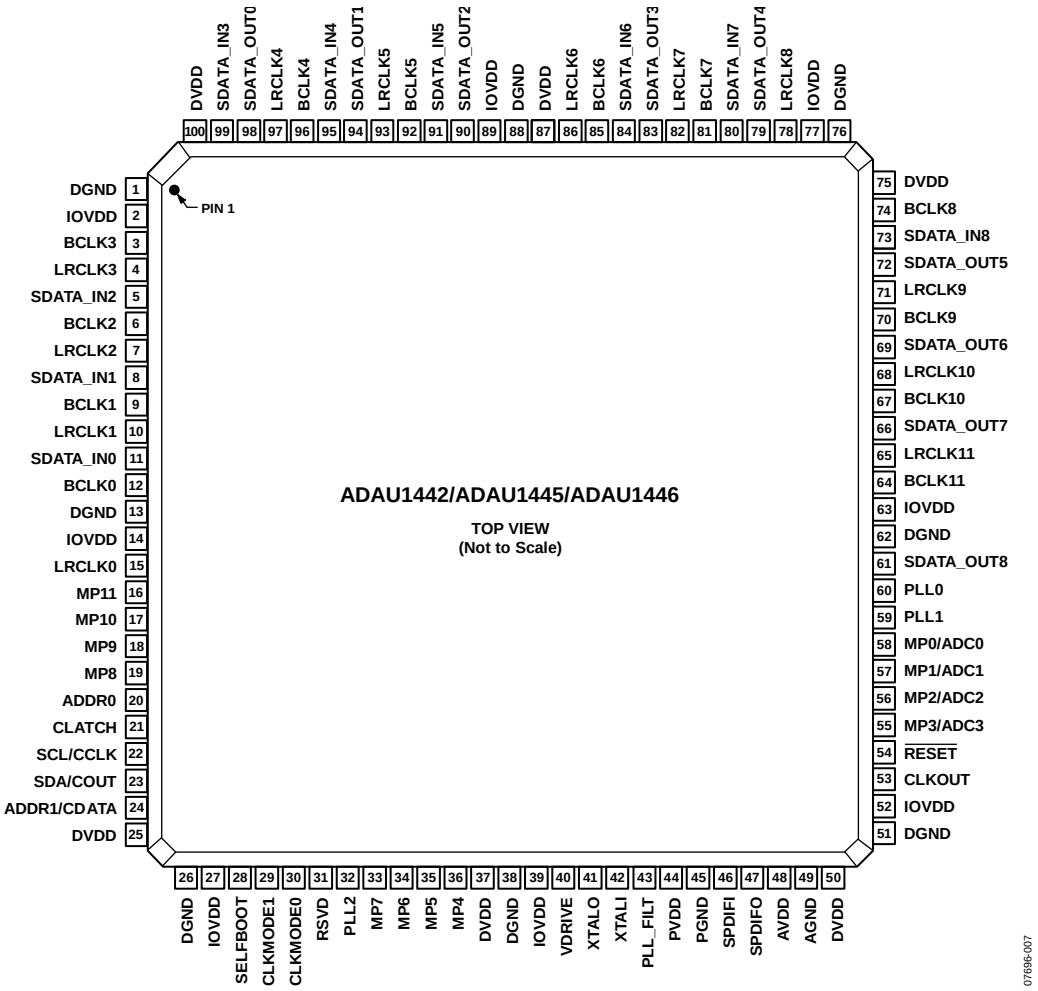
Table 6. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
100-Lead TQFP	26.3	9.4	°C/W
100-Lead LQFP	41.4	9.5	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. THE EXPOSED PAD DOES NOT HAVE AN INTERNAL ELECTRICAL CONNECTION TO THE INTEGRATED CIRCUIT, BUT SHOULD BE CONNECTED TO THE GROUND PLANE OF THE PCB FOR PROPER HEAT DISSIPATION.

Figure 7. Pin Configuration

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
1, 13, 26, 38, 51, 62, 76, 88	DGND	PWR	Digital Ground. The AGND, DGND, and PGND pins should be tied directly together in a common ground plane. DGND pins should be decoupled to a DVDD pin with a 100 nF capacitor.
2, 14, 27, 39, 52, 63, 77, 89	IOVDD	PWR	Input and Output Supply. The voltage on this pin sets the highest input voltage that should be present on the digital input pins. This pin is also the supply for the digital output signals on the clock, data, control port, and MP pins. IOVDD should always be set to 3.3 V. The current draw of this pin is variable because it is dependent on the loads of the digital outputs.
3	BCLK3	D_IO	Bit Clock, Input/Output Clock Domain 3. This pin is bidirectional, with the direction depending on whether the Input/Output Clock Domain 3 is set up as a master or slave. When not used, this pin can be left disconnected.
4	LRCLK3	D_IO	Frame Clock, Input/Output Clock Domain 3. This pin is bidirectional, with the direction depending on whether the Input/Output Clock Domain 3 is set up as a master or slave. When not used, this pin can be left disconnected.
5	SDATA_IN2	D_IN	Serial Data Port 2 Input. When not used, this pin can be left disconnected.

Pin No.	Mnemonic	Type[1]	Description
6	BCLK2	D_IO	Bit Clock, Input Clock Domain 2. This pin is bidirectional, with the direction depending on whether the Input Clock Domain 2 is set up as a master or slave. When not used, this pin can be left disconnected.
7	LRCLK2	D_IO	Frame Clock, Input Clock Domain 2. This pin is bidirectional, with the direction depending on whether the Input Clock Domain 2 is set up as a master or slave. When not used, this pin can be left disconnected.
8	SDATA_IN1	D_IN	Serial Data Port 1 Input. When not used, this pin can be left disconnected.
9	BCLK1	D_IO	Bit Clock, Input Clock Domain 1. This pin is bidirectional, with the direction depending on whether the Input Clock Domain 1 is set up as a master or slave. When not used, this pin can be left disconnected.
10	LRCLK1	D_IO	Frame Clock, Input Clock Domain 1. This pin is bidirectional, with the direction depending on whether the Input Clock Domain 1 is set up as a master or slave. When not used, this pin can be left disconnected.
11	SDATA_IN0	D_IN	Serial Data Port 0 Input. When not used, this pin can be left disconnected.
12	BCLK0	D_IO	Bit Clock, Input Clock Domain 0. This pin is bidirectional, with the direction depending on whether the Input Clock Domain 0 is set up as a master or slave. When not used, this pin can be left disconnected.
15	LRCLK0	D_IO	Frame Clock, Input Clock Domain 0. This pin is bidirectional, with the direction depending on whether the Input Clock Domain 0 is set up as a master or slave. When not used, this pin can be left disconnected.
16	MP11	D_IO	Multipurpose, General-Purpose Input/Output. When not used, this pin can be left disconnected.
17	MP10	D_IO	Multipurpose, General-Purpose Input/Output. When not used, this pin can be left disconnected.
18	MP9	D_IO	Multipurpose, General-Purpose Input/Output. When not used, this pin can be left disconnected.
19	MP8	D_IO	Multipurpose, General-Purpose Input/Output. When not used, this pin can be left disconnected.
20	ADDR0	D_IN	Address 0 for I²C and SPI. In I²C mode, this pin, in combination with ADDR1, allows up to four ADAU1442/ADAU1445/ADAU1446 devices to be used on the same I²C bus. In SPI mode, setting ADDR0 either low or high allows up to two ICs to be used with a common SPI latch signal.
21	CLATCH	D_IN	SPI Latch Signal. Must go low at the beginning of an SPI transaction and high at the end of a transaction. Each SPI transaction may take a different number of CCLK cycles to complete, depending on the address and read/write bits that are sent at the beginning of the SPI transaction. When not used, this pin should be tied to ground, preferably with a 10 kΩ pull-down resistor.
22	SCL/CCLK	D_IN	Serial Clock/Continuous Clock. In I²C mode, this pin functions as SCL and is always an open collector input, except when in self-boot mode, where it is an open collector output (I²C master). The line connected to this pin should have a 2.0 kΩ pull-up resistor. In SPI mode, this pin functions as CCLK and is an input pin that can be either run continuously or gated off between SPI transactions.
23	SDA/COUT	D_IO	Serial Data/Continuous Output. In I²C mode, this pin functions as SDA and is a bidirectional open collector. The line connected to the SDA pin should have a 2.0 kΩ pull-up resistor. In SPI mode, this pin functions as COUT and is used for reading back registers and memory locations. The COUT pin is three-stated when an SPI read is not active.
24	ADDR1/CDATA	D_IN	Address 1/Continuous Data. In I²C mode, this pin functions as ADDR1 and, in combination with ADDR0, sets the I²C address of the IC. This allows up to four ADAU1442/ADAU1445/ADAU1446 devices to be used on the same I²C bus. In SPI mode, this pin functions as CDATA and is the SPI data input.
25, 37, 50, 75, 87, 100	DVDD	PWR	1.8 V Digital Supply. This can be supplied externally or generated from a 3.3 V supply with the on-board 1.8 V regulator. Each DVDD pin should be decoupled to DGND with a 100 nF capacitor.
28	SELFBOOT	D_IN	Self-Boot Select. Allows the ADAU1442/ADAU1445/ADAU1446 to be controlled by the control port or to perform a self-boot. Setting this pin high (that is, to 1) initiates a self-boot operation when the ADAU1442/ADAU1445/ADAU1446 are brought out of a reset. This pin can be tied directly to a voltage source or ground or pulled up/down with a resistor.
29	CLKMODE1	D_IN	Output Clock Mode 1. With CLKMODE0, this pin sets the frequency of the CLKOUT signal.
30	CLKMODE0	D_IN	Output Clock Mode 0. With CLKMODE1, this pin sets the frequency of the CLKOUT signal.
31	RSVD	D_IN	Reserved. Tie this pin to ground, preferably with a 10 kΩ pull-down resistor.
32	PLL2	D_IN	PLL Mode Select Pin 2.
33	MP7	D_IO	Multipurpose, General-Purpose Input/Output. When not used, this pin can be left disconnected.

Pin No.	Mnemonic	Type[1]	Description
34	MP6	D_IO	Multipurpose, General-Purpose Input/Output. When not used, this pin can be left disconnected.
35	MP5	D_IO	Multipurpose, General-Purpose Input/Output. When not used, this pin can be left disconnected.
36	MP4	D_IO	Multipurpose, General-Purpose Input/Output. When not used, this pin can be left disconnected.
40	VDRIVE	A_OUT	Regulator Drive. Supplies the drive current for the 1.8 V regulator. The base of the voltage regulator's external PNP transistor is driven from VDRIVE.
41	XTALO	A_OUT	Crystal Oscillator Output. A 100 Ω damping resistor should be connected between this pin and the crystal. This output should not be used to directly drive a clock to another IC; the CLKOUT pin exists for this purpose. If the crystal oscillator is not used, the XTALO pin can be left unconnected.
42	XTALI	A_IN	Crystal Oscillator Input. This pin provides the master clock for the ADAU1442/ADAU1445/ADAU1446. If the ADAU1442/ADAU1445/ADAU1446 generate the master clock in the system, this pin should be connected to the crystal oscillator circuit. If the ADAU1442/ADAU1445/ADAU1446 are slaves to an external master clock, this pin should be connected to the master clock signal generated by another IC.
43	PLL_FILT	A_OUT	Phase-Locked Loop Filter. Two capacitors and a resistor must be connected to this pin as shown in Figure 11.
44	PVDD	PWR	Phase-Locked Loop Supply. Provides the 3.3 V power supply for the PLL. This should be decoupled to PGND with a100 nF capacitor.
45	PGND	PWR	Phase-Locked Loop Ground. Ground for the PLL supply. The AGND, DGND, and PGND pins can be tied directly together in a common ground plane. PGND should be decoupled to PVDD with a 100 nF capacitor.
46	SPDIFI	D_IN	S/PDIF Input. Accepts digital audio data in the S/PDIF format. When not used, this pin can be left disconnected.
47	SPDIFO	D_OUT	S/PDIF Output. Outputs digital audio data in the S/PDIF format. When not used, this pin can be left disconnected.
48	AVDD	PWR	Analog Supply. 3.3 V analog supply for the auxiliary ADC. This pin should be decoupled to AGND with a 100 nF capacitor.
49	AGND	PWR	Analog Ground. Ground for the analog supply. This pin should be decoupled to AVDD with a 100 nF capacitor.
53	CLKOUT	D_OUT	Master Clock Output. Used to output a master clock to other ICs in the system. Set using the CLKMODEx pins. When not used, this pin can be left disconnected.
54	$\overline{\text{RESET}}$	D_IN	Reset. Active-low reset input. Reset is triggered on a high-to-low edge and exited on a low-to-high edge. For detailed information about initialization, see the Power-Up Sequence section. A reset event sets all RAMs and registers to their default values.
55	MP3/ADC3	D_IO, A_IN	Multipurpose, General-Purpose Input or Output/Auxiliary ADC Input 3. When not used, this pin can be left disconnected.
56	MP2/ADC2	D_IO, A_IN	Multipurpose, General-Purpose Input or Output/Auxiliary ADC Input 2. When not used, this pin can be left disconnected.
57	MP1/ADC1	D_IO, A_IN	Multipurpose, General-Purpose Input or Output/Auxiliary ADC Input 1. When not used, this pin can be left disconnected.
58	MP0/ADC0	D_IO, A_IN	Multipurpose, General-Purpose IO/Auxiliary ADC Input 0. When not used, this pin can be left disconnected.
59	PLL1	D_IN	Phase-Locked Loop Mode Select Pin 1.
60	PLL0	D_IN	Phase-Locked Loop Mode Select Pin 0.
61	SDATA_OUT8	D_OUT	Serial Data Port 0 Output. When not used, this pin can be left disconnected.
64	BCLK11	D_IO	Bit Clock, Output Clock Domain 11. This pin is bidirectional, with the direction depending on whether the Output Clock Domain 11 is set up as a master or slave. When not used, this pin can be left disconnected.
65	LRCLK11	D_IO	Frame Clock, Output Clock Domain 11. This pin is bidirectional, with the direction depending on whether the Output Clock Domain 11 is set up as a master or slave. When not used, this pin can be left disconnected.

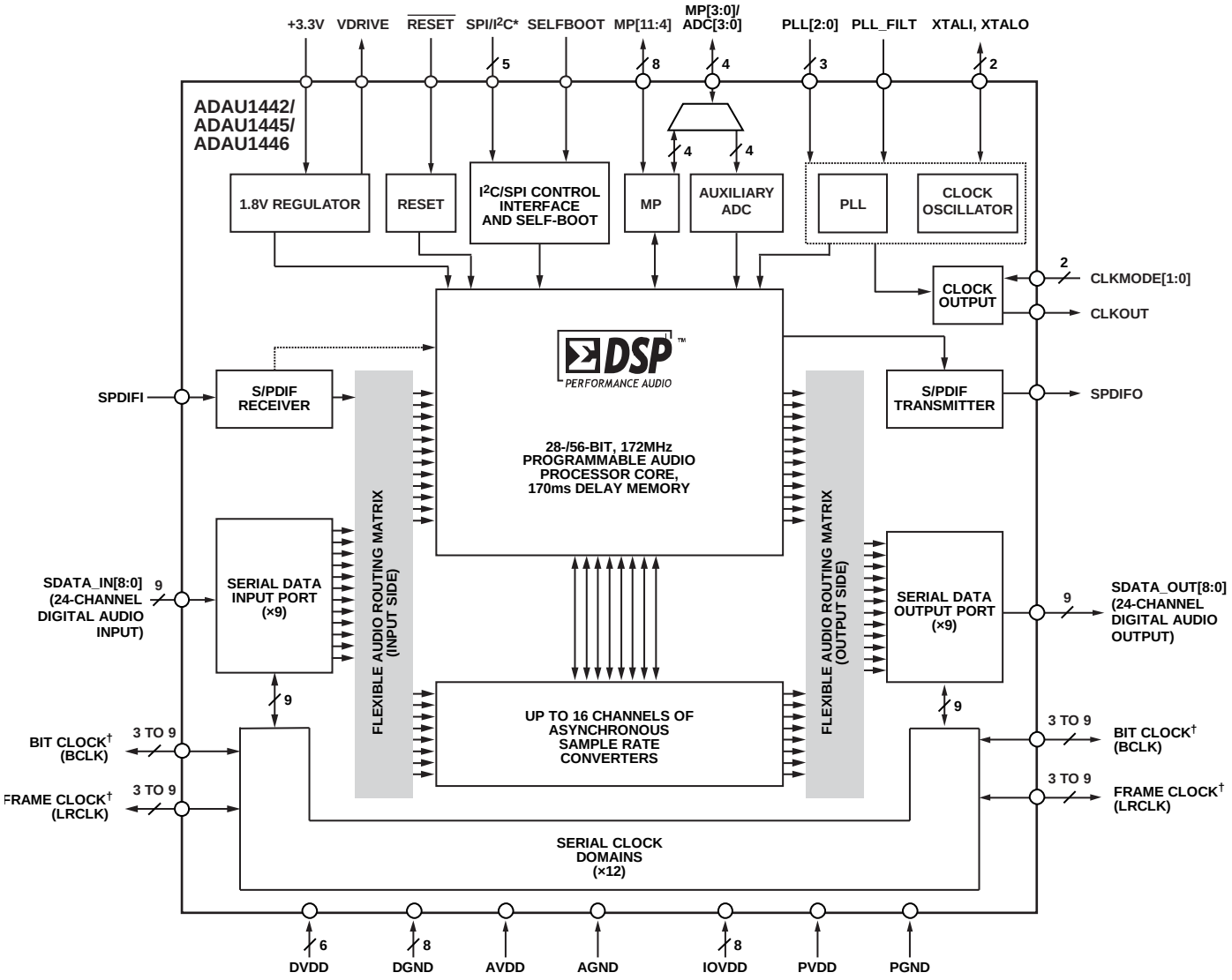
Pin No.	Mnemonic	Type[1]	Description
66	SDATA_OUT7	D_OUT	Serial Data Port 7 Output. When not used, this pin can be left disconnected.
67	BCLK10	D_IO	Bit Clock, Output Clock Domain 10. This pin is bidirectional, with the direction depending on whether the Output Clock Domain 10 is set up as a master or slave. When not used, this pin can be left disconnected.
68	LRCLK10	D_IO	Frame Clock, Output Clock Domain 10. This pin is bidirectional, with the direction depending on whether the Output Clock Domain 10 is set up as a master or slave. When not used, this pin can be left disconnected.
69	SDATA_OUT6	D_OUT	Serial Data Port 6 Output. When not used, this pin can be left disconnected.
70	BCLK9	D_IO	Bit Clock, Output Clock Domain 9. This pin is bidirectional, with the direction depending on whether the Output Clock Domain 9 is set up as a master or slave. When not used, this pin can be left disconnected.
71	LRCLK9	D_IO	Frame Clock, Output Clock Domain 9. This pin is bidirectional, with the direction depending on whether the Output Clock Domain 9 is set up as a master or slave. When not used, this pin can be left disconnected.
72	SDATA_OUT5	D_OUT	Serial Data Port 5 Output. When not used, this pin can be left disconnected.
73	SDATA_IN8	D_IN	Serial Data Port 8 Input. When not used, this pin can be left disconnected.
74	BCLK8	D_IO	Bit Clock, Input/Output Clock Domain 8. This pin is bidirectional, with the direction depending on whether the Input/Output Clock Domain 8 is set up as a master or slave. When not used, this pin can be left disconnected.
78	LRCLK8	D_IO	Frame Clock, Input/Output Clock Domain 8. This pin is bidirectional, with the direction depending on whether the Input/Output Clock Domain 8 is set up as a master or slave. When not used, this pin can be left disconnected.
79	SDATA_OUT4	D_OUT	Serial Data Port 4 Output. When not used, this pin can be left disconnected.
80	SDATA_IN7	D_IN	Serial Data Port 7 Input. When not used, this pin can be left disconnected.
81	BCLK7	D_IO	Bit Clock, Input/Output Clock Domain 7. This pin is bidirectional, with the direction depending on whether the Input/Output Clock Domain 7 is set up as a master or slave. When not used, this pin can be left disconnected.
82	LRCLK7	D_IO	Frame Clock, Input/Output Clock Domain 7. This pin is bidirectional, with the direction depending on whether the Input/Output Clock Domain 7 is set up as a master or slave. When not used, this pin can be left disconnected.
83	SDATA_OUT3	D_OUT	Serial Data Port 3 Output. When not used, this pin can be left disconnected.
84	SDATA_IN6	D_IN	Serial Data Port 6 Input. When not used, this pin can be left disconnected.
85	BCLK6	D_IO	Bit Clock, Input/Output Clock Domain 6. This pin is bidirectional, with the direction depending on whether the Input/Output Clock Domain 6 is set up as a master or slave. When not used, this pin can be left disconnected.
86	LRCLK6	D_IO	Frame Clock, Input/Output Clock Domain 6. This pin is bidirectional, with the direction depending on whether the Input/Output Clock Domain 6 is set up as a master or slave. When not used, this pin can be left disconnected.
90	SDATA_OUT2	D_OUT	Serial Data Port 2 Output. When not used, this pin can be left disconnected.
91	SDATA_IN5	D_IN	Serial Data Port 5 Input. When not used, this pin can be left disconnected.
92	BCLK5	D_IO	Bit Clock, Input/Output Clock Domain 5. This pin is bidirectional, with the direction depending on whether the Input/Output Clock Domain 5 is set up as a master or slave. When not used, this pin can be left disconnected.
93	LRCLK5	D_IO	Frame Clock, Input/Output Clock Domain 5. This pin is bidirectional, with the direction depending on whether the Input/Output Clock Domain 5 is set up as a master or slave. When not used, this pin can be left disconnected.
94	SDATA_OUT1	D_OUT	Serial Data Port 1 Output. When not used, this pin can be left disconnected.
95	SDATA_IN4	D_IN	Serial Data Port 4 Input. When not used, this pin can be left disconnected.

Pin No.	Mnemonic	Type[1]	Description
96	BCLK4	D_IO	Bit Clock, Input/Output Clock Domain 4. This pin is bidirectional, with the direction depending on whether the Input/Output Clock Domain 4 is set up as a master or slave. When not used, this pin can be left disconnected.
97	LRCLK4	D_IO	Frame Clock, Input/Output Clock Domain 4. This pin is bidirectional, with the direction depending on whether the Input/Output Clock Domain 4 is set up as a master or slave. When not used, this pin can be left disconnected.
98	SDATA_OUT0	D_OUT	Serial Data Port 0 Output. When not used, this pin can be left disconnected.
99	SDATA_IN3	D_IN	Serial Data Port 3 Output. When not used, this pin can be left disconnected.

[1] PWR = power/ground, A_IN = analog input, D_IN = digital input, A_OUT = analog output, D_OUT = digital output, D_IO = digital input/output.

THEORY OF OPERATION

SYSTEM BLOCK DIAGRAM



*SPI/I2C = THE ADDR0, CLATCH, SCL/CCLK, SDA/COUT, AND ADDR1/CDATA PINS.
†THERE ARE 12 BIT CLOCKS (BCLK[11:0]) AND 12 FRAME CLOCKS (LRCLK[11:0]) IN TOTAL. OF THE 12 CLOCKS, SIX ARE ASSIGNABLE, THREE MUST BE OUTPUTS, AND THREE MUST BE INPUTS.

07696-008

Figure 8. System Block Diagram

OVERVIEW

The ADAU1442/ADAU1445/ADAU1446 are each a 24-channel audio DSP with an integrated S/PDIF receiver and transmitter, flexible serial audio ports, up to 16 channels of asynchronous sample rate converters (ASRCs), flexible audio routing, and user interface capabilities. Signal processing capabilities include equalization, crossover, bass enhancement, multiband dynamics processing, delay compensation, speaker compensation, and stereo image widening. These algorithms can be used to compensate for the real-world limitations of speakers, amplifiers, and listening environments, resulting in an improvement in the perceived audio quality.

An on-board oscillator can be connected to an external crystal to generate the master clock. A phase-locked loop (PLL) allows the ADAU1442/ADAU1445/ADAU1446 to be clocked from a variety of clock frequencies. The PLL can accept inputs of 64 × f_S, 128 × f_S, 256 × f_S, 384 × f_S, or 512 × f_S to generate the internal master clock of the core, where f_S is the sampling rate of audio in normal-rate processing mode. In dual- or quad-rate mode, these multipliers are halved or quartered, respectively. System sample rates include, but are not limited to, 44.1 kHz, 48 kHz, 88.2 kHz, 96 kHz, and 192 kHz.

Each ADAU1442/ADAU1445/ADAU1446 operates from a 1.8 V digital power supply and a 3.3 V analog supply. An on-board voltage regulator can be used to operate the chip from a single 3.3 V supply.

The ADAU1442/ADAU1445/ADAU1446 have a sophisticated control port that supports complete read and write capability of all memory locations, excluding read-only addresses. Control registers are provided to offer complete control of the chip's configuration and serial modes. Handshaking is included for ease of memory uploads and downloads. The ADAU1442/ADAU1445/ADAU1446 can be configured for either SPI or I²C control. Program RAM, parameter RAM, and register contents can be saved in an external EEPROM, from which the ADAU1442/ADAU1445/ADAU1446 can self-boot on startup.

The ADAU1442/ADAU1445/ADAU1446 serial ports operate with digital audio I/Os in the I²S, left-justified, right-justified, or TDM-compatible mode. The flexible serial data ports allow for direct interconnection to a variety of ADCs, DACs, and general-purpose DSPs. The combination of an on-board S/PDIF transmitter and receiver and 16 channels of ASRCs allows for easy compatibility with an extensive number of external devices, and a system with up to nine sampling rates.

The flexible audio routing matrix (FARM) is a system of multiplexers used to distribute the audio signals in the ADAU1442/ADAU1445/ADAU1446 among the serial inputs and outputs, audio core, and ASRCs. FARM can easily be configured by setting the appropriate registers.

The ADAU1442, ADAU1445, and ADAU1446 are distinguished by the number of on-board ASRCs and maximum sample rates. The ADAU1442 contains eight 2-channel ASRCs, the ADAU1445 contains two 8-channel ASRCs, and the ADAU1446 has no ASRCs.

Two sets of serial ports at the input and output can operate in a special flexible TDM mode, which allows the user to independently assign byte-specific locations to audio streams at varying bit depths. This mode ensures compatibility with codecs using similar flexible TDM streams.

The core of the ADAU1442/ADAU1445/ADAU1446 is a 28-bit DSP (or a 56-bit DSP when using double-precision mode) optimized for audio processing, and it can process audio at sample rates of up to 192 kHz. The program and parameter RAMs can be loaded with a custom audio processing signal flow built with the SigmaStudio graphical programming software from Analog Devices, Inc. The values stored in the parameter RAM control individual signal processing blocks, such as IIR and FIR equalization filters, dynamics processors, audio delays, and mixer levels. A software safeload feature allows for transparent parameter updates and prevents clicks on the output signals.

Reliability features such as a CRC and program counter watchdog help ensure that the system can detect and recover from any errors related to memory corruption.

S/PDIF signals can be routed through an ASRC for processing in the DSP or can be sent directly to output on MP pins for recovery of the embedded audio signal. Other components of the embedded signal, including status and user bits, are not lost and can be output on the MP pins as well.

Multipurpose (MP) pins are available for providing a simple user interface without the need for an external microcontroller. Twelve pins are available to input external control signals and output flags or controls to other devices in the system. Four of these can alternatively be assigned to an auxiliary ADC for use with analog controls such as potentiometers or system voltages. As inputs, MP pins can be connected to push buttons, switches, rotary encoders, potentiometers, or other external control circuitry to control the internal signal processing program. When configured as outputs, these pins can be used to drive LEDs (with a buffer), to output flags to a microcontroller, to control other ICs, or to connect to other external circuitry in an application.

The SigmaStudio software is used to program and control the ADAU1442/ADAU1445/ADAU1446 through the control port. Along with designing and tuning a signal flow, the software can configure all of the DSP registers in real time and download a new program and parameter into the external self-boot EEPROM. SigmaStudio's easy-to-use graphical interface allows anyone with audio processing knowledge to easily design a DSP signal flow and port it to a target application without the need for writing line-level code. At the same time, the software provides enough flexibility and programmability for an experienced DSP programmer to have in-depth control of the design. In SigmaStudio, the user can add signal processing cells from the library by dragging and dropping cells, connect them together in a flow, compile the design, and load the program and parameter files into the ADAU1442/ADAU1445/ADAU1446 memory through the control port. The complicated tasks of linking, compiling, and downloading the project are all handled automatically by the software.

Signal processing algorithms available in the provided libraries include

- Single- and double-precision biquad filter
- Mono and multichannel dynamics processors with peak or rms detection
- Mixer and splitter
- Tone and noise generator
- Fixed and variable gain
- Loudness
- Delay
- Stereo enhancement
- Dynamic bass boost
- Noise and tone source
- Level detector
- MP pin control and conditioning

New processing algorithms are always being developed. Analog Devices also provides proprietary and third-party algorithms for applications such as matrix decoding, bass enhancement, and surround virtualizers. Contact Analog Devices for information about licensing these algorithms.

Several power-saving mechanisms have been designed into the ADAU1442/ADAU1445/ADAU1446, including programmable pad strength for digital I/O pins and the ability to block the master clock from reaching unused subsystems.

The ADAU1442/ADAU1445/ADAU1446 are fabricated on a single monolithic integrated circuit for operation over the −40°C to +105°C temperature range. The ADAU1442 and ADAU1445 are housed in a 100-lead TQFP package, with an exposed pad to assist in heat dissipation, and the ADAU1446, due to its lower power consumption, is housed in a 100-lead LQFP package.

INITIALIZATION

Power-Up Sequence

The ADAU1442/ADAU1445/ADAU1446 have a built-in initialization period, which allows sufficient time for the PLL to lock and the registers to initialize their values. On a positive edge of $\overline{\text{RESET}}$, the PLL settings are immediately set by the PLL0, PLL1, and PLL2 pins, and the master clock signal is blocked from the chip subsystems. The initialization time, which is measured from the rising edge of $\overline{\text{RESET}}$, is dependent on the frequency of the signal input to the XTALI pin, or f_{XTALI}. The total initialization time is

$$1/(f_{XTALI}/D) \times 2^{15} \text{ sec}$$

where D is the PLL divider, as set by the PLL0, PLL1, and PLL2 pins. The PLL divider settings are described in Table 9.

For example, if the signal input to XTALI has a frequency of 12.288 MHz and the PLL divider is set to 4 (PLL = 0, PLL1 = 1, and PLL2 = 0), the initialization time lasts

$$1/(12288000/4) \times 2^{15} \text{ sec} = 0.010667 \text{ sec (or 10.667 ms)}$$

New values should not be written via the control port until the initialization is complete.

Table 8 shows some typical times to boot the ADAU1442/ADAU1445/ADAU1446 into the operational state necessary for an application, assuming that a 400 kHz I²C clock or a 5 MHz SPI clock is used and a full program, parameter set, and all registers (9 kB) are loaded. In reality, most applications use less than this full amount, and unused program and parameter RAM need not be initialized; therefore, the total boot time may be shorter.

Recommended Program/Parameter Loading Procedure

When writing large amounts of data to the program or parameter RAM in direct write mode, such as when downloading the initial contents of the RAMs from an external memory, the processor core should be disabled to prevent unpleasant noises from appearing at the audio output. When small amounts of data are transmitted during real-time operation of the DSP, such as when updating individual parameters, the software safeload mechanism can be used. More information is available in the Software Safeload section.

Power-Reduction Modes

Sections of the ADAU1442/ADAU1445/ADAU1446 chips can be turned on and off as needed to reduce power consumption. These include the ASRCs, S/PDIF receiver and transmitter, auxiliary ADCs, and DSP core. More information is available in the Master Clock and PLL Modes and Settings section.

System Initialization Sequence

Before the IC can process audio in the DSP, the following initialization sequence must be completed. (Step 5 through Step 11 can be performed in any order, as needed.)

1. Power on the IC and bring it out of reset. The order of the power supplies (DVDD, IOVDD, and AVDD) does not matter.
2. Wait at least 10.667 ms for the initialization to complete if the XTALI input is 12.288 MHz and the PLL divider is set to 4 (see the Power-Up Sequence section for information about calculating the initialization time if another f_{XTALI} is used).
3. Enable the master clocks of all modules to be used (see the Master Clock and PLL Modes and Settings section).
4. Set the DSP core rate select register (0xE220) to 0x001C. This disables the start pulse to the core.
5. Deassert the core run bit (see the DSP Core Modes and Settings section).
6. Set the serial input modes (see the Serial Input Port Modes Registers (Address 0xE000 to Address 0xE008) section).
7. Set the serial output modes (see the Serial Output Port Modes Registers (Address 0xE040 to Address 0xE049) section).
8. Set the routing matrix modes (see details of Address 0xE080 to Address 0xE09B in the Flexible Audio Routing Matrix Modes section).
9. Write the parameter RAM (Address 0x0000 to Address 0x0FFF).
10. Write the program RAM (Address 0x2000 to Address 0x2FFF).
11. Write the nonmodulo data RAM (Addresses vary based on the SigmaStudio project file).
12. Write all other necessary control registers, such as ASRCs and S/PDIF (Address 0xE221 to Address 0xE24C).
13. Set the DSP core rate select register (0xE220) to the desired value. This enables the start pulse to the core. Table 12 contains a list of valid settings.
14. Assert the core run bit (see the DSP Core Modes and Settings section).

Table 8. Power-Up Time

PLL Lock Time (ms) (f_{XTALI} = 12.288 MHz, PLL Divider = 4)	Approximate Boot Time; Loading Maximum Program/Parameter/Registers (ms)			
	I²C (at 400 kHz SCL)	SPI (at 5 MHz CCLK)	SPI (at 25 MHz CCLK)	Total (ms)
10.667	25	2	0.4	11.067 to 35.667

MASTER CLOCK AND PLL

Using the Oscillator

The ADAU1442/ADAU1445/ADAU1446 can use an on-board oscillator to generate its master clock. However, an external crystal must be attached to complete the oscillator circuit. The on-board oscillator is designed to work with a 256 × $f_{S,NORMAL}$ master clock, which is 12.288 MHz when $f_{S,NORMAL}$ is 48 kHz and 11.2896 MHz when $f_{S,NORMAL}$ is 44.1 kHz. The resonant frequency of this crystal should be in this range even when the core is processing dual- or quad-rate signals. When the core is processing dual-rate signals (for example, $f_{S,DUAL}$ = 88.2 kHz or 96 kHz), resonant frequency of the crystal should be 128 × $f_{S,DUAL}$. When the core is processing quad-rate signals (for example, $f_{S,QUAD}$ = 192 kHz), the resonant frequency of the crystal should be 64 × $f_{S,QUAD}$.

The external crystal in the circuit should be an AT-cut parallel resonance device operating at its fundamental frequency. Ceramic resonators should not be used. Figure 9 shows the crystal oscillator circuit recommended for proper operation.

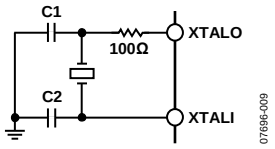


Figure 9. Crystal Oscillator Circuit

The 100 Ω damping resistor on XTALO provides the oscillator with a voltage swing of approximately 2.2 V at the XTALI pin. The crystal shunt capacitance should be 7 pF. Its optimal load capacitance, specified by the manufacturer, should be about 18 pF, although the circuit supports values up to 25 pF. The equivalent series resistance should also be as small as possible. The necessary values of Load Capacitor C1 and Load Capacitor C2 can be calculated from the crystal load capacitance with the following equation:

$$C_L = \frac{C_1 \times C_2}{C_1 + C_2} + C_{STRAY}$$

where C_{STRAY} is the stray capacitance in the circuit and is usually assumed to be approximately 2 pF to 5 pF.

Short trace lengths in the oscillator circuit decrease stray capacitance, thereby increasing the loop gain of the circuit and helping to avoid crystal start-up problems.

On the ADAU1442/ADAU1445/ADAU1446 evaluation boards, the capacitance value for C1 and C2 is 22 pF.

XTALO should not be used to directly drive the crystal signal to another IC. This signal is an analog sine wave and is not appropriate to drive a digital input. A separate pin, CLKOUT, is provided for this purpose. CLKOUT can output 256 × $f_{S,NORMAL}$, 512 × $f_{S,NORMAL}$, or a buffered, digital copy of the crystal oscillator signal to other ICs in the system. CLKOUT is set up using the CLKMODEx pins. For a more detailed explanation of CLKOUT, refer to the Using the ADAU1442/ADAU1445/ADAU1446 as Clock Master section.

Setting Master Clock and PLL Mode

The ADAU1442/ADAU1445/ADAU1446 master clock input feeds a PLL, which generates the 3584 × $f_{S,NORMAL}$ clock (172.032 MHz when $f_{S,NORMAL}$ is 48 kHz) to run the DSP core. This rate is referred to as f_{CORE}. In normal operation, the input to the master clock must be one of the following: 64 × $f_{S,NORMAL}$, 128 × $f_{S,NORMAL}$, 256 × $f_{S,NORMAL}$, 384 × $f_{S,NORMAL}$, or 512 × $f_{S,NORMAL}$, where $f_{S,NORMAL}$ is the audio sampling rate with the core in normal-rate processing mode. The PLL divider mode is set by PLL0, PLL1, and PLL2 as detailed in Table 9.

If the ADAU1442/ADAU1445/ADAU1446 cores are set to receive dual-rate signals (by reducing the number of program steps per sample by a factor of 2 using the DSP core rate select register), then the master clock frequency must be 32 × $f_{S,DUAL}$, 64 × $f_{S,DUAL}$, 128 × $f_{S,DUAL}$, 192 × $f_{S,DUAL}$, or 256 × $f_{S,DUAL}$.

If the ADAU1442/ADAU1445/ADAU1446 cores are set to receive quad-rate signals (by reducing the number of program steps per sample by a factor of 4 using the DSP core rate select register), then the master clock frequency must be 16 × $f_{S,QUAD}$, 32 × $f_{S,QUAD}$, 64 × $f_{S,QUAD}$, 96 × $f_{S,QUAD}$, or 128 × $f_{S,QUAD}$. On power-up, a clock signal must be present on XTALI so that the ADAU1442/ADAU1445/ADAU1446 can complete its initialization routine.

If at any point during operation the clock signal is removed from XTALI, the DSP should be reset to avoid unpredictable behavior on output pins. The clock mode should not be changed without also resetting the ADAU1442/ADAU1445/ADAU1446. If the mode is changed during operation, a click or pop can result on the outputs. The state of the PLLx pins should be changed while $\overline{\text{RESET}}$ is held low.

The phase-locked loop uses the PLL mode select pins (PLL0, PLL1, and PLL2) to derive a 64 × $f_{S,NORMAL}$ clock from whatever signal is present at the XTALI pin. This clock signal is multiplied by 56 to produce the core clock. Therefore, f_{CORE} is 3584 × $f_{S,NORMAL}$. In a system with a $f_{S,NORMAL}$ of 48 kHz, the PLL derives a 3.072 MHz clock and then multiplies it by 56 to produce a 172.032 MHz core clock.

The core clock (f_{CORE}) should never exceed 172.032 MHz, though it may be lower in some applications.

Table 9. PLL Modes

DSP Core Rate[1]	Input to MCLK (XTALI Pin)	PLL2	PLL1	PLL0	PLL Divider[2]	Core Clock Multiplier	Core Clock (f_{CORE})	Instructions per Sample
Normal	64 × $f_{S,NORMAL}$	0	0	0	1	56	3584 × $f_{S,NORMAL}$	3584
	128 × $f_{S,NORMAL}$	0	0	1	2	56	3584 × $f_{S,NORMAL}$	3584
	256 × $f_{S,NORMAL}$	0	1	0	4	56	3584 × $f_{S,NORMAL}$	3584
	384 × $f_{S,NORMAL}$	0	1	1	6	56	3584 × $f_{S,NORMAL}$	3584
	512 × $f_{S,NORMAL}$	1	0	0	8	56	3584 × $f_{S,NORMAL}$	3584
Dual	32 × $f_{S,DUAL}$	0	0	0	1	56	1792 × $f_{S,DUAL}$	1792
	64 × $f_{S,DUAL}$	0	0	1	2	56	1792 × $f_{S,DUAL}$	1792
	128 × $f_{S,DUAL}$	0	1	0	4	56	1792 × $f_{S,DUAL}$	1792
	192 × $f_{S,DUAL}$	0	1	1	6	56	1792 × $f_{S,DUAL}$	1792
	256 × $f_{S,DUAL}$	1	0	0	8	56	1792 × $f_{S,DUAL}$	1792
Quad	16 × $f_{S,QUAD}$	0	0	0	1	56	896 × $f_{S,QUAD}$	896
	32 × $f_{S,QUAD}$	0	0	1	2	56	896 × $f_{S,QUAD}$	896
	64 × $f_{S,QUAD}$	0	1	0	4	56	896 × $f_{S,QUAD}$	896
	96 × $f_{S,QUAD}$	0	1	1	6	56	896 × $f_{S,QUAD}$	896
	128 × $f_{S,QUAD}$	1	0	0	8	56	896 × $f_{S,QUAD}$	896

[1] If the normal DSP core rate ($f_{S,NORMAL}$) is 44.1 kHz, the dual DSP core rate ($f_{S,DUAL}$) is 88.2 kHz, and the quad DSP core rate ($f_{S,QUAD}$) is 176.4 kHz. Likewise, if $f_{S,NORMAL}$ is 48 kHz, then $f_{S,DUAL}$ is 96 kHz and $f_{S,QUAD}$ is 192 kHz.
[2] The PLL divider is set by the PLLx pins.

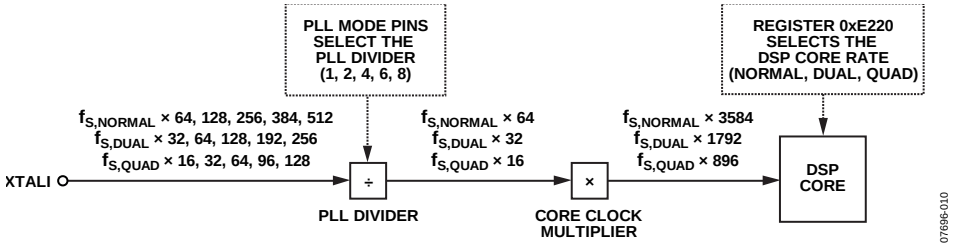


Figure 10. Master Clock Signal Flow

PLL Loop Filter

The PLL loop filter should be connected to the PLL_FILT pin. This filter, shown in Figure 11, includes three passive components—two capacitors and a resistor. The values of these components do not need to be exact; the tolerance can be up to 10% for the resistor and up to 20% for each capacitor. The 3.3 V signal shown in the schematic can be connected to the PVDD supply of the chip.

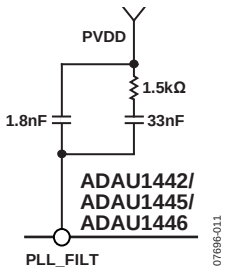


Figure 11. PLL Loop Filter

Using the ADAU1442/ADAU1445/ADAU1446 as Clock Masters

To output a master clock from the ADAU1442/ADAU1445/ADAU1446 to other chips in the system, the CLKOUT pin is used. To set the frequency of this clock signal, the CLKMODEx pins must be set (see Table 10).

Table 10. CLKOUT Modes

CLKOUT Signal	CLKMODE1	CLKMODE0
Disabled	0	0
Buffered Oscillator	0	1
256 × $f_{S,NORMAL}$	1	0
512 × $f_{S,NORMAL}$	1	1

Master Clock and PLL Modes and Settings

DSP Core Rate Select Register (Address 0xE220)

The core's start pulse initiates the operation of the core and determines the sample rate of signals processed inside the core. This pulse can originate from one of three internally generated f_S signals ($f_{S,NORMAL}$, $f_{S,DUAL}$, or $f_{S,QUAD}$), one of the 12 serial input f_S signals (an LRCLK signal associated with a serial input port), one of the 12 serial output f_S signals (an LRCLK signal associated with a serial output port), or LRCLK recovered from the S/PDIF receiver input.

Setting the value of the DSP core rate select register sets the speed of the DSP core (see Table 12). By default, the signals processed in the core are at the normal DSP core rate; therefore, the core clock is 3584 × $f_{S,NORMAL}$. For a system processing signals in the core at the dual rate, the start pulse should be set to the internally generated dual rate, and the core clock is 1792 × $f_{S,DUAL}$. For a system processing signals in the core at the quad rate, the start pulse should be set to the internally generated quad rate, and the core clock is 896 × $f_{S,QUAD}$.

Master Clock Enable Switch Register (Address 0xE280)

For power-saving purposes, various parts of the chip can be switched on and off. Setting the appropriate bit to 0 disables the corresponding subsystem, and setting the bit to 1 enables the subsystem. This is the first register that should be set after the device is powered on and completes its initialization. Failure to set this register may compromise future register writes.

Table 11. Bit Descriptions of Register 0xE280

Bit Position	Description[1]	Default
[15:9]	Reserved	
8	Enable MCLK to auxiliary ADCs	0
7	Enable MCLK to S/PDIF transmitter	0
6	Enable MCLK to S/PDIF receiver	0
5	Enable MCLK to DSP core	0
4	Enable MCLK to Stereo ASRC[7:4][2]	0
3	Enable MCLK to Stereo ASRC[3:0][2]	0
2	Enable MCLK to serial outputs	0
1	Enable MCLK to serial inputs	0
0	Enable MCLK to flexible audio routing matrix (FARM)	0

[1] 0 = disable, 1 = enable.
[2] See the Flexible Audio Routing Matrix—Input Side section for more information.

Table 12. Bit Descriptions of Register 0xE220

Bit Position	Description	Default
[15:5]	Reserved	
[4:0]	Start pulse select 00000 = internally generated normal rate ($f_{S,NORMAL}$) 00001 = internally generated dual rate ($f_{S,DUAL}$) 00010 = internally generated quad rate ($f_{S,QUAD}$) 00011 = f_S from serial input Stereo Pair 0[1] 00100 = f_S from serial input Stereo Pair 1[1] 00101 = f_S from serial input Stereo Pair 2[1] 00110 = f_S from serial input Stereo Pair 3[1] 00111 = f_S from serial input Stereo Pair 4[1] 01000 = f_S from serial input Stereo Pair 5[1] 01001 = f_S from serial input Stereo Pair 6[1] 01010 = f_S from serial input Stereo Pair 7[1] 01011 = f_S from serial input Stereo Pair 8[1] 01100 = f_S from serial input Stereo Pair 9[1] 01101 = f_S from serial input Stereo Pair 10[1] 01110 = f_S from serial input Stereo Pair 11[1] 01111 = f_S from serial output Stereo Pair 0[1] 10000 = f_S from serial output Stereo Pair 1[1] 10001 = f_S from serial output Stereo Pair 2[1] 10010 = f_S from serial output Stereo Pair 3[1] 10011 = f_S from serial output Stereo Pair 4[1] 10100 = f_S from serial output Stereo Pair 5[1] 10101 = f_S from serial output Stereo Pair 6[1] 10110 = f_S from serial output Stereo Pair 7[1] 10111 = f_S from serial output Stereo Pair 8[1] 11000 = f_S from serial output Stereo Pair 9[1] 11001 = f_S from serial output Stereo Pair 10[1] 11010 = f_S from serial output Stereo Pair 11[1] 11011 = f_S from S/PDIF receiver[1] 11100 = no start pulse; core is disabled 11101 = no start pulse; core is disabled 11110 = no start pulse; core is disabled 11111 = no start pulse; core is disabled	00000

[1] f_S is the LRCLK of the associated stereo audio pair in the flexible audio routing matrix whose frequency is dependent on the settings of its associated serial port and the clock pad multiplexer. The intended function of the DSP core rate select register is to allow the DSP core to be synchronized to an external LRCLK signal that is being used by any of the serial ports or S/PDIF receiver.

VOLTAGE REGULATOR

The digital supply voltage of the ADAU1442/ADAU1445/ADAU1446 must be set to 1.8 V. The chip includes an on-board voltage regulator that allows the device to be used in systems where a 1.8 V supply is not available but a 3.3 V supply is. The only external components needed for this are a PNP transistor and one resistor. Only one pin, VDRIVE, is necessary to support the regulator.

The recommended design for the voltage regulator is shown in Figure 12. The 10 µF and 100 nF capacitors shown in this schematic are recommended for bypassing but are not necessary for operation. Each DVDD pin should have its own 100 nF bypass capacitor, but only one bulk capacitor (10 µF) is needed for all pins. In this design, 3.3 V is the main system voltage; 1.8 V is generated at the collector of the transistor, which is connected to the DVDD pins. VDRIVE is connected to the base of the PNP transistor. If the regulator is not used in the design, VDRIVE can be tied to ground.

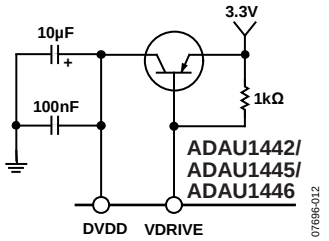


Figure 12. Voltage Regulator Design

Two specifications must be considered when choosing a regulator transistor: the current amplification factor (h_{FE} or beta) should be at least 200, and the collector must be able to dissipate the heat generated when regulating from 3.3 V to 1.8 V. The maximum digital current draw of the ADAU1442 and ADAU1445, which use ASRCs, is 310 mA. The equation to determine the minimum power dissipation specifications of the transistor is as follows:

$$(3.3\text{ V} - 1.8\text{ V}) \times 310\text{ mA} = 465\text{ mW}$$

Many transistors fit these specifications. Analog Devices recommends the NJT4030P from On Semiconductor. For projects with stringent size constraints, an FMMT734 from Zetex can be used.

The ADAU1446, which does not contain ASRCs, has a lower maximum digital current draw of approximately 235 mA. The maximum power dissipation of the transistor in this case should be around 355 mW.

SRC GROUP DELAY

The group delay of the sample rate converter is dependent on the input and output sampling frequencies as described in the following equations.

For $f_{S\_OUT} > f_{S\_IN}$,

$$GDS = \frac{16}{f_{S\_IN}} + \frac{32}{f_{S\_IN}}$$

For $f_{S\_OUT} < f_{S\_IN}$,

$$GDS = \frac{16}{f_{S\_IN}} + \left(\frac{32}{f_{S\_IN}}\right) \times \left(\frac{f_{S\_IN}}{f_{S\_OUT}}\right)$$

where *GDS* is the group delay in seconds.

CONTROL PORT

Overview

The ADAU1442/ADAU1445/ADAU1446 can operate in one of three control modes: I²C control mode, SPI control mode, or self-boot mode (no external controller).

The ADAU1442/ADAU1445/ADAU1446 have both a 4-wire SPI control port and a 2-wire I²C bus control port. Each can be used to set the RAMs and registers. When the SELFBOOT pin is low at power-up, the chip defaults to I²C mode but can be put into SPI control mode by pulling Pin CLATCH low three times. When the SELFBOOT pin is set high at power-up, the ADAU1442/ADAU1445/ADAU1446 load the program, parameters, and register settings from an external EEPROM at startup.

The control port is capable of full read and write operations for all memories and registers, except for those that are read only. Most signal processing parameters are controlled by writing new values to the parameter RAM using the control port. Other functions, such as mute and input/output mode control, are programmed by writing to the registers.

All addresses can be accessed in either a single-word mode or a burst mode. A control word consists of the chip address, the register/RAM subaddress, and the data to be written. The number of bytes per word depends on the type of data that is being written.

The first byte (Byte 0) of a control word contains the 7-bit chip address plus the R/$\overline{W}$ bit. The next two bytes (Byte 1 and Byte 2) together form the subaddress of the memory or register location within the ADAU1442/ADAU1445/ADAU1446. This subaddress must be two bytes because the memory locations within the ADAU1442/ADAU1445/ADAU1446 are directly addressable, and their sizes exceed the range of single-byte addressing. All subsequent bytes (starting with Byte 3) contain the data, such as control port data, program data, or parameter data. The exact formats for specific types of writes are shown in Figure 13 and Figure 19.

The ADAU1442/ADAU1445/ADAU1446 have several mechanisms for updating signal processing parameters in real time without causing pops or clicks in the output. In cases where large blocks of data must be downloaded, the output of the DSP core can be halted, new data can be loaded, and then the output of the DSP core can be restarted. This is typically done during the booting sequence at startup or when loading a new program into RAM. In cases where only a few parameters must be changed, they can be loaded without halting the program. A software-based safeload mechanism is included for this purpose, and it can be used to buffer a full set of parameters (for example, the five coefficients of a biquad) and then transfer these parameters into the active program within one audio frame.

The control port pins are multifunctional according to the mode in which the part is operating. Table 16 details these functions.

I²C Port

The ADAU1442/ADAU1445/ADAU1446 support a 2-wire serial (I²C-compatible) microprocessor bus driving multiple peripherals. Two pins, serial data (SDA) and serial clock (SCL), carry information between the ADAU1442/ADAU1445/ADAU1446 and the system I²C master controller. In I²C mode, the ADAU1442/ADAU1445/ADAU1446 are always slaves on the bus, which means that the parts cannot initiate a data transfer.

Each slave device is recognized by a unique address. The address bit sequence is shown in Table 13. The ADAU1442/ADAU1445/ADAU1446 have eight possible slave addresses: four for writing operations and four for reading. These are unique addresses for the device and are listed in Table 14.

Users can communicate with these addresses by using the USBi communication channel list in the hardware configuration tab of SigmaStudio. The LSB of the byte sets either a read or write operation; Logic Level 1 corresponds to a read operation, and Logic Level 0 corresponds to a write operation. Address Bit 5 and Address Bit 6 are set by tying the ADDRx pins of the ADAU1442/ADAU1445/ADAU1446 to Logic Level 0 or Logic Level 1. Both SDA and SCL should have pull-up resistors on the lines connected to them (a standard value is 2.0 kΩ, but this can be changed depending on the capacitive load on the line). The voltage on these signal lines should not be greater than the voltage of IOVDD (3.3 V).

Table 13. ADAU1442/ADAU1445/ADAU1446 Address Bit Sequence

Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
0	1	1	1	0	ADDR1	ADDR0	R/$\overline{W}$

Table 14. ADAU1442/ADAU1445/ADAU1446 I²C Slave Addresses

ADDR1	ADDR0	Read/Write[1]	Slave Address
0	0	0	0x70
0	0	1	0x71
0	1	0	0x72
0	1	1	0x73
1	0	0	0x74
1	0	1	0x75
1	1	0	0x76
1	1	1	0x77

[1] 0 = write, 1 = read.

Addressing

Initially, all devices on the I²C bus are in an idle state, in which the devices monitor the SDA and SCL lines for a start condition and the proper address. The I²C master initiates a data transfer by establishing a start condition, defined by a high-to-low transition on SDA while SCL remains high. This indicates that an address or an address and data stream follow. All devices on the bus respond to the start condition and shift the next eight bits (7-bit address + R/$\overline{W}$ bit) MSB first. The device that recognizes the transmitted

address responds by pulling the data line low during the ninth clock pulse. This ninth bit is known as an acknowledge bit. All other devices withdraw from the bus at this point and return to the idle condition. The R/$\overline{W}$ bit determines the direction of the data. A Logic 0 on the LSB of the first byte means that the master writes information to the peripheral. A Logic 1 on the LSB of the first byte means that the master reads information from the peripheral. A data transfer takes place until a stop condition is encountered. A stop condition occurs when SDA transitions from low to high while SCL is held high. Figure 13 shows the timing of an I²C write.

Burst mode addressing, where the subaddresses are automatically incremented at word boundaries, can be used for writing large amounts of data to contiguous memory locations. This increment happens automatically, unless a stop condition is encountered after a single-word write. The registers and RAMs in the ADAU1445/ADAU1446 range in width from one to five bytes; therefore, the auto-increment feature knows the mapping between subaddresses and the word length of the destination register (or memory location). A data transfer is always terminated by a stop condition.

Stop and start conditions can be detected at any stage during the data transfer. If these conditions are asserted out of sequence with normal read and write operations, they cause an immediate jump to the idle condition. During a given SCL high period, the user should only issue one start condition, one stop condition, or a single stop condition followed by a single start condition. If an invalid subaddress is issued by the user, the ADAU1442/ADAU1445/ADAU1446 do not issue an acknowledge and return to the idle condition. If the user exceeds the highest subaddress while in auto-increment mode, one of two actions is taken. In read mode, the ADAU1442/ADAU1445/ADAU1446 output the highest subaddress register contents until the master device issues a no acknowledge, indicating the end of a read. A no-acknowledge condition is where the SDA line is not pulled low on the ninth clock pulse on SCL. If the highest subaddress location is reached while in write mode, the data for the invalid byte is not loaded into any subaddress register, a no acknowledge is issued by the ADAU1442/ADAU1445/ADAU1446, and the part returns to the idle condition.

I²C Read and Write Operations

Figure 15 shows the sequence of a single-word write operation. Every ninth clock, the ADAU1442/ADAU1445/ADAU1446 issue an acknowledge by pulling SDA low.

Figure 16 shows the sequence of a burst mode write operation. This figure shows an example in which the target destination registers are two bytes. The ADAU1442/ADAU1445/ADAU1446 know to increment the subaddress register every two bytes because the requested subaddress corresponds to a register or memory area with a 2-byte word length.

The sequence of a single-word read operation is shown in Figure 17. Note that, even though this is a read operation, the first R/$\overline{W}$ bit is a 0, indicating a write operation. This is because the subaddress must be written to set up the internal address. After the ADAU1442/ADAU1445/ADAU1446 acknowledge the receipt of the subaddress, the master must issue a repeated start command followed by the chip address byte with the R/$\overline{W}$ set to 1, indicating a read operation. This causes the SDA pin of the ADAU1442/ADAU1445/ADAU1446 to switch directions and begin driving data back to the master. The master then responds every ninth pulse with an acknowledge pulse to the ADAU1442/ADAU1445/ADAU1446.

Figure 18 shows the sequence of a burst mode read operation. This figure shows an example in which the target read registers are two bytes. The ADAU1442/ADAU1445/ADAU1446 increment the subaddress every two bytes because the requested subaddress corresponds to a register or memory area with word lengths of two bytes. Other address ranges can have a variety of word lengths, ranging from one to five bytes; the ADAU1442/ADAU1445/ADAU1446 always decode the subaddress and set the auto-increment circuit so that the address increments after the appropriate number of bytes.

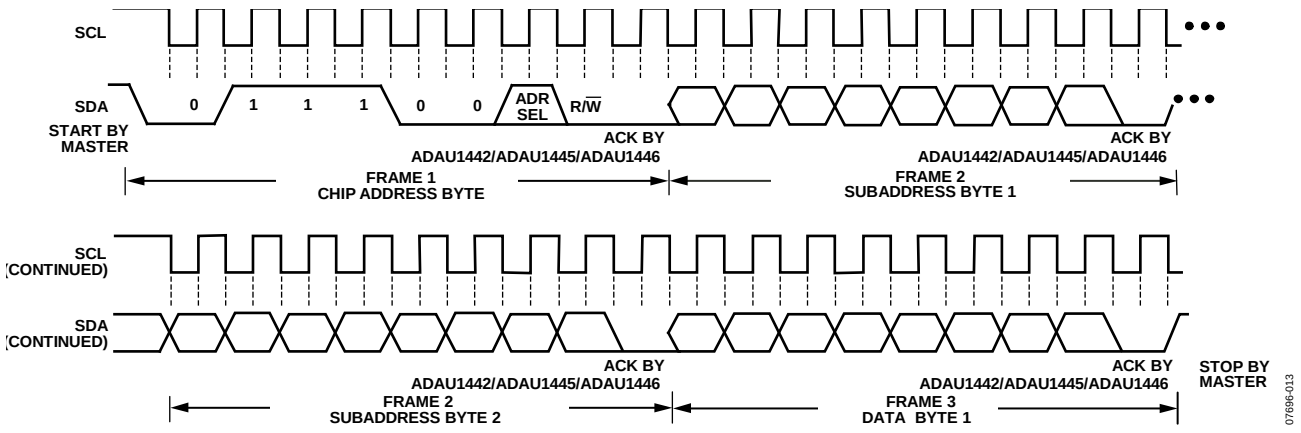


Figure 13. I²C Write Clocking

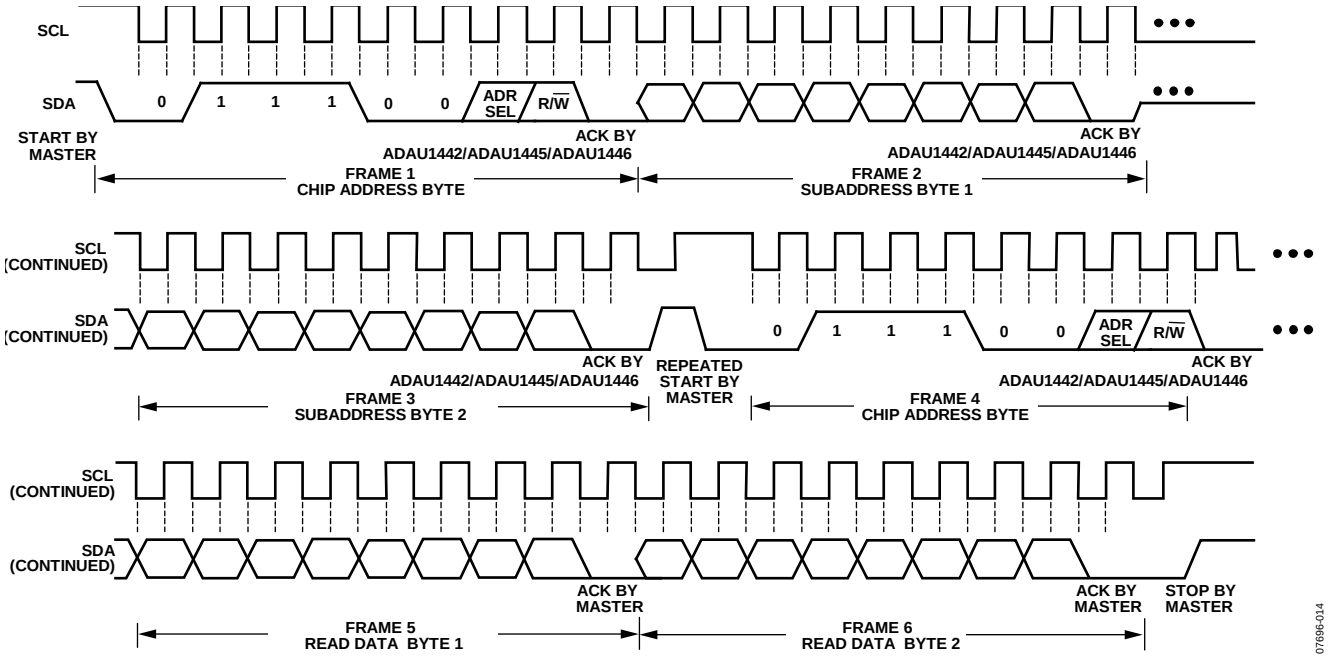


Figure 14. I²C Read Clocking

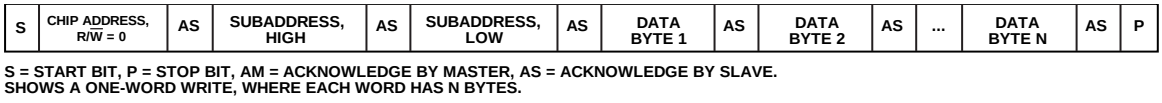


Figure 15. Single-Word I²C Write Sequence

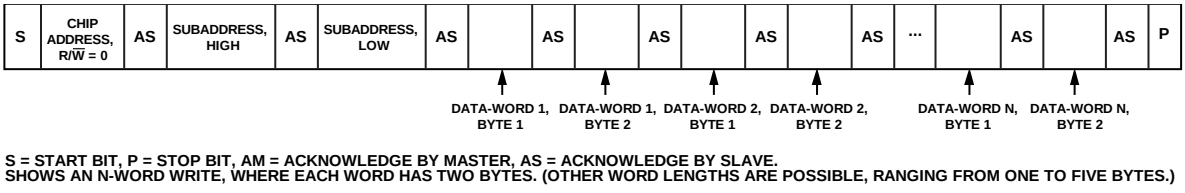


Figure 16. Burst Mode I²C Write Sequence

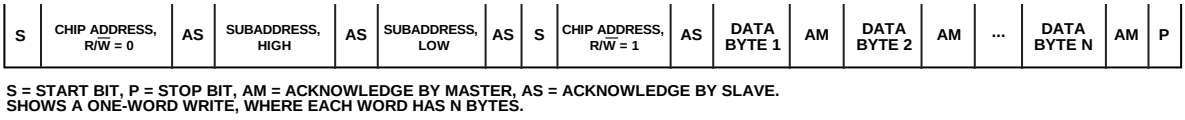


Figure 17. Single-Word I²C Read Sequence

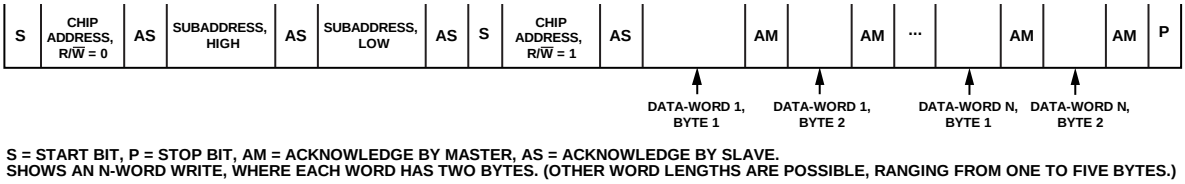


Figure 18. Burst Mode I²C Read Sequence

SPI Port

By default, the ADAU1442/ADAU1445/ADAU1446 are in I²C mode, but these parts can be put into SPI control mode by pulling CLATCH low three times. Each low pulse should have a minimum duration of 20 ns, and the delay between pulses should be at least 20 ns.

The SPI port uses a 4-wire interface, consisting of CLATCH, CCLK, CDATA, and COUT signals. The CLATCH signal goes low at the beginning of a transaction and high at the end of a transaction. The CCLK signal latches CDATA on a low-to-high transition. COUT data is shifted out of the ADAU1442/ADAU1445/ADAU1446 on the falling edge of CCLK and should be clocked into a receiving device, such as a microcontroller, on the next CCLK falling edge (rising edge is possible if t_{COV} timing is met). The CDATA signal carries the serial input data, and the COUT signal is the serial output data. The COUT signal remains three-stated until a read operation is requested. This allows other SPI-compatible peripherals to share the same readback line. All SPI transactions have the same word sequence shown in Table 15 (see Figure 4 for an SPI port timing diagram). All data written should be MSB first.

Chip Address R/$\overline{W}$

The first byte of an SPI transaction includes the 7-bit chip address and a R/$\overline{W}$ bit. The chip address is set by the ADDR0 pin. This allows two ADAU1442/ADAU1445/ADAU1446 devices to share a CLATCH signal, yet still operate independently. When ADDR0 is low, the chip address is 0000000; when ADDR0 is high, the address is 0000001. The LSB of the first byte determines whether the SPI transaction is a read (Logic Level 1) or a write (Logic Level 0). Users can communicate with both ICs with up to five latch signals by using the USBi communication channel list in the hardware configuration tab in SigmaStudio.

Subaddress

The 16-bit subaddress word is decoded into a location in one of the memories or registers. This subaddress is the location of the appropriate RAM location or register.

Data Bytes

The number of data bytes varies according to the register or memory being accessed. In burst write mode, an initial subaddress is given followed by a continuous sequence of data for consecutive memory or register locations.

A sample timing diagram for a single SPI write operation to the parameter RAM is shown in Figure 19. A sample timing diagram of a single SPI read operation is shown in Figure 20. The COUT pin goes from three-state to driven at the beginning of Byte 3. In this example, Byte 0 to Byte 2 contain the addresses and R/$\overline{W}$ bit, and subsequent bytes carry the data.

Table 15. Generic Control Word Sequence

Byte 0	Byte 1	Byte 2	Byte 3	Byte 4[1]
Chip Address[6:0], R/$\overline{W}$	Subaddress[15:8]	Subaddress[7:0]	Data	Data

[1] Continues to end of data.

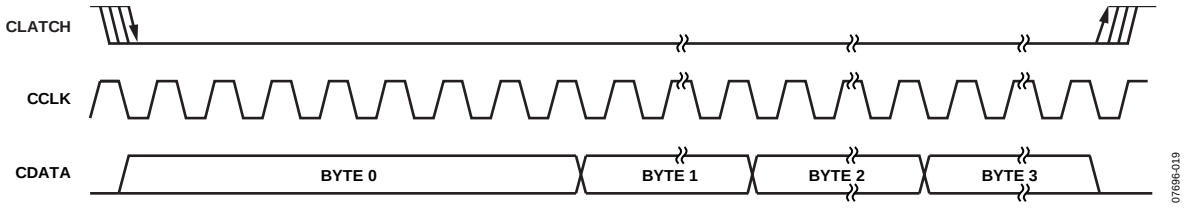


Figure 19. SPI Write Clocking (Single-Write Mode)

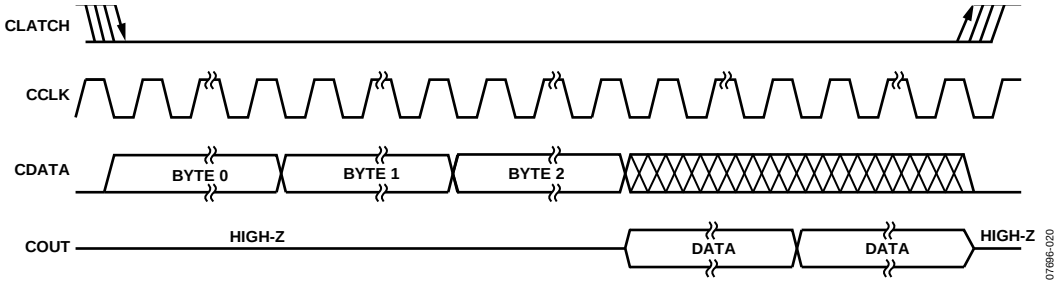


Figure 20. SPI Read Clocking (Single-Read Mode)

Self-Boot

On power-up, the ADAU1442/ADAU1445/ADAU1446 can load a program and a set of parameters that are saved in an external EEPROM. Combined with the auxiliary ADC and the multipurpose pins, this can potentially eliminate the need for a microcontroller in a simple audio system. The self-boot sequence is accomplished by the ADAU1442/ADAU1445/ADAU1446 acting as masters on the I²C bus on startup, which occurs when the SELFBOOT pin is set high. The ADAU1442/ADAU1445/ADAU1446 cannot self-boot in SPI mode.

The maximum necessary EEPROM size is 40,960 bytes, or 40 kB. This much memory is only needed if the program RAM (4096 × 6 bytes) and parameter RAM (4096 × 4 bytes) are each completely full.

A self-boot operation is triggered on the rising edge of $\overline{\text{RESET}}$ when the SELFBOOT pin is set high, and it occurs after 10 ms when the PLL has locked. The ADAU1442/ADAU1445/ADAU1446 read the program, parameter, and register data from the EEPROM. After the ADAU1442/ADAU1445/ADAU1446 have finished self-booting, additional messages can be sent to the ADAU1442/ADAU1445/ADAU1446 on the I²C bus, although this typically is not necessary in a self-booting application. The I²C device address for the ADAU1442/ADAU1445/ADAU1446 is 0x68 for a write and 0x69 for a read in this mode. The ADDRx pins have different functions when the chip is in this mode; therefore, the settings on them are ignored.

The ADAU1442/ADAU1445/ADAU1446 are masters on the I²C bus during a self-boot operation. Care should be taken that no other device on the I²C bus tries to perform a write operation during self-booting. The ADAU1442/ADAU1445/ADAU1446 generate SCL at 8 × f_s; therefore, when $f_{s,NORMAL}$ is 48 kHz, SCL runs at 384 kHz. SCL has a duty cycle of ⅜ in accordance with the I²C specification.

The ADAU1442/ADAU1445/ADAU1446 read from EEPROM Chip Address 0xA1. The LSBs of the addresses of some EEPROMs are pin configurable; in most cases, these pins should be tied low to set this address. SigmaStudio writes to the EEPROM at Address 0xA0.

EEPROM Format

The EEPROM data contains a sequence of messages. Each discrete message is one of the four types defined in Table 17. Each message consists of a sequence of one or more bytes. The first byte identifies the message type. Bytes are written MSB first. Most messages are block write (0x01) types, which are used for writing to the ADAU1442/ADAU1445/ADAU1446 program RAM, parameter RAM, and control registers.

The body of the message following the message type should start with two bytes indicating message length and then include a byte indicating the chip address. Following this is always a 2-byte register or memory address field, as with all other control port transactions.

SigmaStudio is capable of generating the EEPROM data necessary to self-boot the ADAU1442/ADAU1445/ADAU1446, using the function called write latest compilation to E2PROM. This function can be accessed by right-clicking the ADAU1442/ADAU1445/ADAU1446 IC in the hardware configuration window.

Table 16. Functions of the Control Port Pins

Pin	I²C Mode	SPI Mode	Self-Boot
SCL/CCLK	SCL—input	CCLK—input	SCL—output
SDA/COUT	SDA—open collector output	COUT—output	SDA—open collector output
ADDR1/CDATA	ADDR1—input	CDATA—input	Unused input—tie to ground or power
CLATCH	Unused input—tie to ground or power	CLATCH—input	Unused input—tie to ground or power
ADDR0	ADDR0—input	ADDR0—input	Unused input—tie to ground or power

Table 17. EEPROM Message Types

Message ID	Message Type	Following Bytes
0x00	End	None
0x01	Write	One byte indicating message length (including chip address and subaddress), one byte indicating chip address, two bytes indicating subaddress, and an appropriate number of data bytes
0x02	Delay	Two bytes for delay
0x03	No op	None

SERIAL DATA INPUT/OUTPUT

The flexible serial data input and output ports of the ADAU1442/ADAU1445/ADAU1446 can be set to accept or transmit data in a 2-channel (usually I²S format), packed TDM4, or standard 4-, 8-, or 16-channel TDM stream. Data is processed in twos complement, MSB-first format. The left-channel data field always precedes the right-channel data field in 2-channel streams. In the TDMn modes (where n represents the total number of channels in the stream), Slot 0 to Slot (n/2) − 1 fall in the first half of the audio frame, and Slot n/2 to Slot n − 1 are in the second half of the frame. TDM mode allows fewer serial data pins to be used, freeing more pins for other data streams. The serial modes are set in the serial output port modes and serial input port modes control registers.

When referring to audio data streams, the terms *TDM2* and *I²S* should be treated with care. In this document, *TDM2* refers to any 2-channel stream, whereas *I²S* refers specifically to a 2-channel, negative BCLK polarity, negative LRCLK polarity, MSB delay-by-1 stream.

The serial data clocks are fully bidirectional and do not need to be synchronous with the ADAU1442/ADAU1445/ADAU1446 master clock input. However, asynchronous data streams must be routed through an on-board asynchronous sample rate converter to be processed in the core.

The input control registers allow control of clock polarity and data input modes. All common data formats are available with flexible MSB start, bit depth (24-, 20-, or 16-bit), and TDM settings. In all modes except the right-justified modes, the serial port accepts an arbitrary number of bits up to a limit of 24. Extra bits do not cause an error, but they are truncated internally. Proper operation of the right-justified modes requires that there be exactly 64 BCLKs per audio frame (for 2-channel data). The LRCLK in TDM mode can be input to the ADAU1442/ADAU1445/ADAU1446 either as a 50/50 duty cycle clock or as a bit-wide pulse.

In TDM mode, the bit clock supplied by the ADAU1442/ADAU1445/ADAU1446 in master mode is limited to 25 MHz. This, in turn, limits the sampling rate at which it can supply master clocks in various TDM modes. Table 18 displays the modes in which the serial output port functions for some common audio sample rates.

The output control registers give the user control of clock polarities, clock frequencies, clock types, and data format. In all modes except the right-justified modes (MSB delayed by 8, 12, or 16), the serial port accepts an arbitrary number of bits up to a limit of 24. Extra bits do not cause an error, but are truncated internally. Proper operation of the right-justified modes requires the LSB to align with the edge of the LRCLK. The default settings of all serial port control registers correspond to 2-channel, I²S mode, and 24-bit slave mode, and these registers are set as slaves to the clock domain corresponding to their channel number.

Table 18. Serial Input and Output Port TDM Capabilities

Mode	BCLK Cycles per Frame	f_S (kHz)	BCLK Frequency (MHz)	Valid Mode
TDM2	64	44.1	2.8224	Yes
	64	48	3.072	Yes
	64	88.2	5.6448	Yes
	64	96	6.144	Yes
	64	192	12.288	Yes
TDM4	128	44.1	5.6448	Yes
	128	48	6.144	Yes
	128	88.2	11.2896	Yes
	128	96	12.288	Yes
	128	192	24.576	Yes
TDM8	256	44.1	11.2896	Yes
	256	48	12.288	Yes
	256	88.2	22.5792	Yes
	256	96	24.576	Yes
	256	192	49.152	No[1]
TDM16	512	44.1	22.5792	Yes
	512	48	24.576	Yes
	512	88.2	45.1584	No[1]
	512	96	49.152	No[1]
	512	192	98.304	No[1]

[1] The device will not work in this mode.

Connections to an external DAC are handled exclusively with the output port pins. The output LRCLKx and BCLKx pins can be set to be either master or slave, and the SDATA_OUT pins are used to output data from the SigmaDSP to the external DAC.

Table 19 shows the proper configurations for standard audio data formats, and Figure 21 presents an overview of the serial data input/output ports.

Table 19. Configurations for Standard Audio Data Formats

Format	LRCLK Polarity	LRCLK Type	BCLK Polarity	MSB Position
I²S (Figure 22)	Frame begins on falling edge	Clock	Data changes on falling edge	Delayed from LRCLKx edge by 1 BCLK
Left-Justified (Figure 23)	Frame begins on rising edge	Clock	Data changes on falling edge	Aligned with LRCLKx edge
Right-Justified (Figure 24)	Frame begins on rising edge	Clock	Data changes on falling edge	Delayed from LRCLKx edge by 8, 12, or 16 BCLKs
TDM with Clock (Figure 25)	Frame begins on falling edge	Clock	Data changes on falling edge	Delayed from start of frame clock by 1 BCLK
TDM with Pulse (Figure 26)	Frame begins on rising edge	Pulse	Data changes on falling edge	Delayed from start of frame clock by 1 BCLK

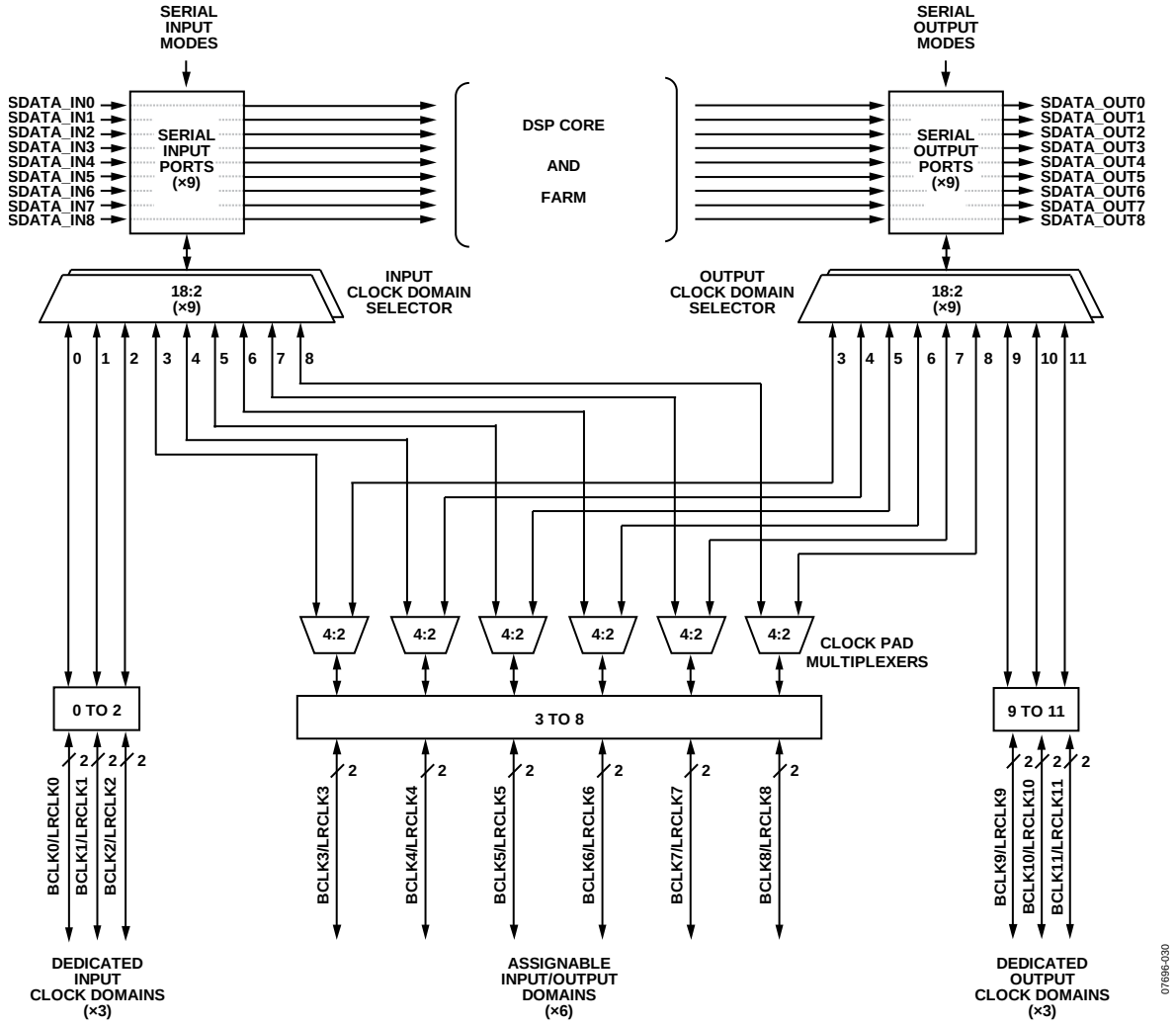


Figure 21. Overview of Serial Data Input/Output Ports

Serial Audio Data Timing Diagrams

Figure 22 to Figure 26 show timing diagrams for standard audio data formats.

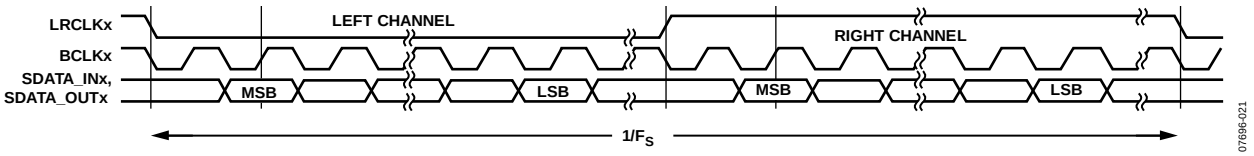


Figure 22. I²S Mode—16 Bits to 24 Bits per Channel

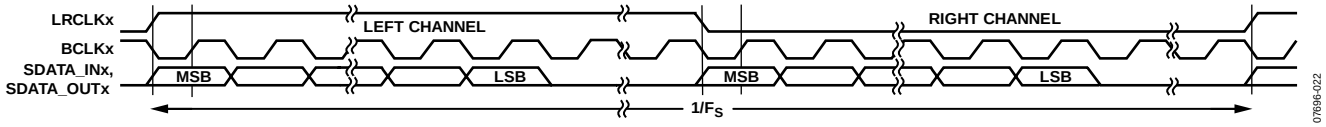


Figure 23. Left-Justified Mode—16 Bits to 24 Bits per Channel

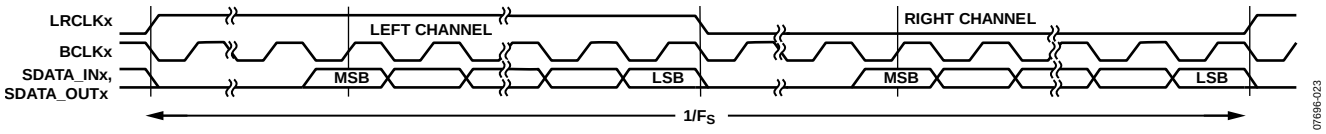


Figure 24. Right-Justified Mode—16 Bits to 24 Bits per Channel

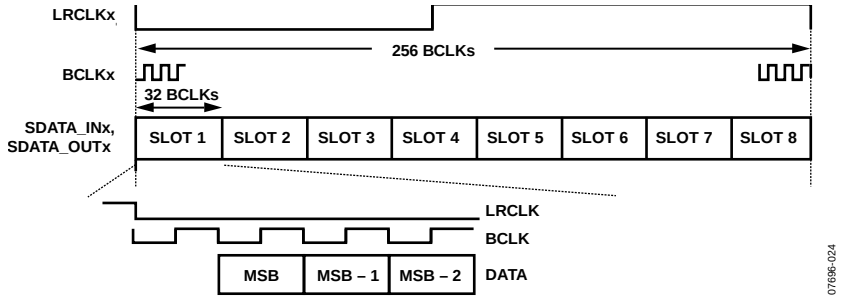


Figure 25. TDM Mode

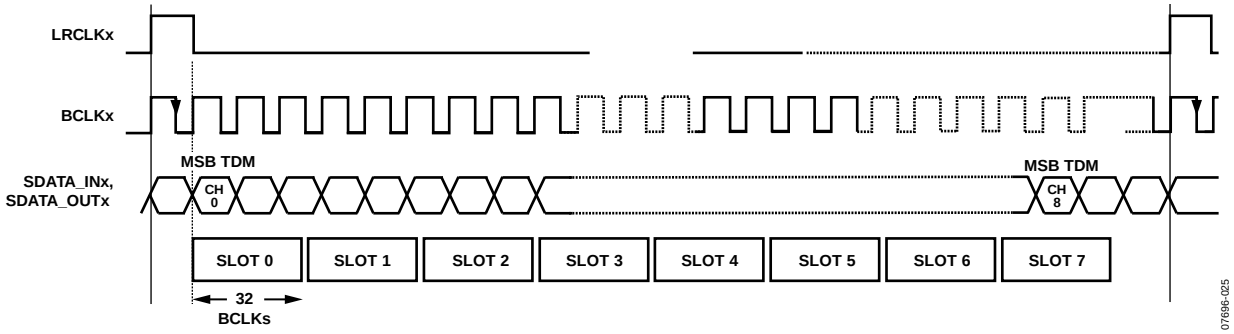


Figure 26. TDM Mode with Pulse Frame Clock

Serial Clock Domains

There are 12 clock domains (pairs of LRCLKx and BCLKx pins) available in the ADAU1442/ADAU1445/ADAU1446. Of these, three are available exclusively to the serial data input ports, three are available exclusively to the serial data output ports, and the remaining six can be assigned to clock either input or output ports.

The ADAU1442 contains eight 2-channel ASRCs and the ADAU1445 contains two 8-channel ASRCs, whereas the ADAU1446 contains no ASRCs. However, all clock domain pins are available on every device. In a system with no sample rate conversion and with serial ports in slave mode, at least two pairs of LRCLKx and BCLKx pins must be connected: one pair for the input serial ports and one pair for the output serial ports. If all serial ports are in master mode and synchronous, then only one pair of LRCLKx and BCLKx pins needs to be connected.

Figure 27 shows a simplified view of the assignment of clock domains to the input and output sides of the chip. Note that each clock domain comprises two signals, namely the BCLK (bit clock) and LRCLK (frame clock). Therefore, the 12 clock domains contain a total of 24 clock signals.

Each clock domain is capable of acting as a master or slave. For this reason, all LRCLK and BCLK pins are bidirectional. In slave mode, the LRCLK and BCLK pins receive clock signals from an external source, such as a codec. In master mode, the LRCLK and BCLK pins output clock signals to external slave ICs.

Although a clock domain in slave mode can clock an arbitrary number of serial ports, a clock domain in master mode can only clock a single serial port. For Clock Domains[2:0] and Clock Domains[11:9], the corresponding serial port is fixed as an input or output. For assignable clock domains (Clock Domains[8:3]), the corresponding serial port can be either an input or output, depending on the setting of the clock pad multiplexer register (see Table 20 for more details).

Table 20. Master Mode Clock Domain Assignment

Clock Domain	Chip Pins	Serial Port
0	LRCLK0, BCLK0	SDATA_IN0
1	LRCLK1, BCLK1	SDATA_IN1
2	LRCLK2, BCLK2	SDATA_IN2
3	LRCLK3, BCLK3	SDATA_IN3 or SDATA_OUT3[1]
4	LRCLK4, BCLK4	SDATA_IN4 or SDATA_OUT4[1]
5	LRCLK5, BCLK5	SDATA_IN5 or SDATA_OUT5[1]
6	LRCLK6, BCLK6	SDATA_IN6 or SDATA_OUT6[1]
7	LRCLK7, BCLK7	SDATA_IN7 or SDATA_OUT7[1]
8	LRCLK8, BCLK8	SDATA_IN8 or SDATA_OUT8[1]
9	LRCLK9, BCLK9	SDATA_OUT0
10	LRCLK10, BCLK10	SDATA_OUT1
11	LRCLK11, BCLK11	SDATA_OUT2

[1] Depends on the setting of the clock pad multiplexer register (Address 0xE240).

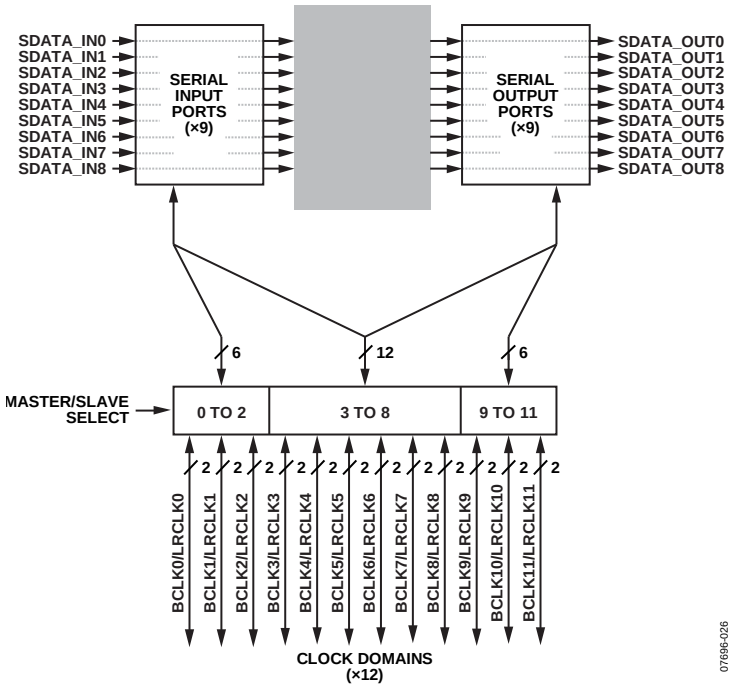


Figure 27. Simplified Serial Clock Domain Assignment

Serial Clock Modes and Settings

Dejitter Window Register (Address 0xE221)

Table 21. Bit Descriptions of Register 0xE221

Bit Position	Description	Default
[15:6]	Reserved	
[5:0]	Dejitter window 000000 = dejitter circuit bypass 000001 = minimum window … 111111 = maximum window	001000

Register 0xE221 is a single 6-bit register that sets the size of the dejitter window. The dejitter circuit prevents samples from being repeated or omitted altogether due to jitter in the frame clock pulses coming from the serial ports in slave mode.

The dejitter window is set by default to 8 MCLK samples, which should be suitable for most applications. However, Register 0xE221 allows this value to be tweaked in case of problems, or it allows the dejitter circuit to be bypassed altogether by setting Bits[5:0] to 000000.

Clock Pad Multiplexer Register (Address 0xE240)

Table 22. Bit Descriptions of Register 0xE240

Bit Position	Clock Domain[1]	Default
[15:6]	Reserved	
5	Clock Domain 8	0
4	Clock Domain 7	0
3	Clock Domain 6	0
2	Clock Domain 5	0
1	Clock Domain 4	0
0	Clock Domain 3	0

[1] 0 = input clock domain, 1 = output clock domain.

There are six clock domains (Clock Domains[8:3]) that can be either input or output clock domains. This is determined by a single bit for each clock domain (see Table 22), where a setting of 0 corresponds with an input clock domain and a setting of 1 corresponds with an output clock domain.

In Figure 28, the clock pad multiplexer is represented by six 4:2 multiplexers.

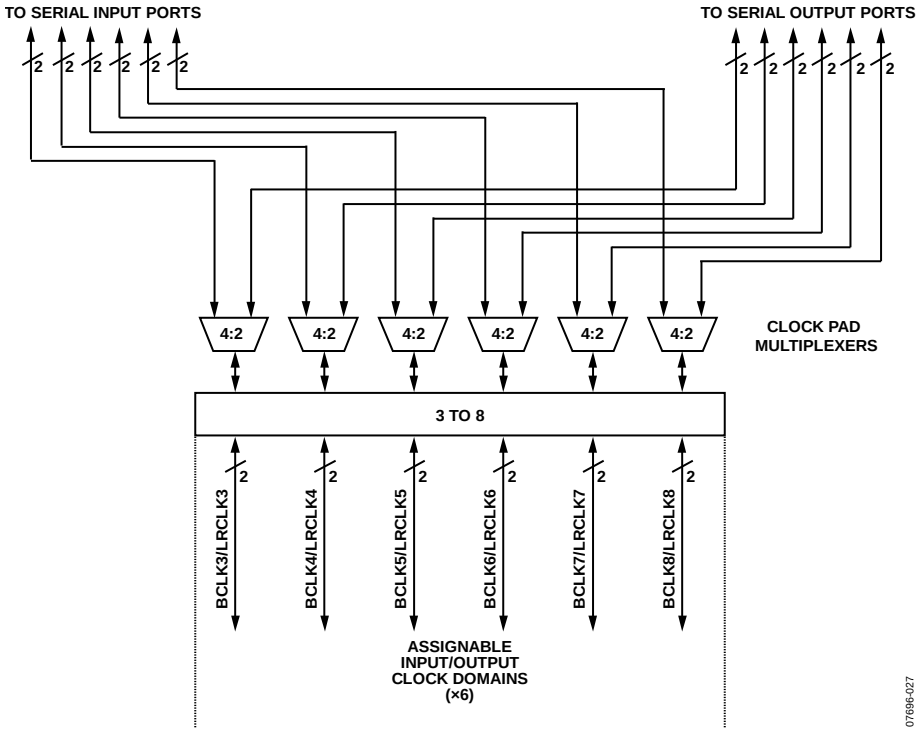


Figure 28. Clock Pad Multiplexer

Packed TDM4 Mode

A special TDM mode is available that allows four channels to be fit into a space of 64 bit clock cycles. This mode is called packed TDM4 mode, or MOST™ mode. MOST (Media Oriented Systems Transport) is a networking standard intended for interconnecting multimedia components in automobiles and other vehicles. Many ICs intended to interface with a MOST bus use a packed TDM4 data format.

For this mode to be used, the serial port must be set up with the following register settings:

- Packed TDM4 mode
- Left-justified or delay by 1
- Word length of 16 bits

See Figure 29 for a timing diagram of the packed TDM4 mode. This figure is shown with a negative BCLK polarity, a negative LRCLK polarity, and an MSB delay of 1.

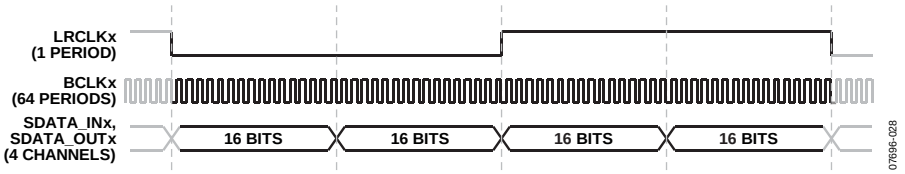


Figure 29. Packed TDM4 Mode

SERIAL INPUT PORTS

The serial input ports convert standard I2S and TDM signals into 16-, 20-, and 24-bit audio signals for input to the audio processor. They support TDM2, TDM4, TDM8, and TDM16 time division multiplexing schemes and I²S, left-justified, right-justified, MSB delay-by-12 and delay-by-16 modes. Different clock polarities and multiple word lengths are supported, as well as the capability to drive in master mode or to be driven in slave mode.

The serial input ports are composed of up to nine clock domains (Clock Domain 0 to Clock Domain 8) and up to nine serial data signals (SDATA_IN0 to SDATA_IN8).

In slave mode, the nine serial input clock domains are driven directly from the corresponding nine pairs of LRCLKx and BCLKx pins on the IC. Three pairs of LRCLKx and BCLKx pins (LRCLK[2:0] and BCLK[2:0]) are hardwired to Clock Domains[2:0], which are serial inputs. The remaining six pairs of LRCLKx and BCLKx pins (LRCLK[8:3] and BCLK[8:3]) are multiplexed to Clock Domains[8:3] as either inputs or outputs. The multiplexer can be set to use these signals as input clock domains by writing to Bits[5:0] of the clock pad multiplexer register (Address 0xE240) as explained in Table 23. This configuration is also valid in master mode.

Figure 30 shows in more detail how the clocks are routed to and from the serial input ports. For the assignable clock domains (Clock Domains[8:3]), the clock pad multiplexer allows them to be routed either to the serial input ports or to the serial output ports independently. In slave mode, the clock domain selector (that is, the 18:2 multiplexer) allows each serial input port to clock from any available clock domain. In master mode, the clock domain selector is bypassed, and the assignments described in Table 24 are used.

The maximum number of audio channels that can be input to SigmaDSP is 24. The serial input ports must be set in a way that respects this (for example, two TDM16 streams is not a valid entry).

Table 23. Input Clock Domain Multiplexing

Clock Domain	Chip Pins	Register 0xE240 Setting
0	LRCLK0, BCLK0	N/A
1	LRCLK1, BCLK1	N/A
2	LRCLK2, BCLK2	N/A
3	LRCLK3, BCLK3	Set Bit 0 to 0
4	LRCLK4, BCLK4	Set Bit 1 to 0
5	LRCLK5, BCLK5	Set Bit 2 to 0
6	LRCLK6, BCLK6	Set Bit 3 to 0
7	LRCLK7, BCLK7	Set Bit 4 to 0
8	LRCLK8, BCLK8	Set Bit 5 to 0

Table 24. Input Clock Domain Assignments in Master Mode

Data Pin	Clock Pins
SDATA_IN0	LRCLK0, BCLK0
SDATA_IN1	LRCLK1, BCLK1
SDATA_IN2	LRCLK2, BCLK2
SDATA_IN3	LRCLK3, BCLK3
SDATA_IN4	LRCLK4, BCLK4
SDATA_IN5	LRCLK5, BCLK5
SDATA_IN6	LRCLK6, BCLK6
SDATA_IN7	LRCLK7, BCLK7
SDATA_IN8	LRCLK8, BCLK8

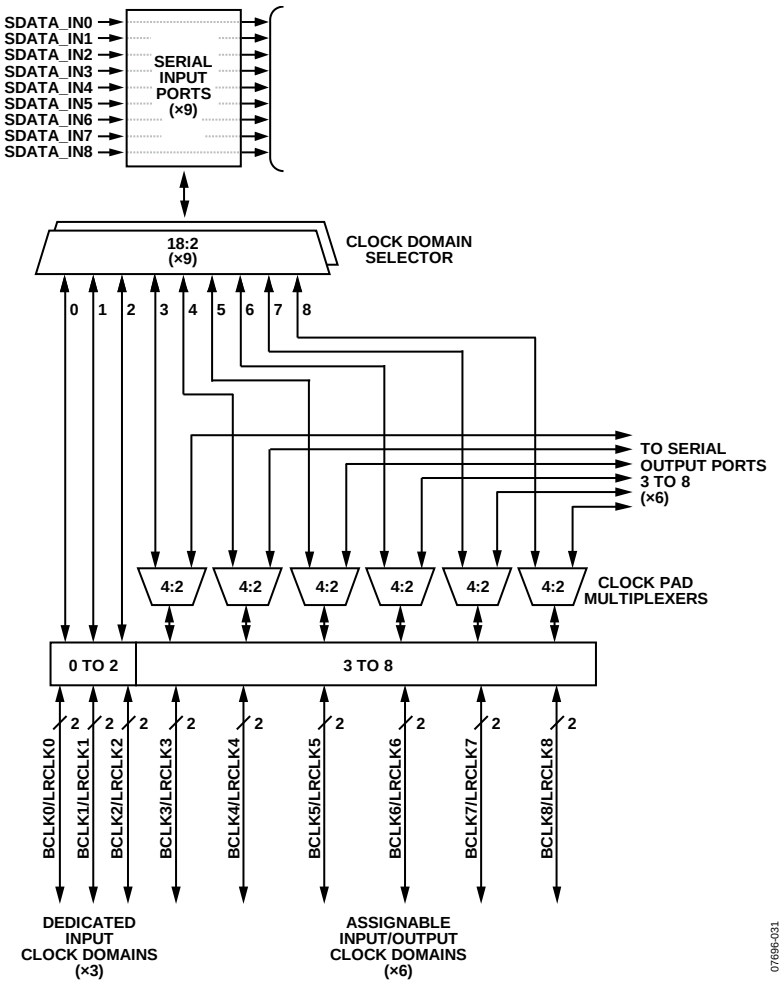


Figure 30. Input Serial Port Clock Multiplexing

SERIAL INPUT PORT MODES AND SETTINGS

Each of the nine serial input ports is controlled by setting an individual 2-byte word in the serial input mode register for each port (see Table 25 for the register addresses). Each serial data signal can be set to use any of the nine clock domains (slave mode) or an internally generated LRCLK signal at $f_{S,NORMAL}$, $f_{S,DUAL}$, or $f_{S,QUAD}$. The default value for each serial port on reset is set to stereo, I²S, 24-bit, negative LRCLK and BCLK polarity slave mode using a 50% duty cycle LRCLK (as opposed to a synchronization pulse). This configuration corresponds to a setting of 0x3C00. The serial data uses its corresponding clock domain (that is, SDATA3 uses LRCLK3 and BCLK3).

Restrictions

When the device is in MOST mode (packed TDM4 mode), the MSB position of the serial data must be delayed by one bit clock from the start of the frame (I²S position) and the data must be 16 bits wide.

Each channel has a frame of 32 bits. Therefore, when the device is in delay-by-12 mode, the serial data can only be 16 or 20 bits wide (not 24 bits). When the device is in delay-by-16 mode, the serial data can only be 16 bits wide.

Due to the limited maximum clock speed, master and slave modes are only compatible with certain TDM modes. See Table 18 for more details.

Serial Input Port Modes Registers (Address 0xE000 to Address 0xE008)

Table 25. Addresses of Serial Input Port Modes Registers

Address			
Decimal	**Hex**	**Name**	**Read/Write Word Length**
57344	E000	Serial Input Port 0 modes	16 bits (2 bytes)
57345	E001	Serial Input Port 1 modes	16 bits (2 bytes)
57346	E002	Serial Input Port 2 modes	16 bits (2 bytes)
57347	E003	Serial Input Port 3 modes	16 bits (2 bytes)
57348	E004	Serial Input Port 4 modes	16 bits (2 bytes)
57349	E005	Serial Input Port 5 modes	16 bits (2 bytes)
57350	E006	Serial Input Port 6 modes	16 bits (2 bytes)
57351	E007	Serial Input Port 7 modes	16 bits (2 bytes)
57352	E008	Serial Input Port 8 modes	16 bits (2 bytes)

Table 26. Bit Descriptions of Serial Input Port Modes Registers

Bit Position	Description	Default
15	Clock output enable[1] 0 = LRCLK and BCLK output pins disabled 1 = LRCLK and BCLK output pins enabled	0
14	Frame sync type 0 = LRCLK 50/50 duty cycle clock signal (square wave) 1 = LRCLK synchronization pulse (narrow pulse)	0
[13:10]	Clock domain master/slave select[1] 0000 = slave to Clock Domain 0 (Port 0) 0001 = slave to Clock Domain 1 (Port 1) 0010 = slave to Clock Domain 2 (Port 2) 0011 = slave to Clock Domain 3 (Port 3) 0100 = slave to Clock Domain 4 (Port 4) 0101 = slave to Clock Domain 5 (Port 5) 0110 = slave to Clock Domain 6 (Port 6) 0111 = slave to Clock Domain 7 (Port 7) 1000 = slave to Clock Domain 8 (Port 8) 1001 = master, clock is $f_{S,NORMAL}$ 1010 = master, clock is $f_{S,DUAL}$ 1011 = master, clock is $f_{S,QUAD}$	Address specific[2]
9	Serial input BCLK polarity 0 = negative BCLK polarity 1 = positive BCLK polarity	0
8	Serial input LRCLK polarity 0 = negative LRCLK polarity 1 = positive LRCLK polarity	0

Bit Position	Description	Default
[7:6]	Word length 00 = 24 bits 01 = 20 bits 10 = 16 bits 11 = flexible TDM mode[3]	00
[5:3]	MSB position 000 = I²S (delayed by 1) 001 = left justified (delayed by 0) 010 = delayed by 8 011 = delayed by 12 100 = delayed by 16	000
[2:0]	TDM type 000 = TDM2 (stereo) 001 = TDM4 010 = TDM8 or flexible TDM mode[3] 011 = TDM16 100 = packed TDM4	000

[1] Bit 15 and Bits[13:10] must be used in conjunction to set the port as a master or slave.
[2] The default depends on the address: 0xE000 = 0001, 0xE001 = 0010, 0xE002 = 0011, 0xE003 = 0100, 0xE004 = 0101, 0xE005 = 0110, 0xE006 = 0111, 0xE007 = 1000, and 0xE008 = 1001.
[3] To activate flexible TDM mode, both Bits[7:6] and Bits[2:0] must be set.

Clock Output Enable Bit (Bit 15)

This bit controls the serial port's respective bit clock as well as the left and right clocks. When this bit is set to 1, the clock pins are set to output. When this bit is set to 0, the clock pins are not output clocks. In Register 0xE000 to Register 0xE008, Bit 15 and Bits[13:10] must be used in conjunction to set the port as a master or slave. Clock domains are assigned to input or output serial ports with the clock pad multiplexer register (Address 0xE240). For more information, see the Clock Pad Multiplexer section.

Frame Sync Type Bit (Bit 14)

This bit sets the type of LRCLK signal that is used. When this bit is set to 0, the clock signal is a square wave. When this bit is set to 1, the signal is a narrow pulse.

Clock Domain Master/Slave Select Bits (Bits[13:10])

These bits determine whether the serial port outputs its clocks as a master or slave to an available clock domain. If a serial port is set to be a master, the clock output enable bit (Bit 15) must be set to 1. If a serial port is set as a slave, the clock output enable bit must be set to 0. In both cases, the corresponding clock pad multiplexer must be set to the serial input domain if it is assignable. For more information, see the Clock Pad Multiplexer section. Note that an arbitrary number of serial ports can be slaves to a single clock domain, but a single serial port can only be a master to one clock domain. The values for $f_{S,NORMAL}$, $f_{S,DUAL}$, and $f_{S,QUAD}$ are 48 kHz, 96 kHz, and 192 kHz, respectively, for a 172.032 MHz core clock signal.

Serial Input BCLK Polarity Bit (Bit 9)

The polarity of BCLKx determines whether LRCLKx and SDATA_INx change on a rising (+) or falling (−) edge of the BCLKx signal. Standard I²S signals use negative BCLK polarity.

Serial Input LRCLK Polarity Bit (Bit 8)

The polarity of LRCLKx determines whether the left stereo channel is initiated on a rising (+) or falling (−) edge of the LRCLKx signal. Standard I²S signals use negative LRCLK polarity.

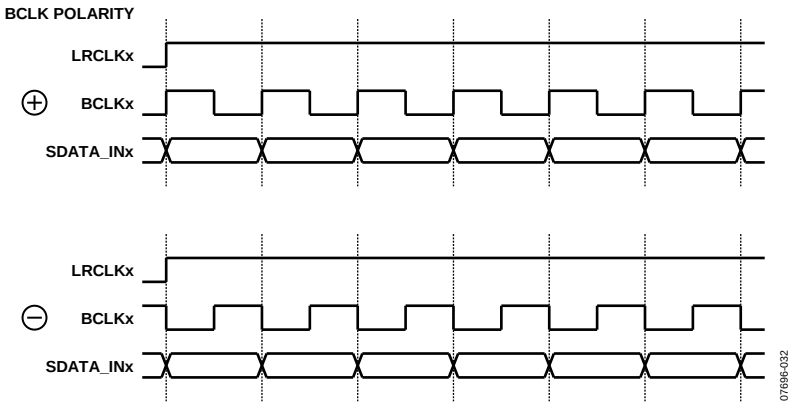


Figure 31. Serial Input BCLK Polarity

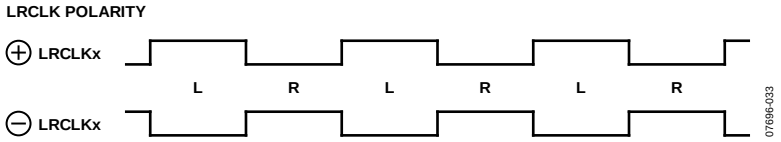


Figure 32. Serial Input LRCLK Polarity

Word Length Bits (Bits[7:6])

These bits set the word length of the input data to 16, 20, or 24 bits. If the input signal has more data bits than this word length, the extra bits are truncated. The fourth setting is flexible TDM. For more information, see the Serial Input Flexible TDM Interface Modes section.

MSB Position Bits (Bits[5:3])

These bits set the position of the MSB in the data stream.

TDM Type (Bits[2:0])

These bits set the number of channels contained in the data stream. The possible choices are TDM2 (stereo), TDM4, TDM8 or flexible TDM, TDM16, and packed TDM4 mode. For more information on the packed TDM4 mode, see the Packed TDM4 Mode section. If the word length bits (Bits[7:6]) are set to 11 for flexible TDM mode, then TDM type bits (Bits[2:0]) must also be set for flexible TDM mode (that is, set to 010).

In master mode, the ADAU1442/ADAU1445/ADAU1446 can generate either an LRCLK clock signal (50% duty cycle) or an LRCLK synchronization pulse at the specified frequency ($f_{S,NORMAL}$, $f_{S,DUAL}$, or $f_{S,QUAD}$). When a pulse is generated, its width is equal to one single internal BCLK. Each channel requires 32 BCLK cycles per LRCLK. Therefore, for TDM4, 128 BCLK cycles are required; for TDM8, 256 BCLK cycles; for TDM16, 512 BCLK cycles; for TDM2, 64 BCLK cycles (except when the LRCLK signal is a 50% duty cycle signal (that is, not a pulse) or when it is running in I²S or left-justified mode); and for packed TDM4, 64 BCLK cycles.

SERIAL OUTPUT PORTS

The serial output ports convert 16-, 20-, and 24-bit audio signals coming from the audio processor to standard I²S and TDM signals on the serial data outputs. They support TDM2, TDM4, TDM8, and TDM16 time division multiplexing schemes and I²S, left-justified, right-justified, and MSB delay-by-12 and delay-by-16 modes. Different clock polarities and multiple word lengths are supported, as well as the capability to drive in master mode or to be driven in slave mode.

The serial output ports are composed of up to nine clock domains (Clock Domain 3 to Clock Domain 11) and up to nine serial data signals (SDATA_IN0 to SDATA_IN8).

In slave mode, the nine serial output clock domains are driven directly from the corresponding nine pairs of LRCLKx and BCLKx pins on the IC. Three pairs of LRCLKx and BCLKx pins (LRCLK[11:9] and BCLK[11:9]) are hardwired to Clock Domains[11:9], which are serial outputs. The remaining six pairs of LRCLKx and BCLKx pins (LRCLK[8:3] and BCLK[8:3]) are multiplexed to Clock Domains[8:3] as either inputs or outputs. The multiplexer can be set to use these signals as output clock domains by writing to Bits[5:0] of the clock pad multiplexer register (Address 0xE240) as explained in Table 27. This configuration is also valid in master mode.

Table 27. Output Clock Domain Multiplexing

Clock Domain	Chip Pins	Register 0xE240 Setting
0	LRCLK9, BCLK9	N/A
1	LRCLK10, BCLK10	N/A
2	LRCLK11, BCLK11	N/A
3	LRCLK3, BCLK3	Set Bit 0 to 1
4	LRCLK4, BCLK4	Set Bit 1 to 1
5	LRCLK5, BCLK5	Set Bit 2 to 1
6	LRCLK6, BCLK6	Set Bit 3 to 1
7	LRCLK7, BCLK7	Set Bit 4 to 1
8	LRCLK8, BCLK8	Set Bit 5 to 1

Figure 33 shows in detail how the clocks are routed to and from the serial output ports. For the assignable clock domains (Clock Domains[8:3]), the clock pad multiplexer allows each clock domain to be individually routed to either the serial input ports or to the serial output ports. In slave mode, the clock domain

selector (that is, the 18:2 multiplexer) allows each serial output port to clock from any available clock domain. In master mode, the clock domain selector is bypassed, and the assignments described in Table 28 are used.

Table 28. Output Clock Domain Assignments in Master Mode

Data Pin	Clock Pins
SDATA_OUT0	LRCLK9, BCLK9
SDATA_OUT1	LRCLK10, BCLK10
SDATA_OUT2	LRCLK11, BCLK11
SDATA_OUT3	LRCLK3, BCLK3
SDATA_OUT4	LRCLK4, BCLK4
SDATA_OUT5	LRCLK5, BCLK5
SDATA_OUT6	LRCLK6, BCLK6
SDATA_OUT7	LRCLK7, BCLK7
SDATA_OUT8	LRCLK8, BCLK8

The maximum number of audio channels that can be output from SigmaDSP is 24. The serial output ports must be set in a way that respects this (for example, two TDM16 streams is not a valid entry).

All data is processed in twos complement, MSB-first format, and the left channel always precedes the right channel.

SERIAL OUTPUT PORT MODES AND SETTINGS

Each of the nine serial output ports is controlled by setting an individual 2-byte word in the serial output mode register for each port (see Table 29 for the register addresses). Each serial data signal can be set to use any of the nine clock domains (slave mode) or an internally generated LRCLK signal at $f_{S,NORMAL}$, $f_{S,DUAL}$, or $f_{S,QUAD}$. The default value for each serial port on reset is set to TDM2, I²S, 24-bit, negative LRCLK and BCLK polarity slave mode using a 50% duty cycle LRCLK clock signal (as opposed to a synchronization pulse). This configuration corresponds to a setting of 0x3C00. The serial data uses its corresponding clock domain (for example, SDATA3 uses LRCLK3 and BCLK3).

Restrictions

When the device is in MOST mode, the MSB position of the serial data is delayed by one bit clock from the start of the frame (I²S position) and the data width is restricted to 16 bits.

When the device is in MSB delay-by-12 mode, the serial data can be 16 or 20 bits wide (not 24 bits). When the device is in MSB delay-by-16 mode, the serial data can only be 16 bits wide.

For information on TDM capabilities, refer to Table 18.

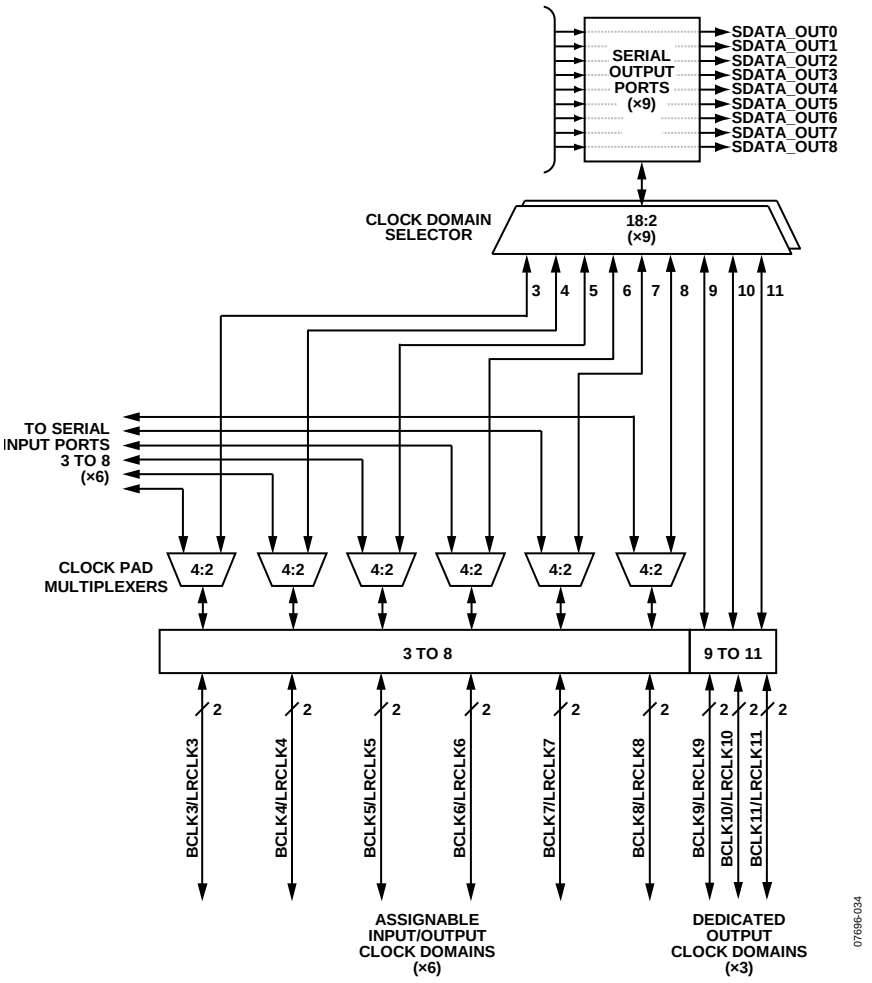


Figure 33. Output Serial Port Clock Multiplexing

Serial Output Port Modes Registers (Address 0xE040 to Address 0xE049)

Table 29. Addresses of Serial Output Port Modes Registers

Address			
Decimal	**Hex**	**Name**	**Read/Write Word Length**
57408	E040	Serial Output Port 0 modes	16 bits (2 bytes)
57409	E041	Serial Output Port 1 modes	16 bits (2 bytes)
57410	E042	Serial Output Port 2 modes	16 bits (2 bytes)
57411	E043	Serial Output Port 3 modes	16 bits (2 bytes)
57412	E044	Serial Output Port 4 modes	16 bits (2 bytes)
57413	E045	Serial Output Port 5 modes	16 bits (2 bytes)
57414	E046	Serial Output Port 6 modes	16 bits (2 bytes)
57415	E047	Serial Output Port 7 modes	16 bits (2 bytes)
57416	E048	Serial Output Port 8 modes	16 bits (2 bytes)
57417	E049	High speed slave interface mode	1 bit (2 bytes)

Table 30. Bit Descriptions of Serial Output Port Modes Registers

Bit Position	Description	Default
15	Clock output enable[1] 0 = LRCLK and BCLK output pins disabled 1 = LRCLK and BCLK output pins enabled	0
14	Frame sync type 0 = LRCLK 50/50 duty cycle clock signal (square wave) 1 = LRCLK synchronization pulse (narrow pulse)	0
[13:10]	Clock domain master/slave select[1] 0000 = slave to Clock Domain 9 (Port 0) 0001 = slave to Clock Domain 10 (Port 1) 0010 = slave to Clock Domain 11 (Port 2) 0011 = slave to Clock Domain 3 (Port 3) 0100 = slave to Clock Domain 4 (Port 4) 0101 = slave to Clock Domain 5 (Port 5) 0110 = slave to Clock Domain 6 (Port 6) 0111 = slave to Clock Domain 7 (Port 7) 1000 = slave to Clock Domain 8 (Port 8) 1001 = master, clock is $f_{S,NORMAL}$ 1010 = master, clock is $f_{S,DUAL}$ 1011 = master, clock is $f_{S,QUAD}$	Address specific[2]
9	Serial output BCLK polarity 0 = negative BCLK polarity 1 = positive BCLK polarity	0
8	Serial output LRCLK polarity 0 = negative LRCLK polarity 1 = positive LRCLK polarity	0
[7:6]	Word length 00 = 24 bits[3] 11 = flexible TDM mode[4]	00
[5:3]	MSB position 000 = I^2S (delayed by 1) 001 = left justified (delayed by 0) 010 = delayed by 8 011 = delayed by 12 100 = delayed by 16	000
[2:0]	TDM type 000 = TDM2 (stereo) 001 = TDM4 010 = TDM8 or flexible TDM mode[4] 011 = TDM16 100 = packed TDM4	000

[1] Bit 15 and Bits[13:10] must be used in conjunction to set the port as a master or slave.
[2] The default depends on the address: 0x040 = 0000, 0xE041 = 0001, 0xE042 = 0010, 0xE043 = 0011, 0xE044 = 0100, 0xE045 = 0101, 0xE046 = 0110, 0xE047 = 0111, 0xE048 = 1000, and 0xE049 = 1001.
[3] Excluding when the serial port is configured in flexible TDM mode, it will always output 24-bit data.
[4] To activate flexible TDM mode, both Bits[7:6] and Bits[2:0] must be set.

Clock Output Enable Bit (Bit 15)

This bit controls the serial port's respective bit clock as well as the left and right clocks. When this bit is set to 1, the clock pins are set to output. When this bit is set to 0, the clock pins are not output clocks. In Register 0xE040 to Register 0xE048, Bit 15 and Bits[13:10] must be used in conjunction to set the port as a master or slave. Clock domains are assigned to input or output serial ports with the clock pad multiplexer register (Address 0xE240). For more information, see the Clock Pad Multiplexer section.

Frame Sync Type Bit (Bit 14)

This bit sets the type of LRCLK signal that is used. When this bit is set to 0, the clock signal is a square wave. When this bit is set to 1, the signal is a narrow pulse.

Clock Domain Master/Slave Select Bits (Bits[13:10])

These bits set whether the serial port outputs its clocks as a master or slave to an available clock domain. If a serial port is set to be a master, the clock output enable bit (Bit 15) must be set to 1. If a serial port is set as a slave, the clock output enable bit (Bit 15) must be set to 0. In both cases, the corresponding clock pad multiplexer must be set to the serial output domain if it is assignable. For more information, see the Clock Pad Multiplexer section. Note that an arbitrary number of serial ports can be slaves to a single clock domain, but a single serial port can only be a master to one clock domain. The values for $f_{S,NORMAL}$, $f_{S,DUAL}$, and $f_{S,QUAD}$ are 48 kHz, 96 kHz, and 192 kHz, respectively, for a 172.032 MHz core clock signal.

Serial Output BCLK Polarity Bit (Bit 9)

The polarity of BCLKx determines whether LRCLKx and SDATA_OUTx change on a rising (+) or falling (−) edge of the BCLKx signal. Standard I²S signals use negative BCLK polarity.

Serial Output LRCLK Polarity Bit (Bit 8)

The polarity of LRCLKx determines whether the left stereo channel is initiated on a rising (+) or falling (−) edge of the LRCLKx signal. Standard I²S signals use negative LRCLK polarity.

Word Length Bits (Bits[7:6])

These bits set the word length of the input data at 16, 20, or 24 bits. The output stream always has space for 24 bits of data, but if the word length is set lower, the extra bits are set as 0s. The fourth setting is flexible TDM. For more information, see the Serial Output Flexible TDM Interface Modes and Settings section.

MSB Position Bits (Bits[5:3])

These bits set the position of the MSB in the data stream.

TDM Type Bits (Bits[2:0])

These bits set the number of channels contained in the data stream. The possible choices are TDM2 (stereo), TDM4, TDM8 or flexible TDM, TDM16, and packed TDM4 mode. For more information on the packed TDM4 mode, see the Packed TDM4 Mode section. If word length bits (Bits[7:6]) are set to 11 for flexible TDM mode, then the TDM type bits (Bits[2:0]) must also be set for flexible TDM mode (that is, set to 010).

High Speed Slave Interface Mode Register (Address 0xE049)

Table 31. Bit Descriptions of Register 0xE049

Bit Position	Description	Default
[15:1]	Reserved	
0	High speed slave interface mode 0 = disabled 1 = enabled	0

High Speed Slave Interface Mode Bit (Bit 0)

If any of the serial output ports are slaves to a bit clock greater than 22 MHz, the high speed slave interface mode must be enabled.

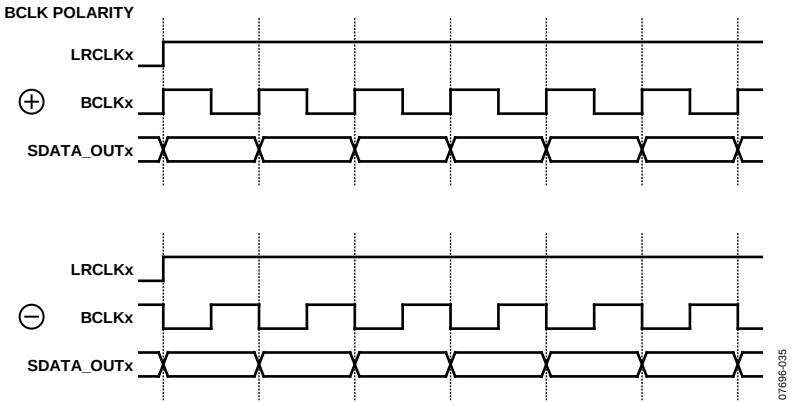


Figure 34. Serial Output BCLK Polarity

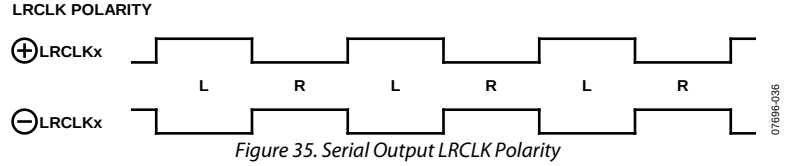


Figure 35. Serial Output LRCLK Polarity

FLEXIBLE AUDIO ROUTING MATRIX (FARM)

The routing matrix distributes audio signals among the serial inputs, serial outputs, ASRCs, S/PDIF receiver and transmitter, and DSP core. This simplifies the design of complex systems that require many inputs and outputs with different sample rates. It also allows signals to be routed in hardware, instead of in software.

Routing Matrix Block Diagram

Figure 36 shows an overview of audio routing in the ADAU1442/ADAU1445/ADAU1446 and details the interaction among the S/PDIF I/O, serial I/O, ASRCs, and DSP via the routing matrix. To reduce the complexity of the system, audio signals are routed in pairs. Therefore, in Figure 36, each solid line represents a stereo pair of audio signals. The corresponding channel numbers are written above the lines. The dotted lines at the bottom of the diagram represent clock signals. The two large gray boxes represent the flexible audio routing matrix, in which one-to-one connections can be made between any input and any output. The signal routing is fully implemented in hardware.

System Delay

Routing data through the serial ports, routing matrix, ASRCs, and DSP core results in a brief delay between the time when an audio sample is input to the IC and when it is output. If the DSP is programmed to simply pass serial inputs to serial outputs with no sample rate conversion or additional processing, the minimum observed delay of an audio sample from the SDATA_INx pin to the SDATA_OUTx pin is equal to four sample periods. At a sample rate of 48 kHz, this corresponds to 83 µs. The system delay increases as sample rate conversion or additional processing is implemented in the system.

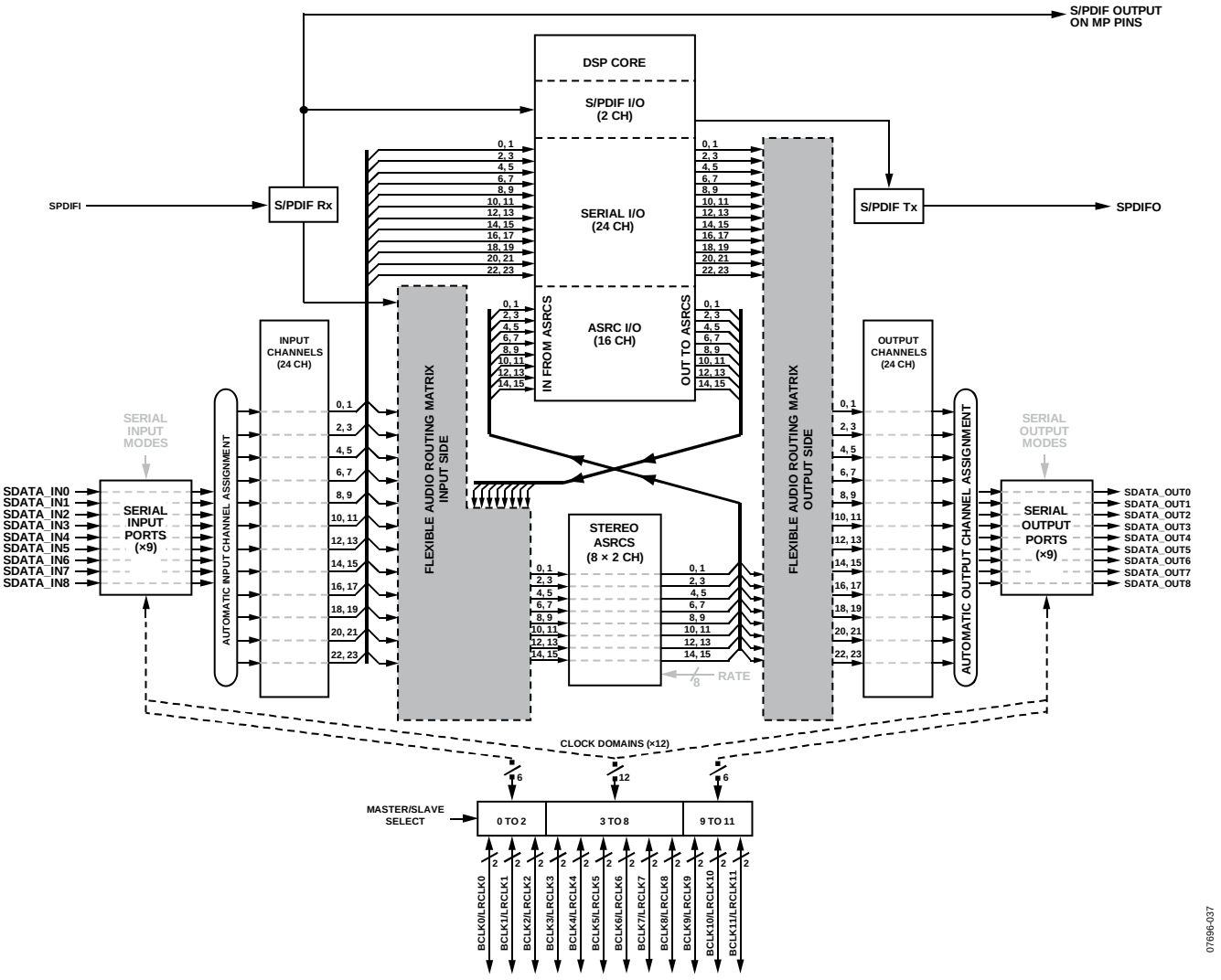


Figure 36. Routing Matrix Block Diagram

Routing Matrix Functionality

Serial Input Ports

The far left side of Figure 36 represents the audio input pins to the ADAU1442/ADAU1445/ADAU1446, namely SDATA_IN0 to SDATA_IN8 and SPDIFI. The serial audio data signals can be represented in any standard mode, including time division multiplexing (TDM) modes, as detailed in the Serial Data Input/Output section. After passing through the serial input ports, the signals undergo an automatic input channel assignment procedure.

Automatic Input Channel Assignment

The serial input ports can handle up to nine input signals. A standard data format is I²S (inter-IC sound), which contains both the left and right channels of a stereo pair. However, some of the signals input to the serial input ports may contain data, in TDM format, for more than two channels. The input to the FARM allows for 24 channels, or 12 stereo pairs. Therefore, a method is required to decompose nine signals (containing two or more channels) into 12 stereo audio channel pairs. This is accomplished by the automatic input channel assignment block. In sequential order, each input signal is appropriated by a number of input channels that corresponds to its channel content.

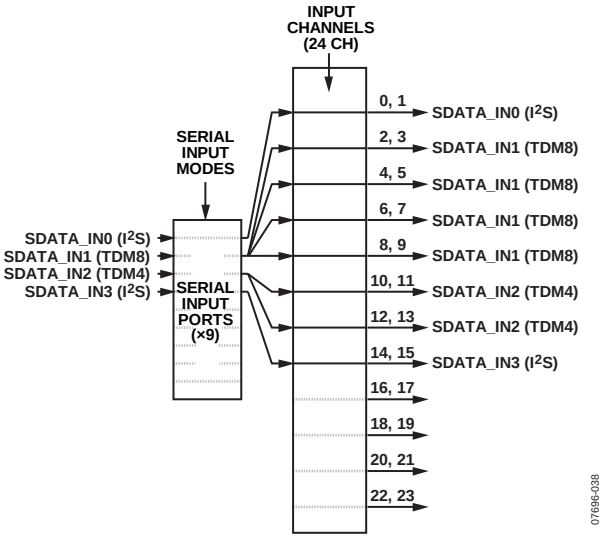


Figure 37. Automatic Input Channel Assignment Example

In the example shown in Figure 37, there are four input signals to the serial input ports: SDATA_IN0 (I²S), SDATA_IN1 (TDM8), SDATA_IN2 (TDM4), and SDATA_IN3 (I²S). SDATA_IN0, containing two channels (I²S), is routed to Input Channel 0 and Input Channel 1. SDATA_IN1, containing eight channels (TDM8), is routed sequentially to the 2, 3, 4, 5, 6, 7, 8, and 9 input channels. SDATA_IN2, containing two stereo pairs (TDM4), is routed sequentially to the 10, 11, 12, and 13 input channels. Finally, SDATA_IN3, containing two channels (I²S), is routed to Input Channel 14 and Input Channel 15.

In this way, the input channels are filled automatically according to the inputs and modes seen on the serial input ports.

When a pin is skipped, it is assigned to input channels regardless, so care must be taken to select the proper input channels within the DSP. Automatic channel assignment is entirely based on the mode settings for a particular serial port; therefore, a port set to a 2-channel mode is assigned to two sequential input channels, and a port set to a 4-channel mode is assigned to four sequential input channels, and so on. Figure 38 shows an example in which several pins are disconnected in hardware and the corresponding empty input channels are automatically assigned.

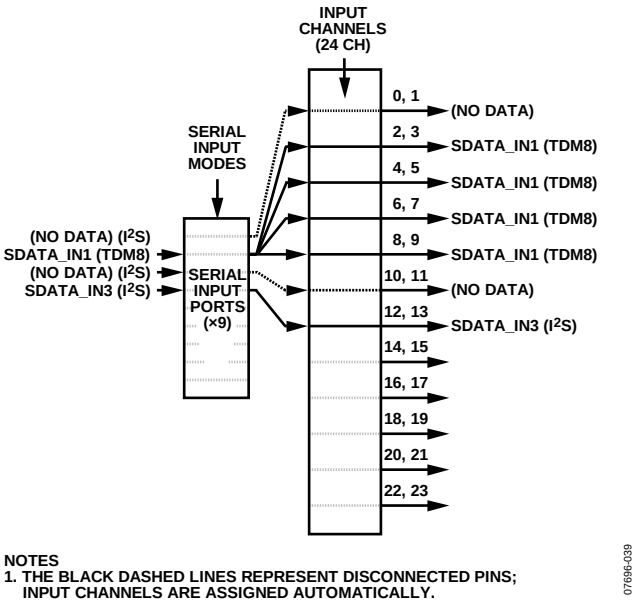


Figure 38. Automatic Input Channel Assignment Example with Skipped Pins

Flexible Audio Routing Matrix—Input Side

Up until this point in the audio signal flow, all signals can be asynchronous to each other. However, before entering the DSP for processing, the signals must be synchronized to the same clock. Therefore, on the input side of the routing matrix, the input channels can be routed, if desired, to the ASRCs for sample rate conversion. The input side of the routing matrix is represented in Figure 39 as a large gray box.

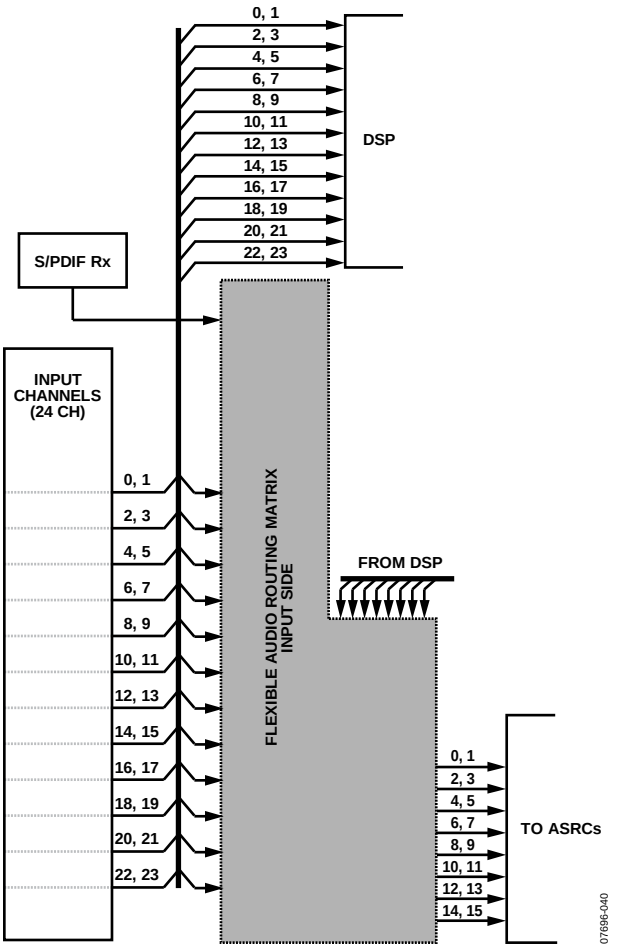


Figure 39. Flexible Audio Routing Matrix—Input Side

As shown in Figure 39, Input Channels[23:0] are hardwired to DSP Inputs[23:0]. However, Input Channels[23:0] are also available at the input side of FARM to be routed to the ASRCs.

Note that there are 13 channel pairs available on the left side of FARM (12 input channel pairs and one S/PDIF Rx pair) and eight channel pairs coming from the top (DSP-to-ASRC pairs). These make up the 21 input channel pairs available to the input side of the routing matrix. In the lower right, there are eight channel pairs output from the routing matrix (inputs to the ASRCs). These make up the eight output channel pairs available to the input side of the routing matrix. Because audio is always routed in pairs, a one-to-one connection can be made between any input pair and any output pair. Therefore, any input channel pair, S/PDIF Rx channel pair, or DSP-to-ASRC channel pair can be connected to any ASRC input pair. Any combination is possible, as long as a one-to-one relationship is maintained.

Note that most applications require sample rate conversion of the S/PDIF Rx signal.

In the case of the ADAU1442, there are eight 2-channel ASRCs. Therefore, Stereo ASRC Input Pair 0 (composed of Channel 0 and Channel 1) corresponds to the first ASRC (Stereo ASRC 0). Stereo ASRC Input Pair 1 (composed of Channel 2 and Channel 3) corresponds to the second ASRC (Stereo ASRC 1). Stereo ASRC Input Pair 2 (composed of Channel 4 and Channel 5) corresponds to the third ASRC (Stereo ASRC 2). Stereo ASRC Input Pair 3 (composed of Channel 6 and Channel 7) corresponds to the fourth ASRC (Stereo ASRC 3). Stereo ASRC Input Pair 4 (composed of Channel 8 and Channel 9) corresponds to the fifth ASRC (Stereo ASRC 4). Stereo ASRC Input Pair 5 (composed of Channel 10 and Channel 11) corresponds to the sixth ASRC (Stereo ASRC 5). Stereo ASRC Input Pair 6 (composed of Channel 12 and Channel 13) corresponds to the seventh ASRC (Stereo ASRC 6). Stereo ASRC Input Pair 7 (composed of Channel 14 and Channel 15) corresponds to the eighth ASRC (Stereo ASRC 7).

In the case of the ADAU1445, there are two 8-channel ASRCs. Therefore, Stereo ASRC Input Pairs[3:0] (composed of Channel 0 to Channel 7) correspond to the first ASRC (Stereo ASRC[3:0]) and must be synchronous to each other. Stereo ASRC Input Pairs[7:4] (composed of Channel 8 to Channel 15) correspond to the second ASRC (Stereo ASRC[7:4]), and must be synchronous to each other.

In the case of the ADAU1446, there are no sample rate converters; therefore, after the automatic channel assignment, the stereo input pairs are hardwired to the DSP core and the input side of the routing matrix is not used. This is shown in Figure 40.

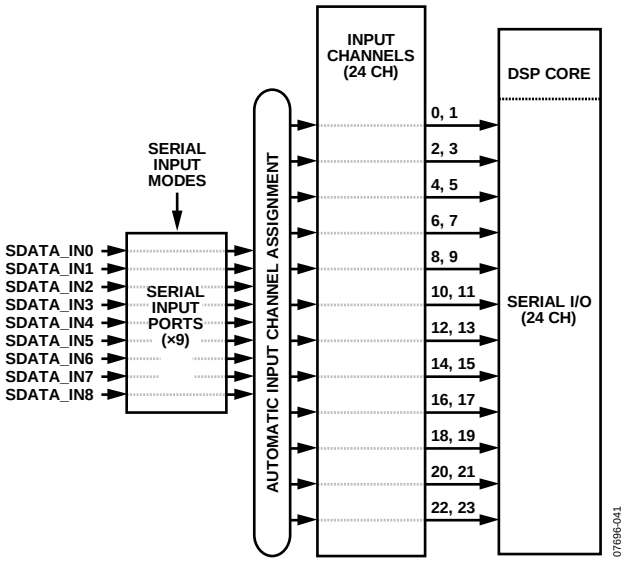


Figure 40. Input Routing in the ADAU1446

Stereo ASRC Routing Overview

Within the ADAU1442 and ADAU1445, signals are required to be synchronous to the master clock only when they are within the DSP core itself. At all other times, signals can be asynchronous to one another and the core. This is illustrated in Figure 42. Because the ADAU1446 has no ASRCs, all audio signals must be synchronous at all times.

The stereo ASRCs allow asynchronous signals to be converted for processing in the DSP.

The input to an ASRC can come from one of 21 sources: the 12 input channel pairs, the S/PDIF Rx pair, or the eight DSP-to-ASRC pairs. This allows the ASRCs to be placed both before and after the DSP. Figure 43 and Figure 44 show examples of how the ASRCs can be used both before and after the DSP.

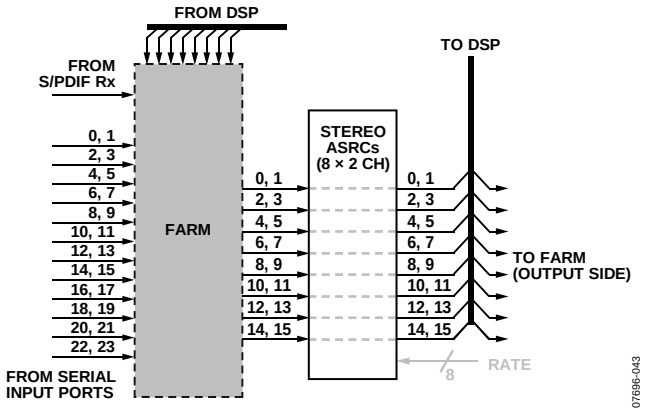


Figure 41. Stereo ASRC Routing

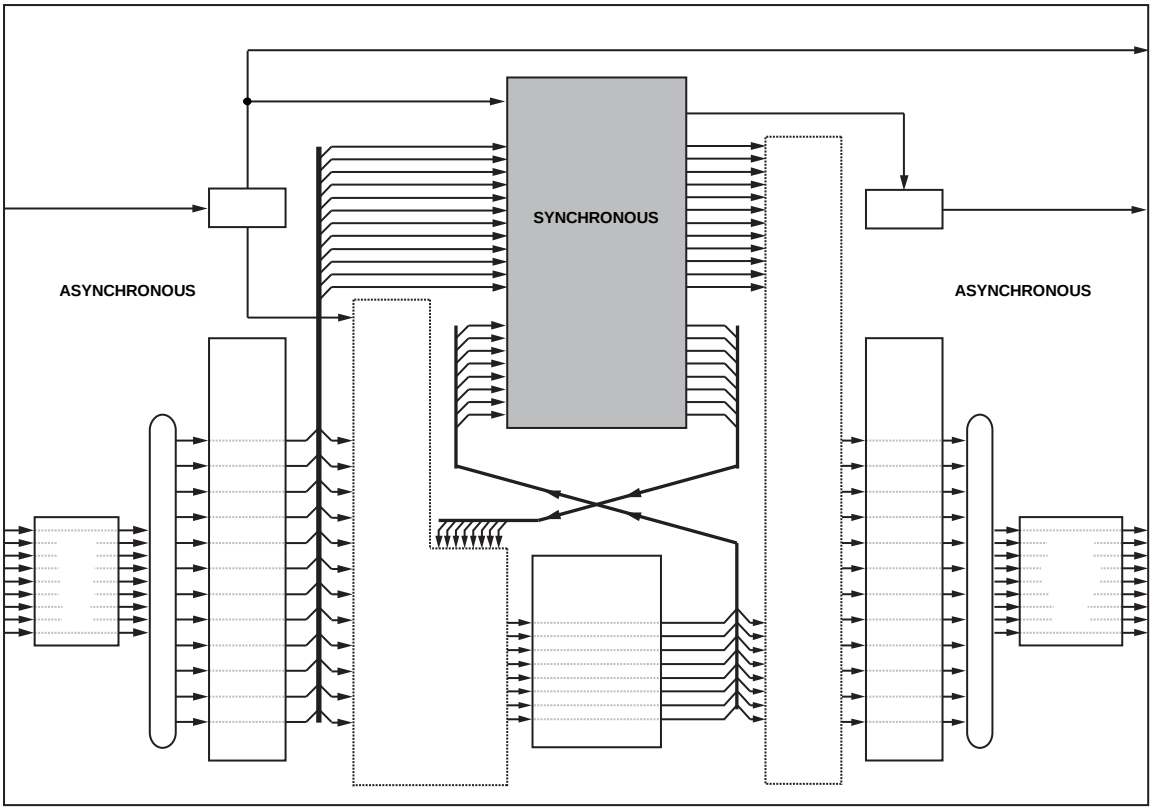


Figure 42. Synchronous and Asynchronous Zones of the ADAU1442 and ADAU1445

Sample Rate Conversion Before the DSP

If asynchronous input signals are present in the system, they must be routed through the ASRC before being processed by the DSP. This is made possible by routing the asynchronous signals through the input side of the routing matrix to the ASRC inputs. This is illustrated in Figure 43.

In such a situation, the ASRC target sample rate should be set synchronous to the DSP. After conversion, the signals are passed to the DSP and are then available in SigmaStudio in the ASRC input cell.

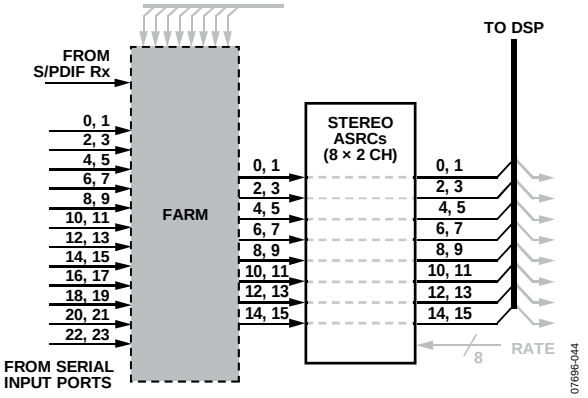


Figure 43. Routing Asynchronous Input Signals to DSP Inputs

Sample Rate Conversion After the DSP

After processing signals in the DSP, it is sometimes desirable to output them asynchronous to the DSP rate, for example, when an asynchronous external DAC is in the system. This can be accomplished by routing the signals through the input side of the routing matrix from the DSP-to-ASRC pairs to the ASRC inputs. This is illustrated in Figure 44.

In this situation, the ASRC target sample rate can be set to any desired value, and the audio data is sent to the output side of the routing matrix.

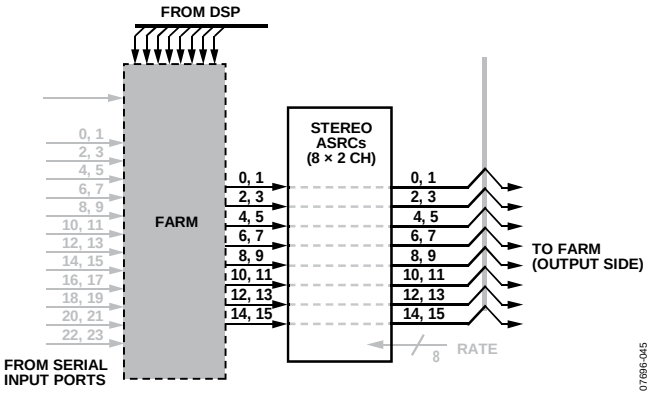


Figure 44. Routing DSP Outputs to Asynchronous Output Signals

DSP Inputs and Outputs

In the DSP, the signals are represented as input and output blocks within the SigmaStudio development tool and then undergo processing as determined by the SigmaStudio schematic. There are 21 input and output channel pairs, as shown in Figure 45. In SigmaStudio, each pair is accessible as individual channels and, therefore, does not need to remain as a pair.

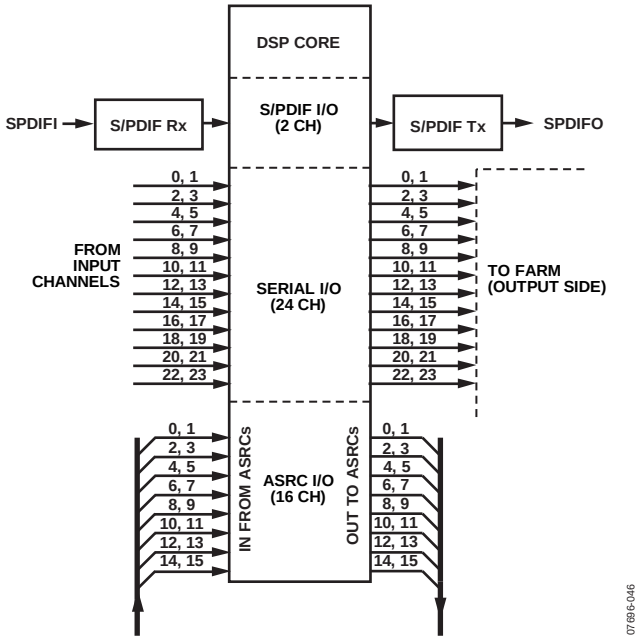


Figure 45. DSP Core Input and Output Signals

Some algorithms running inside the SigmaStudio signal flow may mix or split channels within the DSP. Therefore, the number of output pairs does not necessarily have to equal the number of input pairs.

Note that, while the S/PDIF Rx pair can be routed either to the FARM input side or directly to the DSP, the S/PDIF Tx pair must be routed directly to the S/PDIF output pin (SPDIFO), bypassing the FARM output side.

The ASRC I/O block in Figure 45 represents the interaction between the DSP and the ASRCs. Inputs to the DSP from the ASRCs (ASRC-to-DSP pairs) are represented in SigmaStudio as ASRC input cells, whereas outputs to the ASRCs from the DSP (DSP-to-ASRC pairs) are represented in SigmaStudio as ASRC output cells. The cells are shown in their respective locations in Figure 46.

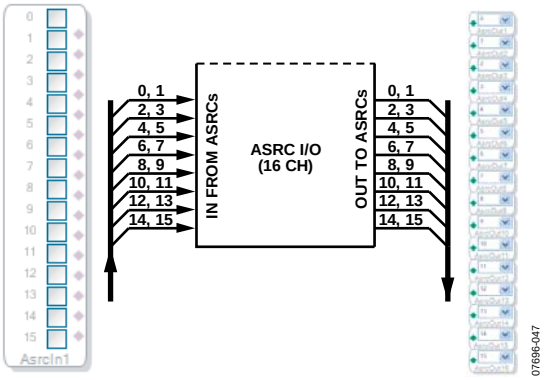


Figure 46. ASRC Input and Output Cells

Flexible Audio Routing Matrix—Output Side

Much like the input side, the output side of the flexible audio routing matrix takes several stereo pairs, which can be asynchronous, and connects them to the 12 stereo pairs that are output from the chip on the serial output ports. The connections must again be one-to-one, meaning that from the 20 possible stereo pairs entering the FARM output side, only 12 can be selected to output from the chip. This process is represented in Figure 47 as a large gray box.

The outputs from the ASRCs are automatically connected to both the DSP and to the FARM output sides.

Note that on the output side, unlike on the input side, the DSP outputs are not hardwired to the output channels.

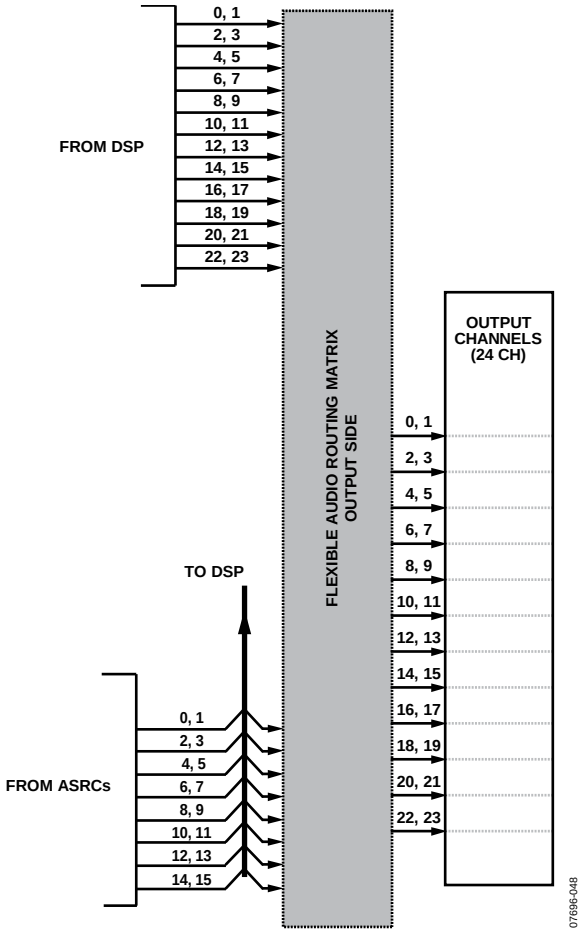


Figure 47. Flexible Audio Routing Matrix—Output Side

Automatic Output Channel Assignment

From the 24 output channels, there are nine serial output ports available to output the data. By selecting different output modes, the user can output the data in the desired format. After the modes are selected for each serial output port, the output channels are automatically assigned to sequentially corresponding serial output ports according to the number of channels desired in the stream. For clarification, see Figure 48.

In this example, 14 output channels must be output on three serial output ports. To accomplish this, serial output modes must be chosen to fit the desired system. In this case, SDATA_OUT0 is set to TDM8 mode, SDATA_OUT1 is set to I²S mode, and SDATA_OUT2 is set to TDM4 mode. Using this information, the automatic output channel assignment algorithm routes Output Channels[7:0] to SDATA_OUT0, Output Channels[9:8] to SDATA_OUT1, and Output Channels[13:10] to SDATA_OUT2. Note that output channels must be assigned sequentially, and no pair can be skipped. If an output channel is left empty (that is, no data is routed to it from the ASRCs or DSP), it is still assigned to a serial output port.

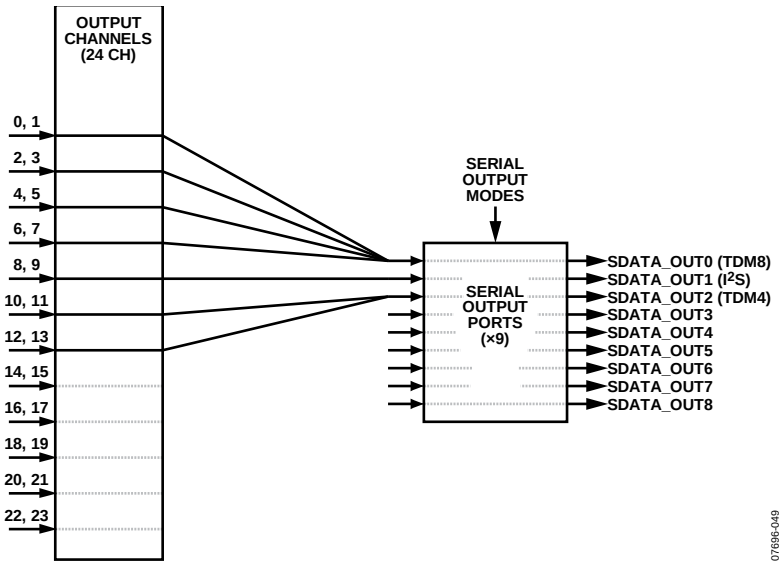


Figure 48. Automatic Output Channel Assignment Example

FLEXIBLE AUDIO ROUTING MATRIX MODES AND SETTINGS

Table 32. Addresses of Flexible Audio Routing Matrix Modes Registers

Address			
Decimal	**Hex**	**Name**	**Read/Write Word Length**
57472	E080	ASRC input select, Pair 0 (Channel 0, Channel 1)	16 bits (2 bytes)
57473	E081	ASRC input select, Pair 1 (Channel 2, Channel 3)	16 bits (2 bytes)
57474	E082	ASRC input select, Pair 2 (Channel 4, Channel 5)	16 bits (2 bytes)
57475	E083	ASRC input select, Pair 3 (Channel 6, Channel 7)	16 bits (2 bytes)
57476	E084	ASRC input select, Pair 4 (Channel 8, Channel 9)	16 bits (2 bytes)
57477	E085	ASRC input select, Pair 5 (Channel 10, Channel 11)	16 bits (2 bytes)
57478	E086	ASRC input select, Pair 6 (Channel 12, Channel 13)	16 bits (2 bytes)
57479	E087	ASRC input select, Pair 7 (Channel 14, Channel 15)	16 bits (2 bytes)
57480	E088	ASRC output rate select, Pair 0 (Channel 0, Channel 1)	16 bits (2 bytes)
57481	E089	ASRC output rate select, Pair 1 (Channel 2, Channel 3)	16 bits (2 bytes)
57482	E08A	ASRC output rate select, Pair 2 (Channel 4, Channel 5)	16 bits (2 bytes)
57483	E08B	ASRC output rate select, Pair 3 (Channel 6, Channel 7)	16 bits (2 bytes)
57484	E08C	ASRC output rate select, Pair 4 (Channel 8, Channel 9)	16 bits (2 bytes)
57485	E08D	ASRC output rate select, Pair 5 (Channel 10, Channel 11)	16 bits (2 bytes)
57486	E08E	ASRC output rate select, Pair 6 (Channel 12, Channel 13)	16 bits (2 bytes)
57487	E08F	ASRC output rate select, Pair 7 (Channel 14, Channel 15)	16 bits (2 bytes)
57488	E090	Serial output select, Pair 0 (Channel 0, Channel 1)	16 bits (2 bytes)
57489	E091	Serial output select, Pair 1 (Channel 2, Channel 3)	16 bits (2 bytes)
57490	E092	Serial output select, Pair 2 (Channel 4, Channel 5)	16 bits (2 bytes)
57491	E093	Serial output select, Pair 3 (Channel 6, Channel 7)	16 bits (2 bytes)
57492	E094	Serial output select, Pair 4 (Channel 8, Channel 9)	16 bits (2 bytes)
57493	E095	Serial output select, Pair 5 (Channel 10, Channel 11)	16 bits (2 bytes)
57494	E096	Serial output select, Pair 6 (Channel 12, Channel 13)	16 bits (2 bytes)
57495	E097	Serial output select, Pair 7 (Channel 14, Channel 15)	16 bits (2 bytes)
57496	E098	Serial output select, Pair 8 (Channel 16, Channel 17)	16 bits (2 bytes)
57497	E099	Serial output select, Pair 9 (Channel 18, Channel 19)	16 bits (2 bytes)
57498	E09A	Serial output select, Pair 10 (Channel 20, Channel 21)	16 bits (2 bytes)
57499	E09B	Serial output select, Pair 11 (Channel 22, Channel 23)	16 bits (2 bytes)

ASRC Input Select Pairs[7:0] Registers (Address 0xE080 to Address 0xE087)

The inputs to each of the eight ASRCs can come from any stereo pair from either the serial input channels or the DSP core.

In the case of the ADAU1442, each input to the stereo ASRCs can receive a separate data input.

In the case of the ADAU1445, each input to the stereo ASRCs can receive a separate data input; however, all inputs to Stereo ASRC[3:0] must be synchronous to each other, and all inputs to Stereo ASRC[7:4] must be synchronous to each other. The first group of ASRCs (Stereo ASRC[3:0]) takes its input rate from the Stereo ASRC 0 input, and the second group of ASRCs (Stereo ASRC[7:4]) takes its input rate from Stereo ASRC 4 input.

In the case of the ADAU1446, which contains no ASRCs, these registers do not affect system operation in any way and can be ignored.

Table 33. Bit Descriptions of ASRC Input Select Pairs[7:0] Registers

Bit Position	Description	Default
[15:6]	Reserved	
[5:0]	ASRC input data selector 000000 = Serial Input Pair 0 (Channel 0, Channel 1) 000001 = Serial Input Pair 1 (Channel 2, Channel 3) 000010 = Serial Input Pair 2 (Channel 4, Channel 5) 000011 = Serial Input Pair 3 (Channel 6, Channel 7) 000100 = Serial Input Pair 4 (Channel 8, Channel 9) 000101 = Serial Input Pair 5 (Channel 10, Channel 11) 000110 = Serial Input Pair 6 (Channel 12, Channel 13) 000111 = Serial Input Pair 7 (Channel 14, Channel 15) 001000 = Serial Input Pair 8 (Channel 16, Channel 17) 001001 = Serial Input Pair 9 (Channel 18, Channel 19) 001010 = Serial Input Pair 10 (Channel 20, Channel 21) 001011 = Serial Input Pair 11 (Channel 22, Channel 23) 010000 = DSP-to-ASRC Pair 0 (Channel 0, Channel 1) 010001 = DSP-to-ASRC Pair 1 (Channel 2, Channel 3) 010010 = DSP-to-ASRC Pair 2 (Channel 4, Channel 5) 010011 = DSP-to-ASRC Pair 3 (Channel 6, Channel 7) 010100 = DSP-to-ASRC Pair 4 (Channel 8, Channel 9) 010101 = DSP-to-ASRC Pair 5 (Channel 10, Channel 11) 010110 = DSP-to-ASRC Pair 6 (Channel 12, Channel 13) 010111 = DSP-to-ASRC Pair 7 (Channel 14, Channel 15) 100000 = S/PDIF Receiver Pair 0 (Channel 0, Channel 1) 111111 = no data	111111

ASRC Input Data Selector Bits (Bits[5:0])

As shown in Figure 49, the gray box representing the input side of the flexible audio routing matrix can be thought of as a multiplexer. Any input to the box can make a one-to-one connection to any output from the box. The inputs are the Serial Input Pairs[11:0] and the DSP-to-ASRC Pairs[7:0]. The outputs from FARM are the Stereo ASRC[7:0] inputs.

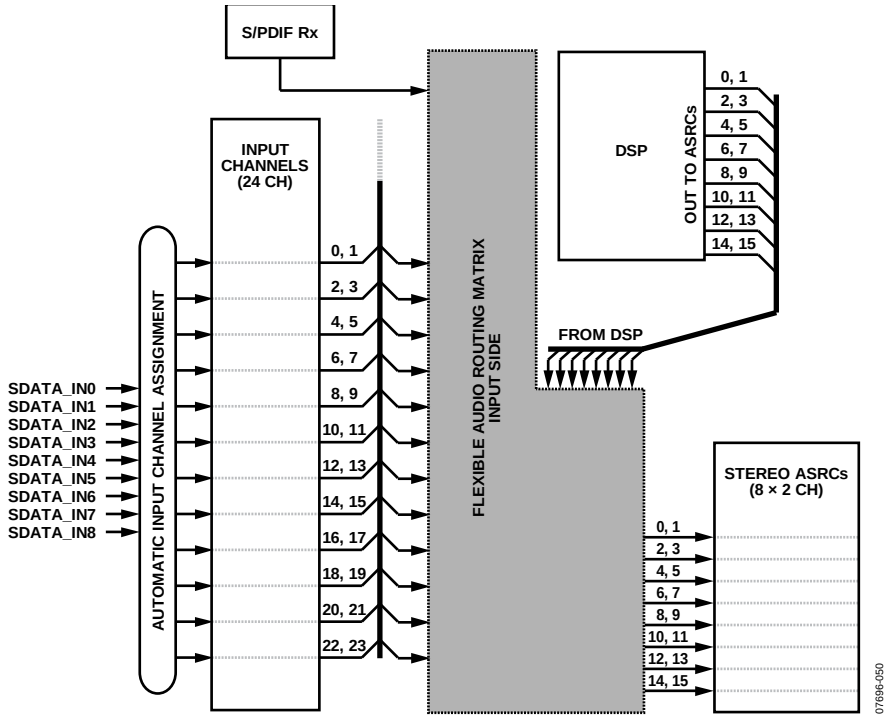


Figure 49. ASRC Input Select

ASRC Output Rate Select Pairs[7:0] Registers (Address 0xE088 to Address 0xE08F)

Table 34. Bit Descriptions of ASRC Output Rate Select Pairs[7:0] Registers

Bit Position	Description	Default
[15:6]	Reserved	
[5:0]	ASRC output rate 000000 = Serial Output Pair 0 (Channel 0, Channel 1) 000001 = Serial Output Pair 1 (Channel 2, Channel 3) 000010 = Serial Output Pair 2 (Channel 4, Channel 5) 000011 = Serial Output Pair 3 (Channel 6, Channel 7) 000100 = Serial Output Pair 4 (Channel 8, Channel 9) 000101 = Serial Output Pair 5 (Channel 10, Channel 11) 000110 = Serial Output Pair 6 (Channel 12, Channel 13) 000111 = Serial Output Pair 7 (Channel 14, Channel 15) 001000 = Serial Output Pair 8 (Channel 16, Channel 17) 001001 = Serial Output Pair 9 (Channel 18, Channel 19) 001010 = Serial Output Pair 10 (Channel 20, Channel 21) 001011 = Serial Output Pair 11 (Channel 22, Channel 23) 010000 = DSP rate 010001 = internal $f_{S,NORMAL}$ rate 010010 = internal $f_{S,DUAL}$ rate 010011 = internal $f_{S,QUAD}$ rate 111111 = no rate	111111

ASRC Output Rate Bits (Bits[5:0])

These bits select the output conversion rate for the eight ASRCs. Any asynchronous input to the ASRC is output at this rate. It can be set by one of the 12 serial output channel pairs' f_S clock signals (the LRCLK associated with their automatically assigned serial port) or by the core's $f_{S,NORMAL}$, $f_{S,DUAL}$, or $f_{S,QUAD}$ clock signals.

In the case of the ADAU1442, each output from the stereo ASRCs can have a separate data output.

In the case of the ADAU1445, each output from the stereo ASRCs can have a separate data output; however, all outputs from Stereo ASRC[3:0] must be synchronous to each other, and all outputs from Stereo ASRC[7:4] must be synchronous to each other. The first group of ASRCs (Stereo ASRC[3:0]) takes its output rate from the setting on the Stereo ASRC 0 output. The output rate for Stereo ASRC[3:1] is automatically set to this rate, ignoring the settings for the Stereo ASCR[3:1] outputs. The second group of ASRCs (Stereo ASRC[7:4]) takes its output rate from the setting on the Stereo ASRC 4 output. The output rate for Stereo ASRC[7:5] is automatically set to this rate, ignoring the settings for the Stereo ASRC[7:5] outputs.

In the case of the ADAU1446, which contains no ASRCs, these registers do not affect system operation in any way and can be ignored.

Serial Output Select Pairs[11:0] Registers (Address 0xE090 to Address 0xE09B)

Table 35. Bit Descriptions of Serial Output Select Pairs[11:0] Registers

Bit Position	Description	Default
[15:6]	Reserved	
[5:0]	Serial output data selector 010000 = DSP Output Pair 0 (Channel 0, Channel 1) 010001 = DSP Output Pair 1 (Channel 2, Channel 3) 010010 = DSP Output Pair 2 (Channel 4, Channel 5) 010011 = DSP Output Pair 3 (Channel 6, Channel 7) 010100 = DSP Output Pair 4 (Channel 8, Channel 9) 010101 = DSP Output Pair 5 (Channel 10, Channel 11) 010110 = DSP Output Pair 6 (Channel 12, Channel 13) 010111 = DSP Output Pair 7 (Channel 14, Channel 15) 011000 = DSP Output Pair 8 (Channel 16, Channel 17) 011001 = DSP Output Pair 9 (Channel 18, Channel 19) 011010 = DSP Output Pair 10 (Channel 20, Channel 21) 011011 = DSP Output Pair 11 (Channel 22, Channel 23) 100000 = ASRC Output Pair 0 (Channel 0, Channel 1) 100001 = ASRC Output Pair 1 (Channel 2, Channel 3) 100010 = ASRC Output Pair 2 (Channel 4, Channel 5) 100011 = ASRC Output Pair 3 (Channel 6, Channel 7) 100100 = ASRC Output Pair 4 (Channel 8, Channel 9) 100101 = ASRC Output Pair 5 (Channel 10, Channel 11) 100110 = ASRC Output Pair 6 (Channel 12, Channel 13) 100111 = ASRC Output Pair 7 (Channel 14, Channel 15) 111111 = no data	111111

Serial Output Data Selector Bits (Bits[5:0])

These bits select where each of the 12 stereo serial output channels comes from. The channels can come either from one of the 12 DSP core stereo outputs or from one of the eight ASRC stereo outputs.

In the case of the ADAU1446, setting the serial output data selector bits to a value corresponding to an ASRC output pair yields no data.

As shown in Figure 50, the stereo output pairs can come from any of the DSP serial or ASRC outputs.

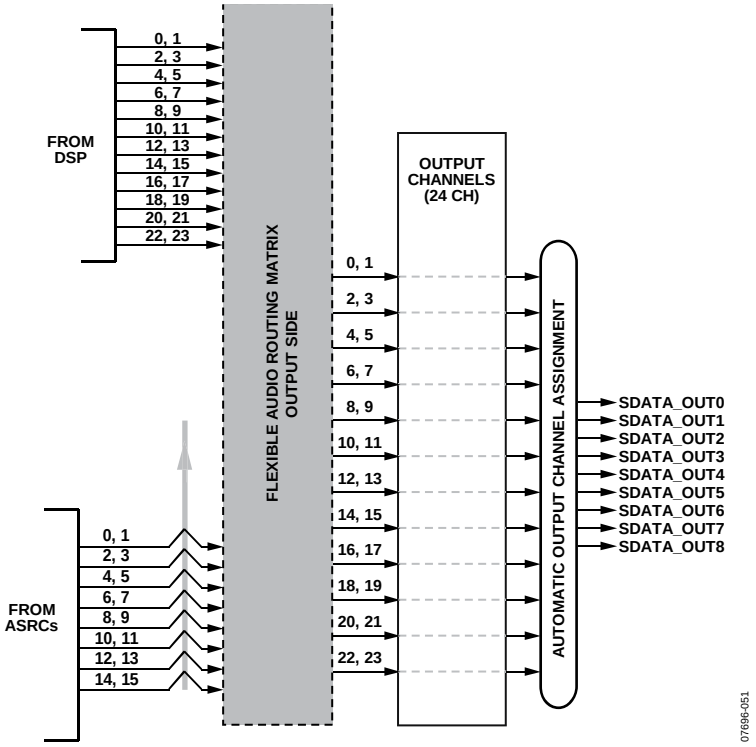


Figure 50. Serial Output Select Pair

ASYNCHRONOUS SAMPLE RATE CONVERTERS

The integrated sample rate converters of the ADAU1442/ADAU1445 processors can be configured in various ways to facilitate asynchronous connectivity to other components in the audio system. The sample rate converters operate completely independent of the serial ports and DSP core, connecting via the flexible audio routing matrix.

ASRC MODES AND SETTINGS

Table 36. Addresses of ASRC Modes Registers

Address			
Decimal	**Hex**	**Name**	**Read/Write Word Length**
57601	E101	Stereo ASRC[3:0] lock status and mute	16 bits (2 bytes)
57603	E103	Stereo ASRC[3:0] mute ramp disable	16 bits (2 bytes)
57665	E141	Stereo ASRC[7:4] lock status and mute	16 bits (2 bytes)
57667	E143	Stereo ASRC[7:4] mute ramp disable	16 bits (2 bytes)

Stereo ASRC[3:0] Lock Status and Mute Register (Address 0xE101)

Table 37. Bit Descriptions of Register 0xE101

Bit Position	Description	Default
[15:12]	Reserved	
11	Stereo ASRC 3 (Channel 6, Channel 7) lock status (read only)	0
10	Stereo ASRC 2 (Channel 4, Channel 5) lock status (read only)	0
9	Stereo ASRC 1 (Channel 2, Channel 3) lock status (read only)	0
8	Stereo ASRC 0 (Channel 0, Channel 1) lock status (read only)	0
[7:4]	Reserved	
3	Stereo ASRC 3 (Channel 6, Channel 7) mute	0
2	Stereo ASRC 2 (Channel 4, Channel 5) mute	0
1	Stereo ASRC 1 (Channel 2, Channel 3) mute	0
0	Stereo ASRC 0 (Channel 0, Channel 1) mute	0

Every sample rate converter pair for Stereo ASRC[3:0] can be muted. This function is controlled by a single 12-bit register. The mute bits (Bits[3:0]) are active high; therefore, a value of 1 mutes the corresponding ASRC, and a value of 0 unmutes the corresponding ASRC. The muting is done with a volume ramp and is click and pop free. If desired, the mute ramp can be disabled (see the Stereo ASRC[3:0] Mute Ramp Disable Register (Address 0xE103) section).

When the device is powered up and brought out of reset, the ASRC lock bits default to a value of 0. When the master clocks to the ASRC are enabled (see the Master Clock Enable Switch Register (Address 0xE280) section), the corresponding ASRC lock bits are set to 1, and the outputs are automatically muted.

When an ASRC's output rate is set (see the ASRC Output Rate Select Pairs[7:0] Registers (Address 0xE088 to Address 0xE08F) section) and it locks to a valid output clock, the corresponding lock bit changes from 1 to 0. This signifies that the ASRC has found the target clock rate and locked to it. From that moment onward, the lock bit remains at 0 until the device is reset. Changing the target rate setting or removing the output clock from the ASRC will not cause its lock bit to change from 0 back to 1.

In the case of the ADAU1446, setting these registers does not affect system operation in any way.

Stereo ASRC[3:0] Mute Ramp Disable Register (Address 0xE103)

Table 38. Bit Descriptions of Register 0xE103

Bit Position	Description	Default
[15:1]	Reserved	
0	Stereo ASRC[3:0] (Channels[7:0]) mute ramp disable 0 = enable ramp 1 = disable ramp	0

This single-bit register controls the mute behavior of Stereo ASRC[3:0] (Channels[7:0]). When Bit 0 is set to the default (0), Stereo ASRC[3:0] (Channels[7:0]) mute with a volume ramp. When Bit 0 is set to 1, Stereo ASRC[3:0] mute abruptly. In addition, setting this bit to 1 ignores the ASRC mute bits (Bits[3:0]) in Register 0xE101 (see the Stereo ASRC[3:0] Lock Status and Mute section); therefore, a mute only occurs on a loss of lock.

In the case of the ADAU1446, setting this register does not affect system operation in any way.

Stereo ASRC[7:4] Lock Status and Mute Register (Address 0xE141)

Table 39. Bit Descriptions of Register 0xE141

Bit Position	Description	Default
[15:12]	Reserved	
11	Stereo ASRC 7 (Channel 14, Channel 15) lock status (read only)	0
10	Stereo ASRC 6 (Channel 12, Channel 13) lock status (read only)	0
9	Stereo ASRC 5 (Channel 10, Channel 11) lock status (read only)	0
8	Stereo ASRC 4 (Channel 8, Channel 9) lock status (read only)	0
[7:4]	Reserved	
3	Stereo ASRC 7 (Channel 14, Channel 15) mute	0
2	Stereo ASRC 6 (Channel 12, Channel 13) mute	0
1	Stereo ASRC 5 (Channel 10, Channel 11) mute	0
0	Stereo ASRC 4 (Channel 8, Channel 9) mute	0

Every sample rate converter pair for Stereo ASRC[7:4]) can be muted. This function is controlled by a single 12-bit register. The mute bits (Bits[3:0]) are active high; therefore, a value of 1 mutes the corresponding ASRC, and a value of 0 unmutes the corresponding ASRC. The muting is done with a volume ramp and is click and pop free. If desired, the mute ramp can be disabled (see the Stereo ASRC[7:4] Mute Ramp Disable Register (Address 0xE143) section).

When the device is powered up and brought out of reset, the ASRC lock bits default to a value of 0. When the master clocks to the ASRC are enabled (see the Master Clock Enable Switch Register (Address 0xE280) section), the corresponding ASRC lock bits are set to 1, and the outputs are automatically muted. When an ASRC's output rate is set (see the ASRC Output Rate Select Pairs[7:0] Registers (Address 0xE088 to Address 0xE08F) section) and it locks to a valid output clock, the corresponding lock bit changes from 1 to 0. This signifies that the ASRC has found the target clock rate and locked to it. From that moment onward, the lock bit remains at 0 until the device is reset. Changing the target rate setting or removing the output clock from the ASRC will not cause its lock bit to change from 0 back to 1.

In the case of the ADAU1446, setting these registers does not affect system operation in any way.

Stereo ASRC[7:4] Mute Ramp Disable Register (Address 0xE143)

Table 40. Bit Descriptions of Register 0xE143

Bit Position	Description	Default
[15:1]	Reserved	
0	Stereo ASRC[7:4] (Channels[15:8]) mute ramp disable 0 = enable ramp 1 = disable ramp	0

This single-bit register controls the mute behavior of Stereo ASRC[7:4] (Channels[15:8]). When Bit 0 is set to the default (0), Stereo ASRC[7:4] (Channels[15:8]) mute with a volume ramp. When Bit 0 is set to 1, Stereo ASRC[7:4] mute abruptly. In addition, setting this bit to 1 ignores the ASRC mute bits (Bits[3:0]) in Register 0xE141 (see the Stereo ASRC[7:4] Lock Status and Mute Register (Address 0xE141) section); therefore, a mute only occurs on a loss of lock.

In the case of the ADAU1446, setting this register does not affect system operation in any way.

DSP CORE

The DSP core performs calculations on audio data as specified by the instruction codes stored in program RAM. Because SigmaStudio generates the instructions, it is not necessary to have a detailed knowledge of the DSP core to use the SigmaDSP, but a brief description is provided in this section.

Architecture

The core consists of a simple 28-/56-bit multiply-accumulate unit (MAC) with two sources: a data source and a coefficient source. The data source can come from the data RAM, a ROM table of commonly used constant values, or the audio inputs to the core. The coefficient source can come from the parameter RAM, a ROM table of commonly used constant values. The two sources are multiplied in a 28-bit fixed-point multiplier, and then the signal is input to the 56-bit adder; the result is usually stored in one of three 56-bit accumulator registers. The accumulators can be output from the core (in 28-bit format) or can optionally be written back into the data or parameter RAMs.

Features

The SigmaDSP core is designed specifically for audio processing and, therefore, includes several features intended for maximizing efficiency. These include hardware decibel conversion and audio-specific ROM constants.

Signal Processing

The ADAU1442/ADAU1445/ADAU1446 are designed to provide all signal processing functions commonly used in stereo or multichannel playback systems. The signal processing flow is designed using SigmaStudio software from Analog Devices. This software allows graphical entry and real-time control of all signal processing functions.

Many of the signal processing functions are coded using full, 56-bit, double-precision arithmetic. The serial port input and output word lengths are 24 bits, but four extra headroom bits are used in the processor to allow internal gains of up to 24 dB without clipping. Additional gains can be achieved by initially scaling down the input signal in the DSP signal flow.

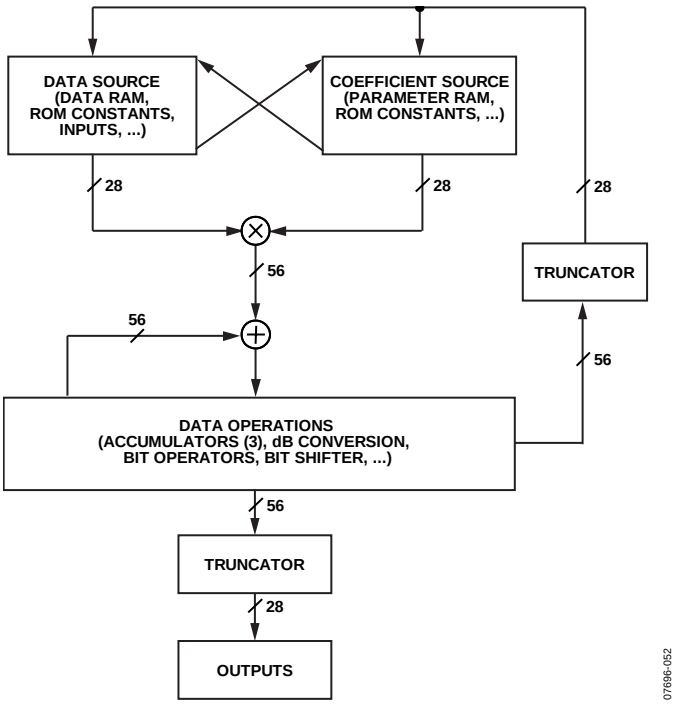


Figure 51. Simplified Core Architecture

Numeric Formats

DSP systems commonly use a standard numeric format. Fractional number systems are specified by an A.B format, where A is the number of bits to the left of the decimal point and B is the number of bits to the right of the decimal point.

The ADAU1442/ADAU1445/ADAU1446 use the same numeric format for both the parameter and data values. The format is as shown in the Numerical Format: 5.23 section.

Numerical Format: 5.23

Linear range: –16.0 to (+16.0 – 1 LSB)

Examples:
1000 0000 0000 0000 0000 0000 0000 = –16.0
1110 0000 0000 0000 0000 0000 0000 = –4.0
1111 1000 0000 0000 0000 0000 0000 = –1.0
1111 1110 0000 0000 0000 0000 0000 = –0.25

1111 1111 0011 0011 0011 0011 0011 = –0.1
1111 1111 1111 1111 1111 1111 1111 = (1 LSB below 0.0)
0000 0000 0000 0000 0000 0000 0000 = 0.0

0000 0000 1100 1100 1100 1100 1101 = 0.1
0000 0010 0000 0000 0000 0000 0000 = 0.25
0000 1000 0000 0000 0000 0000 0000 = 1.0
0010 0000 0000 0000 0000 0000 0000 = 4.0
0111 1111 1111 1111 1111 1111 1111 = (16.0 – 1 LSB).

The serial port accepts up to 24 bits of input and is sign-extended to the full 28 bits of the DSP core. This allows internal gains of up to 24 dB without encountering internal clipping.

A digital clipper circuit is used within the DSP core before outputting to the serial port outputs, ASRCs, and S/PDIF transmitter (see Figure 52). This clips the top four bits of the signal to produce a 24-bit output with a range of 1.0 (minus 1 LSB) to –1.0. Figure 52 shows the maximum signal levels at each point in the data flow in both binary and decibel levels.

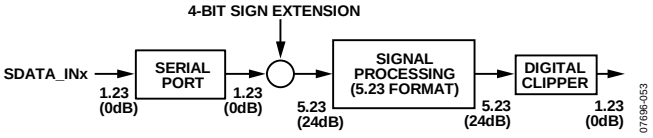


Figure 52. Numeric Precision and Clipping Structure (TBD)

Programming

On power-up, the ADAU1442/ADAU1445/ADAU1446 have no default program loaded. There are 3584 instruction cycles per audio sample, resulting in an internal clock rate of 172.032 MHz when $f_{S,NORMAL}$ is 48 kHz. The DSP runs in a stream-oriented manner, meaning that all 3584 instructions are executed each sample period. The ADAU1442/ADAU1445/ADAU1446 can also be set up to accept dual- or quad-speed inputs by reducing the number of instructions per sample. These modes can be set in the core control register.

The ADAU1442/ADAU1445/ADAU1446 can be programmed easily using SigmaStudio, an entirely graphical tool provided by Analog Devices. No knowledge of writing line-level DSP code is required, and the large library of predesigned algorithms should drastically reduce development time. More information on SigmaStudio can be found at the Analog Devices website.

Program Counter

The execution of instructions in the core is governed by a program counter, which sequentially steps through the addresses of the program RAM. The program counter starts every time a new audio frame is clocked into the core. SigmaStudio inserts a jump-to-start command at the end of every program. The program counter increments sequentially until reaching this command, and then jumps to the program start address (Program RAM Address 0x2010) and waits for the next audio frame to clock into the core.

Branching and Looping

Some cells in SigmaStudio can optionally modify the program counter to implement simple branching and looping structures. However, care must be taken that the program counter returns to its starting address before a new frame is clocked. If the new frame starts before the counter has returned to start, the audio output is corrupted, and a reset is necessary.

The software compiler in SigmaStudio calculates the maximum possible program cycles for a given project and generates an error when a user exceeds the allowable limit.

DSP CORE MODES AND SETTINGS

Core Run Register (Address 0xE228)

Table 41. Descriptions of Register 0xE228

Bit Position	Description	Default
[15:1]	Reserved	
0	Core run bit	0

This single-bit register initiates the run signal to start the core. This should be the very last register that is set when the system is initialized.

Before the core is halted, set the DSP core rate select register (0xE220) to 0x001C. This disables the start pulse to the core.

Before the care is started, set the DSP Core Rate Select register (0xE220) to the desired value. This enables the start pulse to the core. Table 12 contains a list of valid settings.

If the core is halted (that is, if Bit 0 of Register 0xE228 is set to 0) during operation, the serial outputs jump immediately to 0. This ensures that no dc level is left on the serial outputs and helps prevent speaker damage in the system. It also allows the system to mute and unmute all audio channels while minimizing pops and clicks on the outputs.

The core run bit can be used to implement a system mute functionality, as opposed to muting all of the individual channels in software. However, this approach instantaneously mutes the outputs, potentially causing clicks or pops on the output. If a click- and pop-free mute is required, software slew mute cells should be implemented into the DSP core's signal processing flow.

RELIABILITY FEATURES

The ADAU1442/ADAU1445/ADAU1446 contain several subsystems designed to increase the reliability of the system in which they are used. When these functions are used in conjunction with an external host controller device, the DSP can recover from serious errors, such as memory corruption or a program counter crash.

CRC Modes and Settings

Cyclic Redundancy Check (CRC) Registers (Address 0xE200 to Address 0xE202)

Table 42. Register Details of CRC Registers

Address				
Decimal	**Hex**	**Register**	**Function**	**Default**
57856	E200	CRC Ideal Value 1	16 MSBs of the CRC hash sum	0
57857	E201	CRC Ideal Value 2	16 LSBs of the CRC hash sum	0
57858	E202	CRC enable	1-bit CRC enable, active high	0

The CRC constantly checks the validity of the program RAM contents. SigmaStudio generates a 32-bit hash sum when a program is compiled that must be written to two consecutive 16-bit register locations. The CRC must then be enabled. Every 4096 frames (88 ms when $f_{S,NORMAL}$ is 48 kHz), the IC generates its own 32-bit code and compares it with the one stored in these registers. If they do not match, an MP pin is set high (CRC flag). This output flag must be enabled using the output CRC error sticky command in the multipurpose pin control register (see the Multipurpose Pin Control Registers (Address 0xE204 to Address 0xE20F) section).

The user turns this enable on when continuous CRC checking is desired. This defaults to off and can be set high after the user has loaded a program and sent the correct CRC, calculated by SigmaStudio. If there is an error, it can be cleared by setting the enable bit low, fixing the error (presumably by reloading the program) and then setting it high again.

The CRC control registers are configured as follows:

- CRC Ideal Value 1 is the 16 MSBs of the CRC code.
- CRC Ideal Value 2 is the 16 LSBs of the CRC code.
- CRC enable is a 1-bit enable.

The CRC error sticky register is a single-bit read-only register at Address 57893 (Address 0xE225) that acts as the CRC error flag. It can optionally be sent to an MP pin. For example, it can connect to an interrupt pin on an external microcontroller, which triggers a rewrite of the corrupted memory. The register is reset when the CRC enable register goes low.

CRC Error Sticky Register (Address 0xE225)

Table 43. Bit Description of Register 0xE225

Bit Position	Description	Default
[15:1]	Reserved	
0	CRC error sticky (read only)	0

This single-bit read-only register goes high when there is a CRC error. It is reset to 0 when the CRC enable is reset to 0.

Watchdog Modes and Settings

Watchdog Registers (Address 0xE210 to Address 0xE212)

Table 44. Register Details of Watchdog Registers

Address				
Decimal	**Hex**	**Register**	**Function**	**Default**
57872	E210	Watchdog enable	1-bit enable register for watchdog timer	0
57873	E211	Watchdog Value 1	16 MSBs of the watchdog maximum count value	0
57874	E212	Watchdog Value 2	16 LSBs of the watchdog maximum count value	0

A program counter watchdog is used when the core performs block processing (which can span several samples). The watchdog flags an error if the program counter reaches the 32-bit value set in the watchdog value registers. This value consists of two consecutive 16-bit register locations. The error flag sends a high signal to one of the multipurpose pins. The watchdog function must be enabled by setting the single-bit register at Location 57872 high.

The register configuration for the watchdog counter is as follows:

- Watchdog enable is a 1-bit enable.
- Watchdog Value 1 is the 16 MSBs of the watchdog maximum count value.
- Watchdog Value 2 is the 16 LSBs of the watchdog maximum count value.

Table 45. Bit Descriptions of Register 0xE210

Bit Position	Description	Default
[15:1]	Reserved	
0	Watchdog enable	0

Watchdog Error Sticky Register (Address 0xE226)

Table 46. Bit Descriptions of Register 0xE226

Bit Position	Description	Default
[15:1]	Reserved	
0	Watchdog error sticky (read only)	0

This single-bit watchdog error flag goes high when an error occurs. It can optionally be sent to an MP pin, as described in the Multipurpose Pin Control Registers (Address 0xE204 to Address 0xE20F) section. For example, the error flag can connect to an interrupt pin on a microcontroller in the system. It resets to 0 when the watchdog enable is reset to 0.

CRC and Watchdog Mute Register (Address 0xE227)

Table 47. Bit Descriptions of Register 0xE227

Bit Position	Description	Default
[15:2]	Reserved.	
1	A CRC error mutes the core automatically.	0
0	A watchdog error mutes the core automatically.	0

This 2-bit register causes a CRC or watchdog error to automatically mute the core. The default value is off.

RAMS

The ADAU1442/ADAU1445/ADAU1446 have 4k words of program RAM, 4k words of parameter RAM, and 8k words of data RAM.

Program RAM

Table 48. Register Details of Program RAM

Address		Name	Read/Write Word Length
Decimal	Hex		
8192	2000	Program RAM	43 bits (6 bytes)

The program RAM contains the 43-bit operation codes that are executed by the core. It is important to note that although the length of the RAM is 4096, only 3584 instructions can be executed in the span of a single frame for normal rate signals. For dual-rate processing, the maximum allowable instruction count is 1792, and for quad-rate processing, the maximum allowable instruction count is 896. For more information on setting the DSP core rate, see the DSP Core Rate Select Register (Address 0xE220) section.

The additional program space can be used with optimized algorithms and jump commands. The SigmaStudio compiler calculates maximum instructions per frame for a project and generates an error when the value exceeds the maximum allowable instructions per frame based on the sample rate of the signals in the core.

Because the end of a program contains a jump-to-start command, the remaining program RAM space does not need to be filled with no-operation (NOP) commands.

Program Counter Peak Count Register (Address 0xE229)

Table 49. Bit Descriptions of Register 0xE229

Bit Position	Description
[15:0]	Program counter peak count (read only)

This 16-bit, read-only register keeps track of how many cycles elapse from the start of the program until the program counter is reset. The register is updated on every start pulse.

This register should not be used if the watchdog error sticky bit has been activated, which indicates that the maximum allowable clock cycles per frame have been exceeded. In this case, the program counter peak value may be inaccurate.

Parameter RAM

Table 50. Register Details of Parameter RAM

Address		Name	Read/Write Word Length
Decimal	Hex		
0	0000	Parameter RAM	28 bits (4 bytes)

The parameter RAM contains all 28-bit values that are used by algorithms running in the DSP core. SigmaStudio automatically assigns the first eight positions to safeload parameters; therefore, project-specific parameters start at Address 0x0008.

Data RAM

Table 51. Register Details of Data RAM

Address		Name	Read/Write Word Length
Decimal	Hex		
16384	4000	Data RAM	28 bits (4 bytes)

The data RAM stores audio data that must be accessed by the core for more than one frame. Unlike previous generations of SigmaDSP architectures, which used a hardware-based modulo structure, the ADAU1442/ADAU1445/ADAU1446 have a software-based modulo scheme that is controlled by the programmer.

The data RAM should be initialized to all 0s before a boot-up operation is performed to avoid an undefined startup state. SigmaStudio inserts the appropriate data RAM initialization code into projects by default.

Modulo Data Memory Register (Address 0xE21F)

Table 52. Bit Descriptions of Register 0xE21F

Bit Position	Description	Default
[15:14]	Reserved.	
[13:0]	Nonmodulo data memory start. The setting is the address in memory.	01111100000000

This is a single 14-bit register that sets the start of the nonmodulo space of the data memory. The default value is 7936 decimal. SigmaStudio sets this value by default based on the addressing scheme used in the SigmaStudio project. The value should not be modified by the user.

S/PDIF RECEIVER AND TRANSMITTER

The ADAU1442/ADAU1445/ADAU1446 each feature a set of on-chip S/PDIF data ports, which can be wired directly to transmitters and receivers for easy interfacing to other S/PDIF-compatible equipment.

S/PDIF Receiver

The S/PDIF input port is designed to accept both TTL and bipolar signals, provided there is an ac coupling capacitor on the input pin of the chip. Because the S/PDIF input data will most likely be asynchronous to the DSP core, it must be routed through an ASRC.

The S/PDIF ports work with sampling rates between 32 kHz and 108 kHz.

In addition to audio data, S/PDIF streams contain user data, channel status, validity bit, virtual LRCLK, and block start information. The receiver decodes audio data and sends it to the ASRCs and DSP core, but the remaining data passes through directly to the transmitter. This ensures that any user data is unaltered at the output and is reintegrated into the audio stream.

In the ADAU1442/ADAU1445/ADAU1446, clock recovery is entirely digital. As a result, the ADAU1442/ADAU1445/ADAU1446 have better protection against clock jitter.

The ADAU1442/ADAU1445/ADAU1446 S/PDIF ports are designed to meet the following AES and EBU specifications: a jitter of 0.25 UI p-p at 8 kHz and above, a jitter of 10 UI p-p below 200 Hz, and a minimum signal voltage of 200 mV.

To transmit data, the S/PDIF output must be turned on. This is accomplished by writing an activation bit to the S/PDIF transmitter on/off register. More information can be found in the Enable S/PDIF to I²S Output section and the S/PDIF Transmitter—On/Off Switch Register (Address 0xE0C1) section.

Outputting to the Multipurpose Pins

It is possible to send S/PDIF data from the receiver directly to output on the MP pins. This mode is activated in Register 0xE241 (see the Enable S/PDIF to I2S Output section). The pin assignment of signals is shown in Table 53.

Table 53. S/PDIF to MP Pin Assignments

Pin[1]	Group	Signal
MP4	2	Validity bit
MP5	2	User data
MP6	2	Channel select
MP7	2	Block start
MP8	2	Virtual LRCLK
MP9	1	SDATA
MP10	1	BCLK
MP11	1	LRCLK

[1] The MP0 to MP3 pins are not applicable and can be used normally.

There are two groups of signals, each of which can be activated and deactivated independent from one another. All unused MP pins function normally.

S/PDIF Transmitter

The S/PDIF transmitter outputs two channels of audio data directly from the DSP core at the core rate. It does not preserve or output any additional nonaudio information encoded in the S/PDIF input stream. The encoded nonaudio data bits in the S/PDIF stream are low, except for the validity bit, which is high. Some S/PDIF receivers will ignore the transmitted audio data because the high validity bit indicates an error.

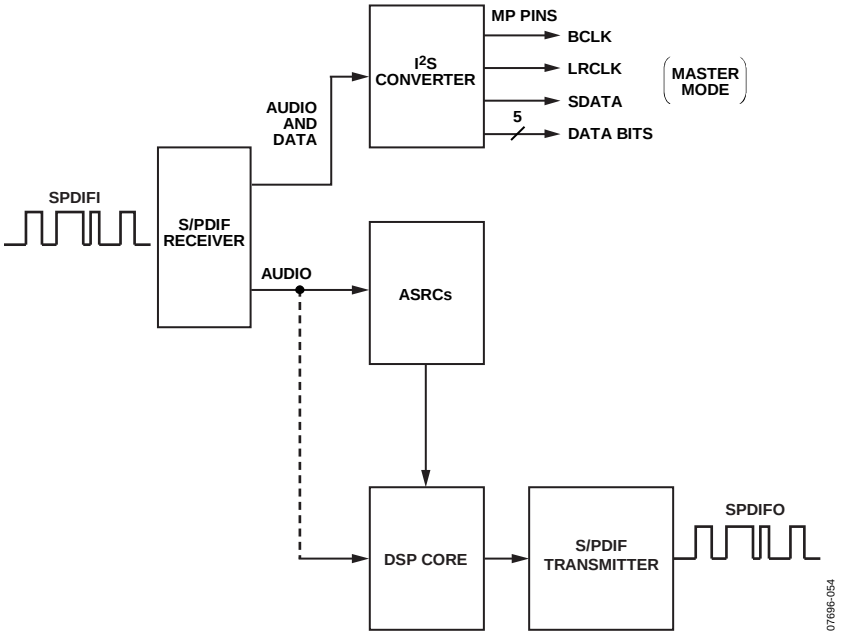


Figure 53. S/PDIF Receiver and Transmitter

S/PDIF MODES AND SETTINGS

Table 54. Addresses of S/PDIF Modes Registers

Address		Name	Read/Write Word Length
Decimal	Hex		
57536	E0C0	S/PDIF receiver—read auxiliary output	16 bits (2 bytes)
57537	E0C1	S/PDIF transmitter—on/off switch	16 bits (2 bytes)
57538	E0C2	S/PDIF read channel status, Byte 0	16 bits (2 bytes)
57539	E0C3	S/PDIF read channel status, Byte 1	16 bits (2 bytes)
57540	E0C4	S/PDIF read channel status, Byte 2	16 bits (2 bytes)
57541	E0C5	S/PDIF read channel status, Byte 3	16 bits (2 bytes)
57542	E0C6	S/PDIF read channel status, Byte 4	16 bits (2 bytes)
57543	E0C7	S/PDIF word length control	16 bits (2 bytes)
57544	E0C8	Auxiliary outputs—set enable mode	16 bits (2 bytes)
57545	E0C9	S/PDIF lock bit detection	16 bits (2 bytes)
57546	E0CA	Set hot enable	16 bits (2 bytes)
57547	E0CB	Read enable auxiliary output	16 bits (2 bytes)
57548	E0CC	S/PDIF loss-of-lock behavior	16 bits (2 bytes)

S/PDIF Receiver—Read Auxiliary Output Register (Address 0xE0C0)

Table 55. Bit Descriptions of Register 0xE0C0

Bit Position	Readback Data
[15:12]	Reserved
11	Virtual LRCLK
10	Block start
9	Channel status
8	User data
[7:2]	Reserved
[1:0]	Validity

This is a read-only register. It allows the S/PDIF auxiliary output (including channel status, user data, and validity bit) to be read.

S/PDIF Transmitter—On/Off Switch Register (Address 0xE0C1)

Table 56. Bit Descriptions of Register 0xE0C1

Bit Position	Description	Default
[15:1]	Reserved	
0	S/PDIF transmitter—on/off switch 0 = S/PDIF transmitter disabled 1 = S/PDIF transmitter enabled	0

This is a single-bit register. Setting Bit 0 to 1 switches the S/PDIF transmitter on; setting it to 0 switches the transmitter off for power savings.

S/PDIF Read Channel Status Register, Bytes[4:0] (Address 0xE0C2 to Address 0xE0C6)

Table 57. Addresses of S/PDIF Read Channel Status Register

Address		Register
Decimal	Hex	
57538	E0C2	Byte 0
57539	E0C3	Byte 1
57540	E0C4	Byte 2
57541	E0C5	Byte 3
57542	E0C6	Byte 4

An S/PDIF stream contains channel status bits (after the audio bits), which contain information such as sample rates, word lengths, and time stamps. The full channel status information contained in the stream is 24 bytes wide for each channel (that is, 48 bytes in total). The ADAU1442/ADAU1445/ADAU1446 make the first five bytes of the left channel available through I²C/SPI.

S/PDIF Word Length Control Register (Address 0xE0C7)

Table 58. Bit Descriptions of Register 0xE0C7

Bit Position	Description	Default
[15:2]	Reserved	
[1:0]	Word length 00 = 24 bit 01 = 20 bit 10 = 16 bit 11 = as decoded from the S/PDIF channel status bits	00

The word length of the audio data decoded from the S/PDIF stream can be controlled using this register. Setting Bits[1:0] to 11 is useful in cases where the S/PDIF stream can come from either a CD or a DVD. From a CD the word length is 16 bits, and from a DVD the word length is 24 bits. This information is contained in the channel status bits and can be used to automatically ignore the least significant byte, if required.

Auxiliary Outputs—Set Enable Mode Register (Address 0xE0C8)

Table 59. Bit Descriptions of Register 0xE0C8

Bit Position	Description	Default
[15:2]	Reserved	
[1:0]	Auxiliary outputs enable mode 00 = auxiliary outputs are always off. 01 = auxiliary outputs are always on. 10 = auxiliary outputs are off on reset. (They switch on as soon as the hot enable bit is 1 and switch off as soon as the S/PDIF lock bit is 0.)	01

This register controls when the S/PDIF stream is active on the multipurpose pins when the S/PDIF to I²S mode is active. For more information, see the Enable S/PDIF to I²S Output section.

Setting Bits[1:0] of Register 0xE0C8 to 10 (auxiliary outputs are off on reset) is useful for situations in which the S/PDIF stream may be interrupted unexpectedly. An interruption causes the S/PDIF lock bit to go low, which in turn disables the auxiliary outputs. When the S/PDIF stream is recovered, the hot enable bit must be activated to restore the auxiliary outputs (see the Set Hot Enable Register (Address 0xE0CA) section for more information).

S/PDIF Lock Bit Detection Register (Address 0xE0C9)

Table 60. Bit Descriptions of Register 0xE0C9

Bit Position	Description
[15:1]	Reserved
0	S/PDIF input lock bit (read only) 0 = no valid input stream 1 = successful lock to input stream

This read-only register shows the status of the S/PDIF input lock bit.

Set Hot Enable Register (Address 0xE0CA)

Table 61. Bit Descriptions of Register 0xE0CA

Bit Position	Description	Default
[15:1]	Reserved	
0	Hot enable bit 0 = hot enable inactive 1 = hot enable active	0

This register allows the hot enable bit to be set, which restarts the auxiliary outputs when they are configured so that the auxiliary outputs are off on a reset (that is, Bits[1:0] of Register 0xE0C8 are set to 10). The hot enable bit is set to 0 automatically in the event that the S/PDIF receiver loses lock. For more information, see the Auxiliary Outputs—Set Enable Mode Register (Address 0xE0C8) section.

Read Enable Auxiliary Output Register (Address 0xE0CB)

Table 62. Bit Descriptions of Register 0xE0CB

Bit Position	Description
[15:1]	Reserved
0	Read enable auxiliary output (read only) 0 = S/PDIF auxiliary outputs disabled 1 = S/PDIF auxiliary outputs enabled

This read-only register shows the status of the S/PDIF auxiliary outputs.

S/PDIF Loss-of-Lock Behavior Register (Address 0xE0CC)

Table 63. Bit Descriptions of Register 0xE0CC

Bit Position	Description	Default
[15:1]	Reserved	
0	S/PDIF loss-of-lock behavior 0 = S/PDIF disable on loss of lock 1 = S/PDIF ignore loss of lock	0

This register controls the behavior of the S/PDIF receiver in the event of a loss of lock to the input stream. A loss of lock can arise when there is severe noise or jitter on the S/PDIF input stream, rendering it unrecognizable to the receiver. In the default mode, such an event disables the S/PDIF receiver, causing it to stop outputting frame sync pulses. This in turn causes the target ASRC to be muted. Frame sync pulses do not resume until lock is regained.

When the register is set to 1, the S/PDIF receiver always outputs frame sync pulses, even if the integrity of the S/PDIF stream is compromised and the audio samples cannot be recovered. In such a case, the S/PDIF receiver data output remains at 0 until lock is regained.

The S/PDIF receiver is robust and can recover streams with integrity well below the standards of the AES/EBU specification. Therefore, even in cases of extreme signal degradation, this register should be used only when audio recovery is required. In general, a loss-of-lock event is much shorter than an ASRC mute or unmute ramp.

Enable S/PDIF to I²S Output Register (Address 0xE241)

Table 64. Bit Descriptions of Register 0xE241

Bit Position	Description	Default
[15:3]	Reserved	
2	Output mode 0 = I²S 1 = TDM	0
1	Group 2 enable 0 = Group 2 off 1 = Group 2 on	0
0	Group 1 enable 0 = Group 1 off 1 = Group 1 on	0

The S/PDIF receiver can be set to send the stereo audio stream and the auxiliary S/PDIF bits in I²S or TDM format on eight of the 12 MP pins. The eight outputs are divided into two groups: Group 1 converts S/PDIF to I²S (LRCLK, BCLK, and SDATA signals), and Group 2 decodes the channel status and user data bits (virtual LRCLK, user data, channel status, validity bit, and block start signal).

This MP output is controlled by setting three bits in Register 0xE241:

- Bit 0 switches Group 1 on and off.
- Bit 1 switches Group 2 on and off.
- Bit 2 switches between I²S and TDM modes.

When S/PDIF to I²S mode is active, the pins described in Table 53 are used.

When TDM mode is active, Slot 0 and Slot 4 contain the audio data, and Slot 1 contains the streamed block start, channel status, user data, and validity bits (see Table 65). The bits are streamed in real time and are synchronized to the audio data. Only the seven MSBs of Slot 1 are used, as shown in Table 65. The corresponding TDM format is shown in more detail in Figure 54.

Table 65. Function of Decoded Bits in Figure 54

Bit Position	Description
31	Block start (high for first 16 samples)
30	Channel status of right channel
29	Channel status of left channel
28	User data bit, right channel
27	User data bit, left channel
26	Validity bit, right channel
25	Validity bit, left channel
[24:0]	Not used

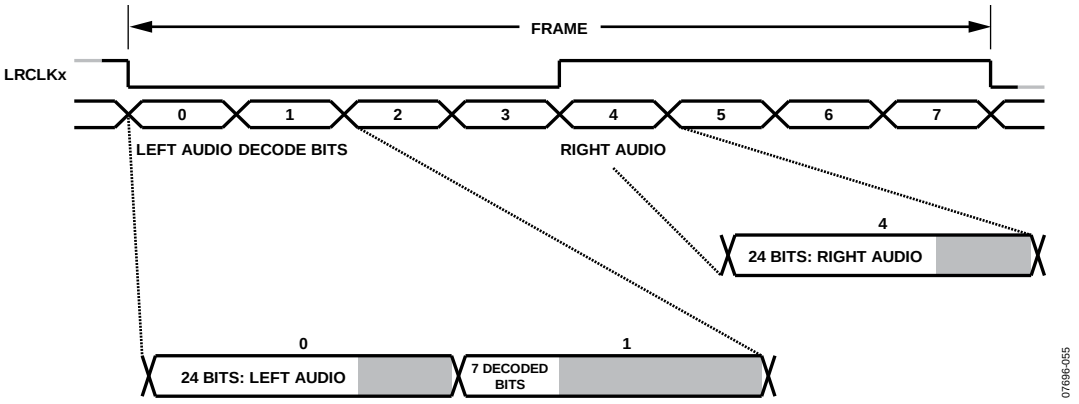


Figure 54. S/PDIF TDM Signal

MULTIPURPOSE PINS

The ADAU1442/ADAU1445/ADAU1446 each include 12 multipurpose pins that can be used either as digital general-purpose inputs/outputs (GPIOs) or as inputs to the 4-channel auxiliary ADC.

Each of the 12 multipurpose pins is controlled by a 4-bit mode. Pins can be configured as digital inputs, digital outputs, or, when applicable, as an analog input to the auxiliary ADC. A debounce circuit is included for use with digital inputs, and it has a range of selectable time constants between 0.3 µs and 40 µs.

When the inputs or outputs are driven by the control port, the value can be directly read or controlled by reading or writing the addresses listed in Table 66.

Each of these registers is four bytes long and is in 5.23 format. To write a Logic 1, the bytes written should be 0x00, 0x80, 0x00, and 0x00. To write a Logic 0, the bytes written should be 0x00, 0x00, 0x00, and 0x00.

When the outputs are driven by the core, they are represented as MP outputs in the SigmaStudio programming tool and are driven directly from the DSP program in 5.23 format.

In addition, there are 12 multipurpose pin value registers that allow the input/output data to be written to or read directly from the control port. The corresponding addresses are listed in Table 68. Each value register contains four bytes and can only store one of two values: logic high or logic low. Logic high is stored as 0x00, 0x80, 0x00, 0x00. Logic low is stored as 0x00, 0x00, 0x00, 0x00. The value of the auxiliary ADC is not stored in these registers. The value of these registers can only be one of two values: 0x00 0x00 0x00 0x00 (digital zero) or 0x00 0x80 0x00 0x00 (digital one). More information about the multipurpose pins can be found in the AN-951 Application Note, *Using Hardware Controls with SigmaDSP GPIO Pins*.

MULTIPURPOSE PINS MODES AND SETTINGS

Multipurpose Pin Control Registers (Address 0xE204 to Address 0xE20F)

Table 66. Addresses of Multipurpose Pin Control Registers

Address		
Decimal	**Hex**	**Register**
57860	E204	Multipurpose pin control, MP0
57861	E205	Multipurpose pin control, MP1
57862	E206	Multipurpose pin control, MP2
57863	E207	Multipurpose pin control, MP3
57864	E208	Multipurpose pin control, MP4
57865	E209	Multipurpose pin control, MP5
57866	E20A	Multipurpose pin control, MP6
57867	E20B	Multipurpose pin control, MP7
57868	E20C	Multipurpose pin control, MP8
57869	E20D	Multipurpose pin control, MP9
57870	E20E	Multipurpose pin control, MP10
57871	E20F	Multipurpose pin control, MP11

Table 67. Bit Settings of Multipurpose Pin Control Registers

Bit Position	Description	Default
[15:4]	Reserved	
[3:0]	MP pin mode 0000 = input without a debounce 0001 = input with a debounce of 0.3 ms 0010 = input with a debounce of 0.6 ms 0011 = input with a debounce of 0.9 ms 0100 = input with a debounce of 5 ms 0101 = input with a debounce of 10 ms 0110 = input with a debounce of 20 ms 0111 = input with a debounce of 40 ms 1000 = input driven by control port 1001 = output driven by control port with pull-up 1010 = output driven by control port without pull-up 1011 = output driven by core with pull-up 1100 = output driven by core without pull-up 1101 = input auxiliary ADC (MP0 to MP3 only) 1110 = output CRC error sticky 1111 = output watchdog error sticky	0000

Multipurpose Pin Value Registers (Address 0x129A to Address 0x12A5)

Table 68. Addresses of Multipurpose Pin Value Registers

Address		
Dec	**Hex**	**Register**
4672	0x1240	Multipurpose pin value, MP0
4673	0x1241	Multipurpose pin value, MP1
4674	0x1242	Multipurpose pin value, MP2
4675	0x1243	Multipurpose pin value, MP3
4676	0x1244	Multipurpose pin value, MP4
4677	0x1245	Multipurpose pin value, MP5
4678	0x1246	Multipurpose pin value, MP6
4679	0x1247	Multipurpose pin value, MP7
4680	0x1248	Multipurpose pin value, MP8
4681	0x1249	Multipurpose pin value, MP9
4682	0x124A	Multipurpose pin value, MP10
4683	0x124B	Multipurpose pin value, MP11

AUXILIARY ADC

The ADAU1442/ADAU1445/ADAU1446 include a 10-bit auxiliary ADC that can be used for control input signals. There is one ADC with four multiplexed inputs. The ADC samples at a rate of f_{CORE}/896 (192 kHz when based on a 172.032 MHz core clock), which results in an effective sampling rate of f_{CORE}/3584 (48 kHz when based on a 172.032 MHz core clock) per channel.

An ADC filtering function is included in the hardware, and hysteresis is available to reduce the effects of noise on the input. More information on these settings is available in Table 70.

The auxiliary ADC is not designed for audio and, therefore, should not be used as an auxiliary audio input. The sample and bit rates are too low to convert signals for audio applications.

The input can be filtered using several methods. The specific filtering modes can be set as described in Table 70.

AUXILIARY ADC MODES AND SETTINGS

ADC Filter Mode Register (Address 0xE224)

Table 69. Bit Descriptions of Register 0xE224

Bit Position	ADC Channel
[15:8]	Reserved
[7:6]	ADC0
[5:4]	ADC1
[3:2]	ADC2
[1:0]	ADC3

Table 70. Settings of Bits[7:0], Register 0xE224

Mode Setting	Function	Default
00	Filter bypass	00
01	ADC data filtered	
10	Filtered with 1-bit hysteresis	
11	Filtered with 2-bit hysteresis	

INTERFACING WITH OTHER DEVICES

When interfacing the ADAU1442/ADAU1445/ADAU1446 to other devices in the system, it may be necessary to set the drive strength of each pin.

DRIVE STRENGTH MODES AND SETTINGS

Bit Clock Pad Strength Register (Address 0xE247)

This register controls the pad drive strength of all bit clock pins configured in master mode. The default 2 mA setting should be adequate for most applications. The 6 mA setting should be used only when the integrity of the signal is compromised.

Table 71. Bit Descriptions of Bit Clock Pad Strength Register

Bit Position	Description	Default
[15:12]	Reserved	
11	BCLK11 0 = low strength (2 mA) 1 = high strength (6 mA)	0
10	BCLK10 0 = low strength (2 mA) 1 = high strength (6 mA)	0
9	BCLK9 0 = low strength (2 mA) 1 = high strength (6 mA)	0
8	BCLK8 0 = low strength (2 mA) 1 = high strength (6 mA)	0
7	BCLK7 0 = low strength (2 mA) 1 = high strength (6 mA)	0
6	BCLK6 0 = low strength (2 mA) 1 = high strength (6 mA)	0
5	BCLK5 0 = low strength (2 mA) 1 = high strength (6 mA)	0
4	BCLK4 0 = low strength (2 mA) 1 = high strength (6 mA)	0
3	BCLK3 0 = low strength (2 mA) 1 = high strength (6 mA)	0
2	BCLK2 0 = low strength (2 mA) 1 = high strength (6 mA)	0
1	BCLK1 0 = low strength (2 mA) 1 = high strength (6 mA)	0
0	BCLK0 0 = low strength (2 mA) 1 = high strength (6 mA)	0

Frame Clock Pad Strength Register (Address 0xE248)

This register controls the pad drive strength of all frame clock pins configured in master mode. The default 2 mA setting should be adequate for most applications. The 6 mA setting should be used only when the integrity of the signal is compromised.

Table 72. Bit Descriptions of Frame Clock Pad Strength Register

Bit Position	Description	Default
[15:12]	Reserved	
11	LRCLK11 0 = low strength (2 mA) 1 = high strength (6 mA)	0
10	LRCLK10 0 = low strength (2 mA) 1 = high strength (6 mA)	0
9	LRCLK9 0 = low strength (2 mA) 1 = high strength (6 mA)	0
8	LRCLK8 0 = low strength (2 mA) 1 = high strength (6 mA)	0
7	LRCLK7 0 = low strength (2 mA) 1 = high strength (6 mA)	0
6	LRCLK6 0 = low strength (2 mA) 1 = high strength (6 mA)	0
5	LRCLK5 0 = low strength (2 mA) 1 = high strength (6 mA)	0
4	LRCLK4 0 = low strength (2 mA) 1 = high strength (6 mA)	0
3	LRCLK3 0 = low strength (2 mA) 1 = high strength (6 mA)	0
2	LRCLK2 0 = low strength (2 mA) 1 = high strength (6 mA)	0
1	LRCLK1 0 = low strength (2 mA) 1 = high strength (6 mA)	0
0	LRCLK0 0 = low strength (2 mA) 1 = high strength (6 mA)	0

Multipurpose Pin Pad Strength Register (Address 0xE249)

This register controls the pad drive strength of all multipurpose pins configured as outputs. The default 2 mA setting should be adequate for most applications. The 6 mA setting should be used only when the integrity of the signal is compromised.

Table 73. Bit Descriptions of Multipurpose Pin Pad Strength Register

Bit Position	Description	Default
[15:12]	Reserved	
11	MP11 0 = low strength (2 mA) 1 = high strength (6 mA)	0
10	MP10 0 = low strength (2 mA) 1 = high strength (6 mA)	0
9	MP9 0 = low strength (2 mA) 1 = high strength (6 mA)	0
8	MP8 0 = low strength (2 mA) 1 = high strength (6 mA)	0
7	MP7 0 = low strength (2 mA) 1 = high strength (6 mA)	0
6	MP6 0 = low strength (2 mA) 1 = high strength (6 mA)	0
5	MP5 0 = low strength (2 mA) 1 = high strength (6 mA)	0
4	MP4 0 = low strength (2 mA) 1 = high strength (6 mA)	0
3	MP3 0 = low strength (2 mA) 1 = high strength (6 mA)	0
2	MP2 0 = low strength (2 mA) 1 = high strength (6 mA)	0
1	MP1 0 = low strength (2 mA) 1 = high strength (6 mA)	0
0	MP0 0 = low strength (2 mA) 1 = high strength (6 mA)	0

Serial Data Output Pad Strength Register (Address 0xE24A)

This register controls the pad drive strength of all serial data output pins. The default 2 mA setting should be adequate for most applications. The 6 mA setting should be used only when the integrity of the signal is compromised.

Table 74. Bit Descriptions of Serial Data Out Pad Strength Register

Bit Position	Description	Default
[15:9]	Reserved	
8	SDATA_OUT8 0 = low strength (2 mA) 1 = high strength (6 mA)	0
7	SDATA_OUT7 0 = low strength (2 mA) 1 = high strength (6 mA)	0
6	SDATA_OUT6 0 = low strength (2 mA) 1 = high strength (6 mA)	0
5	SDATA_OUT5 0 = low strength (2 mA) 1 = high strength (6 mA)	0
4	SDATA_OUT4 0 = low strength (2 mA) 1 = high strength (6 mA)	0
3	SDATA_OUT3 0 = low strength (2 mA) 1 = high strength (6 mA)	0
2	SDATA_OUT2 0 = low strength (2 mA) 1 = high strength (6 mA)	0
1	SDATA_OUT1 0 = low strength (2 mA) 1 = high strength (6 mA)	0
0	SDATA_OUT0 0 = low strength (2 mA) 1 = high strength (6 mA)	0

Other Pad Strength Register (Address 0xE24C)

This register controls the pad drive strength of the communications port, S/PDIF output, and master clock outputs. The default 2 mA setting should be adequate for most applications. The 6 mA setting should be used only when the integrity of the signal is compromised.

Table 75. Bit Descriptions of Other Pad Strength Register

Bit Position	Description	Default
[15:7]	Reserved	
6	SCL/CCLK 0 = low strength (2 mA) 1 = high strength (6 mA)	0
5	CLATCH 0 = low strength (2 mA) 1 = high strength (6 mA)	0
4	ADDR1/CDATA 0 = low strength (2 mA) 1 = high strength (6 mA)	0
3	ADDR0 0 = low strength (2 mA) 1 = high strength (6 mA)	0
2	SDA/COUT 0 = low strength (2 mA) 1 = high strength (6 mA)	0
1	SPDIFO 0 = low strength (2 mA) 1 = high strength (6 mA)	0
0	CLKOUT 0 = low strength (2 mA) 1 = high strength (6 mA)	0

FLEXIBLE TDM MODES

The ADAU1442/ADAU1445/ADAU1446 are able to operate in a flexible TDM mode, which allows them to interface to a wide variety of digital audio devices.

SERIAL INPUT FLEXIBLE TDM INTERFACE MODES AND SETTINGS

The flexible TDM mode is available for the SDATA_IN0 and SDATA_IN1 serial input ports. By using this mode, it is possible to override the default settings of the serial port and flexibly route the contents of an arbitrary TDM input stream to the input channels.

For this mode to be active, the word length bits of the corresponding serial ports must be set to 11 (TDM8 or flexible TDM).

In flexible TDM mode, each flexible TDM stream includes 32 bytes (called slots) of information for every frame on the frame clock. Combining the two serial input ports, this allows for a total of 64 bytes in the flexible stream.

It is important to note that, unlike in the FARM, where signals must be routed as stereo pairs, the data on the flexible TDM stream can be assigned to input channels individually. Each of the 24 input channels is capable of taking data from any slot (or combination of slots) in the flexible TDM stream, as long as data retrieval starts with Input Channel 0 and increases sequentially. This reserves all 24 input channels in the routing matrix for the flexible TDM interface, making them unavailable to the other serial input ports. Because the audio data can be input in 8-, 16-, or 24-bit format, a single channel may occupy more than one slot. An 8-bit channel occupies one slot, a 16-bit channel occupies two slots, and a 24-bit channel occupies three slots. To route flexible TDM data to the input channels, the starting slot number (most significant byte) and the bit depth (number of bytes, or slots, in the stream) must be set in the corresponding input channel register (Flexible TDM to Input Channel[23:0] registers). An example of the input flexible TDM interface mode is shown in Figure 56.

In this example, Input Channel 0 comes from Slot 4, Slot 5, and Slot 6 on the flexible TDM stream (a 24-bit audio channel). Input Channel 1 comes from Slot 12 (an 8-bit audio channel). Input Channel 2 comes from Slot 21 and Slot 22 on the input stream (a 16-bit audio channel). Input Channel 3 comes from Slot 39, Slot 40, and Slot 41 (a 24-bit audio channel). For the audio inputs with a bit depth of less than 24 bits, the LSBs are filled with 0s. Note that the assignment of slots to input channels must be in order, with the lowest slot number starting at Input Channel 0 and increasing sequentially. This is done to ensure compatibility with the automatic input channel assignment (see the Automatic Input Channel Assignment section).

The default setting of all nine bits high (0x01FF) indicates that the input channel is configured in the standard serial input interface mode and does not use the flexible TDM interface mode.

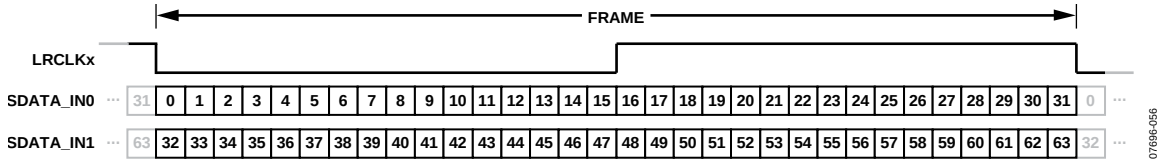


Figure 55. Flexible TDM Interface Mode—Input Streams

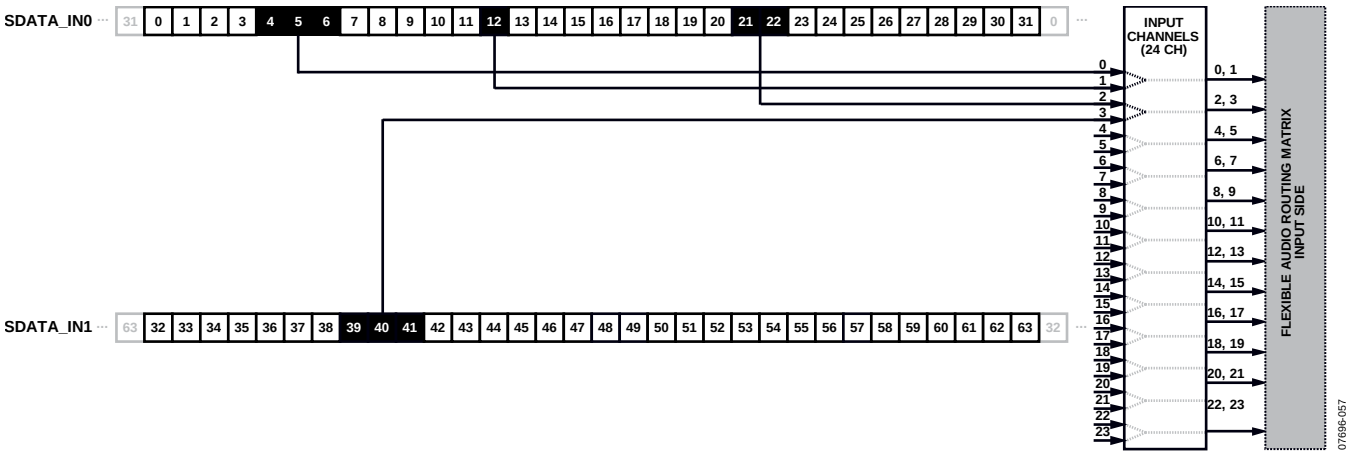


Figure 56. Flexible TDM Interface Mode—Input Routing Example

Flexible TDM to Input Channel Modes Registers (Address 0xE180 to Address 0xE197)

Table 76. Addresses of Serial Input Flexible TDM Interface Modes Registers

Address			
Decimal	**Hex**	**Name**	**Read/Write Word Length**
57728	E180	Flexible TDM to Input Channel 0	16 bits (2 bytes)
57729	E181	Flexible TDM to Input Channel 1	16 bits (2 bytes)
57730	E182	Flexible TDM to Input Channel 2	16 bits (2 bytes)
57731	E183	Flexible TDM to Input Channel 3	16 bits (2 bytes)
57732	E184	Flexible TDM to Input Channel 4	16 bits (2 bytes)
57733	E185	Flexible TDM to Input Channel 5	16 bits (2 bytes)
57734	E186	Flexible TDM to Input Channel 6	16 bits (2 bytes)
57735	E187	Flexible TDM to Input Channel 7	16 bits (2 bytes)
57736	E188	Flexible TDM to Input Channel 8	16 bits (2 bytes)
57737	E189	Flexible TDM to Input Channel 9	16 bits (2 bytes)
57738	E18A	Flexible TDM to Input Channel 10	16 bits (2 bytes)
57739	E18B	Flexible TDM to Input Channel 11	16 bits (2 bytes)
57740	E18C	Flexible TDM to Input Channel 12	16 bits (2 bytes)
57741	E18D	Flexible TDM to Input Channel 13	16 bits (2 bytes)
57742	E18E	Flexible TDM to Input Channel 14	16 bits (2 bytes)
57743	E18F	Flexible TDM to Input Channel 15	16 bits (2 bytes)
57744	E190	Flexible TDM to Input Channel 16	16 bits (2 bytes)
57745	E191	Flexible TDM to Input Channel 17	16 bits (2 bytes)
57746	E192	Flexible TDM to Input Channel 18	16 bits (2 bytes)
57747	E193	Flexible TDM to Input Channel 19	16 bits (2 bytes)
57748	E194	Flexible TDM to Input Channel 20	16 bits (2 bytes)
57749	E195	Flexible TDM to Input Channel 21	16 bits (2 bytes)
57750	E196	Flexible TDM to Input Channel 22	16 bits (2 bytes)
57751	E197	Flexible TDM to Input Channel 23	16 bits (2 bytes)

Table 77. Bit Descriptions of Flexible TDM to Input Channel Modes Registers

Bit Position	Description	Default
[15:9]	Reserved	
8	MSB position 0 = MSB first 1 = LSB first	1
[7:6]	Number of bytes in the channel (audio bit depth) 00 = 1 byte (8-bit audio) 01 = 2 bytes (16-bit audio) 10 = 3 bytes (24-bit audio) 11 = unused	11
[5:0]	Position of the first byte on the TDM stream 000000 = TDM Slot 0 000001 = TDM Slot 1 … 111110 = TDM Slot 62 111111 = TDM Slot 63	111111

SERIAL OUTPUT FLEXIBLE TDM INTERFACE MODES AND SETTINGS

The flexible TDM mode used on the SDATA_IN[1:0] serial input ports can also be used on the SDATA_OUT[1:0] serial output ports. There are 24 output channels available to the output ports in flexible TDM mode.

For this mode to be active, the word length bits of the corresponding serial ports must be set to 11 (TDM8 or flexible TDM).

In flexible TDM mode, each flexible TDM stream includes 32 bytes (slots) of information for every frame on the frame clock. Combining the two serial output ports allows for a total of 64 bytes in the flexible stream.

It is important to note that, unlike in the FARM, where signals must be routed as stereo pairs, the output channels can be individually assigned to different places on the flexible TDM stream. Each of the 64 TDM output slots is capable of taking its data from any of these 24 output channels, as long as data retrieval starts with Output Channel 0 and increases sequentially.

Because the audio data can be input in 8-, 16-, or 24-bit formats, a single channel of audio data may occupy more than one slot. An 8-bit audio channel occupies one slot, a 16-bit audio channel occupies two slots, and a 24-bit audio channel occupies three slots. To set up each slot, the supplying channel (Input Channels[23:0]) and byte position (most significant, middle, or least significant) must be set in the corresponding TDM slot register. An example of the flexible TDM interface mode on the output side is shown in Figure 58.

In this example, three monochannels of audio are sent from the output channels to a flexible TDM stream. Output Channel 0 is 8 bits, Output Channel 1 is 16 bits, and Output Channel 2 is 24 bit. The target slots are set up accordingly. Slot 3 is set to output the most significant (MS) byte of Output Channel 0, or the eight MSBs. Slot 11 is set to output the most significant (MS) byte of Output Channel 1, and Slot 12 is set to output the middle (M) byte; therefore, Slot 11 and Slot 12 together output the 16 MSBs of data from Output Channel 1. Slot 42, Slot 43, and Slot 44 are set to output the most significant (MS), middle (M), and least significant (LS) bytes, respectively, of Output Channel 2, thus accounting for all 24 bits. The flexibility of the system allows for any order or combination of slots to be used for any channel, but most applications follow a sequential MS, M, LS format. Note that any output channel can be assigned to any slot, as long as assignment begins with Output Channel 0 and increases sequentially. This is done to ensure compatibility with the automatic output channel assignment (see the Automatic Output Channel Assignment section).

Two slots are contained within each register. The upper eight bits control the higher slot, and the lower eight bits control the lower slot. For example, in Register 0xE1C0 (SDATA_OUT0) TDM Slot 0 and TDM Slot 1, Bits[15:8] control TDM Slot 1, and Bits[7:0] control TDM Slot 0.

A special condition applies to Slot 31 and Slot 63. These two slots can only be used to hold the MS byte of an 8-bit channel and cannot be used in conjunction with other slots to hold more than eight bits of data.

The default setting of all 16 bits high (0xFFFF) indicates that the channel is configured in the standard serial input interface mode and does not use the flexible TDM interface mode.

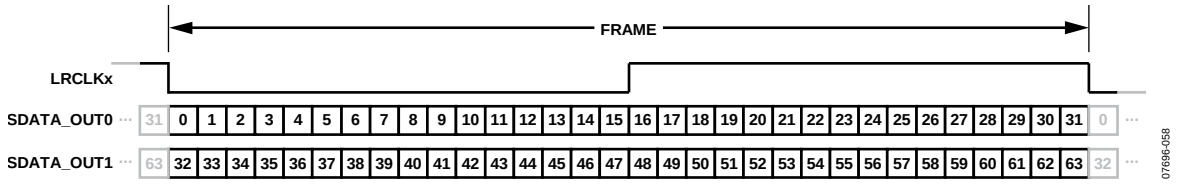


Figure 57. Flexible TDM Interface Mode—Output Streams

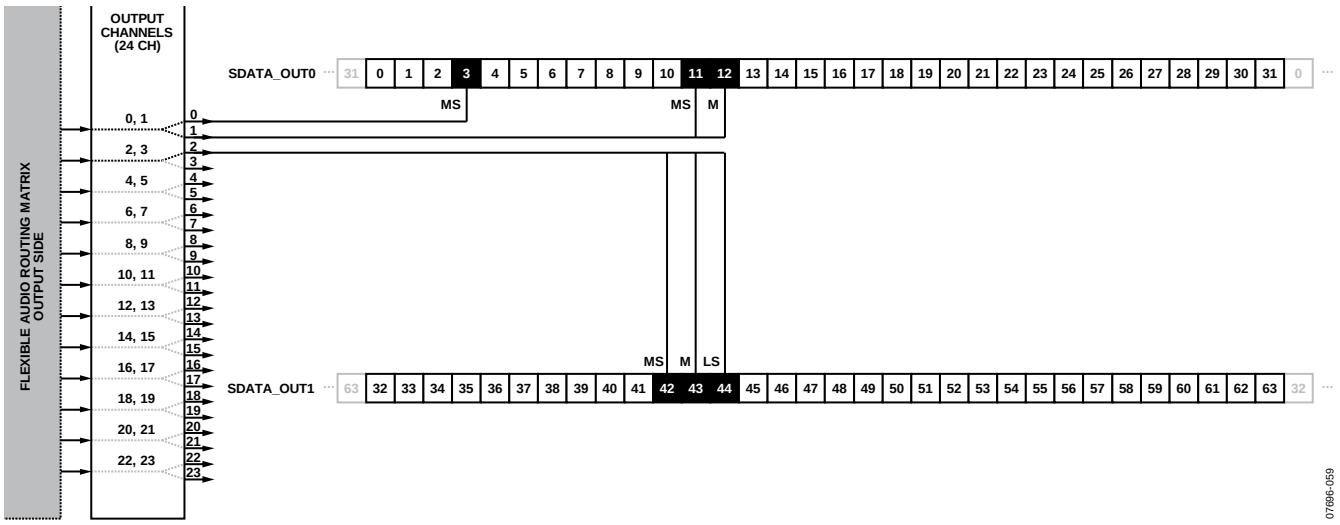


Figure 58. Flexible TDM Interface Mode—Output Routing Example

Serial Output Flexible TDM Interface Modes Registers (Address 0xE1C0 to Address 0xE1DF)

Table 78. Addresses of Serial Output Flexible TDM Interface Modes Registers

Address			
Decimal	**Hex**	**Name**	**Read/Write Word Length**
57792	E1C0	TDM Slot 0 and TDM Slot 1 (SDATA_OUT0)	16 bits (2 bytes)
57793	E1C1	TDM Slot 2 and TDM Slot 3 (SDATA_OUT0)	16 bits (2 bytes)
57794	E1C2	TDM Slot 4 and TDM Slot 5 (SDATA_OUT0)	16 bits (2 bytes)
57795	E1C3	TDM Slot 6 and TDM Slot 7 (SDATA_OUT0)	16 bits (2 bytes)
57796	E1C4	TDM Slot 8 and TDM Slot 9 (SDATA_OUT0)	16 bits (2 bytes)
57797	E1C5	TDM Slot 10 and TDM Slot 11 (SDATA_OUT0)	16 bits (2 bytes)
57798	E1C6	TDM Slot 12 and TDM Slot 13 (SDATA_OUT0)	16 bits (2 bytes)
57799	E1C7	TDM Slot 14 and TDM Slot 15 (SDATA_OUT0)	16 bits (2 bytes)
57800	E1C8	TDM Slot 16 and TDM Slot 17 (SDATA_OUT0)	16 bits (2 bytes)
57801	E1C9	TDM Slot 18 and TDM Slot 19 (SDATA_OUT0)	16 bits (2 bytes)
57802	E1CA	TDM Slot 20 and TDM Slot 21 (SDATA_OUT0)	16 bits (2 bytes)
57803	E1CB	TDM Slot 22 and TDM Slot 23 (SDATA_OUT0)	16 bits (2 bytes)
57804	E1CC	TDM Slot 24 and TDM Slot 25 (SDATA_OUT0)	16 bits (2 bytes)
57805	E1CD	TDM Slot 26 and TDM Slot 27 (SDATA_OUT0)	16 bits (2 bytes)
57806	E1CE	TDM Slot 28 and TDM Slot 29 (SDATA_OUT0)	16 bits (2 bytes)
57807	E1CF	TDM Slot 30 and TDM Slot 31 (SDATA_OUT0)[1]	16 bits (2 bytes)
57808	E1D0	TDM Slot 32 and TDM Slot 33 (SDATA_OUT1)	16 bits (2 bytes)
57809	E1D1	TDM Slot 34 and TDM Slot 35 (SDATA_OUT1)	16 bits (2 bytes)
57810	E1D2	TDM Slot 36 and TDM Slot 37 (SDATA_OUT1)	16 bits (2 bytes)
57811	E1D3	TDM Slot 38 and TDM Slot 39 (SDATA_OUT1)	16 bits (2 bytes)
57812	E1D4	TDM Slot 40 and TDM Slot 41 (SDATA_OUT1)	16 bits (2 bytes)
57813	E1D5	TDM Slot 42 and TDM Slot 43 (SDATA_OUT1)	16 bits (2 bytes)
57814	E1D6	TDM Slot 44 and TDM Slot 45 (SDATA_OUT1)	16 bits (2 bytes)
57815	E1D7	TDM Slot 46 and TDM Slot 47 (SDATA_OUT1)	16 bits (2 bytes)
57816	E1D8	TDM Slot 48 and TDM Slot 49 (SDATA_OUT1)	16 bits (2 bytes)
57817	E1D9	TDM Slot 50 and TDM Slot 51 (SDATA_OUT1)	16 bits (2 bytes)
57818	E1DA	TDM Slot 52 and TDM Slot 53 (SDATA_OUT1)	16 bits (2 bytes)
57819	E1DB	TDM Slot 54 and TDM Slot 55 (SDATA_OUT1)	16 bits (2 bytes)
57820	E1DC	TDM Slot 56 and TDM Slot 57 (SDATA_OUT1)	16 bits (2 bytes)

Address			
Decimal	Hex	Name	Read/Write Word Length
57821	E1DD	TDM Slot 58 and TDM Slot 59 (SDATA_OUT1)	16 bits (2 bytes)
57822	E1DE	TDM Slot 60 and TDM Slot 61 (SDATA_OUT1)	16 bits (2 bytes)
57823	E1DF	TDM Slot 62 and TDM Slot 63 (SDATA_OUT1)[1]	16 bits (2 bytes)

[1] Slot 31 and Slot 63 can only be used to hold the MS byte of an 8-bit channel and cannot be used in conjunction with other slots to hold more than eight bits of data.

Serial Output Flexible TDM Interface Modes Registers—Upper Slot (Address 0xE1C0 to Address 0xE1DF, Bits[15:8])

Table 79. Bit Descriptions of Serial Output Flexible TDM Interface Modes Registers—Upper Slot[1]

Bit Position	Description	Default
15	MSB position 0 = MSB first 1 = LSB first	1
[14:10]	Output channel 00000 = Output Channel 0 00001 = Output Channel 1 … 10110 = Output Channel 22 10111 = Output Channel 23 … 11111 = unused	11111
[9:8]	Byte position 00 = most significant (MS) byte 01 = middle (M) byte 10 = least significant (LS) byte 11 = unused	11

[1] Bits[15:8] control TDM Slot 1.

Serial Output Flexible TDM Interface Modes Registers—Lower Slot (Address 0xE1C0 to Address 0xE1DF, Bits[7:0])

Table 80. Bit Descriptions of Serial Output Flexible TDM Interface Modes Registers—Lower Slot[1]

Bit Position	Description	Default
7	MSB position 0 = MSB first 1 = LSB first	1
[6:2]	Output channel 00000 = Output Channel 0 00001 = Output Channel 1 … 10110 = Output Channel 22 10111 = Output Channel 23 … 11111 = unused	11111
[1:0]	Byte position 00 = most significant (MS) byte 01 = middle (M) byte 10 = least significant (LS) byte 11 = unused	11

[1] Bits[7:0] control TDM Slot 0.

SOFTWARE FEATURES

SOFTWARE SAFELOAD

To update parameters in real time while avoiding pop and click noises on the output, the ADAU1442/ADAU1445/ADAU1446 use a software safeload mechanism. SigmaStudio automatically sets up the necessary code and parameters for new projects. The safeload code, along with other initialization code, fills the first 36 locations in program RAM. The first eight parameter RAM locations (Address 0x0000 to Address 0x0007) are configured by default in SigmaStudio as described in Table 81.

Table 81. Software Safeload Parameter RAM Defaults

Address (Hex)	Function
0x0000	Modulo RAM size
0x0001	Safeload Data 1
0x0002	Safeload Data 2
0x0003	Safeload Data 3
0x0004	Safeload Data 4
0x0005	Safeload Data 5
0x0006	Safeload target address (offset of −1)
0x0007	Number of words to write/safeload trigger

Address 0x0000, which controls the modulo RAM size, is set by SigmaStudio and is based on the dynamic address generator mode of the project.

Address 0x0001 to Address 0x0005 are the five data slots for storing the safeload data. The safeload parameter space contains five data slots by default because most standard signal processing algorithms have five parameters or fewer.

Address 0x0006 is the target address in parameter RAM (with an offset of −1). This designates the first address to be written. If more than one word is written, the address increments automatically for each data-word. The reason for the target address offset of −1 is that the write address is calculated relative to the address of the data, which starts at Address 0x0001. Therefore, if the intention is to update a parameter at Address 0x000A, the target address should be 0x0009.

Address 0x0007 designates the number of words to be written. For a biquad filter, the number is five. For a simple monogain cell, the number is one. This address also serves as the trigger; when it is written, a safeload write is triggered on the next frame.

The safeload mechanism is software based and executes once per audio frame. Therefore, system designers should take care when designing the communication protocol. A delay equal to or greater than the sampling period (the inverse of sampling frequency) is required between each safeload write. At a sample rate of 48 kHz, this equates to a delay of greater than or equal to 20.83 µs. If this delay is not observed, the downloaded data will be corrupted.

SOFTWARE SLEW

When the values of signal processing parameters are changed abruptly in real time, they sometimes cause pop and click sounds to appear on the audio outputs. To avoid this, some algorithms in SigmaStudio implement a software slew functionality. Software slew algorithms set a target value for the parameter and continuously update the parameter's value until it reaches the target.

The target value takes an additional space in parameter RAM, and the current value of the parameter is updated in the nonmodulo section of data RAM. Assignment of parameters and nonmodulo data RAM is handled by the SigmaStudio compiler and does not need to be programmed manually.

Slew parameters can follow several different curves, including an RC-type curve and a linear curve. These curve types are coded into each algorithm and cannot be modified by the user.

Because algorithms that use software slew generally require more RAM than their nonslew equivalents, they should be used only in situations in which a parameter is expected to change during operation of the device.

Figure 59 shows an example of a volume slew applied to a sine wave.

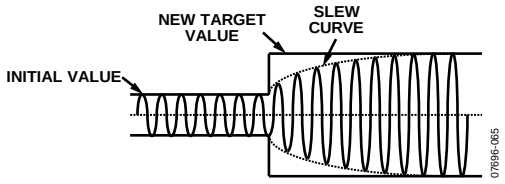


Figure 59. Example of Volume Slew

GLOBAL RAM AND REGISTER MAP

This section contains a list of all RAMS and registers.

OVERVIEW OF REGISTER ADDRESS MAP

Table 82. ADAU1442/ADAU1445/ADAU1446 RAM and Register Map

Address					
Decimal		Hex			
Start Value	End Value	Start Value	End Value	Name	Read/Write Word Length
0	4095	0000	0FFF	Parameter RAM	28 bits (4 bytes)
8192	12287	2000	2FFF	Program RAM	43 bits (6 bytes)
16384	24575	4000	5FFF	Data RAM	28 bits (4 bytes)
57344	57352	E000	E008	Serial input port modes	16 bits (2 bytes)
57408	57417	E040	E049	Serial output port modes	16 bits (2 bytes)
57472	57499	E080	E09B	Flexible audio routing matrix modes	16 bits (2 bytes)
57536	57548	E0C0	E0CC	S/PDIF modes	16 bits (2 bytes)
57601	57667	E101	E143	ASRC modes	16 bits (2 bytes)
57728	57751	E180	E197	Serial input flexible TDM interface modes	16 bits (2 bytes)
57792	57823	E1C0	E1DF	Serial output flexible TDM interface modes	16 bits (2 bytes)
57856	57984	E200	E280	Other modes	16 bits (2 bytes)

DETAILS OF REGISTER ADDRESS MAP

Table 83. Program RAM Registers

Address			
Decimal	Hex	Name	Read/Write Word Length
8192	2000	Program RAM	43 bits (6 bytes)

Table 84. Parameter RAM Registers

Address			
Decimal	Hex	Name	Read/Write Word Length
0	0000	Parameter RAM	28 bits (4 bytes)

Table 85. Data RAM Registers

Address			
Decimal	Hex	Name	Read/Write Word Length
16384	4000	Data RAM	28 bits (4 bytes)

Table 86. Serial Input Port Modes Registers

Address			
Decimal	**Hex**	**Name**	**Read/Write Word Length**
57344	E000	Serial Input Port 0 modes	16 bits (2 bytes)
57345	E001	Serial Input Port 1 modes	16 bits (2 bytes)
57346	E002	Serial Input Port 2 modes	16 bits (2 bytes)
57347	E003	Serial Input Port 3 modes	16 bits (2 bytes)
57348	E004	Serial Input Port 4 modes	16 bits (2 bytes)
57349	E005	Serial Input Port 5 modes	16 bits (2 bytes)
57350	E006	Serial Input Port 6 modes	16 bits (2 bytes)
57351	E007	Serial Input Port 7 modes	16 bits (2 bytes)
57352	E008	Serial Input Port 8 modes	16 bits (2 bytes)

Table 87. Serial Output Port Modes Registers

Address			
Decimal	**Hex**	**Name**	**Read/Write Word Length**
57408	E040	Serial Output Port 0 modes	16 bits (2 bytes)
57409	E041	Serial Output Port 1 modes	16 bits (2 bytes)
57410	E042	Serial Output Port 2 modes	16 bits (2 bytes)
57411	E043	Serial Output Port 3 modes	16 bits (2 bytes)
57412	E044	Serial Output Port 4 modes	16 bits (2 bytes)
57413	E045	Serial Output Port 5 modes	16 bits (2 bytes)
57414	E046	Serial Output Port 6 modes	16 bits (2 bytes)
57415	E047	Serial Output Port 7 modes	16 bits (2 bytes)
57416	E048	Serial Output Port 8 modes	16 bits (2 bytes)
57417	E049	High speed slave interface mode	16 bit (2 bytes)

Table 88. Flexible Audio Routing Matrix Modes Registers

Address			
Decimal	**Hex**	**Name**	**Read/Write Word Length**
57472	E080	ASRC input select, Pair 0 (Channel 0, Channel 1)	16 bits (2 bytes)
57473	E081	ASRC input select, Pair 1 (Channel 2, Channel 3)	16 bits (2 bytes)
57474	E082	ASRC input select, Pair 2 (Channel 4, Channel 5)	16 bits (2 bytes)
57475	E083	ASRC input select, Pair 3 (Channel 6, Channel 7)	16 bits (2 bytes)
57476	E084	ASRC input select, Pair 4 (Channel 8, Channel 9)	16 bits (2 bytes)
57477	E085	ASRC input select, Pair 5 (Channel 10, Channel 11)	16 bits (2 bytes)
57478	E086	ASRC input select, Pair 6 (Channel 12, Channel 13)	16 bits (2 bytes)
57479	E087	ASRC input select, Pair 7 (Channel 14, Channel 15)	16 bits (2 bytes)
57480	E088	ASRC output rate select, Pair 0 (Channel 0, Channel 1)	16 bits (2 bytes)
57481	E089	ASRC output rate select, Pair 1 (Channel 2, Channel 3)	16 bits (2 bytes)
57482	E08A	ASRC output rate select, Pair 2 (Channel 4, Channel 5)	16 bits (2 bytes)
57483	E08B	ASRC output rate select, Pair 3 (Channel 6, Channel 7)	16 bits (2 bytes)
57484	E08C	ASRC output rate select, Pair 4 (Channel 8, Channel 9)	16 bits (2 bytes)
57485	E08D	ASRC output rate select, Pair 5 (Channel 10, Channel 11)	16 bits (2 bytes)
57486	E08E	ASRC output rate select, Pair 6 (Channel 12, Channel 13)	16 bits (2 bytes)
57487	E08F	ASRC output rate select, Pair 7 (Channel 14, Channel 15)	16 bits (2 bytes)
57488	E090	Serial output select, Pair 0 (Channel 0, Channel 1)	16 bits (2 bytes)
57489	E091	Serial output select, Pair 1 (Channel 2, Channel 3)	16 bits (2 bytes)
57490	E092	Serial output select, Pair 2 (Channel 4, Channel 5)	16 bits (2 bytes)

Address			
Decimal	Hex	Name	Read/Write Word Length
57491	E093	Serial output select, Pair 3 (Channel 6, Channel 7)	16 bits (2 bytes)
57492	E094	Serial output select, Pair 4 (Channel 8, Channel 9)	16 bits (2 bytes)
57493	E095	Serial output select, Pair 5 (Channel 10, Channel 11)	16 bits (2 bytes)
57494	E096	Serial output select, Pair 6 (Channel 12, Channel 13)	16 bits (2 bytes)
57495	E097	Serial output select, Pair 7 (Channel 14, Channel 15)	16 bits (2 bytes)
57496	E098	Serial output select, Pair 8 (Channel 16, Channel 17)	16 bits (2 bytes)
57497	E099	Serial output select, Pair 9 (Channel 18, Channel 19)	16 bits (2 bytes)
57498	E09A	Serial output select, Pair 10 (Channel 20, Channel 21)	16 bits (2 bytes)
57499	E09B	Serial output select, Pair 11 (Channel 22, Channel 23)	16 bits (2 bytes)

Table 89. S/PDIF Modes Registers

Address			
Decimal	Hex	Name	Read/Write Word Length
57536	E0C0	S/PDIF receiver—read auxiliary output	16 bits (2 bytes)
57537	E0C1	S/PDIF transmitter—on/off switch	16 bits (2 bytes)
57538	E0C2	S/PDIF read channel status, Byte 0	16 bits (2 bytes)
57539	E0C3	S/PDIF read channel status, Byte 1	16 bits (2 bytes)
57540	E0C4	S/PDIF read channel status, Byte 2	16 bits (2 bytes)
57541	E0C5	S/PDIF read channel status, Byte 3	16 bits (2 bytes)
57542	E0C6	S/PDIF read channel status, Byte 4	16 bits (2 bytes)
57543	E0C7	S/PDIF word length control	16 bits (2 bytes)
57544	E0C8	Auxiliary outputs—set enable mode	16 bits (2 bytes)
57545	E0C9	S/PDIF lock bit detection	16 bits (2 bytes)
57546	E0CA	Set hot enable	16 bits (2 bytes)
57547	E0CB	Read enable auxiliary output	16 bits (2 bytes)
57548	E0CC	S/PDIF loss-of-lock behavior	16 bits (2 bytes)

Table 90. ASRC Modes Registers

Address			
Decimal	Hex	Name	Read/Write Word Length
57601	E101	Stereo ASRC[3:0] lock status and mute	16 bits (2 bytes)
57603	E103	Stereo ASRC[3:0] mute ramp disable	16 bits (2 bytes)
57665	E141	Stereo ASRC[7:4] lock status and mute	16 bits (2 bytes)
57667	E143	Stereo ASRC[7:4] mute ramp disable	16 bits (2 bytes)

Table 91. Serial Input Flexible TDM Interface Modes Registers

Address			
Decimal	Hex	Name	Read/Write Word Length
57728	E180	Flexible TDM to Input Channel 0	16 bits (2 bytes)
57729	E181	Flexible TDM to Input Channel 1	16 bits (2 bytes)
57730	E182	Flexible TDM to Input Channel 2	16 bits (2 bytes)
57731	E183	Flexible TDM to Input Channel 3	16 bits (2 bytes)
57732	E184	Flexible TDM to Input Channel 4	16 bits (2 bytes)
57733	E185	Flexible TDM to Input Channel 5	16 bits (2 bytes)
57734	E186	Flexible TDM to Input Channel 6	16 bits (2 bytes)
57735	E187	Flexible TDM to Input Channel 7	16 bits (2 bytes)

Address			
Decimal	Hex	Name	Read/Write Word Length
57736	E188	Flexible TDM to Input Channel 8	16 bits (2 bytes)
57737	E189	Flexible TDM to Input Channel 9	16 bits (2 bytes)
57738	E18A	Flexible TDM to Input Channel 10	16 bits (2 bytes)
57739	E18B	Flexible TDM to Input Channel 11	16 bits (2 bytes)
57740	E18C	Flexible TDM to Input Channel 12	16 bits (2 bytes)
57741	E18D	Flexible TDM to Input Channel 13	16 bits (2 bytes)
57742	E18E	Flexible TDM to Input Channel 14	16 bits (2 bytes)
57743	E18F	Flexible TDM to Input Channel 15	16 bits (2 bytes)
57744	E190	Flexible TDM to Input Channel 16	16 bits (2 bytes)
57745	E191	Flexible TDM to Input Channel 17	16 bits (2 bytes)
57746	E192	Flexible TDM to Input Channel 18	16 bits (2 bytes)
57747	E193	Flexible TDM to Input Channel 19	16 bits (2 bytes)
57748	E194	Flexible TDM to Input Channel 20	16 bits (2 bytes)
57749	E195	Flexible TDM to Input Channel 21	16 bits (2 bytes)
57750	E196	Flexible TDM to Input Channel 22	16 bits (2 bytes)
57751	E197	Flexible TDM to Input Channel 23	16 bits (2 bytes)

Table 92. Serial Output Flexible TDM Interface Modes Registers

Address			
Decimal	Hex	Name	Read/Write Word Length
57792	E1C0	TDM Slot 0 and TDM Slot 1 (SDATA_OUT0)	16 bits (2 bytes)
57793	E1C1	TDM Slot 2 and TDM Slot 3 (SDATA_OUT0)	16 bits (2 bytes)
57794	E1C2	TDM Slot 4 and TDM Slot 5 (SDATA_OUT0)	16 bits (2 bytes)
57795	E1C3	TDM Slot 6 and TDM Slot 7 (SDATA_OUT0)	16 bits (2 bytes)
57796	E1C4	TDM Slot 8 and TDM Slot 9 (SDATA_OUT0)	16 bits (2 bytes)
57797	E1C5	TDM Slot 10 and TDM Slot 11 (SDATA_OUT0)	16 bits (2 bytes)
57798	E1C6	TDM Slot 12 and TDM Slot 13 (SDATA_OUT0)	16 bits (2 bytes)
57799	E1C7	TDM Slot 14 and TDM Slot 15 (SDATA_OUT0)	16 bits (2 bytes)
57800	E1C8	TDM Slot 16 and TDM Slot 17 (SDATA_OUT0)	16 bits (2 bytes)
57801	E1C9	TDM Slot 18 and TDM Slot 19 (SDATA_OUT0)	16 bits (2 bytes)
57802	E1CA	TDM Slot 20 and TDM Slot 21 (SDATA_OUT0)	16 bits (2 bytes)
57803	E1CB	TDM Slot 22 and TDM Slot 23 (SDATA_OUT0)	16 bits (2 bytes)
57804	E1CC	TDM Slot 24 and TDM Slot 25 (SDATA_OUT0)	16 bits (2 bytes)
57805	E1CD	TDM Slot 26 and TDM Slot 27 (SDATA_OUT0)	16 bits (2 bytes)
57806	E1CE	TDM Slot 28 and TDM Slot 29 (SDATA_OUT0)	16 bits (2 bytes)
57807	E1CF	TDM Slot 30 and TDM Slot 31 (SDATA_OUT0)	16 bits (2 bytes)
57808	E1D0	TDM Slot 32 and TDM Slot 33 (SDATA_OUT1)	16 bits (2 bytes)
57809	E1D1	TDM Slot 34 and TDM Slot 35 (SDATA_OUT1)	16 bits (2 bytes)
57810	E1D2	TDM Slot 36 and TDM Slot 37 (SDATA_OUT1)	16 bits (2 bytes)
57811	E1D3	TDM Slot 38 and TDM Slot 39 (SDATA_OUT1)	16 bits (2 bytes)
57812	E1D4	TDM Slot 40 and TDM Slot 41 (SDATA_OUT1)	16 bits (2 bytes)
57813	E1D5	TDM Slot 42 and TDM Slot 43 (SDATA_OUT1)	16 bits (2 bytes)
57814	E1D6	TDM Slot 44 and TDM Slot 45 (SDATA_OUT1)	16 bits (2 bytes)
57815	E1D7	TDM Slot 46 and TDM Slot 47 (SDATA_OUT1)	16 bits (2 bytes)
57816	E1D8	TDM Slot 48 and TDM Slot 49 (SDATA_OUT1)	16 bits (2 bytes)
57817	E1D9	TDM Slot 50 and TDM Slot 51 (SDATA_OUT1)	16 bits (2 bytes)
57818	E1DA	TDM Slot 52 and TDM Slot 53 (SDATA_OUT1)	16 bits (2 bytes)
57819	E1DB	TDM Slot 54 and TDM Slot 55 (SDATA_OUT1)	16 bits (2 bytes)
57820	E1DC	TDM Slot 56 and TDM Slot 57 (SDATA_OUT1)	16 bits (2 bytes)

Address			
Decimal	Hex	Name	Read/Write Word Length
57821	E1DD	TDM Slot 58 and TDM Slot 59 (SDATA_OUT1)	16 bits (2 bytes)
57822	E1DE	TDM Slot 60 and TDM Slot 61 (SDATA_OUT1)	16 bits (2 bytes)
57823	E1DF	TDM Slot 62 and TDM Slot 63 (SDATA_OUT1)	16 bits (2 bytes)

Table 93. Other Modes Registers

Address			
Decimal	Hex	Name	Read/Write Word Length
57856	E200	Cyclic Redundancy Check Ideal Value 1	16 bits (2 bytes)
57857	E201	Cyclic Redundancy Check Ideal Value 2	16 bits (2 bytes)
57858	E202	Cyclic redundancy check enable	16 bits (2 bytes)
57860	E204	Multipurpose pin control, MP0	16 bits (2 bytes)
57861	E205	Multipurpose pin control, MP1	16 bits (2 bytes)
57862	E206	Multipurpose pin control, MP2	16 bits (2 bytes)
57863	E207	Multipurpose pin control, MP3	16 bits (2 bytes)
57864	E208	Multipurpose pin control, MP4	16 bits (2 bytes)
57865	E209	Multipurpose pin control, MP5	16 bits (2 bytes)
57866	E20A	Multipurpose pin control, MP6	16 bits (2 bytes)
57867	E20B	Multipurpose pin control, MP7	16 bits (2 bytes)
57868	E20C	Multipurpose pin control, MP8	16 bits (2 bytes)
57569	E20D	Multipurpose pin control, MP9	16 bits (2 bytes)
57870	E20E	Multipurpose pin control, MP10	16 bits (2 bytes)
57871	E20F	Multipurpose pin control, MP11	16 bits (2 bytes)
57872	E210	Watchdog enable	16 bits (2 bytes)
57873	E211	Watchdog Value 1	16 bits (2 bytes)
57874	E212	Watchdog Value 2	16 bits (2 bytes)
57887	E21F	Modulo data memory	16 bits (2 bytes)
57888	E220	DSP core rate select	16 bits (2 bytes)
57889	E221	Dejitter window	16 bits (2 bytes)
57892	E224	ADC filter mode	16 bits (2 bytes)
57893	E225	Cyclic redundancy check error sticky	16 bits (2 bytes)
57894	E226	Watchdog error sticky	16 bits (2 bytes)
57895	E227	CRC and watchdog mute	16 bits (2 bytes)
57896	E228	Core run	16 bits (2 bytes)
57897	E229	Program counter peak count	16 bits (2 bytes)
57920	E240	Clock pad multiplexer	16 bits (2 bytes)
57921	E241	Enable S/PDIF to I^2S output	16 bits (2 bytes)
57927	E247	Bit clock pad strength	16 bits (2 bytes)
57928	E248	Frame clock pad strength	16 bits (2 bytes)
57929	E249	Multipurpose pin pad strength	16 bits (2 bytes)
57930	E24A	Serial data output pad strength	16 bits (2 bytes)
57932	E24C	Other pad strength	16 bits (2 bytes)
57984	E280	Master clock enable switch	16 bits (2 bytes)

APPLICATIONS INFORMATION

LAYOUT RECOMMENDATIONS

Parts Placement

All 100 nF bypass capacitors, which are recommended for every analog, digital, and PLL power-ground pair, should be placed as close to the ADAU1442/ADAU1445/ADAU1446 as possible. The AVDD, DVDD, PVDD, and IOVDD supply signals on the board should each be bypassed with an additional single bulk capacitor (10 µF to 47 µF).

All traces in the crystal oscillator circuit (Figure 9) should be kept as short as possible to minimize stray capacitance. There should not be any long board traces connected to crystal oscillator circuit components because such traces may affect crystal startup and operation.

Grounding

A single ground plane should be used in the application layout. Components in an analog signal path should be placed away from digital signals.

Exposed Pad PCB Design

The ADAU1442 and ADAU1445 packages include an exposed pad for improved heat dissipation. When designing a board for such a package, special consideration should be given to the following:

- A copper layer equal in size to the exposed pad should be on all layers of the board, from top to bottom, and should connect somewhere to a dedicated copper board layer (see Figure 60).
- Vias should be placed to connect all layers of copper, allowing for efficient heat and energy conductivity. For an example, see Figure 61, which has 16 vias arranged in a 4 × 4 grid in the pad area.

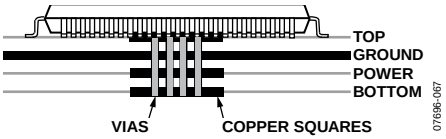


Figure 60. Exposed Pad Layout Example—Side View

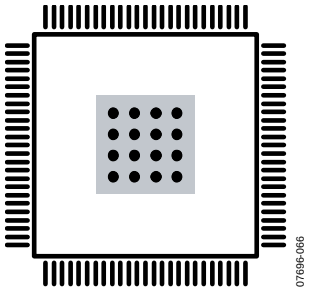


Figure 61. Exposed Pad Layout Example—Top View

PLL Loop Filter

The single resistor and two capacitors in the PLL loop filter should be connected to the PLL_FILT and PVDD pins with short traces to minimize jitter.

Power Supply Bypass Capacitors

Each power supply pin should be bypassed to its nearest appropriate ground pin with a single 100 nF capacitor. The connections to each side of the capacitor should be as short as possible, and the trace should stay on a single layer with no vias. For maximum effectiveness, the capacitor should preferably be located either equidistant from the power and ground pins or, when equidistant placement is not possible, slightly closer to the power pin. Thermal connections to the planes should be made on the far side of the capacitor.

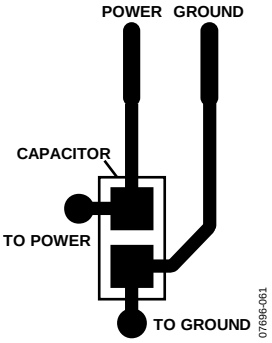


Figure 62. Recommended Power Supply Bypass Capacitor Layout

EOS/ESD Protection

Although the ADAU1442/ADAU1445/ADAU1446 have robust internal protection circuitry against overvoltages and electrostatic discharge, an external transient voltage suppressor (TVS) is recommended for all systems to prevent damage to the IC. Examples can be found in the AN-311 Application Note on the Analog Devices website.

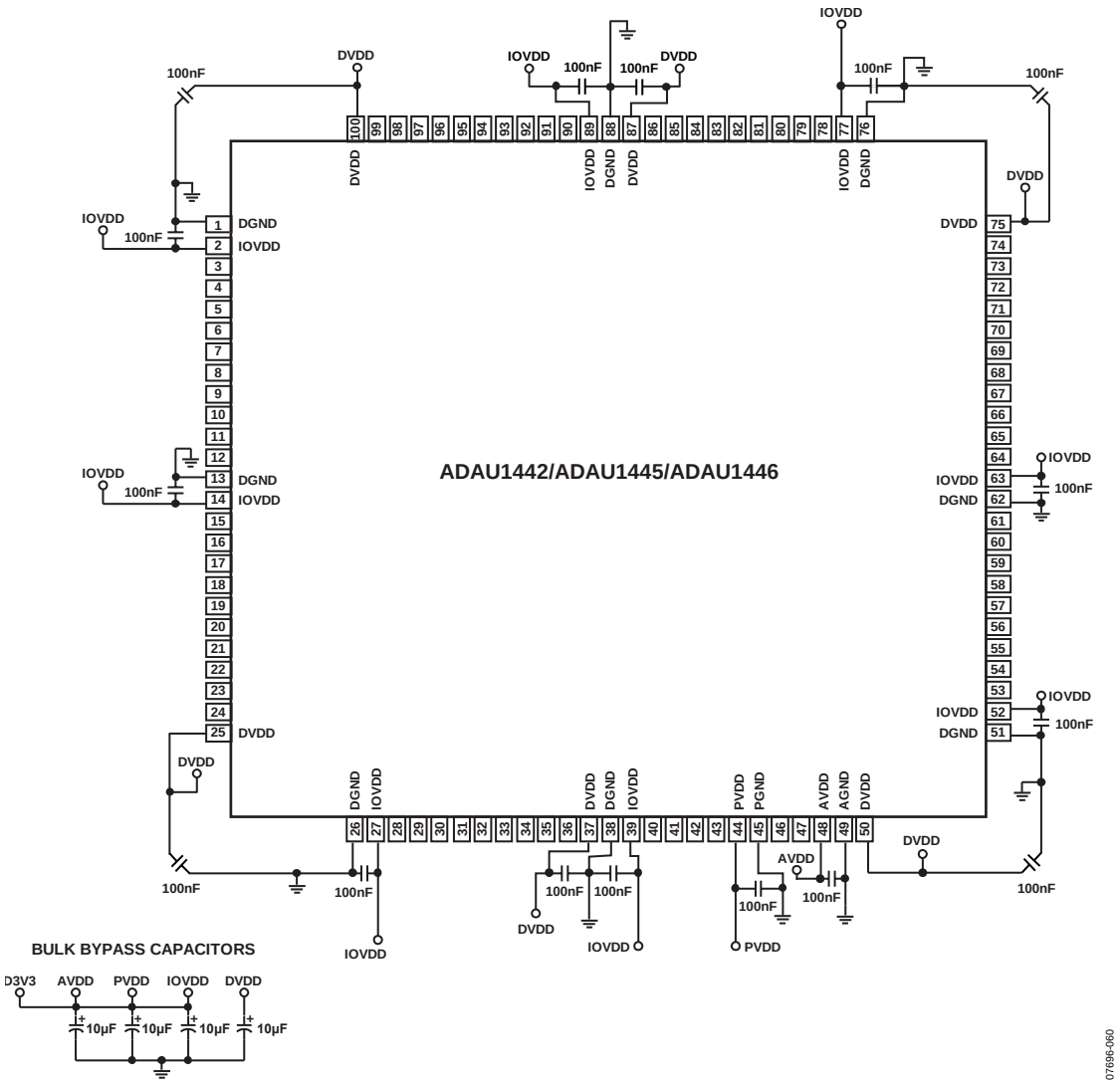


Figure 63. Recommended Power Supply Bypass Capacitor Connections

TYPICAL APPLICATION SCHEMATICS

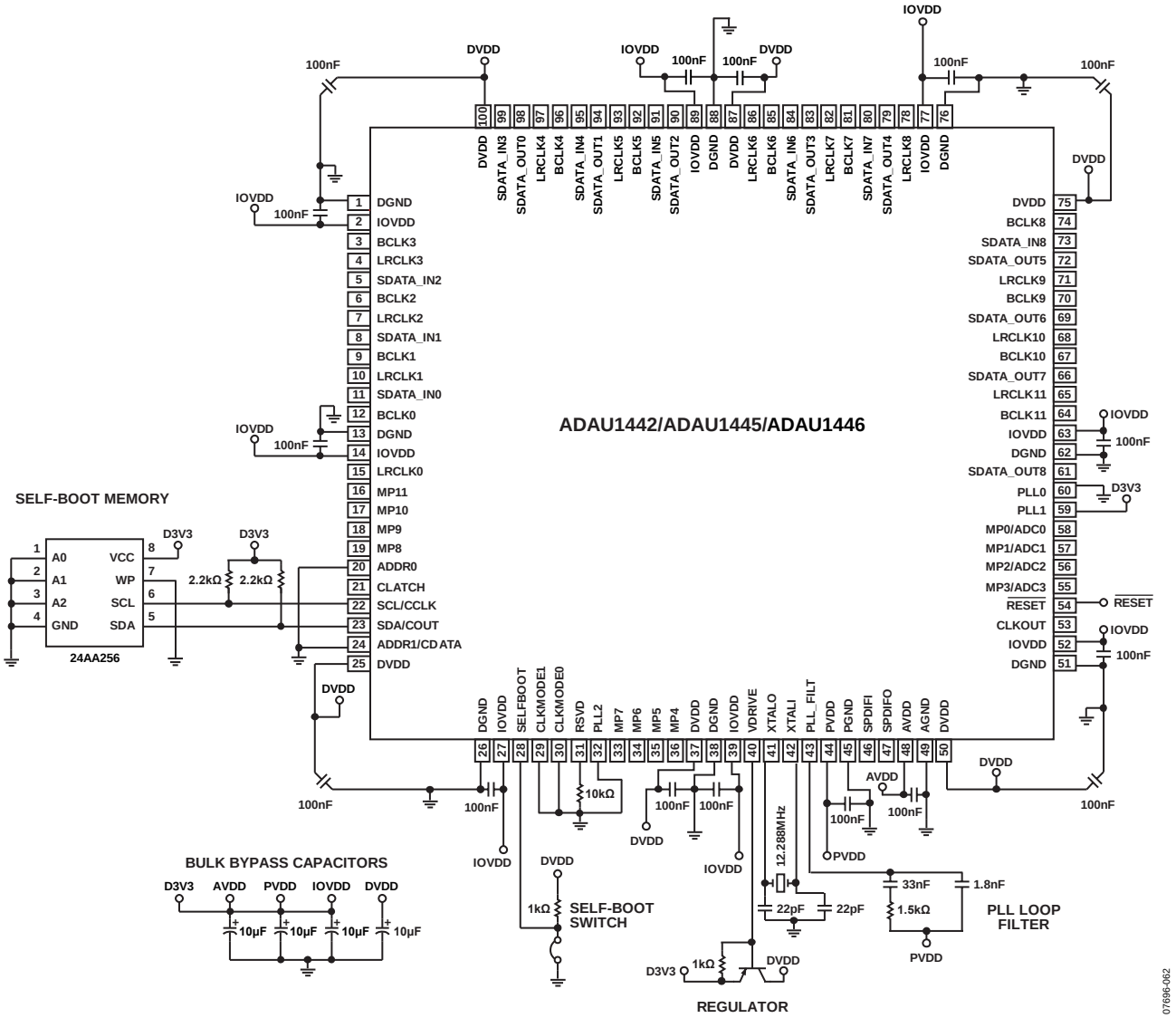


Figure 64. Self-Boot Application Schematic

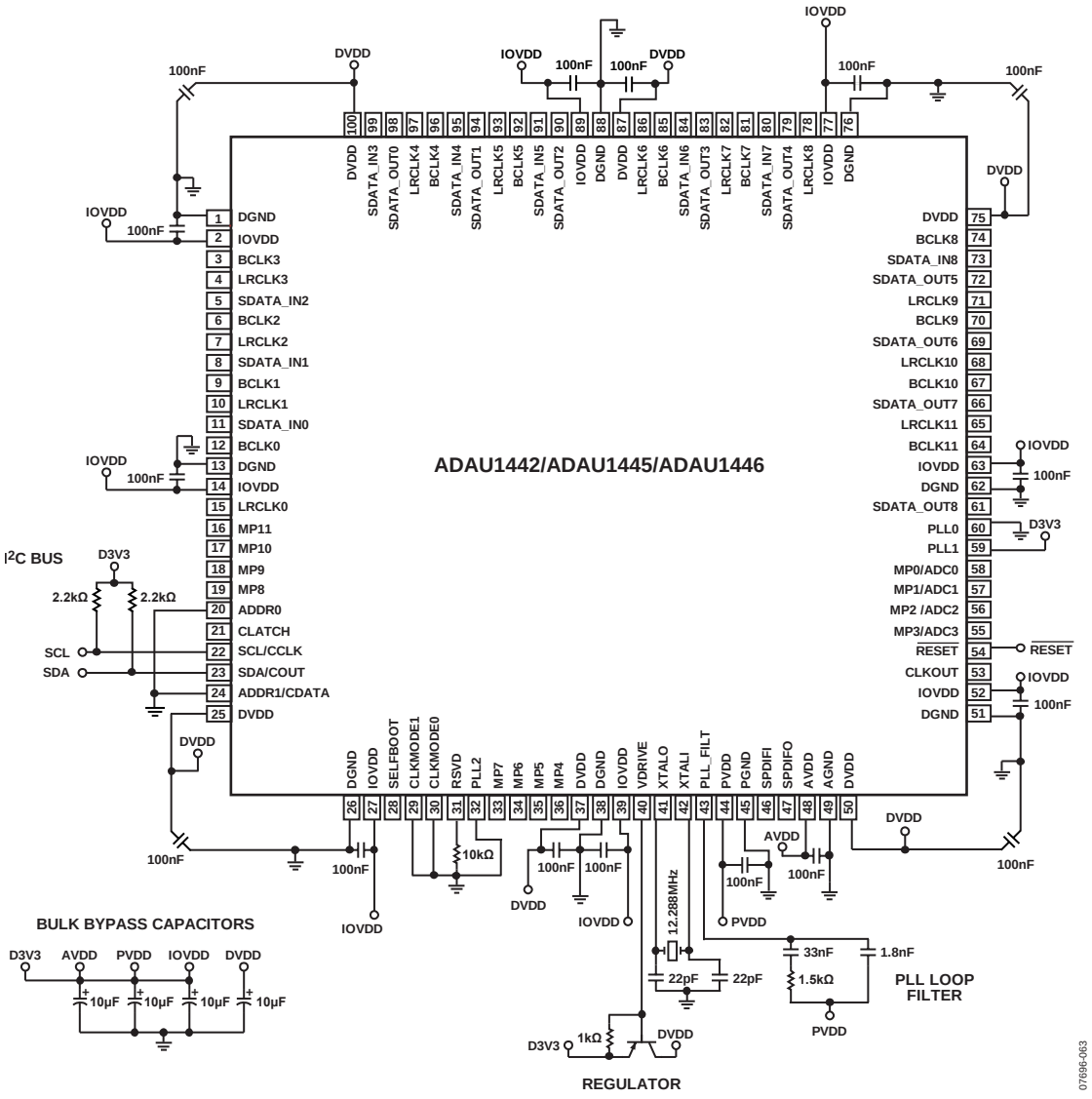


Figure 65. I²C Control Application Schematic

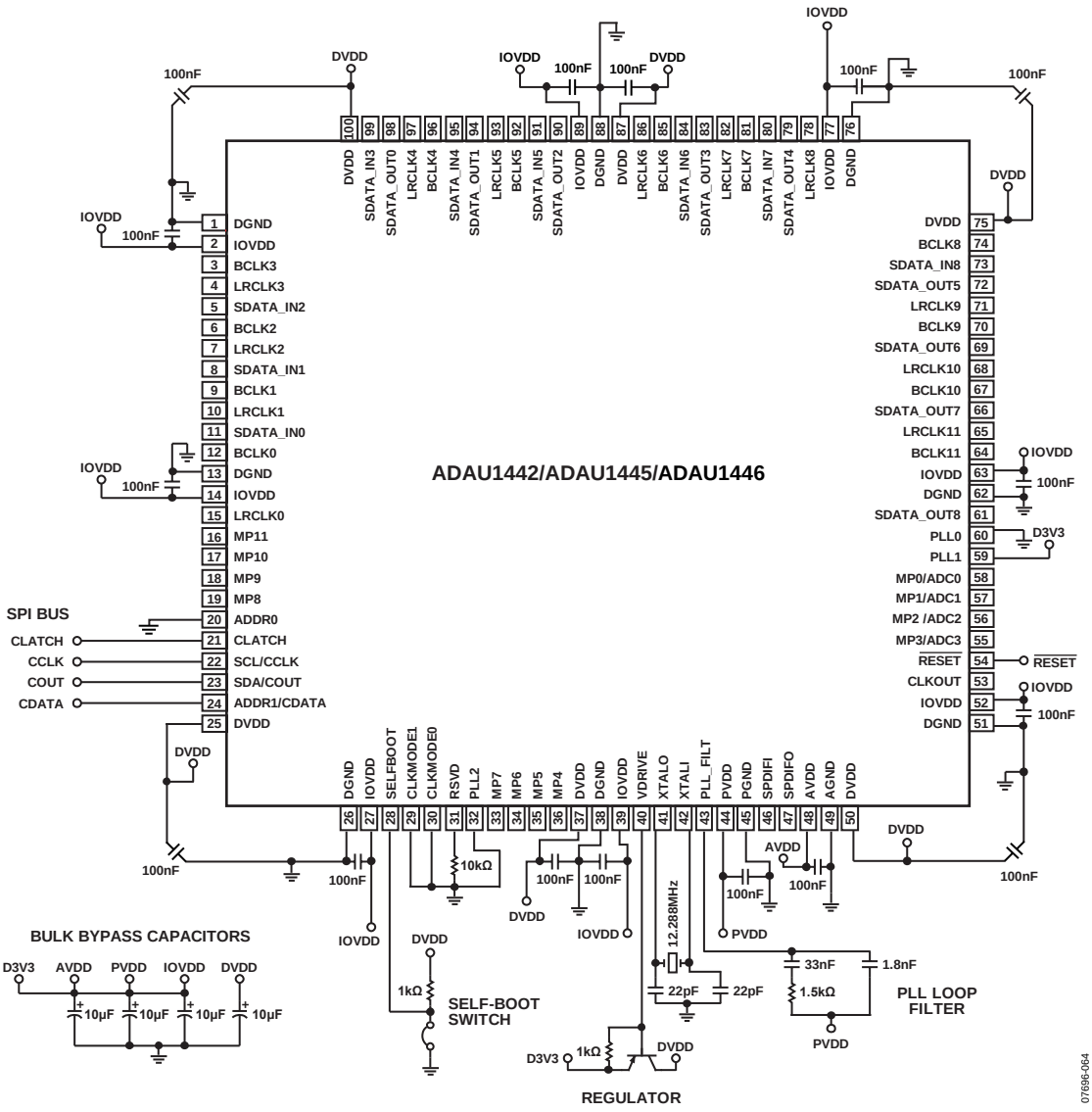
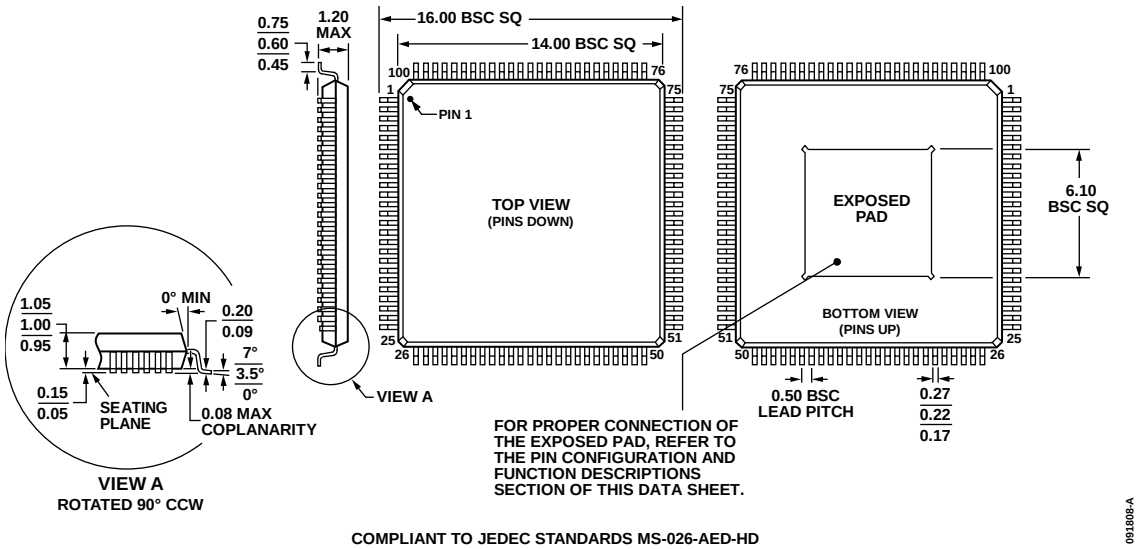


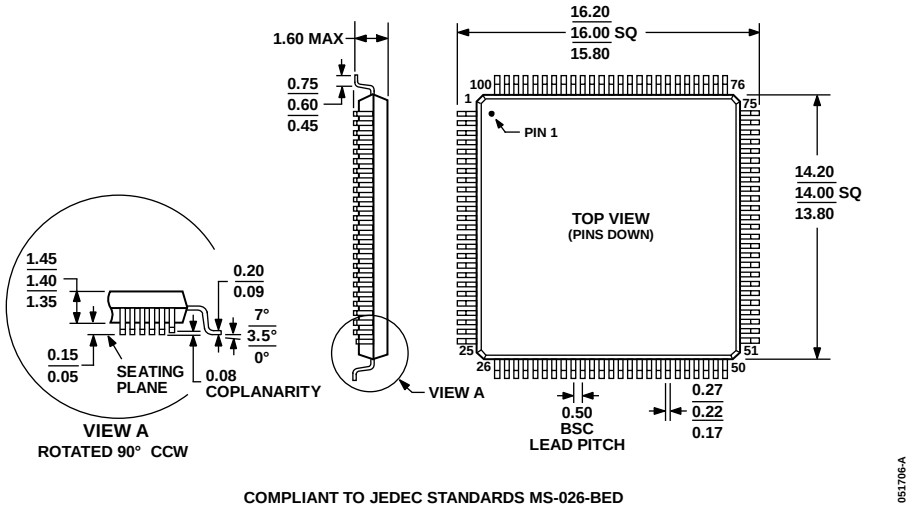
Figure 66. SPI Control Application Schematic

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-026-AED-HD

Figure 67. 100-Lead Thin Quad Flat Package, Exposed Pad [TQFP_EP]
(SV-100-8)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MS-026-BED

Figure 68. 100-Lead Thin Quad Flat Package [LQFP]
(ST-100-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADAU1442YSVZ-3A	−40°C to +105°C	100-Lead TQFP_EP	SV-100-8
ADAU1442YSVZ-3A-RL	−40°C to +105°C	100-Lead TQFP_EP, 13″ Tape and Reel	SV-100-8
ADAU1445YSVZ-3A	−40°C to +105°C	100-Lead TQFP_EP	SV-100-8
ADAU1445YSVZ-3A-RL	−40°C to +105°C	100-Lead TQFP_EP, 13″ Tape and Reel	SV-100-8
ADAU1446YSTZ-3A	−40°C to +105°C	100-Lead LQFP	ST-100-1
ADAU1446YSTZ-3A-RL	−40°C to +105°C	100-Lead LQFP, 13″ Tape and Reel	ST-100-1
EVAL-ADAU1442EBZ		Evaluation Board Used for the ADAU1442/ADAU1445	
EVAL-ADAU1446EBZ		ADAU1446 Evaluation Board	

[1] Z = RoHS Compliant Part.

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