BATTERY PROTECTION IC WITH CELL-BALANCE FUNCTION

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Rev.3.8_00

The S-8209B Series is a protection IC for lithium-ion / lithium polymer rechargeable batteries and includes a high-accuracy voltage detection circuit and a delay circuit.
The S-8209B Series has a transmission function and two types of cell-balance function so that users are also able to configure a protection circuit with series multi-cell.

■ Features

- High-accuracy voltage detection circuit

Overcharge detection voltage*1	3.55 V to 4.40 V (5 mV step)	Accuracy ±25 mV
Overcharge release voltage*1	3.50 V to 4.40 V*2	Accuracy ±50 mV
Cell-balance detection voltage*1	3.55 V to 4.40 V (5 mV step)*3	Accuracy ±25 mV
Cell-balance release voltage*1	3.50 V to 4.40 V*4	Accuracy ±50 mV
Overdischarge detection voltage	2.0 V to 3.0 V (10 mV step)	Accuracy ±50 mV
Overdischarge release voltage	2.0 V to 3.4 V*5	Accuracy ±100 mV

- Settable delay time by external capacitor for output pin
- Control charging, discharging, cell-balance by CTLC pin, CTLD pin
- Two types of cell-balance function; charge / discharge*6
- Wide range of operation temperature Ta = −40°C to +85°C
- Low current consumption 7.0 μA max.
- Lead-free, Sn 100%, halogen-free*7

***1.** Regarding selection of overcharge detection voltage, overcharge release voltage, cell-balance detection voltage and cell-balance release voltage, refer to **Remark 3** in "**3. Product name list**" of "**■ Product Name Structure**".
***2.** Overcharge release voltage = Overcharge detection voltage − Overcharge hysteresis voltage
(Overcharge hysteresis voltage is selectable in 0 V to 0.4 V in 50 mV step.)
***3.** Select as to overcharge detection voltage > cell-balance detection voltage.
***4.** Cell-balance release voltage = Cell-balance detection voltage − Cell-balance hysteresis voltage
(Cell-balance hysteresis voltage is selectable in 0 V to 0.4 V in 50 mV step.)
***5.** Overdischarge release voltage = Overdischarge detection voltage + Overdischarge hysteresis voltage
(Overdischarge hysteresis voltage is selectable in 0 V to 0.7 V in 100 mV step.)
***6.** Also available the product without discharge cell-balance function
***7.** Refer to "**■ Product Name Structure**" for details.

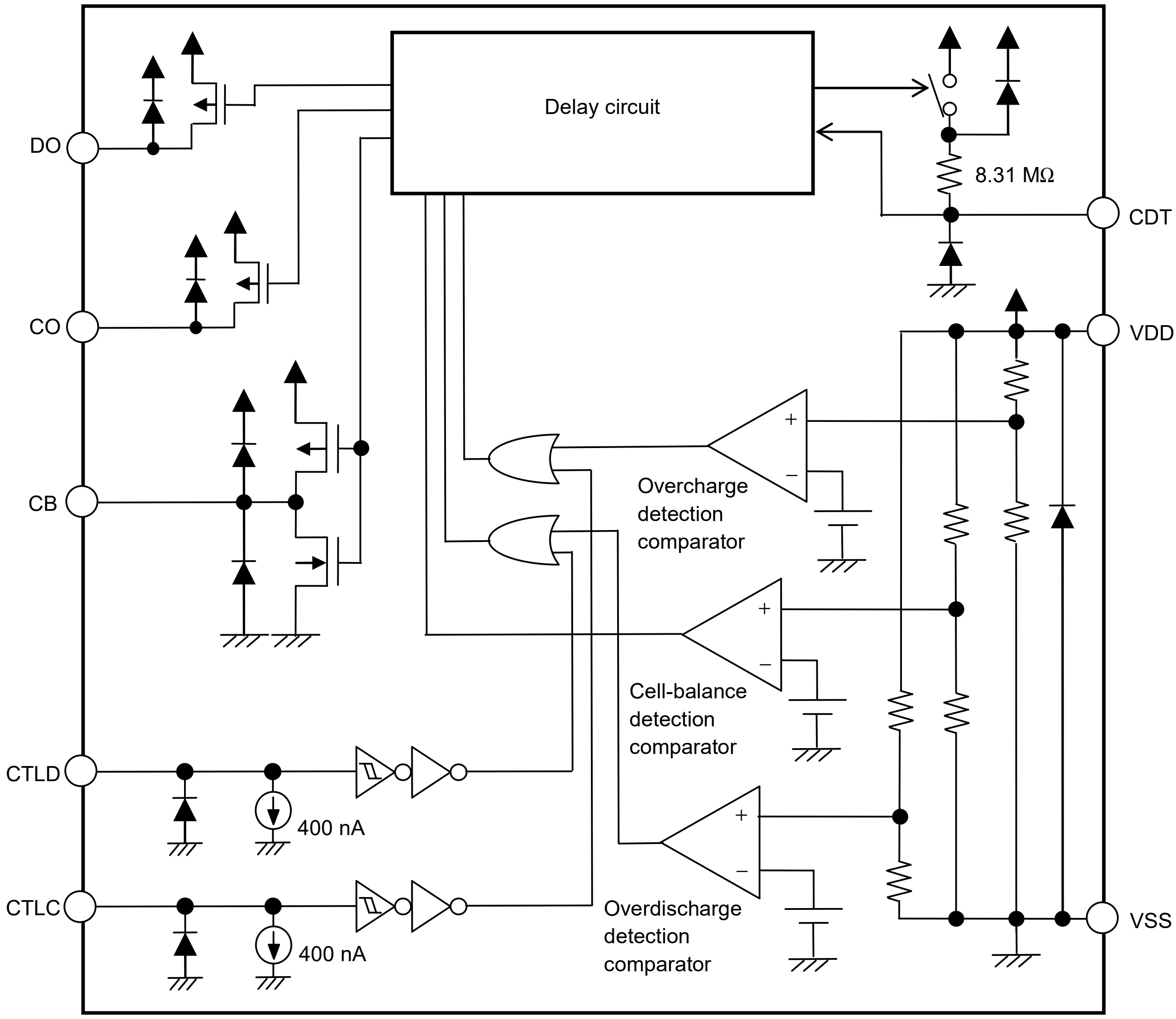
■ Applications

- Lithium-ion rechargeable battery pack
- Lithium polymer rechargeable battery pack

■ Packages

- SNT-8A
- 8-Pin TSSOP

■ Block Diagram



Remark The diodes in the IC are parasitic diodes.

Figure 1

■ Product Name Structure

1. Product name

1. 1 8-Pin TSSOP

S-8209B xx - T8T1 x

- x: Environmental code
  - U: Lead-free (Sn 100%), halogen-free
  - S: Lead-free, halogen-free
- T8T1: Package name abbreviation and IC packing specifications*1
  - T8T1: 8-Pin TSSOP, Tape
- xx: Serial code
  - Sequentially set from AA to ZZ

***1.** Refer to the tape drawing.

1. 2 SNT-8A

S-8209B xx - I8T1 U

- U: Environmental code
  - U: Lead-free (Sn 100%), halogen-free
- I8T1: Package name abbreviation and IC packing specifications*1
  - I8T1: SNT-8A, Tape
- xx: Serial code
  - Sequentially set from AA to ZZ

***1.** Refer to the tape drawing.

2. Packages

Table 1 Package Drawing Codes

Package Name		Dimension	Tape	Reel	Land
8-Pin TSSOP	Environmental code = S	FT008-A-P-SD	FT008-E-C-SD	FT008-E-R-SD	−
	Environmental code = U	FT008-A-P-SD	FT008-E-C-SD	FT008-E-R-S1	
SNT-8A		PH008-A-P-SD	PH008-A-C-SD	PH008-A-R-SD	PH008-A-L-SD

3. Product name list

3. 1 8-Pin TSSOP

Table 2

Product Name	Overcharge Detection Voltage (V_{CU})	Overcharge Release Voltage (V_{CL})	Cell-balance Detection Voltage (V_{BU})	Cell-balance Release Voltage (V_{BL})	Overdischarge Detection Voltage (V_{DL})	Overdischarge Release Voltage (V_{DU})	Discharge Cell-balance Function
S-8209BAA-T8T1y	4.100 V	4.000 V	4.050 V	4.000 V	2.50 V	2.70 V	Yes
S-8209BAD-T8T1y	4.150 V	3.950 V	3.900 V	3.900 V	2.00 V	2.70 V	Yes
S-8209BAG-T8T1y	3.800 V	3.650 V	3.700 V	3.700 V	2.20 V	2.50 V	No
S-8209BAH-T8T1y	4.250 V	4.150 V	4.200 V	4.200 V	2.50 V	2.80 V	No
S-8209BAI-T8T1y	4.250 V	4.150 V	4.100 V	4.050 V	2.50 V	2.70 V	Yes
S-8209BAJ-T8T1y	4.150 V	3.950 V	3.900 V	3.900 V	2.30 V	3.00 V	No
S-8209BAK-T8T1y	4.215 V	4.215 V	4.190 V	4.190 V	2.00 V	2.50 V	Yes
S-8209BAL-T8T1y	4.300 V	4.100 V	4.225 V	4.225 V	2.00 V	2.50 V	Yes
S-8209BAN-T8T1U	4.250 V	4.150 V	4.200 V	4.200 V	2.00 V	2.10 V	No
S-8209BAO-T8T1U	4.300 V	4.200 V	4.200 V	4.200 V	2.30 V	3.00 V	No
S-8209BAP-T8T1U	3.900 V	3.900 V	3.700 V	3.700 V	2.00 V	2.50 V	Yes
S-8209BAU-T8T1U	4.225 V	4.175 V	4.215 V	4.165 V	2.30 V	3.00 V	Yes
S-8209BAW-T8T1U	4.225 V	4.175 V	4.215 V	4.165 V	2.30 V	3.00 V	No
S-8209BAX-T8T1U	4.210 V	4.160 V	4.190 V	4.140 V	2.50 V	3.20 V	No
S-8209BAY-T8T1U	4.210 V	4.160 V	4.190 V	4.140 V	2.50 V	3.00 V	No
S-8209BAZ-T8T1U	4.195 V	4.145 V	4.100 V	4.050 V	2.50 V	2.70 V	No
S-8209BBA-T8T1U	3.700 V	3.500 V	3.550 V	3.550 V	2.00 V	2.50 V	Yes
S-8209BBB-T8T1U	4.275 V	4.225 V	4.145 V	4.095 V	2.00 V	2.30 V	No
S-8209BBC-T8T1U	4.200 V	4.100 V	4.145 V	4.095 V	2.00 V	2.30 V	No

3. 2 SNT-8A

Table 3

Product Name	Overcharge Detection Voltage (V_{CU})	Overcharge Release Voltage (V_{CL})	Cell-balance Detection Voltage (V_{BU})	Cell-balance Release Voltage (V_{BL})	Overdischarge Detection Voltage (V_{DL})	Overdischarge Release Voltage (V_{DU})	Discharge Cell-balance Function
S-8209BAA-I8T1U	4.100 V	4.000 V	4.050 V	4.000 V	2.50 V	2.70 V	Yes
S-8209BAM-I8T1U	4.000 V	3.800 V	3.900 V	3.850 V	3.00 V	3.40 V	No
S-8209BAO-I8T1U	4.300 V	4.200 V	4.200 V	4.200 V	2.30 V	3.00 V	No
S-8209BAP-I8T1U	3.900 V	3.900 V	3.700 V	3.700 V	2.00 V	2.50 V	Yes
S-8209BAR-I8T1U	4.230 V	4.170 V	4.180 V	4.180 V	2.80 V	3.00 V	No

Remark 1. y: S or U
2. Please select products of environmental code = U for Sn 100%, halogen-free products.

3. Please contact our sales representatives for products other than the above.
Users are able to select the overcharge detection voltage, overcharge release voltage, cell-balance detection voltage and cell-balance release voltage from the range shown in **Figure 2** and **Figure 3**.
Users are able to select how to combine the overcharge detection voltage (V_{CU}) and the overcharge release voltage (V_{CL}) from the range A or B shown in **Figure 2**[*1].
Similarly, select how to combine the cell-balance detection voltage (V_{BU}) and the cell-balance release voltage (V_{BL}) from the range of C or D in **Figure 3**[*2].
In selecting the combination of V_{CU} and V_{CL} from the range A, select the combination of V_{BU} and V_{BL} from the range C. Similarly, in selecting the combination of V_{CU} and V_{CL} from the B range, select the combination of V_{BU} and V_{BL} from the range D[*3].

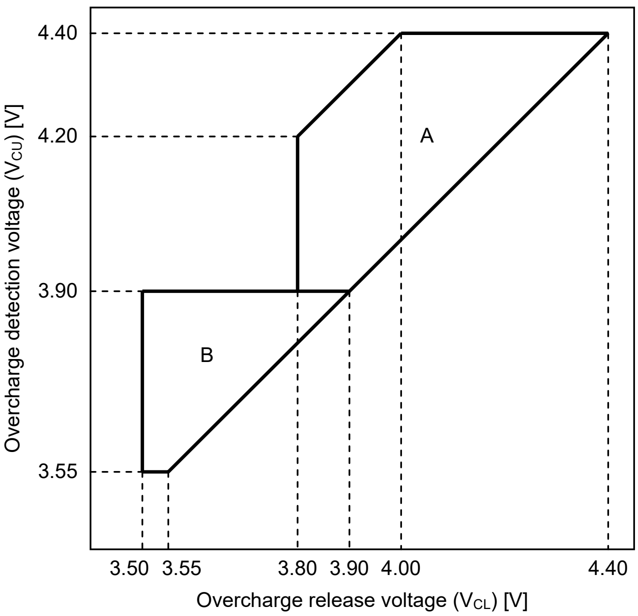


Figure 2

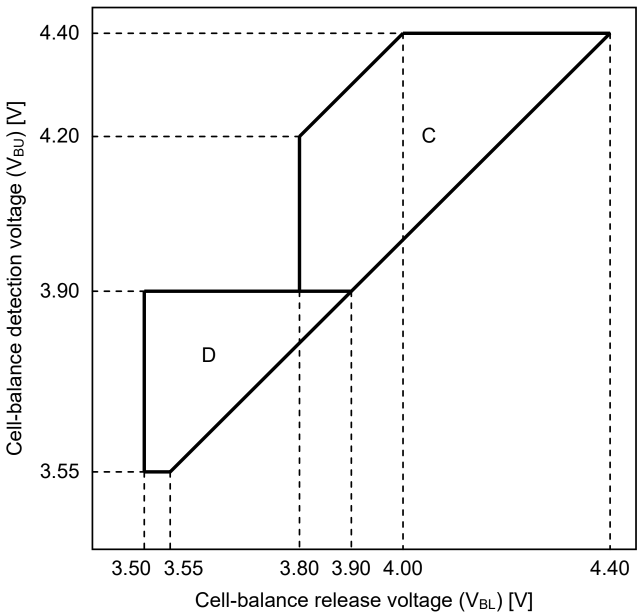


Figure 3

***1.** Users are able to select the overcharge hysteresis voltage ($V_{CU} - V_{CL}$) in 0 V to 0.4 V, in 50 mV step.
***2.** Users are able to select the cell-balancce hysteresis voltage ($V_{BU} - V_{BL}$) in 0 V to 0.4 V, in 50 mV step.
***3.** Select as to set $V_{CU} > V_{BU}$.

■ Pin Configurations

1. 8-Pin TSSOP

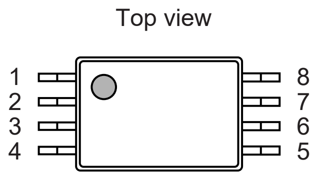


Figure 4

Table 4

Pin No.	Symbol	Description
1	CTLC	Pin for charge control
2	CTLD	Pin for dischage control
3	VDD	Input pin for positive power supply; Connection pin for battery's positive voltage
4	CDT	Capacitor connection pin for overcharge detection delay, cell-balance detection delay and overdischarge detection delay
5	VSS	Input pin for negative power supply; Connection pin for batter's negative voltage
6	DO	Output pin for discharge control (Pch open-drain output)
7	CO	Output pin for charge control (Pch open-drain output)
8	CB	Output pin for cell-balance control (CMOS output)

2. SNT-8A

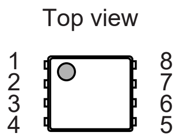


Figure 5

Table 5

Pin No.	Symbol	Description
1	CTLC	Pin for charge control
2	CTLD	Pin for dischage control
3	VDD	Input pin for positive power supply; Connection pin for battery's positive voltage
4	CDT	Capacitor connection pin for overcharge detection delay, cell-balance detection delay and overdischarge detection delay
5	VSS	Input pin for negative power supply; Connection pin for battery's negative voltage
6	DO	Output pin for discharge control (Pch open-drain output)
7	CO	Output pin for charge control (Pch open-drain output)
8	CB	Output pin for cell-balance control (CMOS output)

■ Absolute Maximum Ratings

Table 6

(Ta = +25°C unless otherwise specified)

Item		Symbol	Applied pin	Absolute Maximum Rating	Unit
Input voltage between VDD and VSS		V_{DS}	VDD	V_{SS} – 0.3 to V_{SS} + 12	V
CB pin output voltage		V_{CB}	CB	V_{SS} – 0.3 to V_{DD} + 0.3	V
CDT pin voltage		V_{CDT}	CDT	V_{SS} – 0.3 to V_{DD} + 0.3	V
DO pin output voltage		V_{DO}	DO	V_{DD} – 24 to V_{DD} + 0.3	V
CO pin output voltage		V_{CO}	CO	V_{DD} – 24 to V_{DD} + 0.3	V
CTLC pin input voltage		V_{CTLC}	CTLC	V_{SS} – 0.3 to V_{SS} + 24	V
CTLD pin input voltage		V_{CTLD}	CTLD	V_{SS} – 0.3 to V_{SS} + 24	V
Power dissipation	8-Pin TSSOP	P_D	–	700*1	mW
	SNT-8A			450*1	mW
Operating ambient temperature		T_{opr}	–	–40 to +85	°C
Storage temperature		T_{stg}	–	–55 to +125	°C

***1.** When mounted on board
[Mounted board]
(1) Board size: 114.3 mm × 76.2 mm × t1.6 mm
(2) Board name: JEDEC STANDARD51-7

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

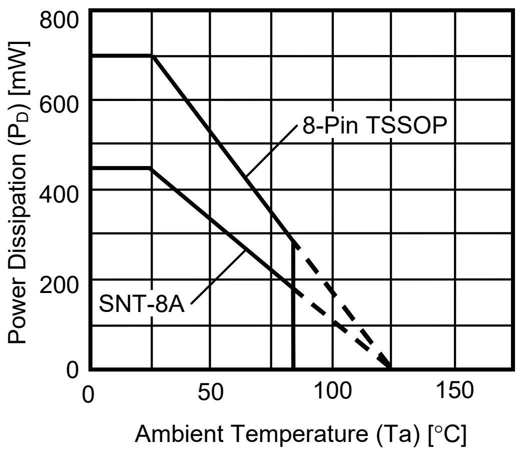


Figure 6 Power Dissipation of Package (When mounted on board)

■ Electrical Characteristics

Table 7

(Ta = +25°C unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Overcharge detection voltage	V_{CU}	–	V_{CU} – 0.025	V_{CU}	V_{CU} + 0.025	V	1
Overcharge release voltage	V_{CL}	$V_{CL} \neq V_{CU}$	V_{CL} – 0.05	V_{CL}	V_{CL} + 0.05	V	1
		$V_{CL} = V_{CU}$	V_{CL} – 0.05	V_{CL}	V_{CL} + 0.025	V	1
Cell-balance detection voltage	V_{BU}	–	V_{BU} – 0.025	V_{BU}	V_{BU} + 0.025	V	1
Cell-balance release voltage	V_{BL}	$V_{BL} \neq V_{BU}$	V_{BL} – 0.05	V_{BL}	V_{BL} + 0.05	V	1
		$V_{BL} = V_{BU}$	V_{BL} – 0.05	V_{BL}	V_{BL} + 0.025	V	1
Overdischarge detection voltage	V_{DL}	–	V_{DL} – 0.05	V_{DL}	V_{DL} + 0.05	V	1
Overdischarge release voltage	V_{DU}	–	V_{DU} – 0.10	V_{DU}	V_{DU} + 0.10	V	1
CDT pin resistance*1	R_{CDT}	V_{DS} = 3.5 V, V_{CDT} = 0 V	4.76	8.31	10.9	MΩ	2
CDT pin detection voltage*1	V_{CDET}	V_{DS} = 3.5 V	$V_{DS} \times 0.65$	$V_{DS} \times 0.70$	$V_{DS} \times 0.75$	V	3
Operating voltage between VDD and VSS	V_{DSOP}	Output voltage of CO pin, DO pin and CB pin are determined	1.5	–	8.0	V	–
CTLC pin H voltage	V_{CTLCH}	V_{DS} = 3.5 V	$V_{DS} \times 0.55$	–	$V_{DS} \times 0.90$	V	4
CTLD pin H voltage	V_{CTLDH}	V_{DS} = 3.5 V	$V_{DS} \times 0.55$	–	$V_{DS} \times 0.90$	V	4
CTLC pin L voltage	V_{CTLCL}	V_{DS} = 3.5 V	$V_{DS} \times 0.10$	–	$V_{DS} \times 0.45$	V	4
CTLD pin L voltage	V_{CTLDL}	V_{DS} = 3.5 V	$V_{DS} \times 0.10$	–	$V_{DS} \times 0.45$	V	4
Current consumption during operation*2	I_{OPE}	V_{DS} = 3.5 V	–	3.5	7.0	μA	5
Sink current CTLC*2	I_{CTLCL}	V_{DS} = 3.5 V, V_{CTLC} = 3.5 V	320	400	480	nA	6
Sink current CTLD*2	I_{CTLDL}	V_{DS} = 3.5 V, V_{CTLD} = 3.5 V	320	400	480	nA	6
Source current CB	I_{CBH}	V_{CB} = 4.0 V, V_{DS} = 4.5 V	30	–	–	μA	7
Sink current CB	I_{CBL}	V_{CB} = 0.5 V, V_{DS} = 3.5 V	30	–	–	μA	7
Source current CO	I_{COH}	V_{CO} = 3.0 V, V_{DS} = 3.5 V	30	–	–	μA	7
Leakage current CO	I_{COL}	V_{CO} = 24 V, V_{DS} = 4.5 V	–	–	0.1	μA	8
Source current DO	I_{DOH}	V_{DO} = 3.0 V, V_{DS} = 3.5 V	30	–	–	μA	7
Leakage current DO	I_{DOL}	V_{DO} = 24 V, V_{DS} = 1.8 V	–	–	0.1	μA	8

***1.** In the S-8209B Series, users are able to set delay time for the output pins. By using the following formula, delay time is calculated with the value of CDT pin's resistance in the IC (R_{CDT}) and the value of capacitor set externally at the CDT pin (C_{CDT}).

$$t_D\,[s] = -\ln(1 - V_{CDET} / V_{DS}) \times C_{CDT}\,[\mu F] \times R_{CDT}\,[M\Omega]$$
$$= -\ln(1 - 0.7\text{ (typ.)}) \times C_{CDT}\,[\mu F] \times 8.31\text{ M}\Omega\text{ (typ.)}$$
$$= 10.0\text{ M}\Omega\text{ (typ.)} \times C_{CDT}\,[\mu F]$$

In case of the capacitance of CDT pin C_{CDT} = 0.01 μF, the output pin delay time t_D is calculated by using the above formula and as follows.

$$t_D\,[s] = 10.0\text{ M}\Omega\text{ (typ.)} \times 0.01\ \mu F = 0.1\text{ s (typ.)}$$

Test R_{CDT} and the CDT pin detection voltage (V_{CDET}) by test circuits shown in this datasheet after applying the power supply while pulling-up the CTLC pin, CTLD pin to the level of VDD pin outside the IC.

***2.** In case of using CTLC pin, CTLD pin pulled-up to the level of VDD pin externally, the current flows from the VSS pin (I_{SS}) is calculated by the following formula.

$$I_{SS} = I_{OPE} + I_{CTLCL} + I_{CTLDL}$$

■ Test Circuits

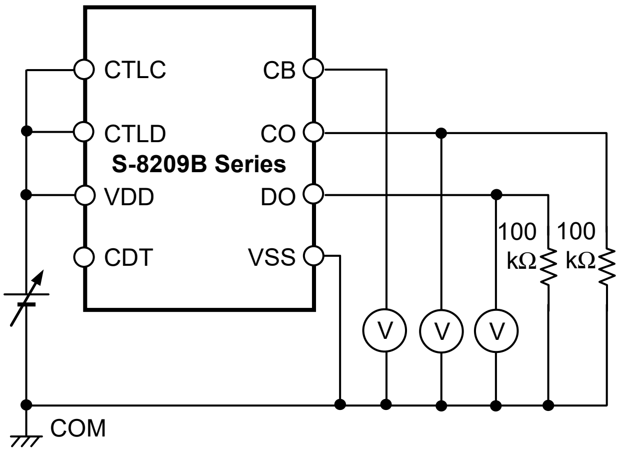


Figure 7 Test circuit 1

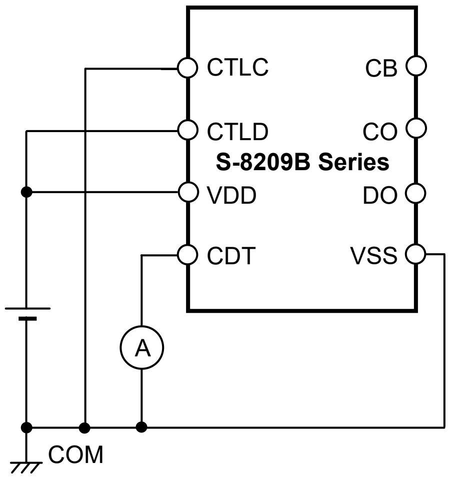


Figure 8 Test circuit 2

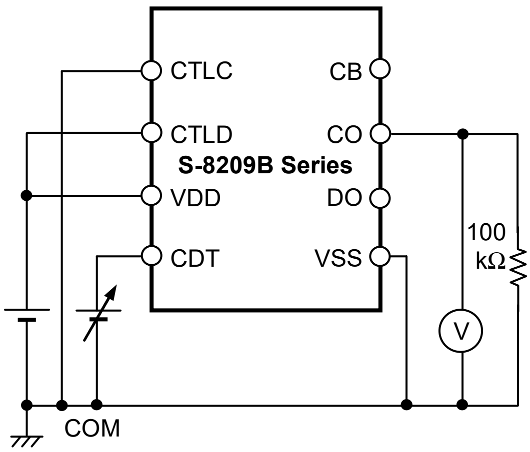


Figure 9 Test circuit 3

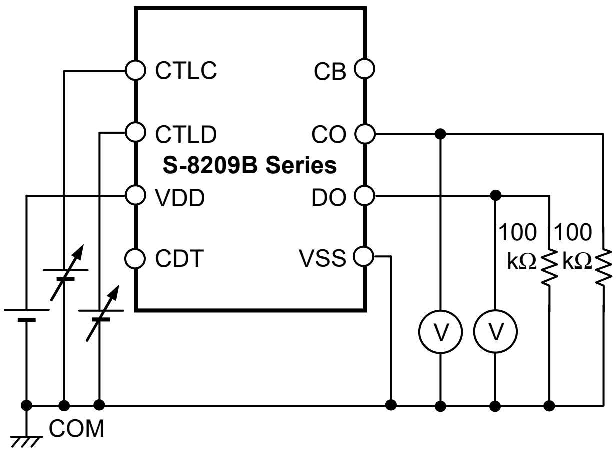


Figure 10 Test circuit 4

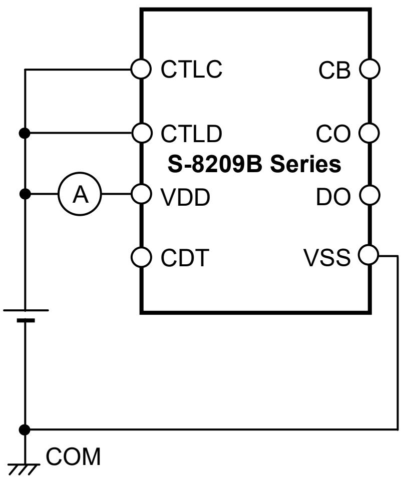


Figure 11 Test circuit 5

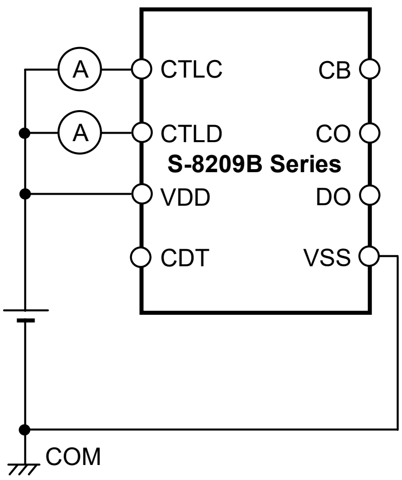


Figure 12 Test circuit 6

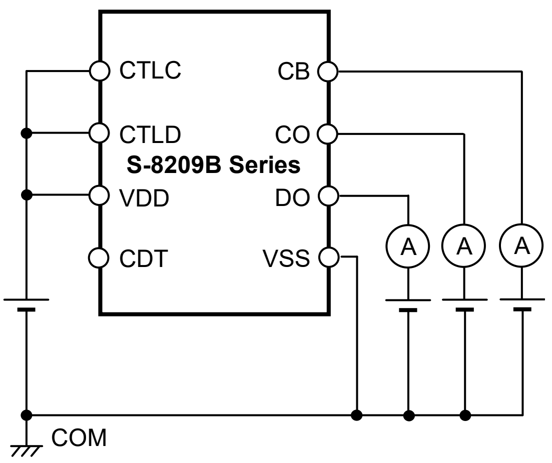


Figure 13 Test circuit 7

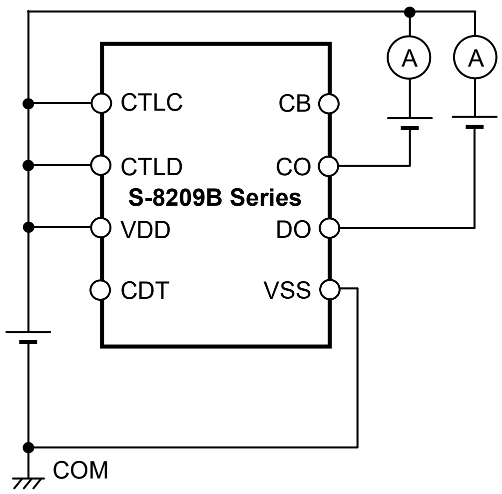
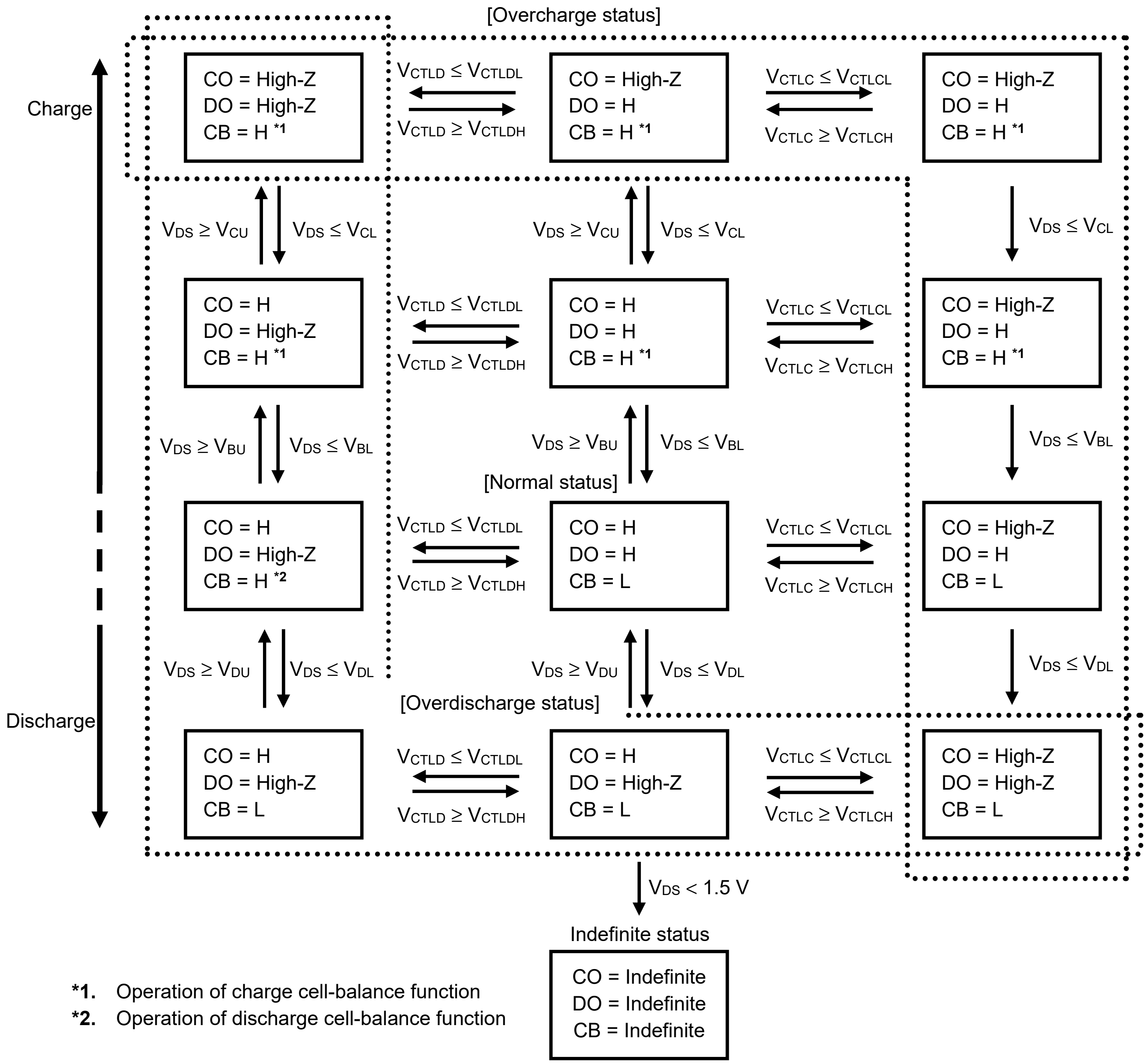


Figure 14 Test circuit 8

■ Operation

Figure 15 shows the operation transition of the S-8209B Series



***1.** Operation of charge cell-balance function
***2.** Operation of discharge cell-balance function

Figure 15 Operation Transition

1. Normal status

In the S-8209B Series, both of CO and DO pin get the V_{DD} level; the voltage between VDD and VSS (V_{DS}) is more than the overdischarge detection voltage (V_{DL}), and is less than the overcharge detection voltage (V_{CU}) and respectively, the CTLC pin input voltage (V_{CTLC}) > the CTLC pin voltage "L" (V_{CTLCL}), the CTLD pin input voltage (V_{CTLD}) > the CTLD pin voltage "L" (V_{CTLDL}). This is the normal status.

2. Overcharge status

In the S-8209B Series, the CO pin is in high impedance; when V_{DS} gets V_{CU} or more, or V_{CTLC} gets V_{CTLCL} or less. This is the overcharge status.

If V_{DS} gets the overcharge release voltage (V_{CL}) or less, and V_{CTLC} gets the CTLC pin voltage "H" (V_{CTLCH}) or more, the S-8209B Series releases the overcharge status to return to the normal status.

3. Overdischarge status

In the S-8209B Series, the DO pin is in high impedance; when V_{DS} gets V_{DL} or less, or V_{CTLD} gets V_{CTLDL} or less. This is the overdischarge status.

If V_{DS} gets the overdischarge release voltage (V_{DU}) or more, and V_{CTLD} gets the CTLD pin voltage "H" (V_{CTLDH}) or more, the S-8209B Series releases the overdischarge status to return to the normal status.

4. Cell-balance function

In the S-8209B Series, the CB pin gets the level of VDD pin; when V_{DS} gets the cell-balance detection voltage (V_{BU}) or more. This is the charge cell-balance function.
If V_{DS} gets the cell-balance release voltage (V_{BL}) or less again, the S-8209B Series sets the CB pin the level of VSS pin.

In addition, the CB pin gets the level of VDD pin; when V_{DS} is more than V_{DL}, and V_{CTLD} is V_{CTLDL} or less. This is the discharge cell-balance function.
If V_{CTLD} gets V_{CTLDH} or more, or V_{DS} is V_{DL} or less again, the S-8209B Series sets the CB pin the level of VSS pin.

5. Delay circuit

In the S-8209B Series, users are able to set delay time which is from detection of changes in V_{DS}, V_{CTLC}, V_{CTLD} to output to the CO, DO, CB pin.

For example in the detection of overcharge status, when V_{DS} exceeds V_{CU}, or V_{CTLC} gets V_{CTLCH} or less, charging to C_{CDT} starts via R_{CDT}. If the voltage between CDT and VSS (V_{CDT}) reaches the CDT pin detection voltage (V_{CDET}), the CO pin is in high impedance. The output pin delay time t_D is calculated by the following formula.

$$t_D\ [s] = 10.0\ M\Omega\ (typ.) \times C_{CDT}\ [\mu F]$$

The electric charge in C_{CDT} starts to be discharged when the delay time has finished.
The delay time that users have set for the CO pin, as seen above, is settable for each output pin DO, CB.

■ Battery Protection IC Connection Examples

Regarding the operation of protection circuit with the S-8209B Series for series-connected batteries, refer to the application note "**S-8209B Series Usage Guidelines**".

1. Example of Protection Circuit with the S-8209B Series (Without Discharge Cell-balance Function) for Series Multi-Cells

Figure 16 shows the example of protection circuit with the S-8209B Series (without discharge cell-balance function) for series multi-cells.

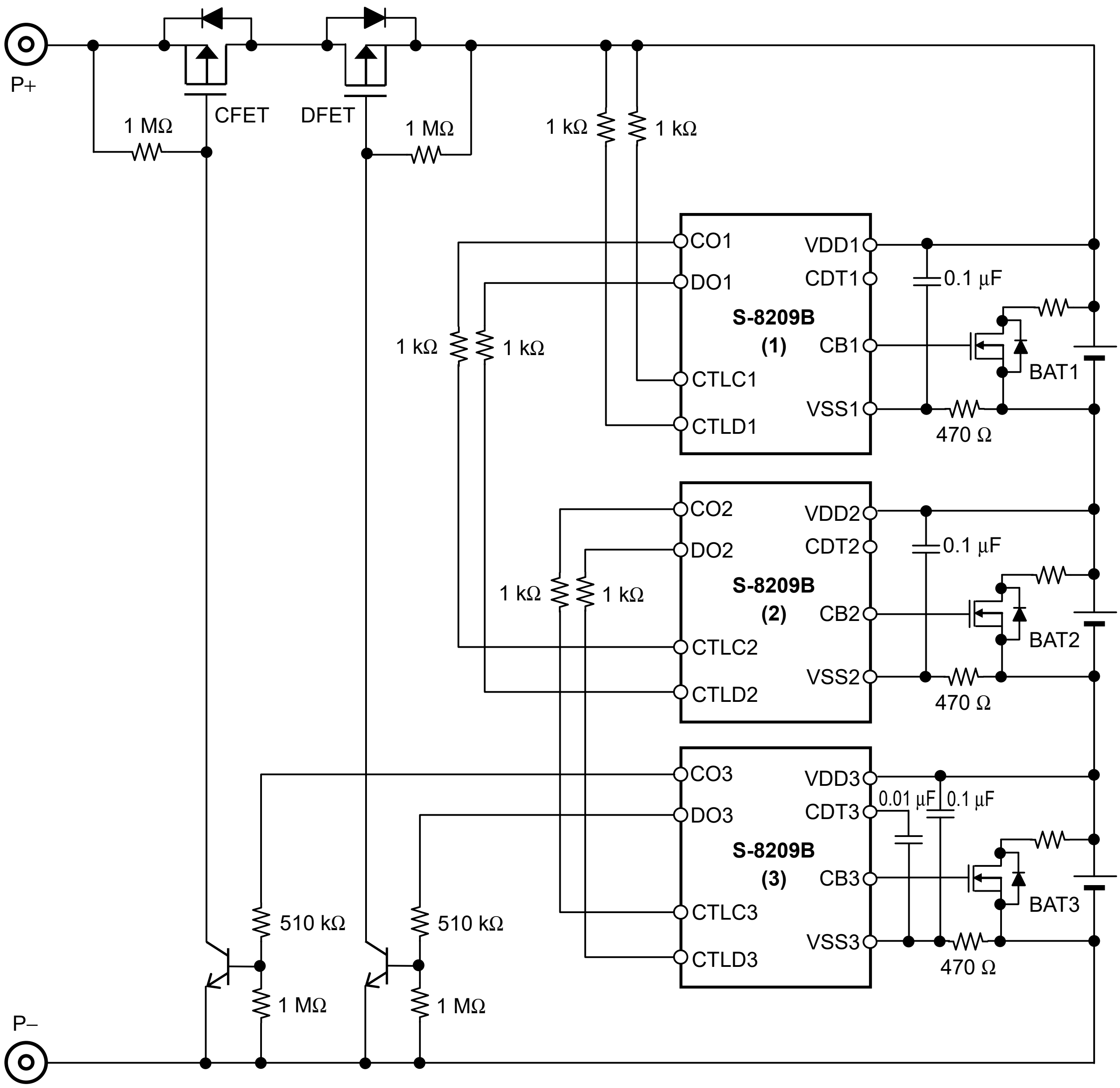


Figure 16

2. Example of Protection Circuit with the S-8209B Series (With Discharge Cell-balance Function) for Series Multi-Cells

Figure 17 shows the example of protection circuit with the S-8209B Series (with discharge cell-balance function) for series multi-cells.

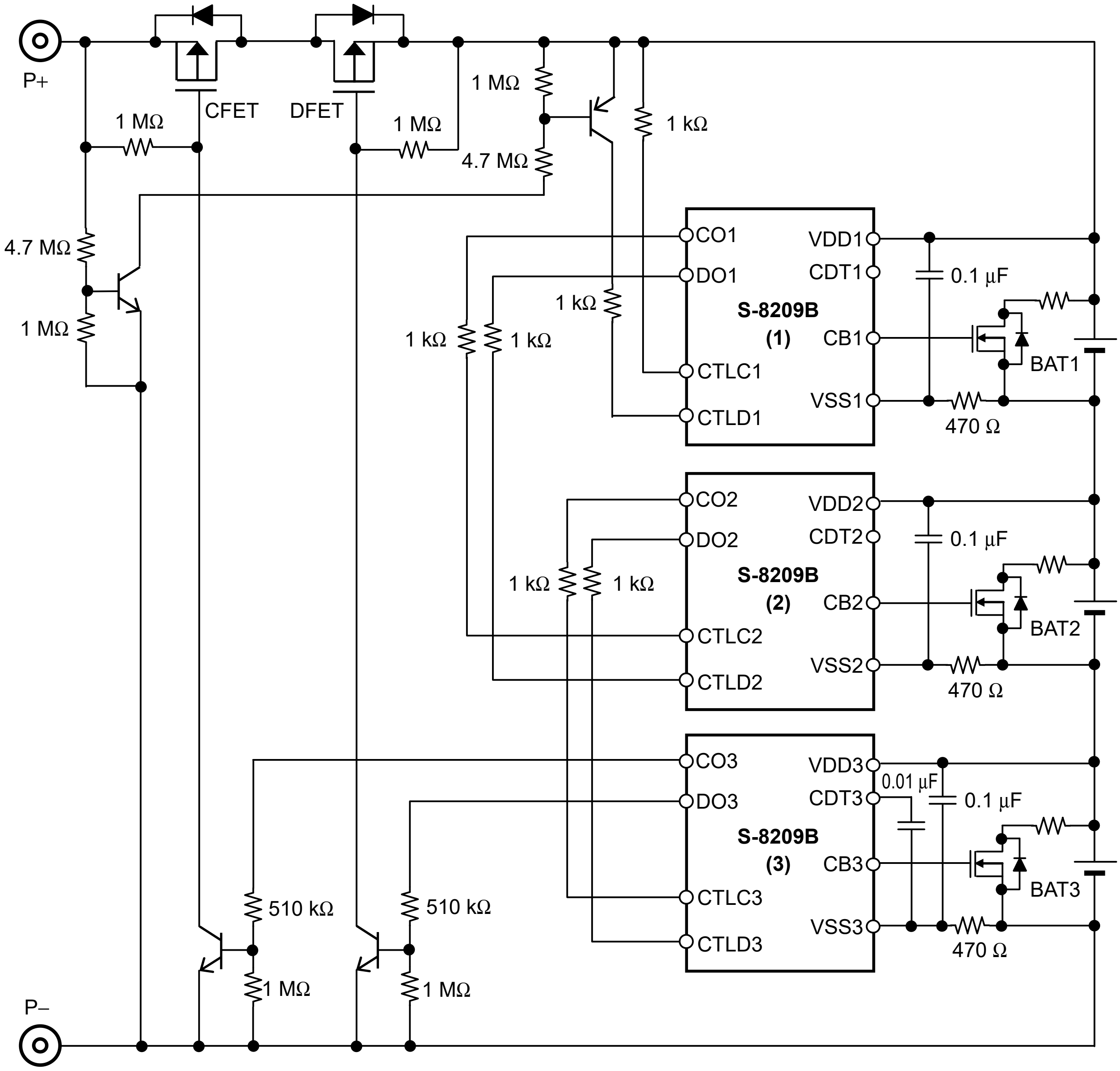


Figure 17

Caution 1. The constants may be changed without notice.

2. It has not been confirmed whether the operation is normal or not in circuits other than the connection examples. In addition, the connection examples and the constants do not guarantee proper operation. Perform thorough evaluation using the actual application to set the constants.

■ Precautions

- The application conditions for the input voltage, output voltage, and load current should not exceed the package power dissipation.
- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.
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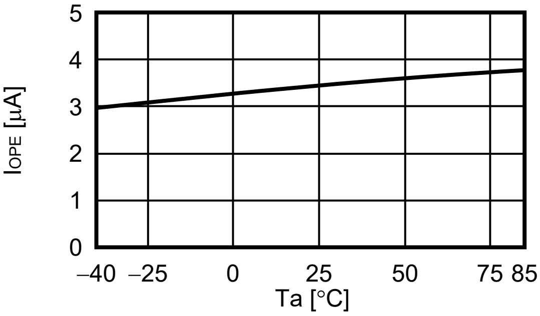
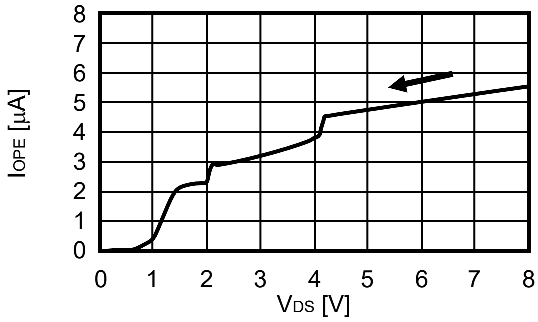
■ Characteristics (Typical Data)

1. Current consumption

1. 1 I_{OPE} vs. Ta

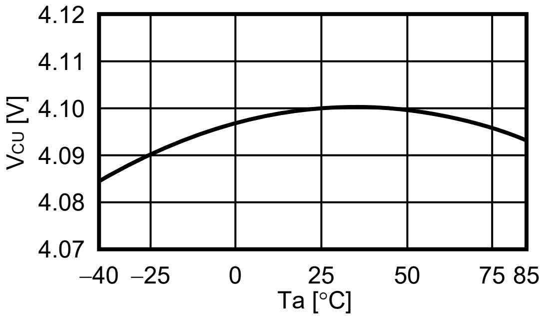


1. 2 I_{OPE} vs. V_{DS}

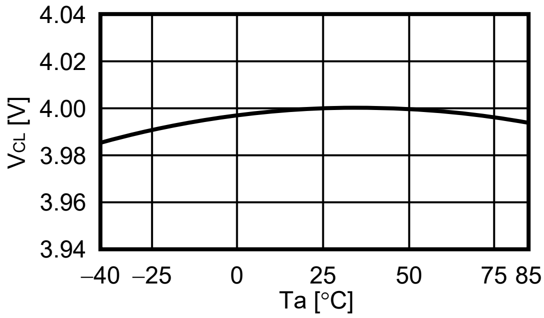


2. Overcharge detection / release voltages, Cell-balance detection / release voltages, Overdischarge detection / release voltages

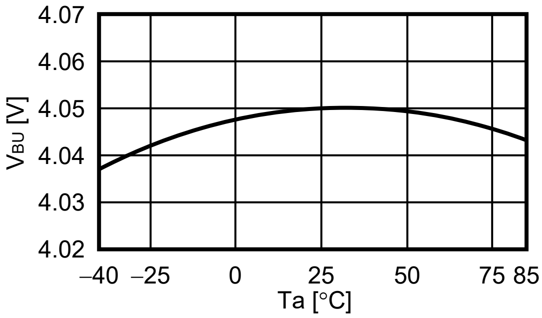
2. 1 V_{CU} vs. Ta



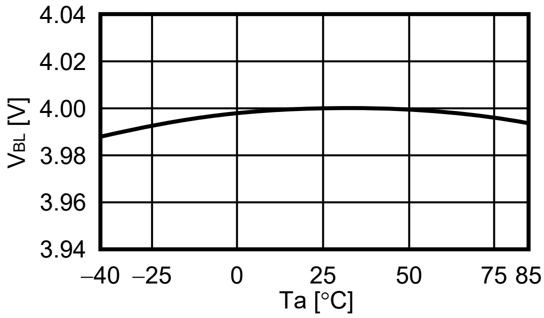
2. 2 V_{CL} vs. Ta



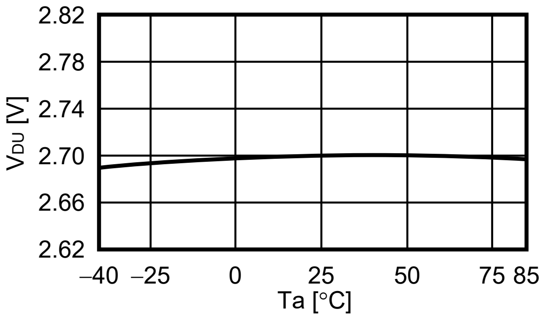
2. 3 V_{BU} vs. Ta



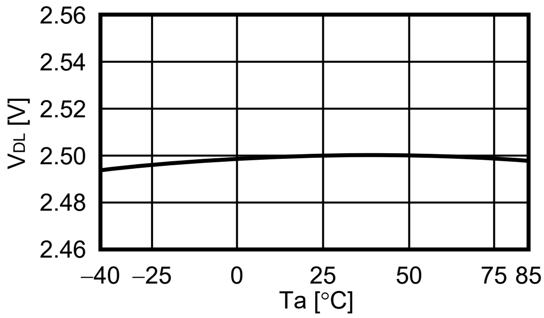
2. 4 V_{BL} vs. Ta



2. 5 V_{DU} vs. Ta

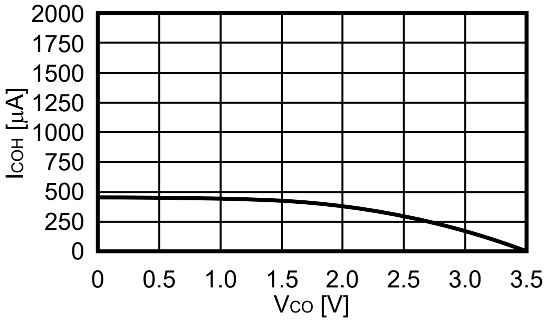


2. 6 V_{DL} vs. Ta

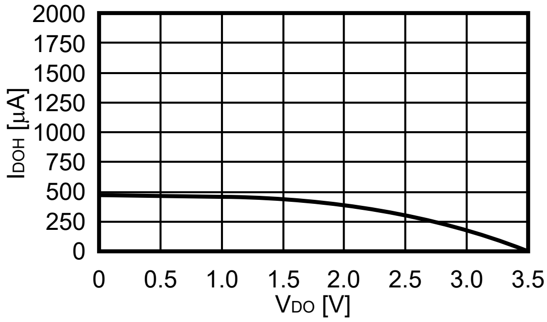


3. CO / DO / CB pin current

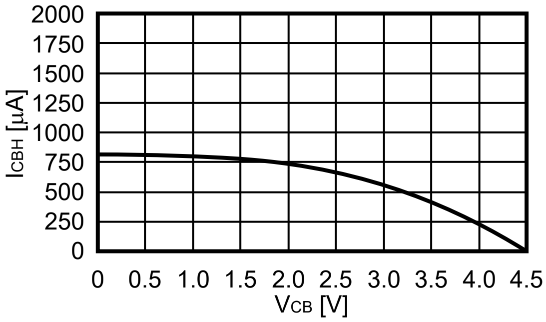
3. 1 I_{COH} vs. V_{CO} (V_{DS} = 3.5 V)



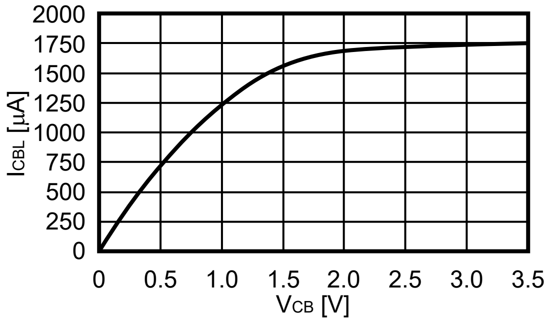
3. 2 I_{DOH} vs. V_{DO} (V_{DS} = 3.5 V)



3. 3 I_{CBH} vs. V_{CB} (V_{DS} = 4.5 V)

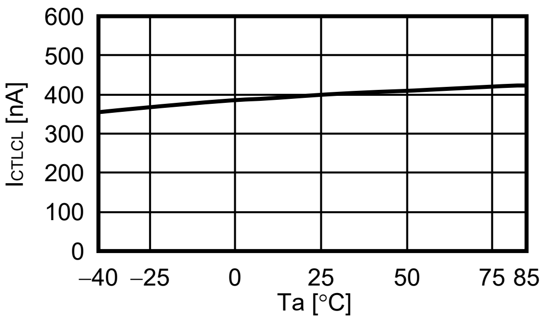


3. 4 I_{CBL} vs. V_{CB} (V_{DS} = 3.5 V)

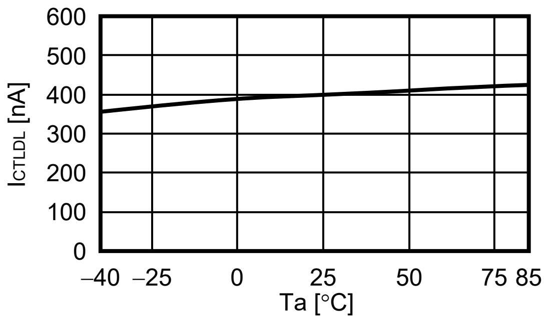


4. CTLC / CTLD pin current

4. 1 I_{CTLCL} vs. Ta (V_{DS} = 3.5 V)

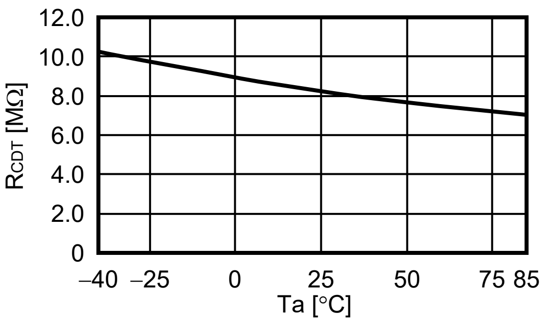


4. 2 I_{CTLDL} vs. Ta (V_{DS} = 3.5 V)

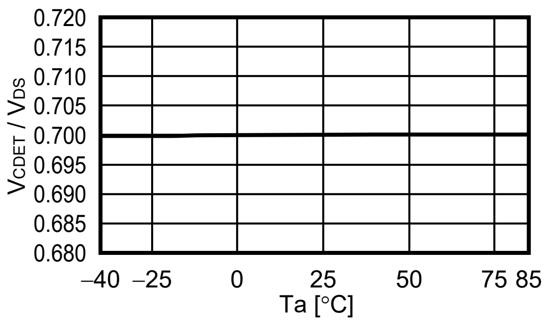


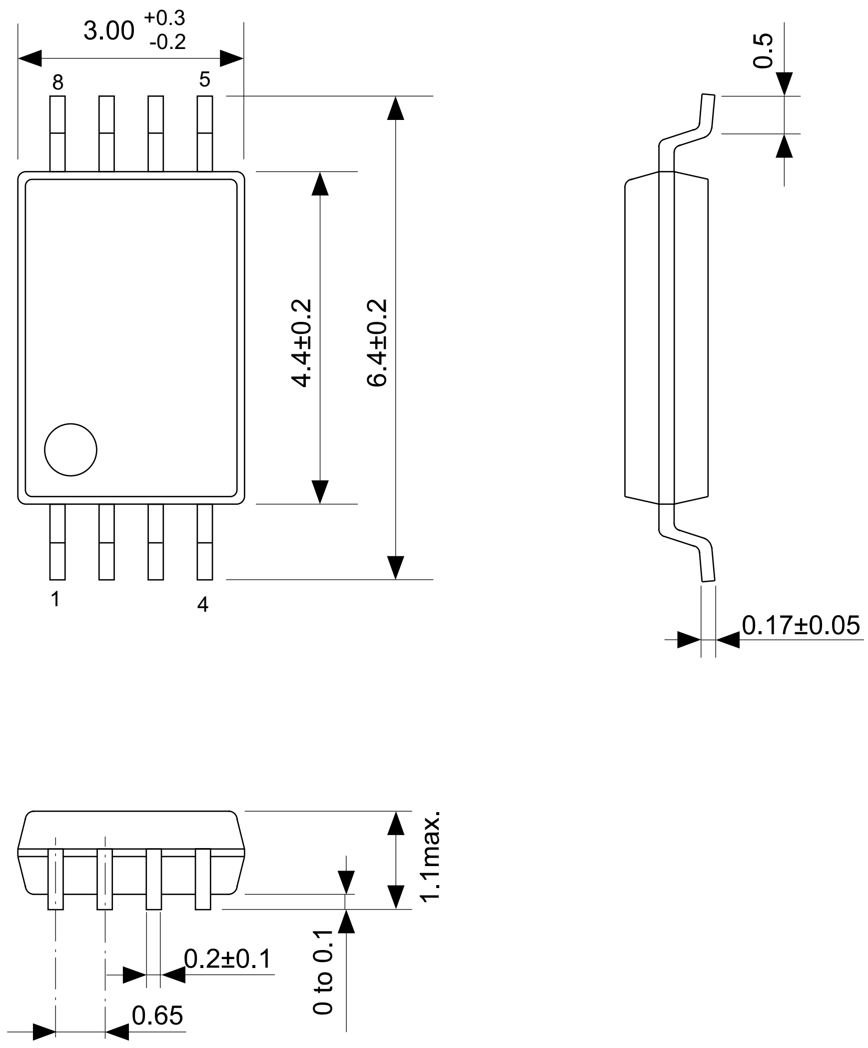
5. CDT pin resistance / CDT pin detection voltage

5. 1 R_{CDT} vs. Ta



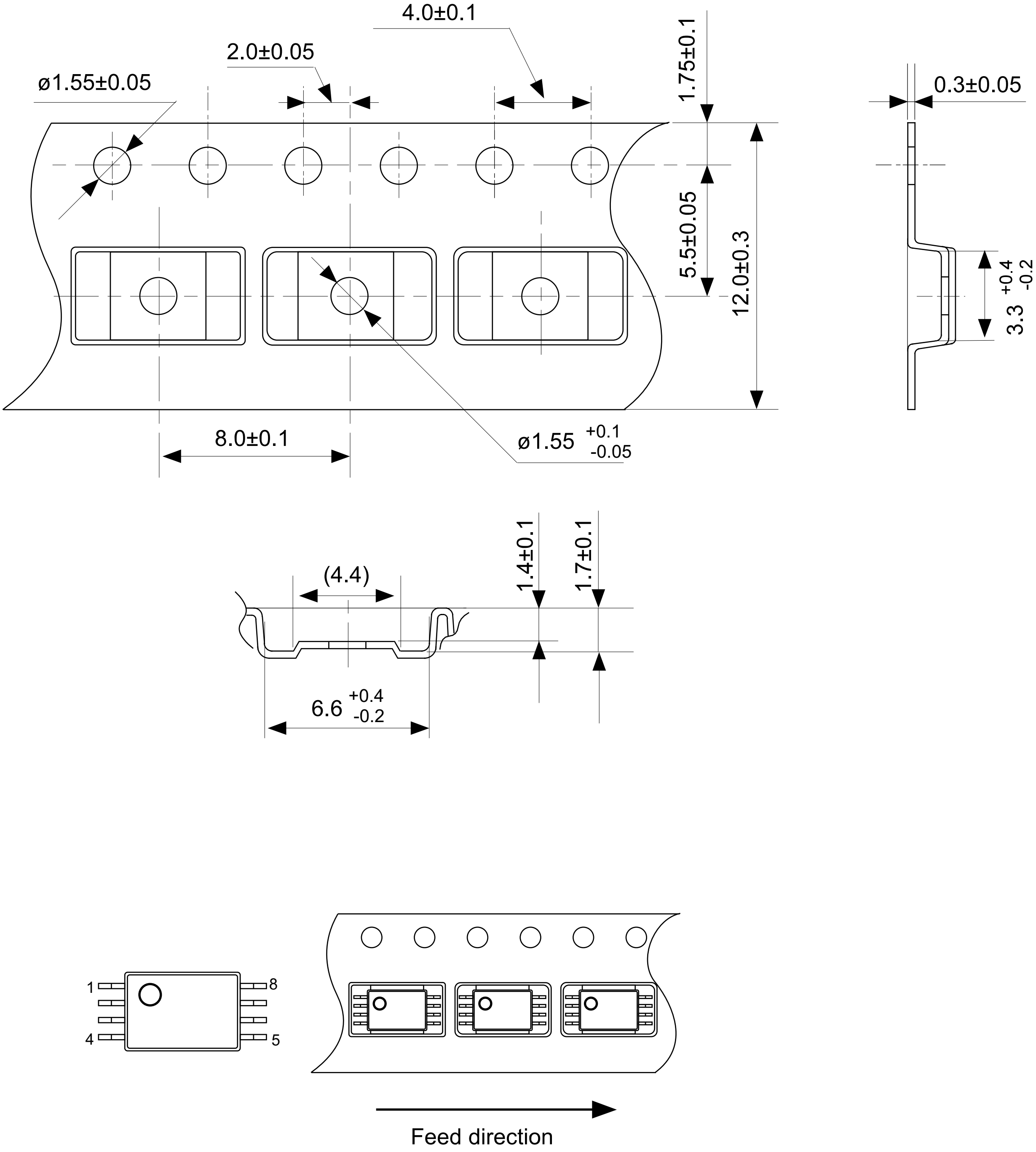
5. 2 V_{CDET} / V_{DS} vs. Ta





No. FT008-A-P-SD-1.2

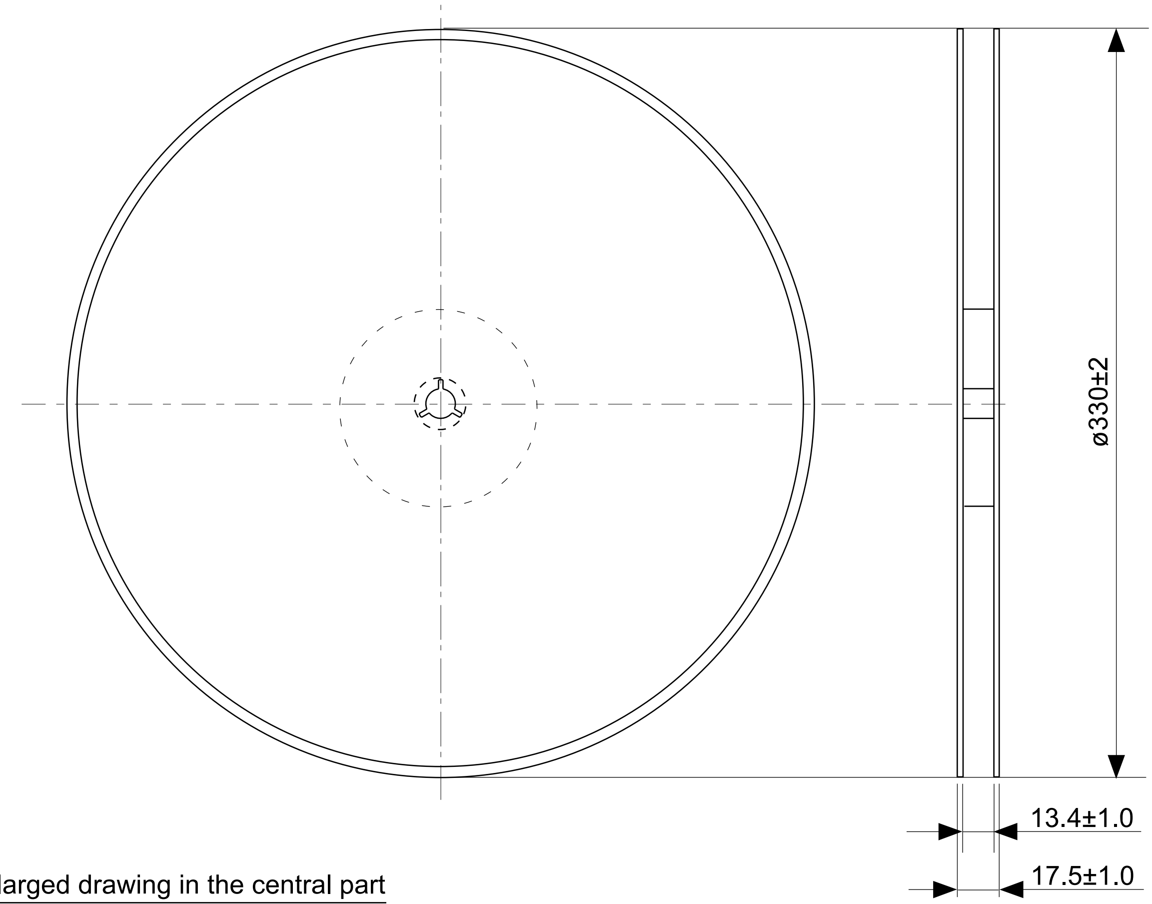
TITLE	TSSOP8-E-PKG Dimensions
No.	FT008-A-P-SD-1.2
ANGLE	
UNIT	mm
ABLIC Inc.	



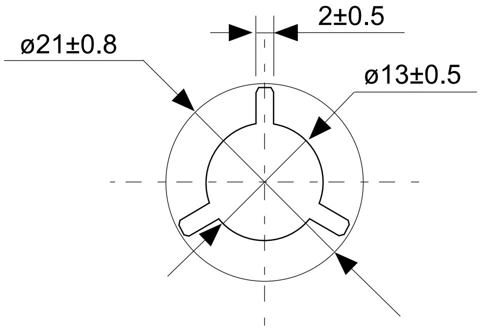
No. FT008-E-C-SD-1.0

TITLE	TSSOP8-E-Carrier Tape
No.	FT008-E-C-SD-1.0
ANGLE	
UNIT	mm

ABLIC Inc.



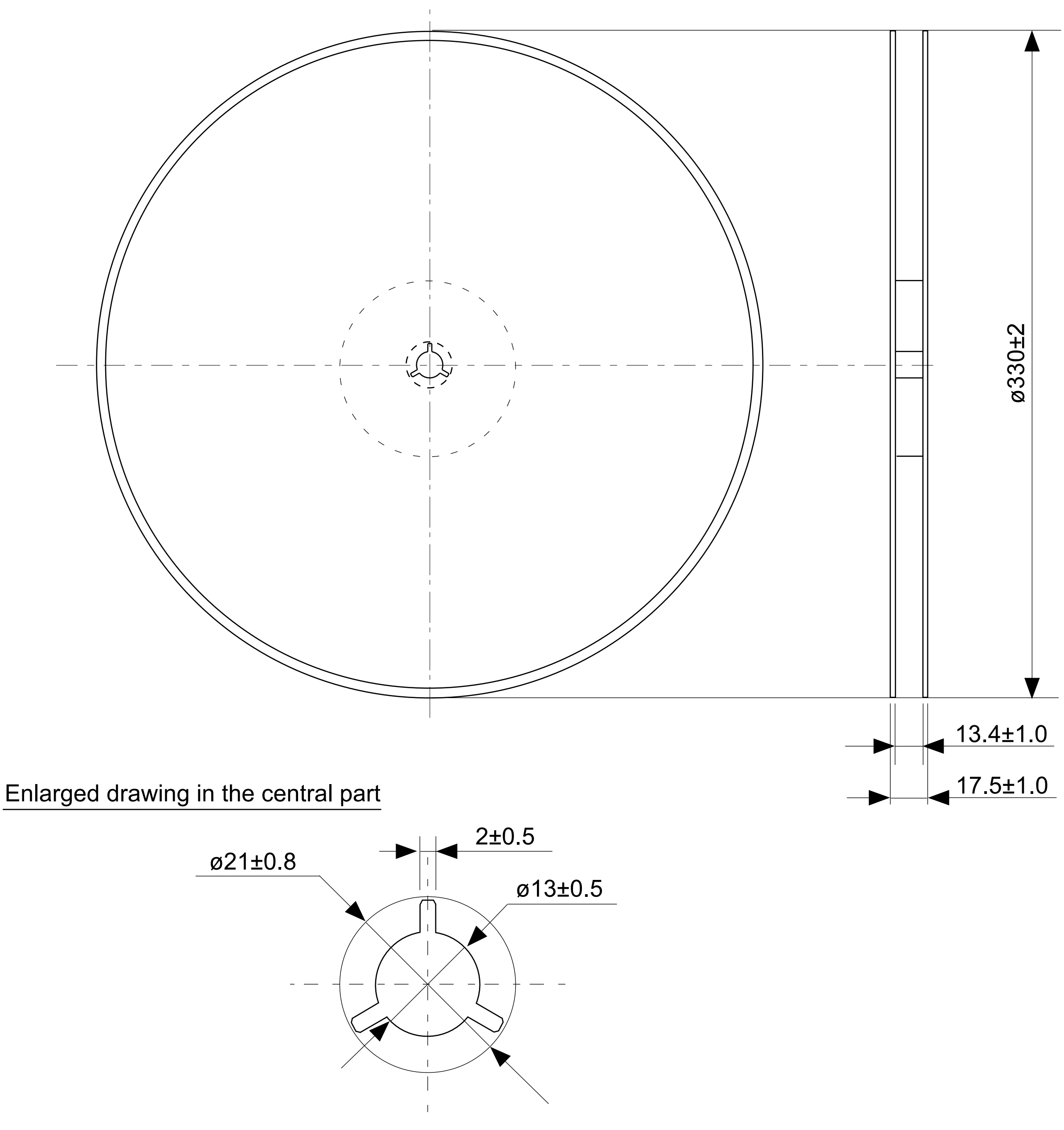
Enlarged drawing in the central part



No. FT008-E-R-SD-1.0

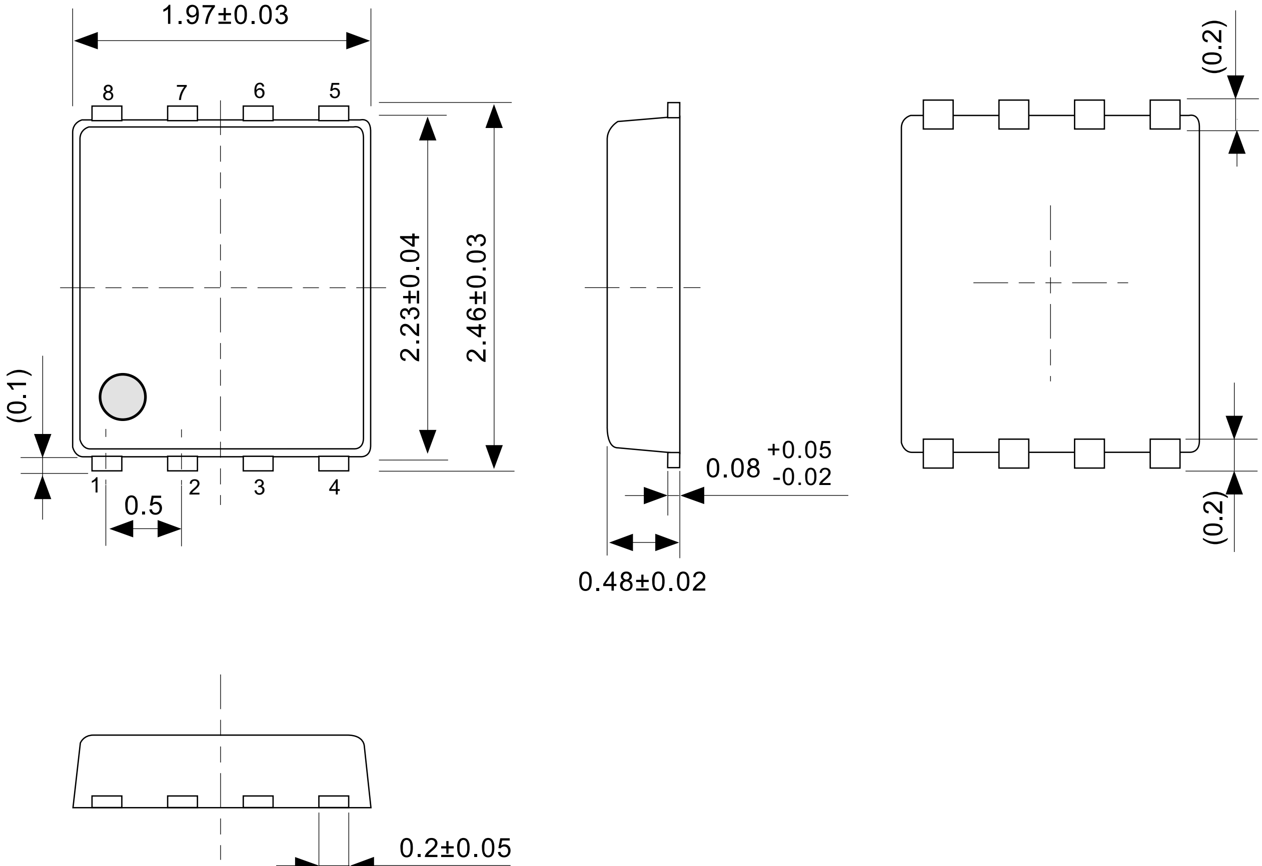
TITLE	TSSOP8-E-Reel		
No.	FT008-E-R-SD-1.0		
ANGLE		QTY.	3,000
UNIT	mm		

ABLIC Inc.



No. FT008-E-R-S1-1.0

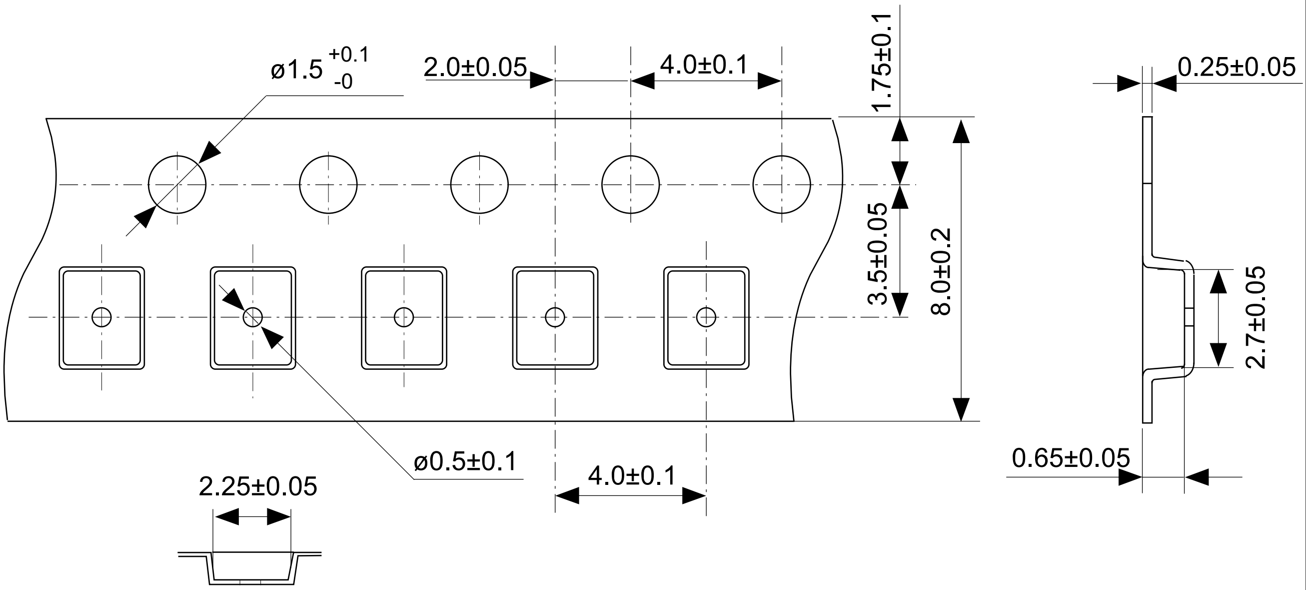
TITLE	TSSOP8-E-Reel		
No.	FT008-E-R-S1-1.0		
ANGLE		QTY.	4,000
UNIT	mm		
ABLIC Inc.			

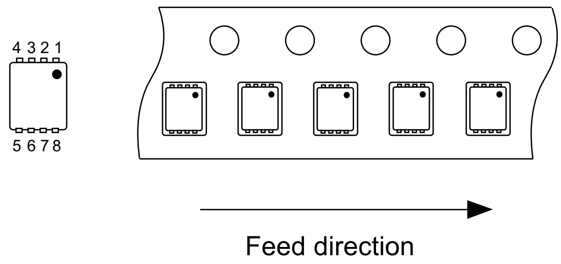


No. PH008-A-P-SD-2.1

TITLE	SNT-8A-A-PKG Dimensions
No.	PH008-A-P-SD-2.1
ANGLE	
UNIT	mm

ABLIC Inc.

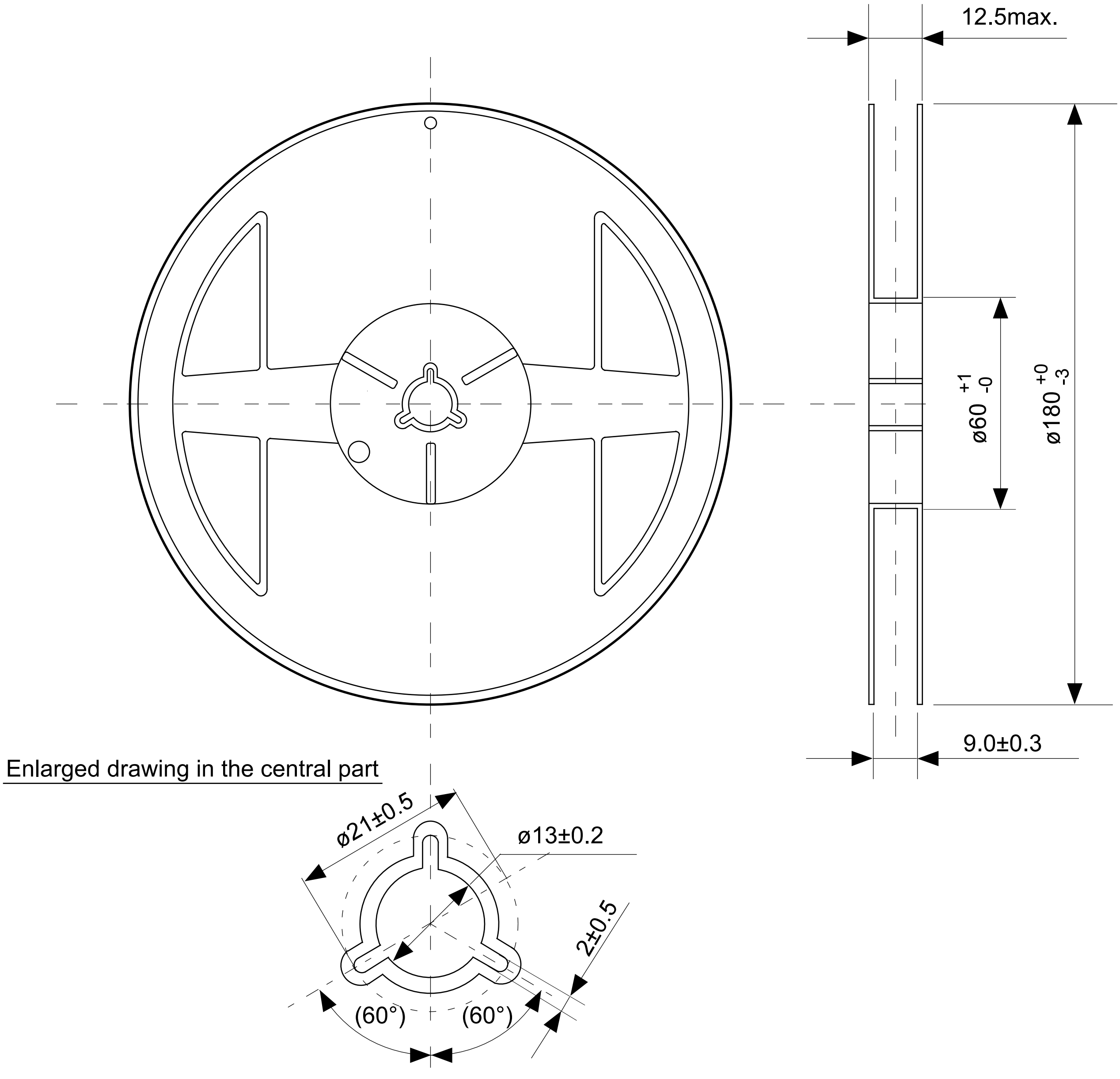




No. PH008-A-C-SD-2.0

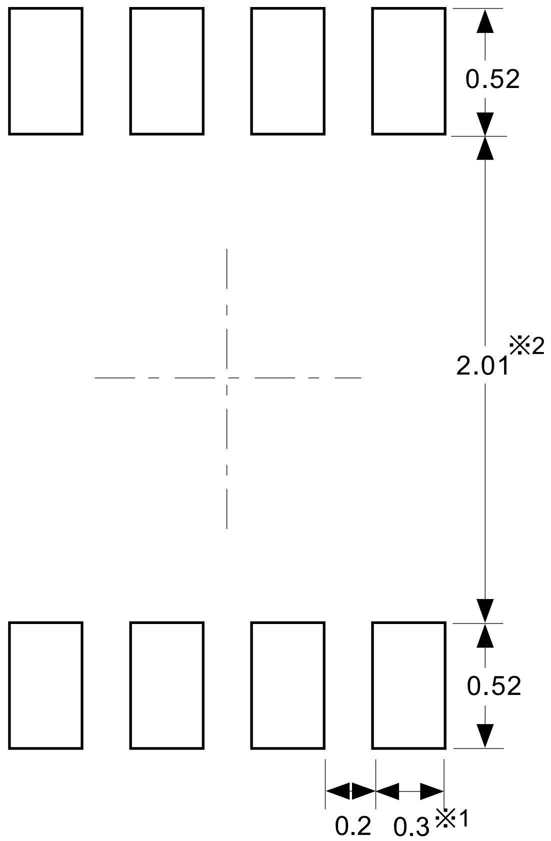
TITLE	SNT-8A-A-Carrier Tape
No.	PH008-A-C-SD-2.0
ANGLE	
UNIT	mm

ABLIC Inc.



No. PH008-A-R-SD-1.0

TITLE	SNT-8A-A-Reel		
No.	PH008-A-R-SD-1.0		
ANGLE		QTY.	5,000
UNIT	mm		
ABLIC Inc.			



※1. ランドパターンの幅に注意してください (0.25 mm min. / 0.30 mm typ.)。
※2. パッケージ中央にランドパターンを広げないでください (1.96 mm ~ 2.06 mm)。

注意 1. パッケージのモールド樹脂下にシルク印刷やハンダ印刷などしないでください。
2. パッケージ下の配線上のソルダーレジストなどの厚みをランドパターン表面から0.03 mm 以下にしてください。
3. マスク開口サイズと開口位置はランドパターンと合わせてください。
4. 詳細は〝SNTパッケージ活用の手引き〟を参照してください。

※1. Pay attention to the land pattern width (0.25 mm min. / 0.30 mm typ.).
※2. Do not widen the land pattern to the center of the package (1.96 mm to 2.06mm).

Caution 1. Do not do silkscreen printing and solder printing under the mold resin of the package.
2. The thickness of the solder resist on the wire pattern under the package should be 0.03 mm or less from the land pattern surface.
3. Match the mask aperture size and aperture position with the land pattern.
4. Refer to "SNT Package User's Guide" for details.

※1. 请注意焊盘模式的宽度 (0.25 mm min. / 0.30 mm typ.)。
※2. 请勿向封装中间扩展焊盘模式 (1.96 mm ~ 2.06 mm)。

注意 1. 请勿在树脂型封装的下面印刷丝网、焊锡。
2. 在封装下、布线上的阻焊膜厚度（从焊盘模式表面起）请控制在 0.03 mm 以下。
3. 钢网的开口尺寸和开口位置请与焊盘模式对齐。
4. 详细内容请参阅 "SNT 封装的应用指南"。

No. PH008-A-L-SD-4.1

TITLE	SNT-8A-A -Land Recommendation
No.	PH008-A-L-SD-4.1
ANGLE	
UNIT	mm

ABLIC Inc.

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2.4-2019.07

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