20-Bit, 1.8 MSPS/1 MSPS/500 kSPS, Easy Drive, Differential SAR ADCs

Data Sheet **AD4020/AD4021/AD4022**

FEATURES

- **Easy Drive**
  - Greatly reduced input kickback
    - Input current reduced to 0.5 µA/MSPS
  - Enhanced acquisition phase, ≥77% of cycle time at 1 MSPS
  - First conversion accurate, no latency or pipeline delay
  - Input span compression for single-supply operation
  - Fast conversion allows low SPI clock rates
  - Input overvoltage clamp protection sinks up to 50 mA
  - SPI-/QSPI-/MICROWIRE-/DSP-compatible serial interface
- **High performance**
  - Differential analog input range: $\pm V_{REF}$, V_{REF} from 2.4 V to 5.1 V
  - Throughput: 1.8 MSPS/1 MSPS/500 kSPS options
  - INL: ±3.1 ppm maximum
  - Guaranteed 20-bit no missing codes
  - SNR: 100.5 dB at f_{IN} = 1 kHz at V_{REF} 5 V
  - THD: −123 dB at f_{IN} = 1 kHz, −100 dB at f_{IN} = 100 kHz
  - SINAD: 89 dB at f_{IN} = 900 kHz (see Figure 17)
- **Oversampled dynamic range**
  - 104 dB for OSR = 2
  - 131 dB for OSR = 1024
- **Low power**
- **Single 1.8 V supply operation with 1.71 V to 5.5 V logic interface**
  - 2.7 mW at 500 kSPS (VDD only)
  - 83 µW at 10 kSPS, 15 mW at 1.8 MSPS (total power)
- **10-lead packages: 3 mm × 3 mm LFCSP, 3 mm × 4.90 mm MSOP**
  - Pin compatible with AD4003/AD4007/AD4011 family
- **Guaranteed operation: −40°C to +125°C**

APPLICATIONS

- **Automatic test equipment**
- **Machine automation**
- **Medical equipment**
- **Battery-powered equipment**
- **Precision data acquisition systems**
- **Instrumentation and control systems**

FUNCTIONAL BLOCK DIAGRAM

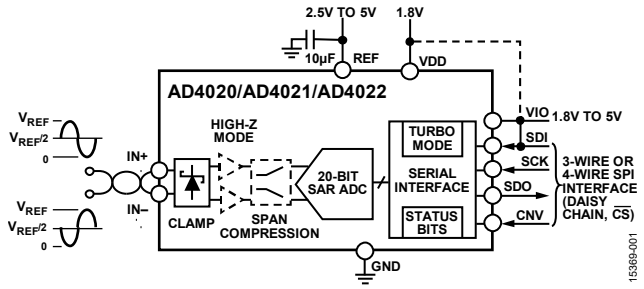

Figure 1.

GENERAL DESCRIPTION

The AD4020/AD4021/AD4022 are high accuracy, high speed, low power, 20-bit, Easy Drive, precision successive approximation register (SAR) analog-to-digital converters (ADCs) that operate from a single power supply, VDD. The reference voltage, V_{REF}, is applied externally and can be set independent of the supply voltage. The AD4020/AD4021/AD4022 power scales linearly with throughput.

Easy Drive features reduce both signal chain complexity and power consumption while enabling higher channel density. The reduced input current, particularly in high-Z mode, coupled with a long signal acquisition phase, eliminates the need for a dedicated ADC driver. Easy Drive broadens the range of companion circuitry that is capable of driving these ADCs (see Figure 2).

Input span compression eliminates the need to provide a negative supply to the ADC driver amplifier while preserving access to the full ADC code range. The input overvoltage clamp protects the ADC inputs against overvoltage events, minimizing disturbances on the reference pin, and eliminating the need for external protection diodes.

Fast device throughput up to 1.8 MSPS allows users to accurately capture high frequency signals and to implement oversampling techniques to alleviate the challenges associated with antialias filter designs. Decreased serial peripheral interface (SPI) clock rate requirements reduce digital input/output power consumption, broadens digital host options, and simplifies the task of sending data across digital isolation. The SPI-compatible serial user interface is compatible with 1.8 V, 2.5 V, 3 V, and 5 V logic by using the separate VIO logic supply.

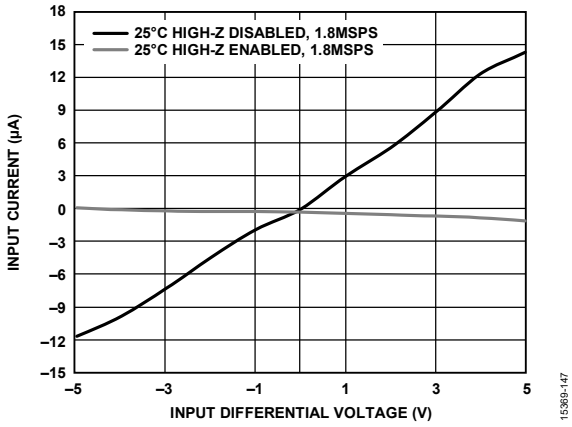

Figure 2. Input Current vs. Input Differential Voltage

Rev. B Document Feedback

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7/2017—Rev. 0 to Rev. A
Change to Integral Nonlinearity Error (INL) Parameter, Table 1 3

7/2017—Revision 0: Initial Version

SPECIFICATIONS

VDD = 1.71 V to 1.89 V, VIO = 1.71 V to 5.5 V, REF pin voltage (V_{REF}) = 5 V, all specifications T_{MIN} to T_{MAX}, high-Z mode disabled, span compression disabled, turbo mode enabled, and sampling frequency (f_S) = 1.8 MSPS for the AD4020, f_S = 1 MSPS for the AD4021, and f_S = 500 kSPS for the AD4022, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
RESOLUTION		20			Bits
ANALOG INPUT					
Voltage Range	IN+ voltage (V_{IN+}) – IN– voltage (V_{IN-})	$-V_{REF}$		$+V_{REF}$	V
	Span compression enabled	$-V_{REF} \times 0.8$		$+V_{REF} \times 0.8$	V
Operating Input Voltage	V_{IN+}, V_{IN-} to GND	−0.1		$+V_{REF}$ + 0.1	V
	Span compression enabled	$0.1 \times V_{REF}$		$0.9 \times V_{REF}$	V
Common-Mode Input Range		$V_{REF}/2 - 0.125$	$V_{REF}/2$	$V_{REF}/2 + 0.125$	V
Common-Mode Rejection Ratio (CMRR)	Input frequency (f_{IN}) = 500 kHz		68		dB
Analog Input Current	Acquisition phase, T_A = 25°C		0.3		nA
	High-Z mode enabled, converting dc input at 1.8 MSPS		1		µA
THROUGHPUT					
Complete Cycle					
AD4020		555			ns
AD4021		1000			ns
AD4022		2000			ns
Conversion Time		300	320	350	ns
Acquisition Phase[1]					
AD4020		325			ns
AD4021		770			ns
AD4022		1770			ns
Throughput Rate[2] (f_S)					
AD4020		0		1.8	MSPS
AD4021		0		1	MSPS
AD4022		0		500	kSPS
Transient Response[3]			325		ns
DC ACCURACY					
No Missing Codes		20			Bits
Integral Nonlinearity Error (INL)		−3.1	±1	+3.1	ppm
	T = 0°C to 70°C	−2	±1	+2	ppm
Differential Nonlinearity Error (DNL)		−0.5	±0.3	+0.5	LSB
Transition Noise			3.3		LSB
Zero Error		−35		+35	LSB
Zero Error Drift[4]		−0.3		+0.3	ppm/°C
Gain Error		−88	±12	+88	LSB
Gain Error Drift[4]		−1.2		+1.2	ppm/°C
Power Supply Sensitivity	VDD = 1.8 V ± 5%		±6		LSB
1/f Noise[5]	Bandwidth = 0.1 Hz to 10 Hz		6		µV p-p

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
AC ACCURACY					
Dynamic Range			101		dB
Oversampled Dynamic Range	Oversampling ratio (OSR) = 2		104		dB
	OSR = 256		125		dB
	OSR = 1024		131		dB
Total RMS Noise			31.5		µV rms
f_{IN} = 1 kHz, −0.5 dBFS, V_{REF} = 5 V					
Signal-to-Noise Ratio (SNR)		99	100.5		dB
Spurious-Free Dynamic Range (SFDR)			122		dB
Total Harmonic Distortion (THD)			−123		dB
Signal-to-Noise-and-Distortion Ratio (SINAD)		98.5	100		dB
f_{IN} = 1 kHz, −0.5 dBFS, V_{REF} = 2.5 V					
SNR		93.3	94.7		dB
SFDR			122		dB
THD			−119		dB
SINAD		93	94.5		dB
f_{IN} = 100 kHz, −0.5 dBFS, V_{REF} = 5 V					
SNR			99		dB
THD			−100		dB
SINAD			96.5		dB
f_{IN} = 400 kHz, −0.5 dBFS, V_{REF} = 5 V					
SNR			92.5		dB
THD			−94		dB
SINAD			90		dB
−3 dB Input Bandwidth			10		MHz
Aperture Delay			1		ns
Aperture Jitter			1		ps rms
REFERENCE					
Voltage Range (V_{REF})		2.4		5.1	V
Current	V_{REF} = 5 V				
AD4020	1.8 MSPS		1.1		mA
AD4021	1 MSPS		0.58		mA
AD4022	500 kSPS		0.32		mA
INPUT OVERVOLTAGE CLAMP					
IN+/IN− Current (I_{IN+}/I_{IN-})	V_{REF} = 5 V			50	mA
	V_{REF} = 2.5 V			50	mA
V_{IN+}/V_{IN-} at Maximum I_{IN+}/I_{IN-}	V_{REF} = 5 V		5.4		V
	V_{REF} = 2.5 V		3.1		V
V_{IN+}/V_{IN-} Clamp On/Off Threshold	V_{REF} = 5 V	5.25	5.4		V
	V_{REF} = 2.5 V	2.68	2.8		V
Deactivation Time			360		ns
REF Current at Maximum I_{IN+}/I_{IN-}	V_{IN+}/V_{IN-} > V_{REF}		100		µA
DIGITAL INPUTS					
Logic Levels					
Input Voltage Low (V_{IL})	VIO > 2.7 V	−0.3		+0.3 × VIO	V
	VIO ≤ 2.7 V	−0.3		+0.2 × VIO	V
Input Voltage High (V_{IH})	VIO > 2.7 V	0.7 × VIO		VIO + 0.3	V
	VIO ≤ 2.7 V	0.8 × VIO		VIO + 0.3	V
Input Current Low (I_{IL})		−1		+1	µA
Input Current High (I_{IH})		−1		+1	µA
Input Pin Capacitance			6		pF

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DIGITAL OUTPUTS					
Data Format			Serial, 20 bits, twos complement		
Pipeline Delay			Conversion results available immediately after completed conversion		
Output Voltage Low (V_{OL})	Output current = 500 µA			0.4	V
Output Voltage High (V_{OH})	Output current = −500 µA	VIO − 0.3			V
POWER SUPPLIES					
VDD		1.71	1.8	1.89	V
VIO		1.71		5.5	V
Standby Current	VDD = 1.8 V, VIO = 1.8 V, T_A = 25°C		1.6		µA
Power Dissipation	VDD = 1.8 V, VIO = 1.8 V, V_{REF} = 5 V				
	10 kSPS, high-Z mode disabled		83		µW
	500 kSPS, high-Z mode disabled		4.5	5.1	mW
	1 MSPS, high-Z mode disabled		8.3	10	mW
	1.8 MSPS, high-Z mode disabled		15	19	mW
	500 kSPS, high-Z mode enabled		5.7	6.9	mW
	1 MSPS, high-Z mode enabled		10.8	13	mW
	1.8 MSPS, high-Z mode enabled		19	25	mW
VDD Only	500 kSPS, high-Z mode disabled		2.7		mW
	1 MSPS, high-Z mode disabled		5.1		mW
	1.8 MSPS, high-Z mode disabled		9.0		mW
REF Only	500 kSPS, high-Z mode disabled		1.6		mW
	1 MSPS, high-Z mode disabled		2.9		mW
	1.8 MSPS, high-Z mode disabled		5.0		mW
VIO Only	500 kSPS, high-Z mode disabled		0.13		mW
	1 MSPS, high-Z mode disabled		0.4		mW
	1.8 MSPS, high-Z mode disabled		1.0		mW
Energy per Conversion			8.3		nJ/sample
TEMPERATURE RANGE					
Specified Performance	T_{MIN} to T_{MAX}	−40		+125	°C

[1] The acquisition phase is the time available for the input sampling capacitors to acquire a new input with the ADC running at a throughput rate of 1.8 MSPS for the AD4020, 1 MSPS for the AD4021, and 500 kSPS for the AD4022.
[2] A throughput rate of 1.8 MSPS can only be achieved with turbo mode enabled and a minimum serial clock (SCK) rate of 71 MHz. Refer to Table 4 for the maximum achievable throughput for different modes of operation.
[3] Transient response is the time required for the ADC to acquire a full-scale input step to ±2 LSB accuracy.
[4] The minimum and maximum values are guaranteed by characterization, but not production tested.
[5] See the 1/f noise plot in Figure 25.

TIMING SPECIFICATIONS

VDD = 1.71 V to 1.89 V, VIO = 1.71 V to 5.5 V, V_{REF} = 5 V, all specifications T_{MIN} to T_{MAX}, high-Z mode disabled, span compression disabled, turbo mode enabled, and f_S = 1.8 MSPS for the AD4020, f_S = 1 MSPS for the AD4021, and f_S = 500 kSPS for the AD4022, unless otherwise noted. See Figure 49 to Figure 52, Figure 54, Figure 56, Figure 58, Figure 60, Figure 62, Figure 64, and Figure 66 for timing diagrams.

Table 2. Digital Interface Timing

Parameter[1]	Symbol	Min	Typ	Max	Unit
CONVERSION TIME—CNV RISING EDGE TO DATA AVAILABLE	t_{CONV}	300	320	350	ns
ACQUISITION PHASE[2]	t_{ACQ}				
AD4020		325			ns
AD4021		770			ns
AD4022		1770			ns
TIME BETWEEN CONVERSIONS	t_{CYC}				
AD4020		555			ns
AD4021		1000			ns
AD4022		2000			ns
CNV PULSE WIDTH ($\overline{CS}$ MODE)[3]	t_{CNVH}	10			ns
SCK PERIOD	t_{SCK}				
$\overline{CS}$ Mode[4]					
VIO > 2.7 V		9.8			ns
VIO > 1.7 V		12.3			ns
Daisy-Chain Mode[5]					
VIO > 2.7 V		20			ns
VIO > 1.7 V		25			ns
SCK					
Low Time	t_{SCKL}	3			ns
High Time	t_{SCKH}	3			ns
Falling Edge to Data Remains Valid Delay	t_{HSDO}	1.5			ns
Falling Edge to Data Valid Delay	t_{DSDO}				
VIO > 2.7 V				7.5	ns
VIO > 1.7 V				10.5	ns
CNV OR SDI LOW TO SDO D17 MSB VALID DELAY ($\overline{CS}$ MODE)	t_{EN}				
VIO > 2.7 V				10	ns
VIO > 1.7 V				13	ns
CNV RISING EDGE TO FIRST SCK RISING EDGE DELAY	t_{QUIET1}	200			ns
LAST SCK FALLING EDGE TO CNV RISING EDGE DELAY[6]	t_{QUIET2}	60			ns
CNV OR SDI HIGH OR LAST SCK FALLING EDGE TO SDO HIGH IMPEDANCE ($\overline{CS}$ MODE)	t_{DIS}			20	ns
SDI					
Valid Setup Time from CNV Rising Edge	$t_{SSDICNV}$	2			ns
Valid Hold Time from CNV Rising Edge ($\overline{CS}$ Mode)	$t_{HSDICNV}$	2			ns
Valid Setup Time from SCK Rising Edge (Daisy-Chain Mode)	$t_{SSDISCK}$	2			ns
Valid Hold Time from SCK Rising Edge (Daisy-Chain Mode)	$t_{HSDISCK}$	2			ns
SCK VALID HOLD TIME FROM CNV RISING EDGE (DAISY-CHAIN MODE)	$t_{HSCKCNV}$	12			ns

[1] Timing parameters measured with respect to a falling edge are defined as triggered at X% VIO. Timing parameters measured with respect to a rising edge are defined as triggered at Y% VIO. For VIO ≤ 2.7 V, X = 80, and Y = 20. For VIO > 2.7 V, X = 70, and Y = 30. The minimum VIH and maximum VIL are used. See Digital Inputs Specifications in Table 1.

[2] The acquisition phase is the time available for the input sampling capacitors to acquire a new input with the ADC running at a throughput rate of 1.8 MSPS for the AD4020, 1 MSPS for the AD4021, and 500 kSPS for the AD4022.

[3] For turbo mode, t_{CNVH} must match the t_{QUIET1} minimum.

[4] A throughput rate of 1.8 MSPS can only be achieved with turbo mode enabled and a minimum SCK rate of 71 MHz. Refer to Table 4 for the maximum achievable throughput for different modes of operation. See the Serial Clock Frequency Requirements section for guidelines on determining the minimum SCK rate required for a given throughput.

[5] A 50% duty cycle is assumed for SCK.

[6] See Figure 24 for SINAD vs. t_{QUIET2}.

Table 3. Register Read/Write Timing

Parameter	Symbol[1]	Min	Typ	Max	Unit
READ/WRITE OPERATION					
CNV Pulse Width[2]	t_{CNVH}	10			ns
SCK Period	t_{SCK}				
VIO > 2.7 V		9.8			ns
VIO > 1.7 V		12.3			ns
SCK Low Time	t_{SCKL}	3			ns
SCK High Time	t_{SCKH}	3			ns
READ OPERATION					
CNV Low to SDO D17 MSB Valid Delay	t_{EN}				
VIO > 2.7 V				10	ns
VIO > 1.7 V				13	ns
SCK Falling Edge to Data Remains Valid	t_{HSDO}	1.5			ns
SCK Falling Edge to Data Valid Delay	t_{DSDO}				
VIO > 2.7 V				7.5	ns
VIO > 1.7 V				10.5	ns
CNV Rising Edge to SDO High Impedance	t_{DIS}			20	ns
WRITE OPERATION					
SDI Valid Setup Time from SCK Rising Edge	$t_{SSDISCK}$	2			ns
SDI Valid Hold Time from SCK Rising Edge	$t_{HSDISCK}$	2			ns
CNV Rising Edge to SCK Edge Hold Time	$t_{HCNVSCK}$	0			ns
CNV Falling Edge to SCK Active Edge Setup Time	$t_{SCNVSCK}$	6			ns

[1] See Figure 49 to Figure 52, Figure 54, Figure 56, Figure 58, Figure 60, Figure 62, Figure 64, and Figure 66
[2] For turbo mode, t_{CNVH} must match the t_{QUIET1} minimum.

Table 4. Achievable Throughput for Different Modes of Operation

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
THROUGHPUT, $\overline{CS}$ MODE					
3-Wire and 4-Wire Turbo Mode	f_{SCK} = 100 MHz, VIO ≥ 2.7 V			1.80	MSPS
	f_{SCK} = 80 MHz, VIO < 2.7 V			1.80	MSPS
3-Wire and 4-Wire Turbo Mode and Six Status Bits	f_{SCK} = 100 MHz, VIO ≥ 2.7 V			1.80	MSPS
	f_{SCK} = 80 MHz, VIO < 2.7 V			1.67	MSPS
3-Wire and 4-Wire Mode	f_{SCK} = 100 MHz, VIO ≥ 2.7 V			1.61	MSPS
	f_{SCK} = 80 MHz, VIO < 2.7 V			1.49	MSPS
3-Wire and 4-Wire Mode and Six Status Bits	f_{SCK} = 100 MHz, VIO ≥ 2.7 V			1.47	MSPS
	f_{SCK} = 80 MHz, VIO < 2.7 V			1.34	MSPS

ABSOLUTE MAXIMUM RATINGS

Note that the input overvoltage clamp cannot sustain the overvoltage condition for an indefinite amount of time.

Table 5.

Parameter	Rating
Analog Inputs	
IN+, IN− to GND[1]	−0.3 V to V_{REF} + 0.4 V, or ±50 mA[2]
Supply Voltage	
REF, VIO to GND	−0.3 V to +6.0 V
VDD to GND	−0.3 V to +2.1 V
VDD to VIO	−6 V to +2.4 V
Digital Inputs to GND	−0.3 V to VIO + 0.3 V
Digital Output to GND	−0.3 V to VIO + 0.3 V
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
Lead Temperature Soldering Reflow	260°C as per (JEDEC J-STD-020)
ESD Ratings	
Human Body Model	4 kV
Machine Model	200 V
Field Induced Charged Device Model	1.25 kV

[1] See the Analog Inputs section for an explanation of IN+ and IN−.
[2] Current condition tested over a 10 ms interval.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the natural convection junction to ambient thermal resistance measured in a one cubic foot sealed enclosure.

θ_{JC} is the junction to case thermal resistance.

Table 6. Thermal Resistance

Package Type[1]	θ_{JA}	θ_{JC}	Unit
RM-10	147	38	°C/W
CP-10-9	114	33	°C/W

[1] Test Condition 1: thermal impedance simulated values are based upon use of 2S2P JEDEC PCB. See the Ordering Guide section.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

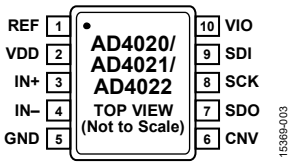


Figure 3. 10-Lead MSOP Pin Configuration

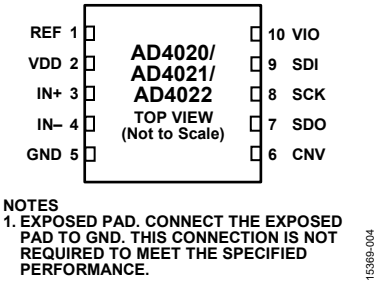


Figure 4. 10-Lead LFCSP Pin Configuration

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
1	REF	AI	Reference Input Voltage. The V_{REF} range is 2.4 V to 5.1 V. This pin is referred to the GND pin and must be decoupled closely to the GND pin with a 10 µF X7R ceramic capacitor.
2	VDD	P	1.8 V Power Supply. The VDD range is 1.71 V to 1.89 V. Bypass VDD to GND with a 0.1 µF ceramic capacitor.
3	IN+	AI	Differential Positive Analog Input. See the Differential Input Considerations section.
4	IN−	AI	Differential Negative Analog Input. See the Differential Input Considerations section.
5	GND	P	Power Supply Ground. Connect to the ground plane of the board.
6	CNV	DI	Convert Input. This input has multiple functions. On the leading edge, the input initiates the conversions and selects the interface mode of the device, which is either daisy-chain mode or $\overline{CS}$ mode. In $\overline{CS}$ mode, the SDO pin is enabled when CNV is low. In daisy-chain mode, the data is read when CNV is high.
7	SDO	DO	Serial Data Output. The conversion result is output on this pin. The pin is synchronized to the SCK signal on the SCK pin.
8	SCK	DI	Serial Data Clock Input. When the device is selected, the conversion result is shifted out by this clock.
9	SDI	DI	Serial Data Input. This input provides multiple features and selects the interface mode of the ADC as follows. Daisy-chain mode is selected if SDI is low during the CNV rising edge. In this mode, SDI is used as a data input to daisy-chain the conversion results of two or more ADCs onto a single SDO line. The digital data level on SDI is output on SDO with a delay of 20 SCK cycles. $\overline{CS}$ mode is selected if SDI is high during the CNV rising edge. In this mode, either SDI or CNV can enable the serial output signals when low. If SDI or CNV is low when the conversion is complete, the busy indicator feature is enabled. With CNV low, program the device by clocking in a 16-bit word on SDI on the rising edge of SCK.
10	VIO	P	Input/Output Interface Digital Power. Nominally, this pin is at the same supply as the host interface (1.8 V, 2.5 V, 3 V, or 5 V). Bypass VIO to ground with a 0.1 µF ceramic capacitor.
N/A[2]	EPAD	P	Exposed Pad. Connect the exposed pad to GND. This connection is not required to meet the specified performance. Note that the exposed pad only applies to the LFCSP.

[1] AI is analog input, P is power, DI is digital input, and DO is digital output.
[2] N/A means not applicable.

TYPICAL PERFORMANCE CHARACTERISTICS

VDD = 1.8 V, VIO = 3.3 V, V_{REF} = 5 V, T = 25°C, high-Z mode disabled, span compression disabled, turbo mode enabled, and f_S = 1.8 MSPS for the AD4020, f_S = 1 MSPS for the AD4021, and f_S = 500 kSPS for the AD4022, unless otherwise noted.

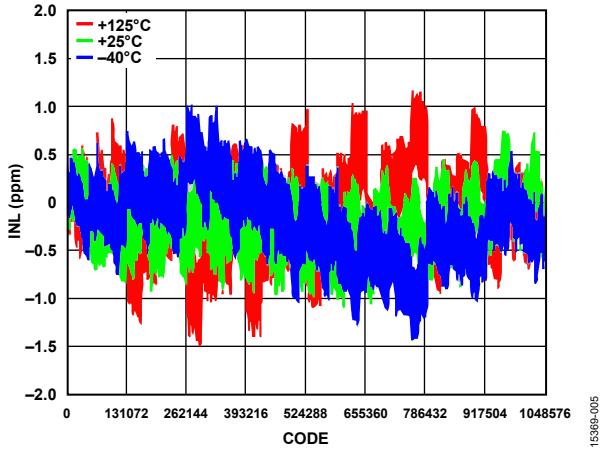


Figure 5. INL vs. Code for Various Temperatures, V_{REF} = 5 V

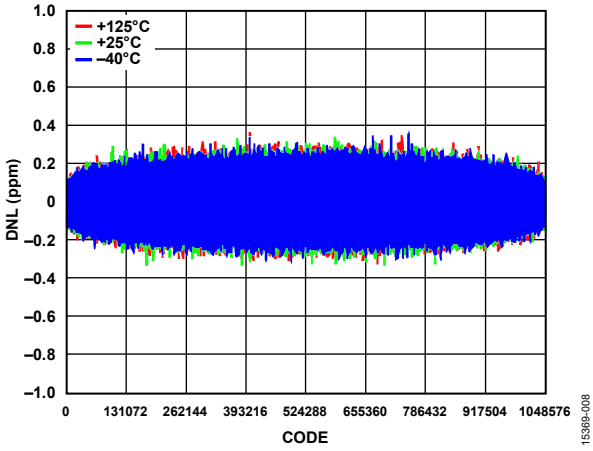


Figure 8. DNL vs. Code for Various Temperatures, V_{REF} = 5 V

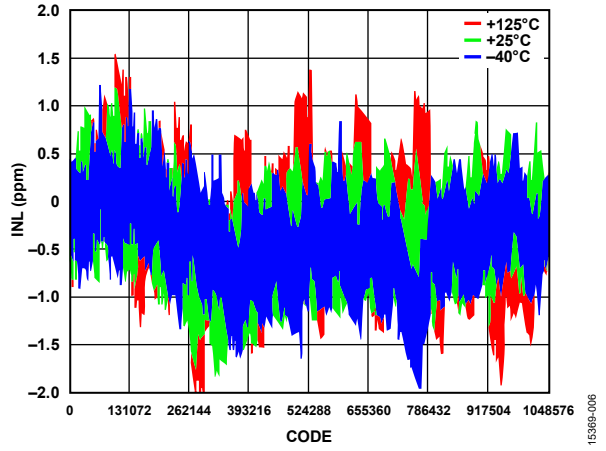


Figure 6. INL vs. Code for Various Temperatures, V_{REF} = 2.5 V

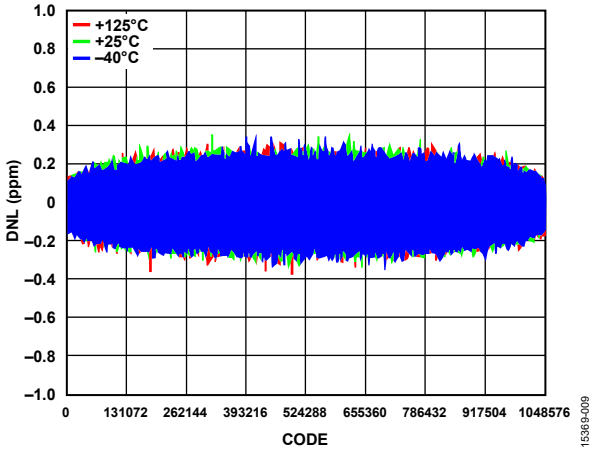


Figure 9. DNL vs. Code for Various Temperatures, V_{REF} = 2.5 V

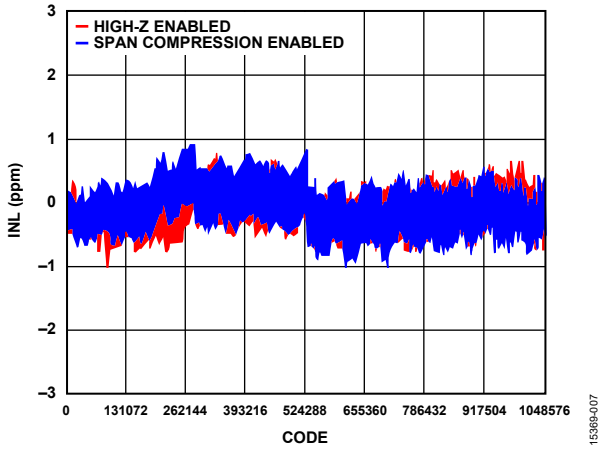


Figure 7. INL vs. Code for High-Z and Span Compression Modes Enabled, V_{REF} = 5 V

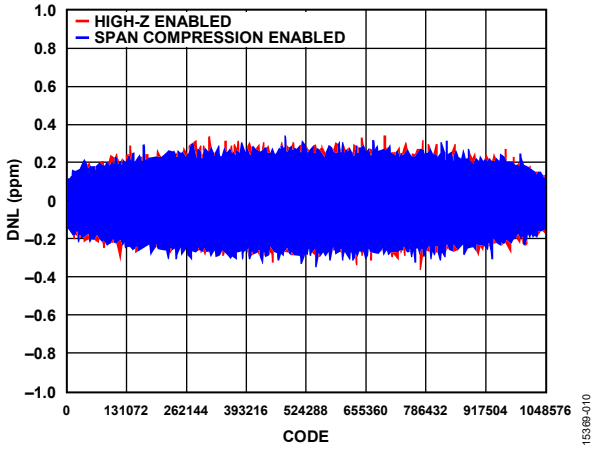


Figure 10. DNL vs. Code for High-Z and Span Compression Modes Enabled, V_{REF} = 5V

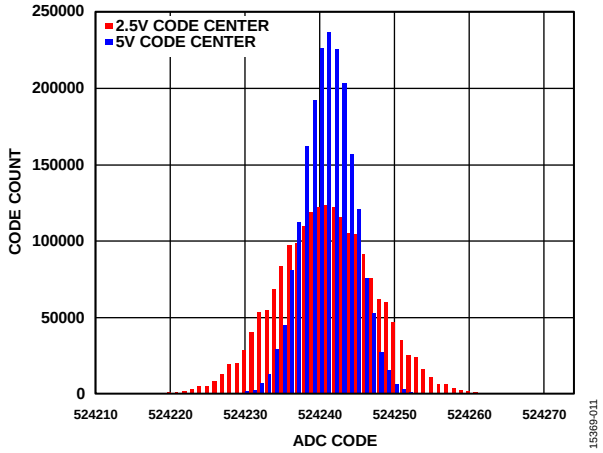


Figure 11. Histogram of a DC Input at Code Center, V_{REF} = 2.5 V and V_{REF} = 5 V

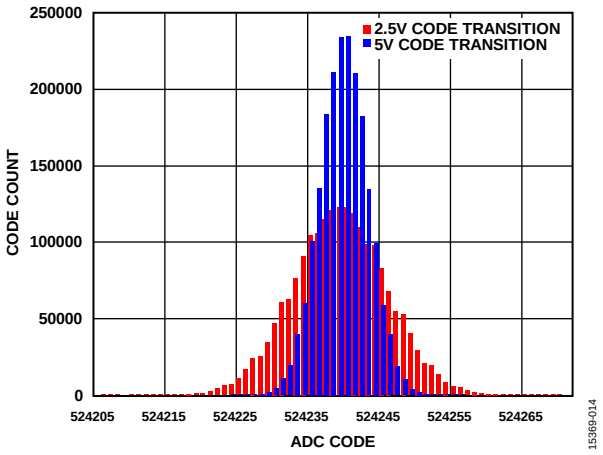


Figure 14. Histogram of a DC Input at Code Transition, V_{REF} = 2.5 V and V_{REF} = 5 V

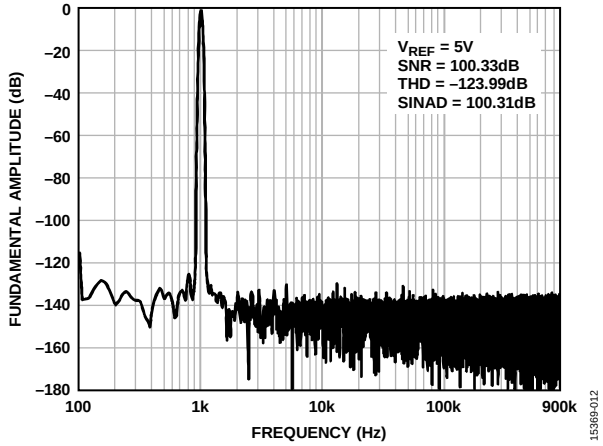


Figure 12. 1 kHz, –0.5 dBFS Input Tone Fast Fourier Transform (FFT), V_{REF} = 5 V

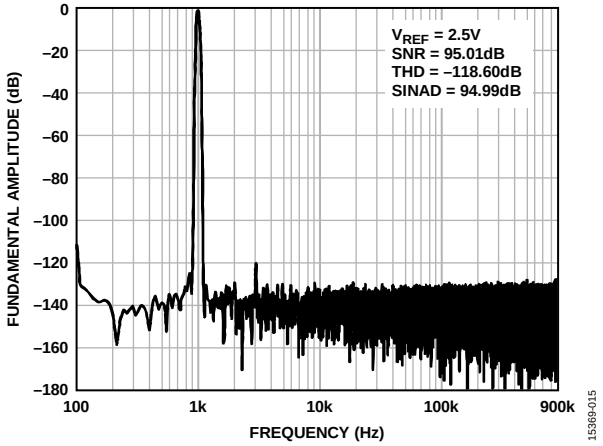


Figure 15. 1 kHz, –0.5 dBFS Input Tone FFT, V_{REF} = 2.5 V

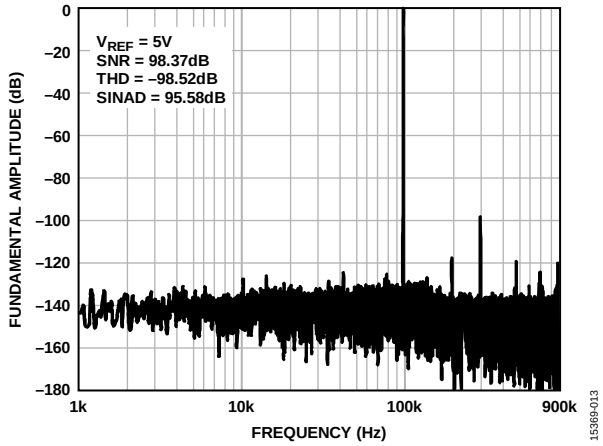


Figure 13. 100 kHz, –0.5 dBFS Input Tone FFT

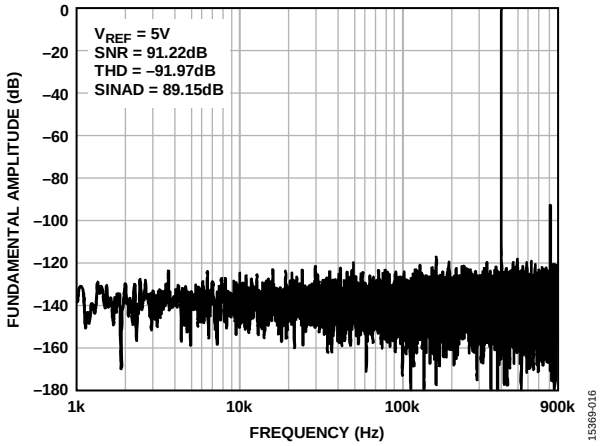


Figure 16. 400 kHz, –0.5 dBFS Input Tone FFT

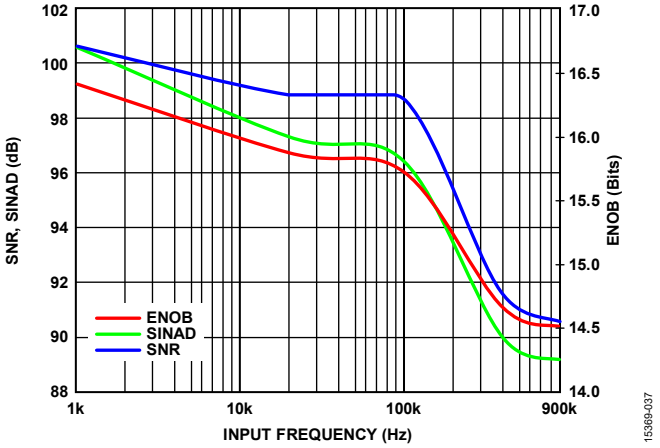


Figure 17. SNR, SINAD, and Effective Number of Bits (ENOB) vs. Input Frequency

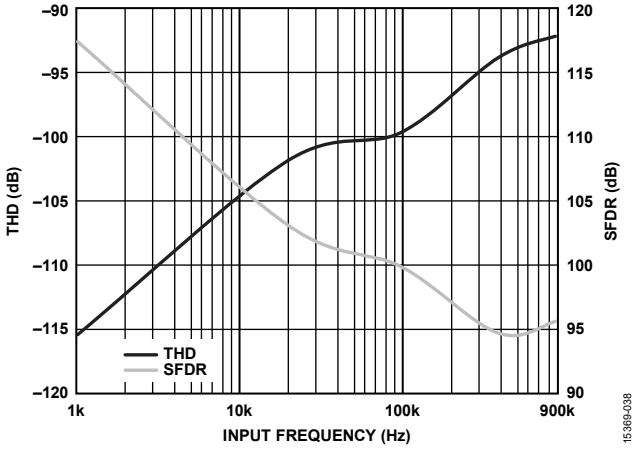


Figure 20. THD and SFDR vs. Input Frequency

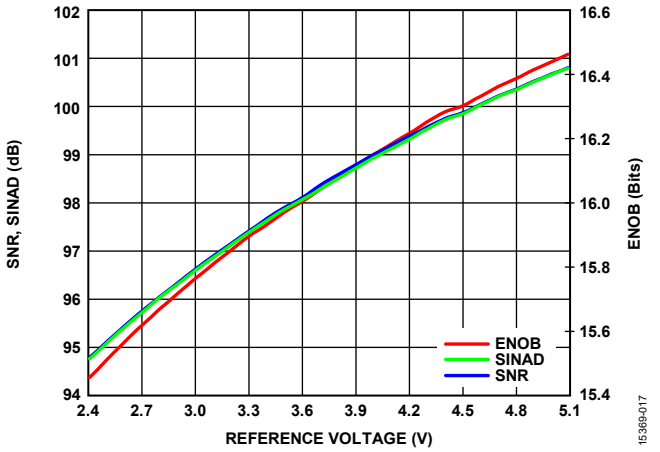


Figure 18. SNR, SINAD, and ENOB vs. Reference Voltage, f_{IN} = 1 kHz

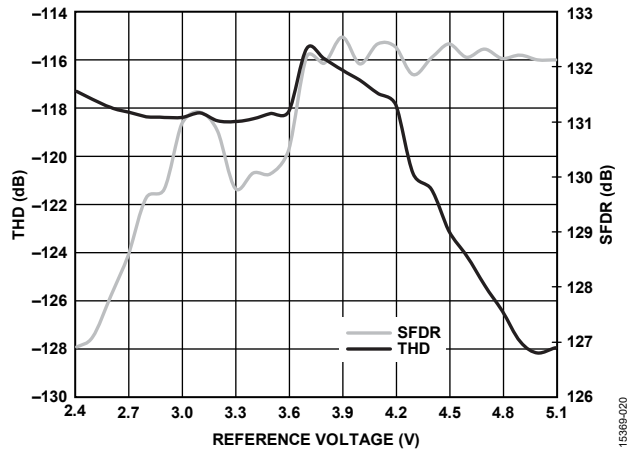


Figure 21. THD and SFDR vs. Reference Voltage, f_{IN} = 1 kHz

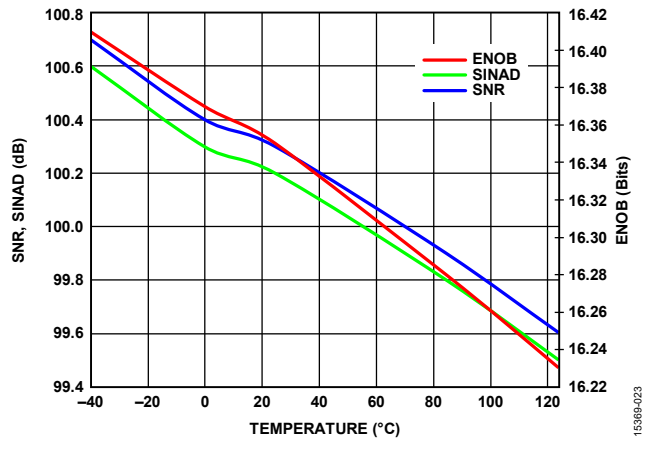


Figure 19. SNR, SINAD, and ENOB vs. Temperature, f_{IN} = 1 kHz

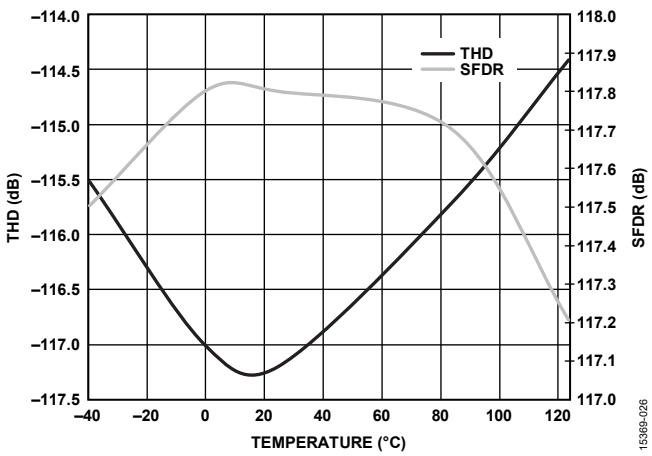


Figure 22. THD and SFDR vs. Temperature, f_{IN} = 1 kHz

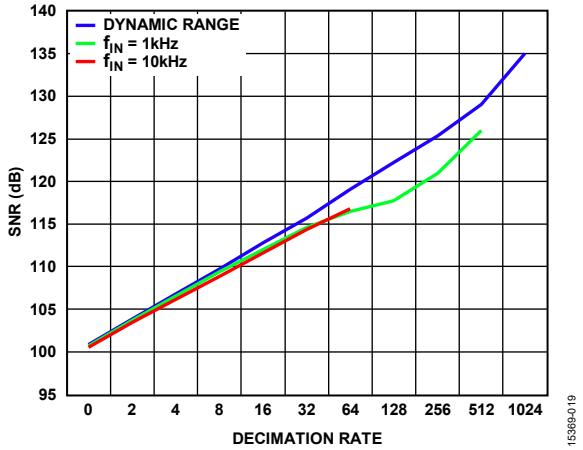


Figure 23. SNR vs. Decimation Rate for Various Input Frequencies, 1.8 MSPS

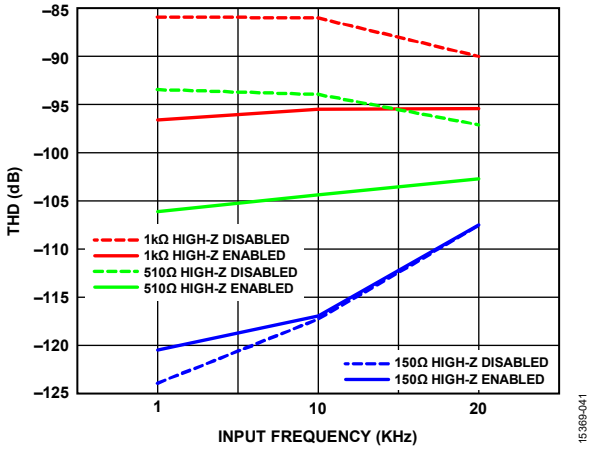


Figure 26. THD vs. Input Frequency for Various Source Impedances

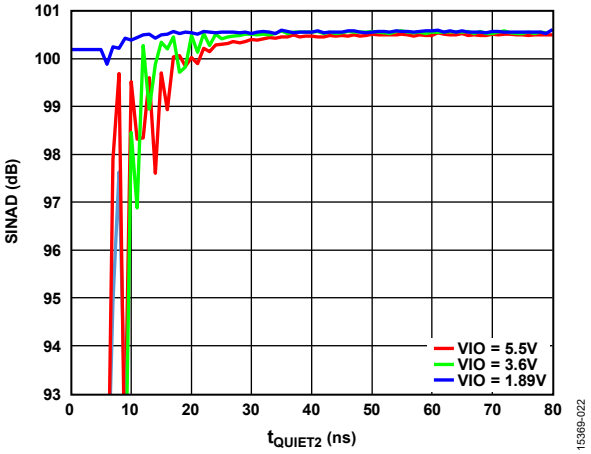


Figure 24. SINAD vs. t_{QUIET2}

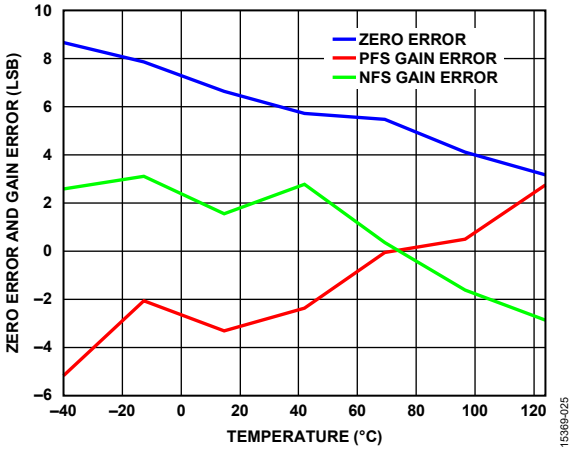


Figure 27. Zero Error and Gain Error vs. Temperature (PFS Is Positive Full Scale and NFS Is Negative Full Scale)

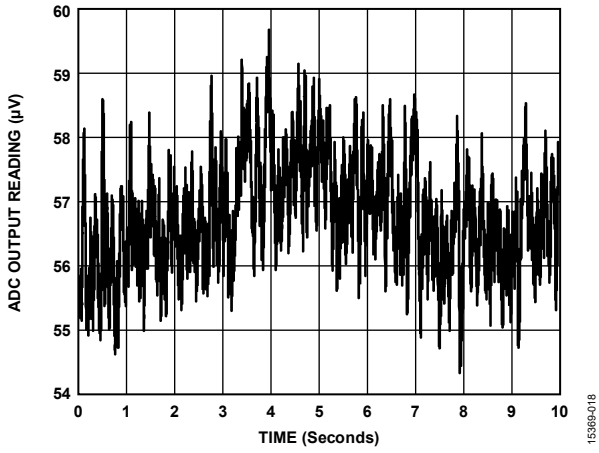


Figure 25. 1/f Noise for 0.1 Hz to 10 Hz Bandwidth, 50 kSPS, 2500 Samples Averaged per Reading

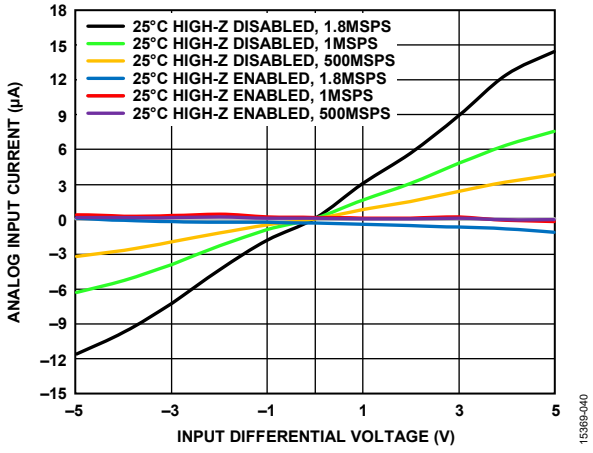


Figure 28. Analog Input Current vs. Input Differential Voltage

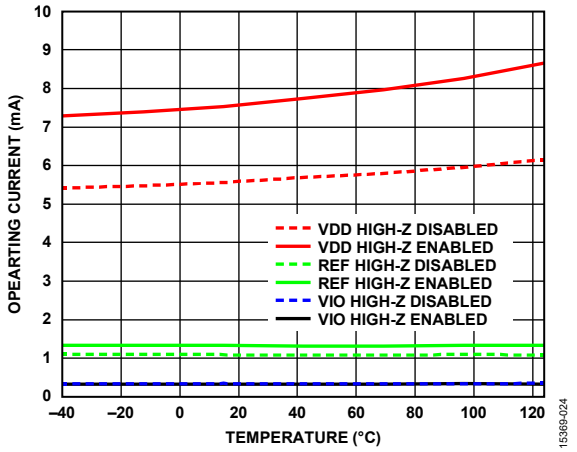


Figure 29. Operating Current vs. Temperature, AD4020, 1.8 MSPS

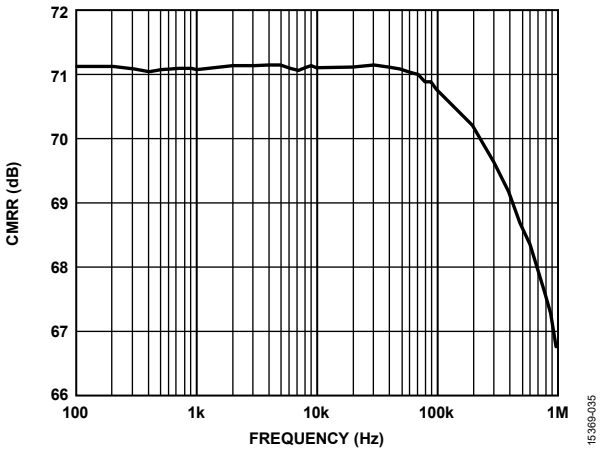


Figure 32. Common-Mode Rejection Ratio (CMRR) vs. Frequency

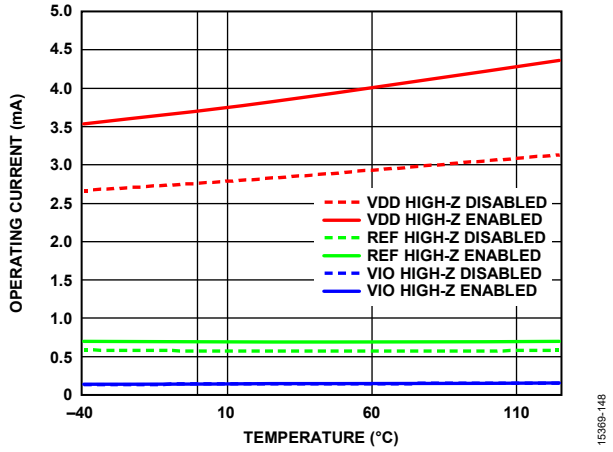


Figure 30. Operating Current vs. Temperature, AD4021, 1 MSPS

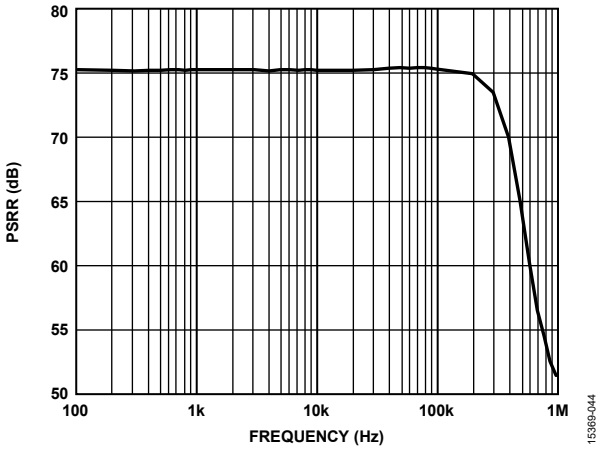


Figure 33. PSRR vs. Frequency

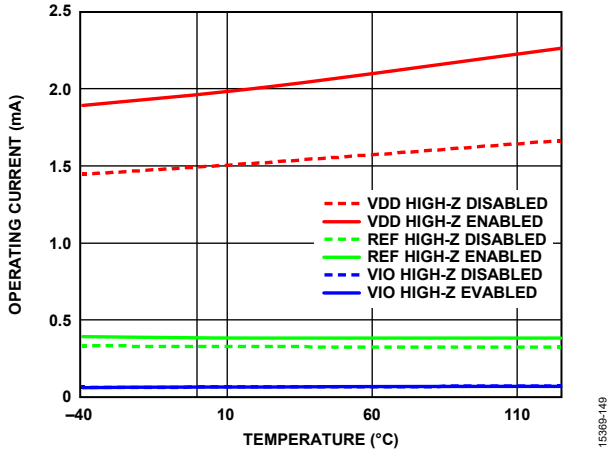


Figure 31. Operating Current vs. Temperature, AD4022, 500 kSPS

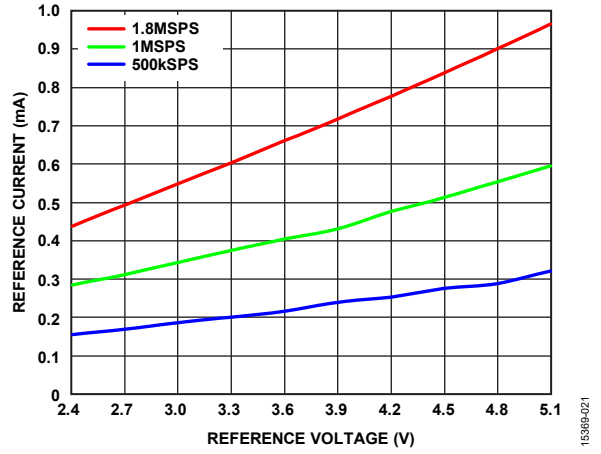


Figure 34. Reference Current vs. Reference Voltage

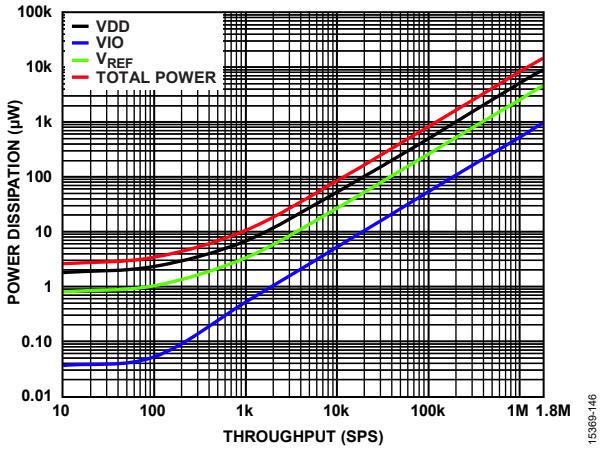


Figure 35. Power Dissipation vs. Throughput, VIO = 1.8 V, V_{REF} = 5 V

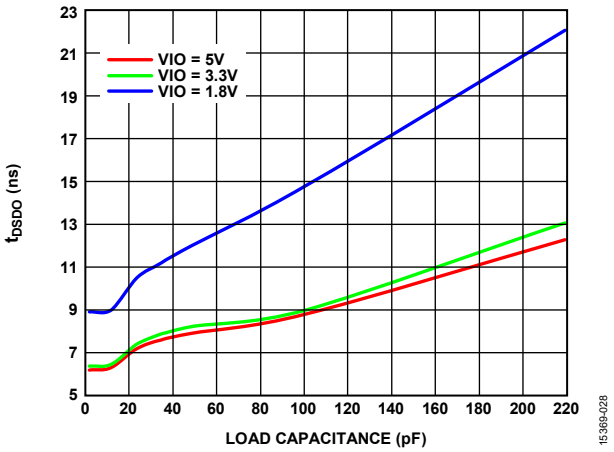


Figure 37 . t_{DSDO} vs. Load Capacitance

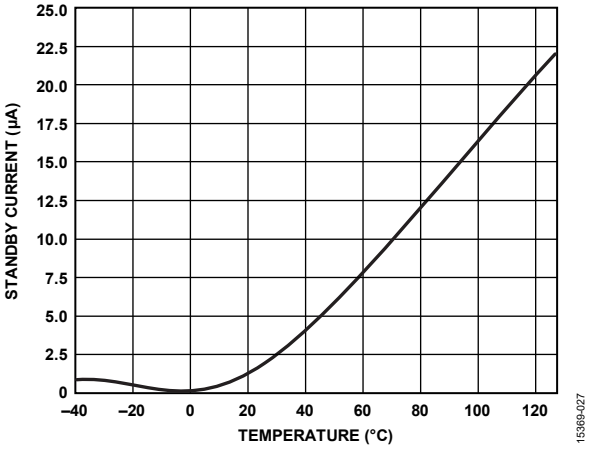


Figure 36. Standby Current vs. Temperature

TERMINOLOGY

Integral Nonlinearity Error (INL)
INL is the deviation of each individual code from a line drawn from negative full scale through positive full scale. The point used as negative full scale occurs ½ LSB before the first code transition. Positive full scale is defined as a level 1½ LSB beyond the last code transition. The deviation is measured from the middle of each code to the true straight line (see Figure 39).

Differential Nonlinearity Error (DNL)
In an ideal ADC, code transitions are 1 LSB apart. DNL is the maximum deviation from this ideal value. It is often specified in terms of resolution for which no missing codes are guaranteed.

Zero Error
Zero error is the difference between the ideal voltage that results in the first code transition (½ LSB above analog ground) and the actual voltage producing that code.

Gain Error
The first transition (from 100 … 00 to 100 … 01) occurs at a level ½ LSB above nominal negative full scale (−4.999995 V for the ±5 V range). The last transition (from 011 … 10 to 011 … 11) occurs for an analog voltage 1½ LSB below the nominal full scale (+4.999986 V for the ±5 V range). The gain error is the deviation of the difference between the actual level of the last transition and the actual level of the first transition from the difference between the ideal levels.

Spurious-Free Dynamic Range (SFDR)
SFDR is the difference, in decibels (dB), between the rms amplitude of the input signal and the peak spurious signal.

Effective Number of Bits (ENOB)
ENOB is a measurement of the resolution with a sine wave input. It is related to SINAD as follows:

$$ENOB = (SINAD - 1.76)/6.02$$

ENOB is expressed in bits and SINAD is expressed in dB..

Total Harmonic Distortion (THD)
THD is the ratio of the rms sum of the first five harmonic components to the rms value of a full-scale input signal and is expressed in decibels.

Dynamic Range
Dynamic range is the ratio of the rms value of the full scale to the total rms noise measured. The value for dynamic range is expressed in decibels. It is measured with a signal at −60 dBFS so that it includes all noise sources and DNL artifacts.

Signal-to-Noise Ratio (SNR)
SNR is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, excluding harmonics and dc. The value for SNR is expressed in decibels.

Signal-to-Noise-and-Distortion Ratio (SINAD)
SINAD is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components that are less than the Nyquist frequency, including harmonics but excluding dc. The value of SINAD is expressed in decibels.

Aperture Delay
Aperture delay is the measure of the acquisition performance and is the time between the rising edge of the CNV input and when the input signal is held for a conversion.

Transient Response
Transient response is the time required for the ADC to acquire a full-scale input step to ±1 LSB accuracy.

Common-Mode Rejection Ratio (CMRR)
CMRR is the ratio of the power in the ADC output at the frequency, f, to the power of a 200 mV p-p sine wave applied to the common-mode voltage of IN+ and IN− of frequency, f.

$$CMRR\ (\text{dB}) = 10\log(P_{ADC\_IN}/P_{ADC\_OUT})$$

where:
P_{ADC_IN} is the common-mode power at the frequency, f, applied to the IN+ and IN− inputs.
P_{ADC_OUT} is the power at the frequency, f, in the ADC output.

Power Supply Rejection Ratio (PSRR)
PSRR is the ratio of the power in the ADC output at the frequency, f, to the power of a 200 mV p-p sine wave applied to the ADC VDD supply of frequency, f.

$$PSRR\ (\text{dB}) = 10\log(P_{VDD\_IN}/P_{ADC\_OUT})$$

where:
P_{VDD_IN} is the power at the frequency, f, at the VDD pin.
P_{ADC_OUT} is the power at the frequency, f, in the ADC output.

THEORY OF OPERATION

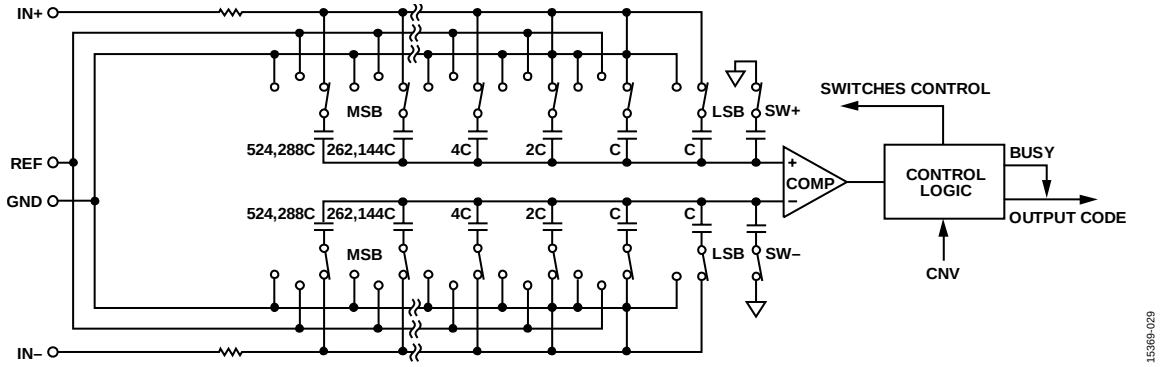


Figure 38. ADC Simplified Schematic

CIRCUIT INFORMATION

The AD4020/AD4021/AD4022 are high speed, low power, single-supply, precise, 20-bit differential ADCs based on a SAR architecture.

The AD4020 is capable of converting 1,800,000 samples per second (1.8 MSPS), the AD4021 is capable of converting 1,000,000 samples per second (1 MSPS), and the AD4022 is capable of converting 500,000 samples per second (500 kSPS). The power consumption of the AD4020/AD4021/AD4022 scales with throughput because they power down in between conversions. For example, when operating at 10 kSPS, they typically consume 83 µW, making them ideal for battery-powered applications. The AD4020/AD4021/AD4022 also have a valid first conversion after being powered down for long periods, which can further reduce power consumed in applications in which the ADC does not need to be constantly converting.

The AD4020/AD4021/AD4022 provide the user with an on-chip track-and-hold and do not exhibit any pipeline delay or latency, making them ideal for multiplexed applications.

The AD4020/AD4021/AD4022 incorporate a multitude of unique, easy to use features that result in a lower system power and smaller footprint.

The AD4020/AD4021/AD4022 each have an internal voltage clamp that protects the device from overvoltage damage on the analog inputs.

The analog input incorporates circuitry that reduces the nonlinear charge kickback seen from a typical switched capacitor SAR input. This reduction in kickback, combined with a longer acquisition phase, allows the use of lower bandwidth and lower power amplifiers as drivers. This combination has the additional benefit of allowing a larger resistor value in the input RC filter and a corresponding smaller capacitor, which results in a smaller RC load for the amplifier, improving stability and power dissipation.

High-Z mode can be enabled via the SPI interface by programming a register bit (see Table 12). When high-Z mode is enabled, the ADC input has a low input charging current at low input signal frequencies as well as improved distortion over a wide frequency range up to 100 kHz. For frequencies greater than 100 kHz and multiplexing functionality, disable high-Z mode.

For single-supply applications, a span compression feature creates additional headroom and footroom for the driving amplifier to access the full range of the ADC.

The fast conversion time of the AD4020/AD4021/AD4022, along with turbo mode, allows low clock rates to read back conversions even when running at their respective maximum throughput rates. Note that, for the AD4020, the full throughput rate of 1.8 MSPS can be achieved only with turbo mode enabled.

The AD4020/AD4021/AD4022 can interface with any 1.8 V to 5 V digital logic family. These devices are available in a 10-lead MSOP or a tiny 10-lead LFCSP that allows space savings and flexible configurations.

The AD4020/AD4021/AD4022 are pin for pin compatible with some of the 14-/16-/18-/20-bit precision SAR ADCs listed in Table 8.

Table 8. MSOP and LFCSP 14-/16-/18-/20-Bit Precision SAR ADCs

Bits	100 kSPS	250 kSPS	400 kSPS to 500 kSPS	≥1000 kSPS
20[1]	Not applicable	Not applicable	AD4022[2]	AD4020[2] AD4021[2]
18[1]	AD7989-1[2]	AD7691[2]	AD7690,[2] AD7989-5,[2] AD4011[2]	AD4003,[2] AD4007,[2] AD7982,[2] AD7984[2]
16[1]	AD7684	AD7687	AD7688,[2] AD7693[2]	AD4001,[2] AD4005,[2] AD7915[2]
16[3]	AD7680, AD7683, AD7988-1[2]	AD7685,[2] AD7694[2]	AD7686,[2] AD7988-5[2]	AD4000,[2] AD4004,[2] AD7980,[2] AD7983[2]
14[3]	AD7940	AD7942[2]	AD7946[2]	Not applicable

[1] True differential.
[2] Pin for pin compatible.
[3] Pseudo differential.

CONVERTER OPERATION

The AD4020/AD4021/AD4022 are SAR-based ADCs using a charge redistribution sampling digital-to-analog converter (DAC). Figure 38 shows the simplified schematic of the ADC. The capacitive DAC consists of two identical arrays of 20 binary weighted capacitors that are connected to the comparator inputs.

During the acquisition phase, terminals of the array tied to the input of the comparator are connected to the GND pin via the SW+ and SW− switches (see Figure 38). All independent switches connect the other terminal of each capacitor to the analog inputs. The capacitor arrays are used as sampling capacitors and acquire the analog signal on the IN+ and IN− inputs.

When the acquisition phase is complete and the CNV input goes high, a conversion phase initiates. When the conversion phase begins, SW+ and SW− are opened first. The two capacitor arrays are then disconnected from the inputs and connected to the GND input. The differential voltage between the IN+ and IN− inputs captured at the end of the acquisition phase is applied to the comparator inputs, unbalancing the comparator. By switching each element of the capacitor array between the GND pin and V_{REF}, the comparator input varies by binary weighted voltage steps ($V_{REF}/2$, $V_{REF}/4$, …, $V_{REF}/1{,}048{,}576$). The control logic toggles these switches, starting with the MSB, to bring the comparator back into a balanced condition. After the process completes, the control logic generates the ADC output code and a busy signal indicator.

Because the AD4020/AD4021/AD4022 have on-board conversion clocks, the serial clock, SCK, is not required for the conversion process.

TRANSFER FUNCTIONS

The ideal transfer characteristics for the AD4020/AD4021/AD4022 are shown in Figure 39 and Table 9.

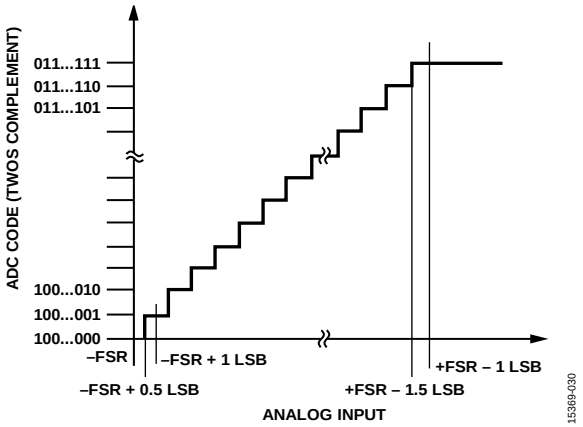


Figure 39. ADC Ideal Transfer Function (FSR Is Full-Scale Range)

Table 9. Output Codes and Ideal Input Voltages

Description	Analog Input, V_{REF} = 5 V	V_{REF} = 5 V with Span Compression Enabled	Digital Output Code (Hex)
FSR − 1 LSB	+4.99999046 V	+3.99999237 V	0x7FFFF[1]
Midscale + 1 LSB	+9.54 µV	+7.63 µV	0x00001
Midscale	0 V	0 V	0x00000
Midscale − 1 LSB	−9.54 µV	−7.63 µV	0xFFFFF
−FSR + 1 LSB	−4.99999046 V	−3.99999237 V	0x80001
−FSR	−5 V	−4 V	0x80000[2]

[1] This output code is also the code for an overranged analog input ($V_{IN+} - V_{IN-}$ above V_{REF} with span compression disabled and above $0.8 \times V_{REF}$ with span compression enabled).
[2] This output code is also the code for an underranged analog input ($V_{IN+} - V_{IN-}$ below $-V_{REF}$ with span compression disabled and below $-0.8 \times V_{REF}$ with span compression enabled).

APPLICATIONS INFORMATION

TYPICAL APPLICATION DIAGRAMS

Figure 40 shows an example of the recommended connection diagram for the AD4020/AD4021/AD4022 when multiple supplies, V+ and V−, are available. This configuration is used for optimal performance because the amplifier supplies can be selected to allow the maximum signal range (see Figure 40 for the range).

Figure 41 shows a recommended connection diagram when using a single-supply system. This setup is preferable when only a limited number of rails are available in the system and power dissipation is of critical importance.

Figure 42 shows a typical application diagram when using a fully differential amplifier.

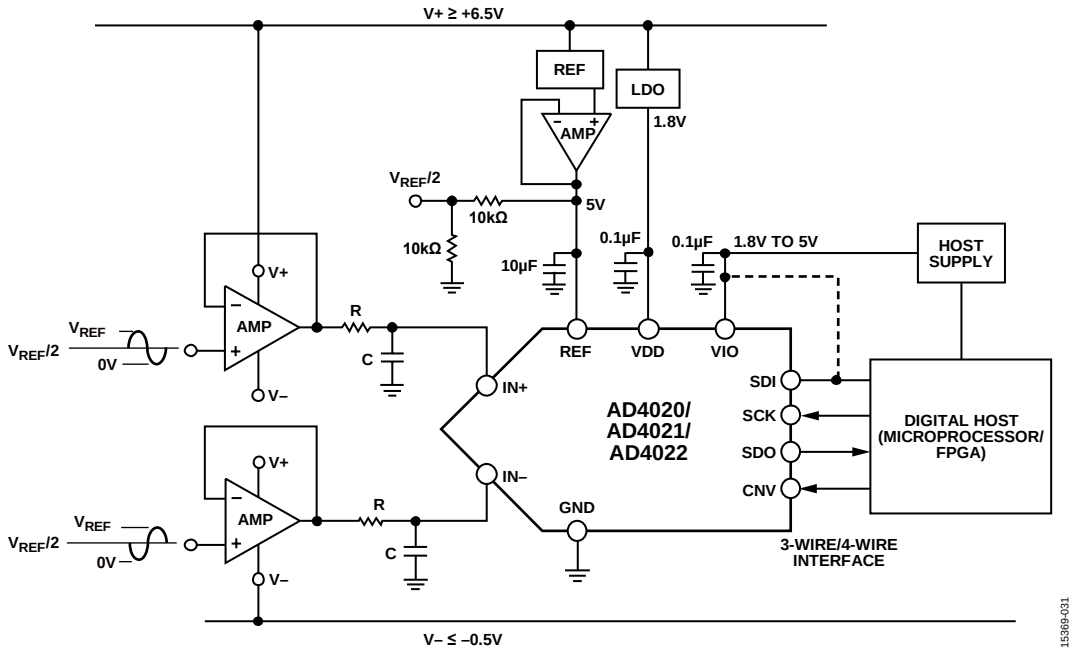
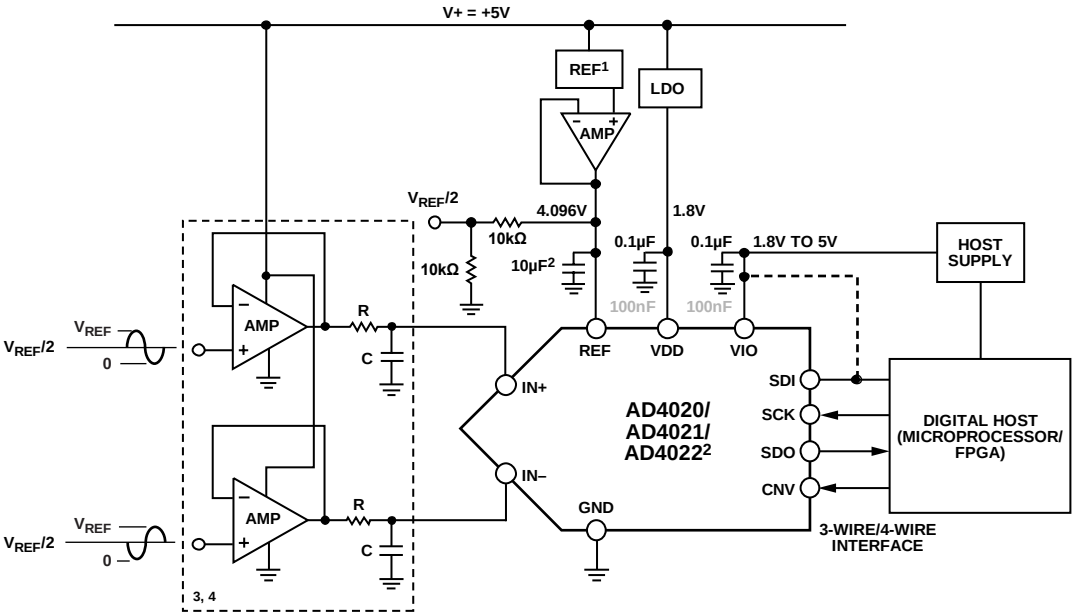


Figure 40. Typical Application Diagram with Multiple Supplies



[1]SEE THE VOLTAGE REFERENCE INPUT SECTION FOR REFERENCE SELECTION.
[2]C_{REF} IS USUALLY A 10µF CERAMIC CAPACITOR (X7R).
[3]SEE THE DRIVER AMPLIFIER CHOICE SECTION.
[4]SEE THE ANALOG INPUTS SECTION.

Figure 41. Typical Application Diagram with a Single Supply

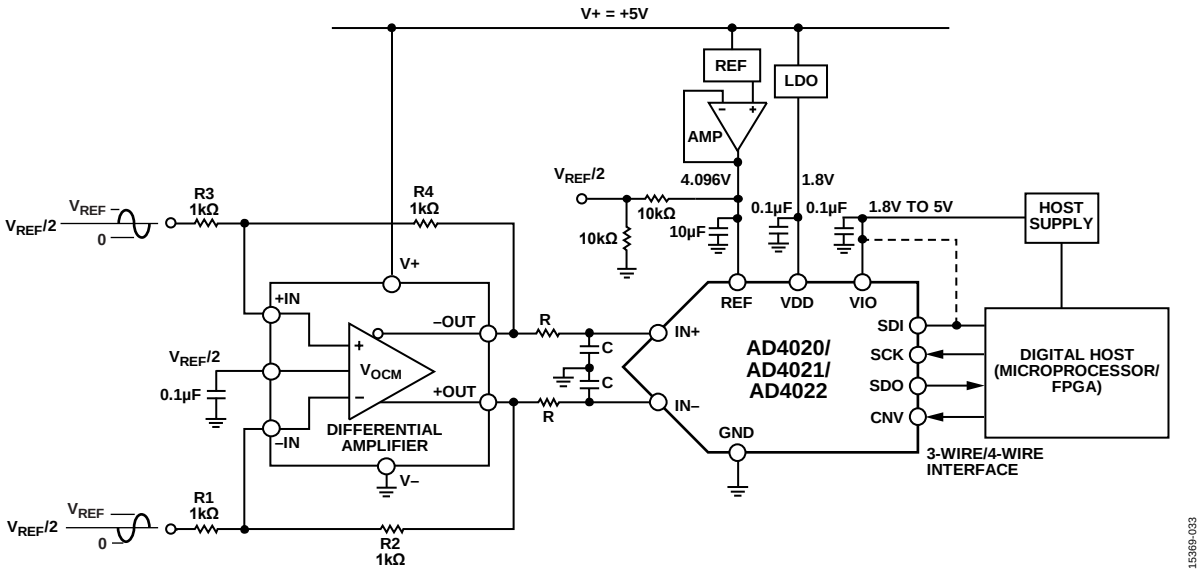


Figure 42. Typical Application Diagram with a Fully Differential Amplifier

ANALOG INPUTS

Figure 43 shows an equivalent circuit of the analog input structure, including the overvoltage clamp of the AD4020/AD4021/AD4022.

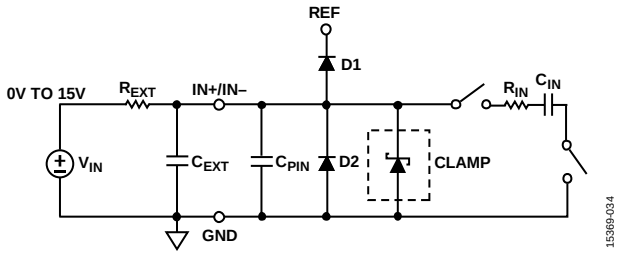


Figure 43. Equivalent Analog Input Circuit

Input Overvoltage Clamp Circuit

Most ADC analog inputs, IN+ and IN−, have no overvoltage protection circuitry apart from ESD protection diodes. During an overvoltage event, an ESD protection diode from an analog input pin (IN+ or IN−) to REF forward biases and shorts the input pin to REF, potentially overloading the reference or damaging the device. The AD4020/AD4021/AD4022 internal overvoltage clamp circuit with a larger external resistor (R_{EXT} = 200 Ω) eliminates the need for external protection diodes and protects the ADC inputs against dc overvoltages.

In applications where the amplifier rails are greater than V_{REF} and less than ground, it is possible for the output to exceed the input voltage range (specified in Table 1) of the device. In this case, the AD4020/AD4021/AD4022 internal voltage clamp circuit ensures that the voltage on the input pin does not exceed V_{REF} + 0.4 V and prevents damage to the device by clamping the input voltage in a safe operating range and avoiding disturbance of the reference, which is particularly important for systems that share the reference among multiple ADCs.

If the analog input exceeds the reference voltage by 0.4 V, the internal clamp circuit turns on and the current flows through the clamp into ground, preventing the input from rising further and potentially causing damage to the device. The clamp turns on before D1 (see Figure 43) and can sink up to 50 mA of current.

When the clamp is active, it sets the overvoltage ($\overline{OV}$) clamp flag bit in the configuration register that is accessed with a 16-bit SPI read command or via the $\overline{OV}$ in the status bits. The $\overline{OV}$ clamp flag gives an indication of overvoltage condition when it is set to 0. The $\overline{OV}$ clamp flag is a read only sticky bit, and is cleared only if the register is read while the overvoltage condition is no longer present.

The clamp circuit does not dissipate static power in the off state. Note that the clamp cannot sustain the overvoltage condition for an indefinite amount of time.

The external RC filter, formed by Resistor R_{EXT} and Capacitor C_{EXT} (see Figure 43), is usually present at the ADC input to band limit the input signal. During an overvoltage event, excessive voltage is dropped across R_{EXT}, and R_{EXT} becomes part of a protection circuit. The R_{EXT} value can vary from 200 Ω to 20 kΩ for 15 V protection. The C_{EXT} value can be as low as 100 pF for correct operation of the clamp. See Table 1 for input overvoltage clamp specifications.

Differential Input Considerations

The analog input structure allows the sampling of the true differential signal between IN+ and IN−. By using these differential inputs, signals common to both inputs are rejected. Figure 32 shows the common-mode rejection capability of the AD4020/AD4021/AD4022 over frequency. It is important to note that the differential input signals must be truly antiphase in nature, 180° out of phase, which is required to keep the common-mode voltage of the input signal within the specified range around $V_{REF}/2$, as shown in Table 1.

Switched Capacitor Input

During the acquisition phase, the impedance of the analog inputs (IN+ or IN−) can be modeled as a parallel combination of Capacitor C_{PIN} and the network formed by the series connection of R_{IN} and C_{IN}. C_{PIN} is primarily the pin capacitance. R_{IN} is typically 400 Ω and is a lumped component composed of serial resistors and the on resistance of the switches. C_{IN} is typically 40 pF and is mainly the ADC sampling capacitor.

During the conversion phase, where the switches are open, the input impedance is limited to C_{PIN}. R_{IN} and C_{IN} make a single-pole, low-pass filter that reduces undesirable aliasing effects and limits noise.

RC Filter Values

The RC filter value (represented by R and C in Figure 40 to Figure 42 and Figure 44) and driving amplifier can be selected depending on the input signal bandwidth of interest at the full throughput. Lower input signal bandwidth means that the RC cutoff can be lower, thereby reducing noise into the converter. For optimum performance at various throughputs, use the recommended RC values (200 Ω, 180 pF) and the ADA4807-1.

The RC values in Table 10 are chosen for ease of drive considerations and greater ADC input protection. The combination of a large R value (200 Ω) and small C value results in a reduced dynamic load for the amplifier to drive. The smaller value of C means fewer stability and phase margin concerns with the amplifier. The large value of R limits the current into the ADC input when the amplifier output exceeds the ADC input range.

DRIVER AMPLIFIER CHOICE

Although the AD4020/AD4021/AD4022 are easy to drive, the driver amplifier must meet the following requirements:

- The noise generated by the driver amplifier must be kept low enough to preserve the SNR and transition noise performance of the AD4020/AD4021/AD4022. The noise from the driver is filtered by the single-pole, low-pass filter of the analog input circuit made by R_{IN} and C_{IN}, or by the external filter, if one is used. Because the typical noise of the AD4020/AD4021/AD4022 is 31.5 μV rms, the SNR degradation due to the amplifier is the following:

$$SNR_{LOSS} = 20 \log\left(\frac{31.5}{\sqrt{31.5^2 + \frac{\pi}{2} f_{-3dB} (Ne_N)^2}}\right)$$

  where:
  $f_{-3\,dB}$ is the input bandwidth, in megahertz, of the AD4020/AD4021/AD4022 (10 MHz) or the cutoff frequency of the input filter, if one is used.
  N is the noise gain of the amplifier (for example, 1 in buffer configuration).
  e_N is the equivalent input noise voltage of the operational amplifier in nV/√Hz.
- For ac applications, the driver must have a THD performance commensurate with the AD4020/AD4021/AD4022.
- For multichannel multiplexed applications, the driver amplifier and the analog input circuit of the AD4020/AD4021/AD4022 must settle for a full-scale step onto the capacitor array at a 20-bit level (0.00001%, 1 ppm). In the amplifier data sheets, settling at 0.1% to 0.01% is more commonly specified. Settling at 0.1% to 0.01% can differ significantly from the settling time at a 20-bit level and must be verified prior to driver selection.

Table 10. RC Filter and Amplifier Selection for Various Input Bandwidths

Input Signal Bandwidth (kHz)	R (Ω)	C (pF)	Recommended Amplifier	Recommended Fully Differential Amplifier
<10	See the High-Z Mode section	See the High-Z Mode section	See the High-Z Mode section	ADA4940-1
<200	200	180	ADA4807-1	ADA4940-1
>200	200	120	ADA4897-1	ADA4932-1
Multiplexed	200	120	ADA4897-1	ADA4932-1

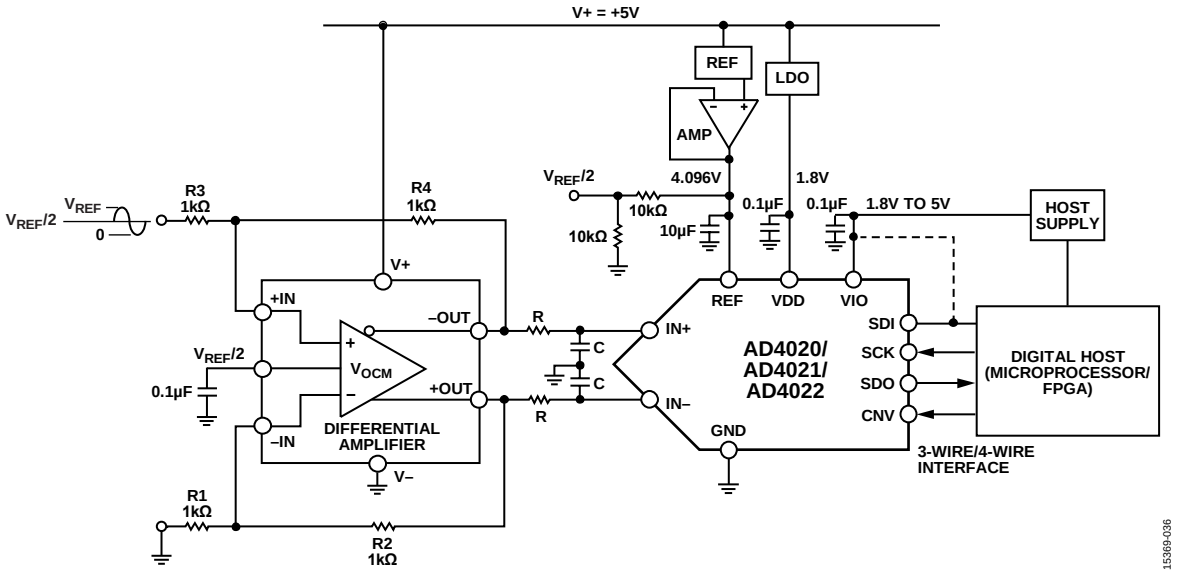


Figure 44. Typical Application Diagram for Single-Ended to Differential Conversion with a Fully Differential Amplifier

Single to Differential Driver

The AD4020/AD4021/AD4022 requires a differential input signal for proper operation. For applications using a single-ended analog signal, either bipolar or unipolar, a fully differential amplifier, such as the ADA4940-1 or ADA4945-1, can be used to convert the single-ended signal to a differential signal, as shown in Figure 44.

High Frequency Input Signals

The AD4020/AD4021/AD4022 ac performance over a wide input frequency range is shown in Figure 17 and Figure 20. Unlike other traditional SAR ADCs, the AD4020/AD4021/AD4022 maintain exceptional ac performance for input frequencies up to the Nyquist frequency with minimal performance degradation. Note that the input frequency is limited to the Nyquist frequency of the sample rate in use.

Multiplexed Applications

The AD4020/AD4021/AD4022 significantly reduce system complexity for multiplexed applications that require superior performance in terms of noise, power, and throughput. Figure 45 shows a simplified block diagram of a multiplexed data acquisition system including a multiplexer, an ADC driver, and the precision SAR ADC.

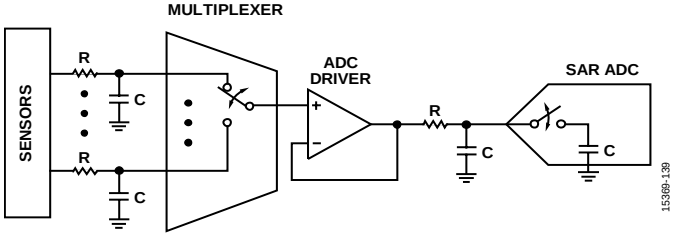


Figure 45. Multiplexed Data Acquisition Signal Chain Using the AD4020/AD4021/AD4022

Switching multiplexer channels typically results in large voltage steps at the ADC inputs. To ensure an accurate conversion result, the step must be given adequate time to settle before the ADC samples the inputs (on the rising edge of CNV). The settling time error is dependent on the drive circuitry (multiplexer and ADC driver), RC filter values, and the time when the multiplexer channels are switched. Switch the multiplexer channels immediately after t_{QUIET1} has elapsed from the start of the conversion to maximize settling time and to prevent corruption of the conversion result. To avoid conversion corruption, do not switch the channels during the t_{QUIET1} time. If the analog inputs are multiplexed during the quiet conversion time (t_{QUIET1}), the current conversion is possibly corrupted.

EASE OF DRIVE FEATURES

Input Span Compression

In single-supply applications, it is recommended to use the full range of the ADC. However, the amplifier can have some headroom and footroom requirements, which can be a problem, even if it is a rail-to-rail input and output amplifier. The AD4020/AD4021/AD4022 include a span compression feature that increases the headroom and footroom available to the amplifier by reducing the input range by 10% from the top and bottom of the range while still accessing all available ADC codes (see Figure 46). The SNR decreases by approximately 1.9 dB (20 × log(8/10)) for the reduced input range when span compression is enabled. Span compression is disabled by default but is enabled by writing to the relevant register bit (see the Digital Interface section).

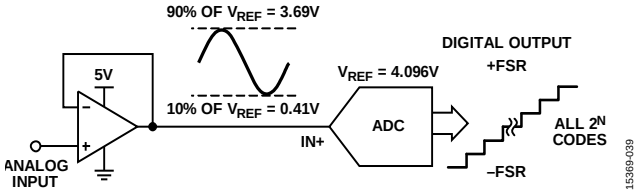


Figure 46. Span Compression

High-Z Mode

The AD4020/AD4021/AD4022 incorporate high-Z mode, which reduces the nonlinear charge kickback when the capacitor DAC switches back to the input at the start of acquisition. Figure 28 shows the analog input current of the AD4020/AD4021/AD4022 with high-Z mode enabled and disabled. The low input current makes the ADC easier to drive than the traditional SAR ADCs available in the market, even with high-Z mode disabled. The input current reduces further to submicroampere range when high-Z mode is enabled. The high-Z mode is disabled by default, but can be enabled by writing to the configuration register (see Table 12). Disable high-Z mode for input frequencies above 100 kHz or when multiplexing.

To achieve the optimum data sheet performance from traditional high resolution precision SAR ADCs, system designers must often use a dedicated high power, high speed amplifier to drive the switched capacitor SAR ADC inputs. High-Z mode allows a choice of lower power and lower bandwidth precision amplifiers with a lower RC filter cutoff to drive the ADC, removing the need for dedicated high speed ADC drivers, which saves system power, size, and cost in precision, low bandwidth applications. High-Z mode allows the amplifier and RC filter in front of the ADC to be chosen based on the signal bandwidth of interest, and not based on the settling requirements of the switched capacitor SAR ADC inputs. High-Z mode also improves THD performance and reduces analog input current for input signals up to 100 kHz.

Additionally, the AD4020/AD4021/AD4022 can be driven with a much higher source impedance than traditional SARs, which means the resistor in the RC filter can have a value 10 times larger than previous SAR designs and, with high-Z mode enabled, can tolerate even greater impedance. Figure 26 shows the THD performance for various source impedances with high-Z mode disabled and enabled.

Figure 47 and Figure 48 show the AD4020/AD4021/AD4022 SNR and THD performance using the ADA4077-1 (supply current per amplifier (I_{SY}) = 400 µA) and ADA4610-1 (I_{SY} = 1.50 mA) precision amplifiers when driving the AD4020/AD4021/AD4022 at full throughput for high-Z mode both enabled and disabled with various RC filter values. These amplifiers achieve +96 dB to +99 dB typical SNR and close to −110 dB typical THD with high-Z enabled for a 2.27 MHz RC bandwidth. THD is approximately 10 dB better with high-Z mode enabled, even for large R values greater than 200 Ω. SNR maintains close to 99 dB, even with a low RC filter cutoff.

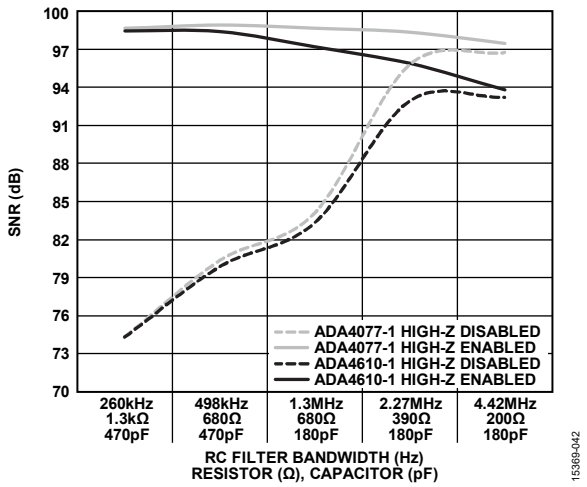


Figure 47. SNR vs. RC Filter Bandwidth for Various Precision ADC Drivers, f_{IN} = 1 kHz (See the Typical Performance Characteristics Section for Operating Conditions)

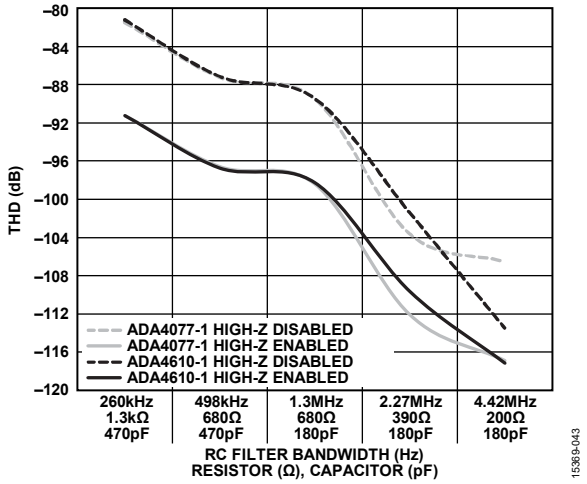


Figure 48. THD vs. RC Filter Bandwidth for Various Precision ADC Drivers, f_{IN} = 1 kHz (See the Typical Performance Characteristics Section for Operating Conditions)

When high-Z mode is enabled, the ADC consumes approximately 2.0 mW per MSPS of extra power. However, this additional power is still significantly lower than using dedicated ADC drivers like the ADA4807-1. For any system, the front end usually limits the overall ac/dc performance of the signal chain. The ADA4077-1 and ADA4610-1 data sheets of the selected precision amplifiers (see Figure 47 and Figure 48) show that their own noise and distortion performance dominates the SNR and THD specification at a certain input frequency.

Long Acquisition Phase

The AD4020/AD4021/AD4022 also feature a fast conversion time of 320 ns, which results in a long acquisition phase. The acquisition is further extended by a key feature of the AD4020/AD4021/AD4022. The ADC returns to the acquisition phase typically 100 ns before the end of the conversion. This feature provides an even longer time for the ADC to acquire the new input voltage. A longer acquisition phase reduces the settling requirement on the driving amplifier, and a lower power and

lower bandwidth amplifier can be chosen. The longer acquisition phase means that a lower RC filter (represented by R and C in Figure 40 to Figure 42 and Figure 44) cutoff can be used, which means a noisier amplifier can also be tolerated. A larger value of R can be used in the RC filter with a corresponding smaller value of C, reducing amplifier stability concerns without affecting distortion performance significantly. A larger value of R also results in reduced dynamic power dissipation in the amplifier.

See Table 10 for details on setting the RC filter bandwidth and choosing a suitable amplifier.

VOLTAGE REFERENCE INPUT

A 10 µF (X7R, 0805 size) ceramic chip capacitor is appropriate for the optimum performance of the reference input.

For higher performance and lower drift, use a reference such as the ADR4550. Using a low power reference such as the ADR3450 can result in a slight decrease in the noise performance. It is recommended to use a reference buffer, such as the ADA4807-1, between the reference and the ADC reference input. It is important to consider the optimum capacitance necessary to keep the reference buffer stable as well as to meet the minimum ADC requirement stated previously in this section (that is, a 10 µF ceramic chip capacitor, C_{REF}).

POWER SUPPLY

The AD4020/AD4021/AD4022 use two power supply pins: a core supply (VDD) and a digital input/output interface supply (VIO). VIO allows direct interface with any logic between 1.8 V and 5.5 V. To reduce the number of supplies needed, VIO and VDD can be tied together for 1.8 V operation. The ADP7118 low noise, complementary metal-oxide semiconductor (CMOS), low dropout (LDO) linear regulator is recommended to power the VDD and VIO pins. The AD4020/AD4021/AD4022 are independent of power supply sequencing between VIO and VDD. Additionally, the AD4020/AD4021/AD4022 are insensitive to power supply rejection variations over a wide frequency range, as shown in Figure 33.

The AD4020/AD4021/AD4022 automatically power down at the end of each conversion phase. Therefore, the power scales linearly with the sampling rate. This feature makes the device ideal for low sampling rates (even a few samples per second) and battery-powered applications. Figure 35 shows the AD4020/AD4021/AD4022 total power dissipation and individual power dissipation for each rail.

DIGITAL INTERFACE

The AD4020/AD4021/AD4022 digital interface is used to perform analog to digital conversions and to enable and disable various features. The AD4020/AD4021/AD4022 are compatible with SPI, QSPI™, and MICROWIRE digital hosts and DSPs. SCK must be set with clock polarity (CPOL) = clock phase (CPHA) = 0. A 3-wire interface using the CNV, SCK, and SDO signals minimizes wiring connections, which is useful in applications with digital isolation. A 4-wire interface using the SDI, CNV, SCK, and SDO signals allows CNV, which initiates the conversions, to be independent of the readback timing (SDI). This interface is useful in low jitter sampling or simultaneous sampling applications. In either 3-wire or 4-wire $\overline{CS}$ mode, a busy signal can be enabled to indicate when the conversion result is ready. The busy signal acts as an interrupt to the digital host to initiate data readback.

The AD4020/AD4021/AD4022 digital interface also supports daisy-chaining multiple devices to read back results from multiple ADCs over a single SPI bus.

Timing diagrams and explanations for each digital interface mode are given in the $\overline{CS}$ Mode, 3-Wire Turbo Mode section through the Daisy-Chain Mode section.

Turbo mode allows the use of slower SPI clock rates by extending the amount of time available to clock out conversion results. Turbo mode is enabled by setting the turbo mode enable bit to 1 in the configuration register (see Table 12), and replaces the busy indicator feature when enabled. The maximum throughput of 1.8 MSPS for the AD4020 can only be achieved with turbo mode enabled and a minimum SCK frequency of 71 MHz (see the Serial Clock Frequency Requirements section). See the $\overline{CS}$ Mode, 3-Wire Turbo Mode section, and $\overline{CS}$ Mode, 4-Wire Turbo Mode section for descriptions of turbo mode operation.

Status bits can also be clocked out at the end of the conversion data if the status bits are enabled in the configuration register (see the Status Bits section).

For isolated systems, the ADuM141D is recommended to support the 71 MHz SCK frequency required to run the AD4020 at the full throughput of 1.8 MSPS.

The state of SDO on power-up is either low or high-Z, depending on the states of CNV and SDI, as shown in Table 11.

Table 11. State of SDO on Power-Up

CNV	SDI	SDO
0	0	Low
0	1	Low
1	0	Low
1	1	High-Z

Configuration Register Details

The AD4020/AD4021/AD4022 features are controlled via the configuration register. The configuration register is eight bits wide and contains enable bits for the status bits, span compression, high-Z mode, and turbo mode, as well as an overvoltage detection flag. 16-bit SPI instructions are used to read from and write to the contents in the configuration register (see the Configuration Register Details section). Table 12 shows the locations and descriptions of each field in the configuration register.

Serial Clock Frequency Requirements

The AD4020/AD4021/AD4022 digital interface minimizes the SCK frequency required for reading back conversion results, even when operating at a high throughput. The minimum SCK frequency required for a given application depends on the number of bits being read on SDO, whether turbo mode is enabled or disabled, and the throughput in use. See Table 13 for several examples of SCK frequency requirements for different throughputs.

The minimum SCK frequency (f_{SCK}) required to access the conversion result plus status bits when turbo mode is enabled is calculated with the following equation:

$$f_{SCK} > \frac{N_D + N_S}{t_{CYC} - t_{QUIET1} - t_{EN} - t_{QUIET2}}$$

where:

N_D is the ADC resolution (20 bits).

N_S is the number of status bits being accessed.

t_{CYC}, t_{QUIET1}, t_{EN}, and t_{QUIET2} correspond to timing specifications described in Table 2.

The minimum SCK frequency required to access the conversion result plus status bits when turbo mode is not enabled is calculated with the following equation:

$$f_{SCK} > \frac{N_D + N_S}{t_{CYC} - t_{CONV} - t_{EN} - t_{QUIET2}}$$

where t_{CONV} corresponds to the conversion time, and is described in Table 2.

Table 12. Configuration Register

Bits	Bit Name	Description	Reset	Access[1]
[7:5]	Reserved	Reserved memory.	0x0	R
4	Status bits enable	Enables status bits (see the Status Bits section). 0: disables status bits. 1: enables status bits.	0x0	R/W
3	Span compression enable	Enables span compression (see the Input Span Compression section). 0: disables span compression. 1: enables span compression.	0x0	R/W
2	High-Z mode enable	Enables high-Z mode (see the High-Z Mode section). 0: disables high-Z mode. 1: enables high-Z mode.	0x0	R/W
1	Turbo mode enable	Enables turbo mode. 0: disables turbo mode. 1: enables turbo mode.	0x0	R/W
0	$\overline{OV}$ clamp flag	Indicates an overvoltage event triggered the input overvoltage clamp circuit (see the Input Overvoltage Clamp Circuit section). This bit is sticky, and clears only when read after the overvoltage event has ended. 0: indicates an overvoltage event has occurred. 1: indicates no overvoltage event has occurred.	0x1	R

[1] R is read-only and R/W is read/write. Read only bits cannot be updated with a register write operation. R/W bits can be updated with a register write operation.

Table 13. SCK Frequency Requirements for Various Throughputs

$\overline{CS}$ Mode	Throughput	Minimum SCK Frequency (MHz)
3-Wire and 4-Wire Turbo Modes	1.8 MSPS (AD4020)	71
	1 MSPS (AD4020, AD4021)	28
	500 kSPS (AD4020, AD4021, AD4022)	12
	100 kSPS (AD4020, AD4021, AD4022)	2.5
3-Wire and 4-Wire Turbo Modes with Six Status Bits	1.8 MSPS (AD4020)	92
	1 MSPS (AD4020, AD4021)	36
	500 kSPS (AD4020, AD4021, AD4020)	16
	100 kSPS (AD4020, AD4021, AD4022)	3
3-Wire and 4-Wire Modes	1.6 MSPS (AD4020)	98
	1 MSPS (AD4020, AD4021)	35
	500 kSPS (AD4020, AD4021, AD4022)	13
	100 kSPS (AD4020, AD4021, AD4022)	2.5
3-Wire and 4-Wire Modes with Status Word	1.4 MSPS (AD4020)	90
	1 MSPS (AD4020, AD4021)	45
	500 kSPS (AD4020, AD4021, AD4022)	17
	100 kSPS (AD4020, AD4021, AD4022)	3

REGISTER READ/WRITE FUNCTIONALITY

The AD4020/AD4021/AD4022 configuration register is read from and written to with a 16-bit SPI instruction. The state of the fields in the configuration register determine which of the device features are enabled or disabled (see the Configuration Register Details section).

The 16-bit SPI instructions consist of the 8-bit register access command (see Table 14) followed by the register data. When performing register read and write operations, CNV is analogous to a chip select signal, and CNV must be brought low to access the configuration register contents. Data on SDI is latched in on each SCK rising edge. Data is shifted out on SDO on each SCK falling edge. SDO returns to a high impedance state when CNV is brought high.

The first bit read on SDI after a CNV falling edge (represented by $\overline{WEN}$ in Table 14) must be a 0 to initiate the register access command. The next bit ($R/\overline{W}$) determines whether the instruction is a write or a read. The following six bits must match the values for Bit 5 through Bit 0, shown in Table 14, to perform the SPI read/write.

When performing a write operation, the new register contents are written over SDI MSB first, and the writeable bits in the configuration register are updated after the device receives the full byte. When performing a read operation, the current register contents are shifted out on SDO, MSB first. Figure 49 and Figure 50 show timing diagrams for register read and write operations when using any of the $\overline{CS}$ modes. Figure 51 shows the timing diagram for performing a write operation to multiple devices connected in daisy-chain mode.

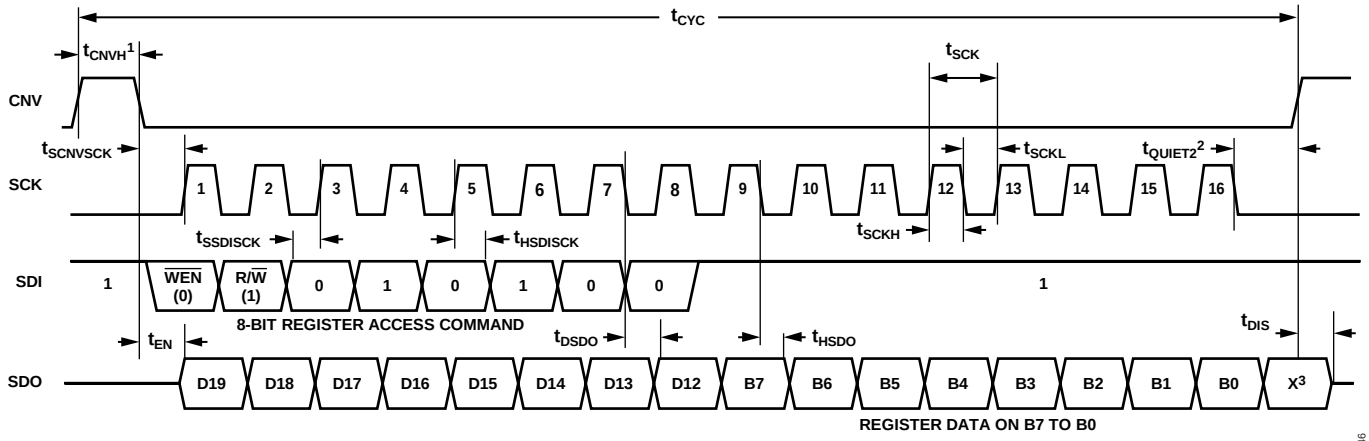
Register reads are not supported when daisy-chaining multiple devices (see the Daisy-Chain Mode section). To verify the contents of the configuration register, enable and read the status bits (see the Status Bits section).

The LSB of the configuration register (Bit 0) is a read only bit that allows digital hosts to ensure the desired digital interface mode is selected in the frame immediately following a register write operation. For digital hosts that are limited to 16-bit SPI frames (such as some microcontrollers), set this bit accordingly to ensure SDI is at the desired level on the rising edge of CNV. For example, set this bit to 1 and/or set the idle state of SDI to 1 when using any of the $\overline{CS}$ modes.

SPI write instructions can be performed in the same frame as reading a conversion result. To ensure the conversion is executed correctly, the CNV signal must obey the timing requirements for the selected interface mode.

Table 14. Register Access Command

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$\overline{WEN}$	$R/\overline{W}$	0	1	0	1	0	0



[1]THE CNV HIGH TIME MUST FOLLOW THE t_{CONV} SPECIFICATION TO GENERATE A VALID CONVERSION RESULT.
[2]THE SCK FALLING EDGE TO CNV RISING EDGE DELAY MUST FOLLOW THE t_{QUIET2} SPECIFICATION TO ENSURE SPECIFIED PERFORMANCE.
[3]X MEANS DON'T CARE.

Figure 49. Register Read Timing Diagram

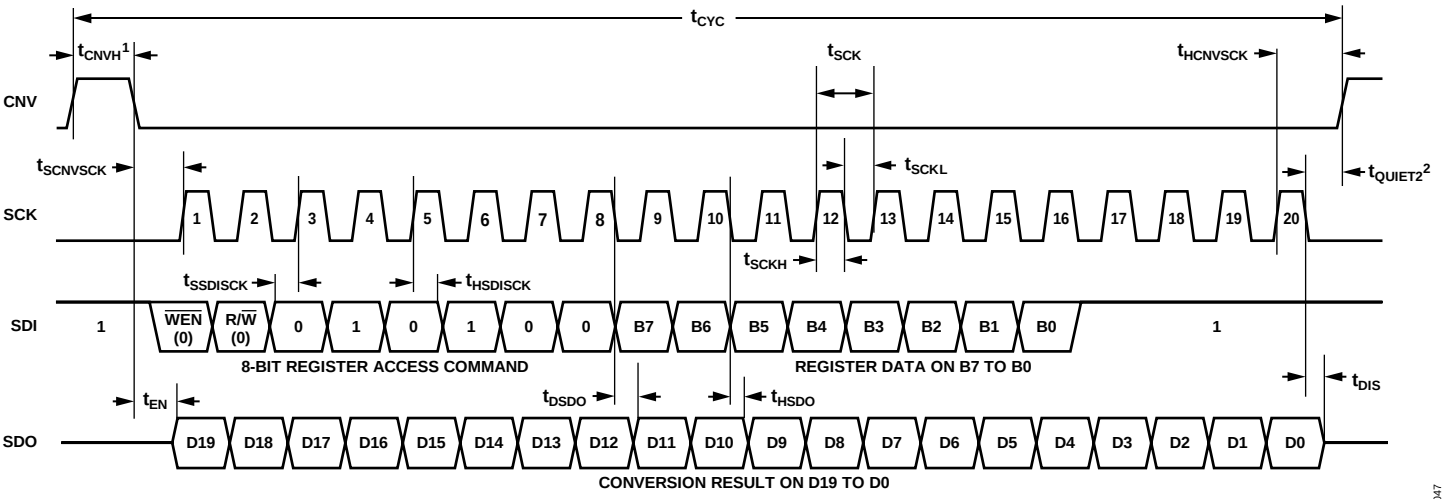


Figure 50. Register Write Timing Diagram

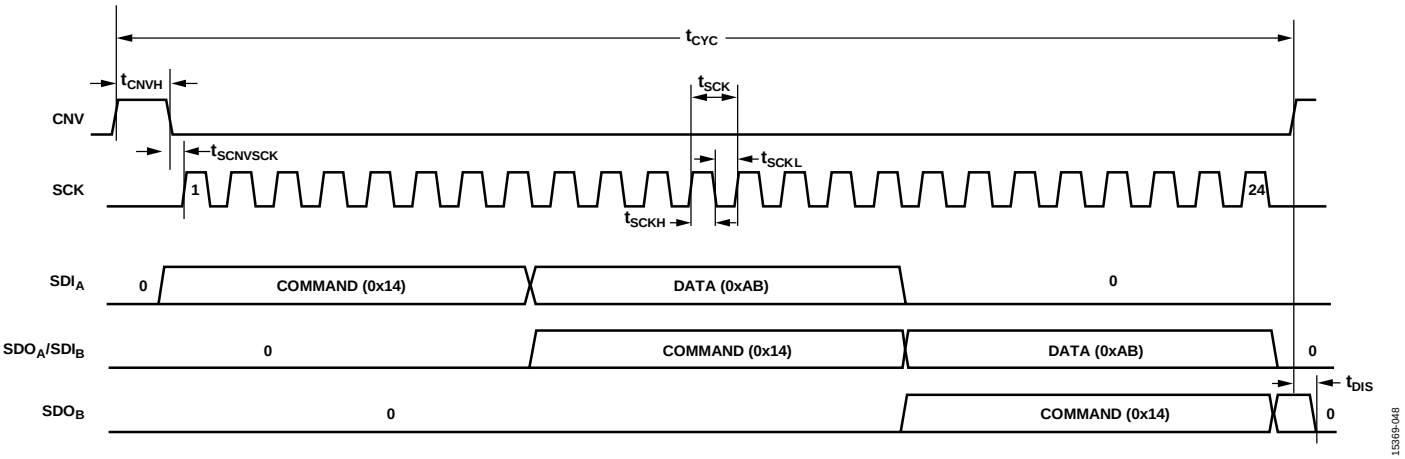


Figure 51. Register Write Timing Diagram, Daisy-Chain Mode

STATUS BITS

A set of six optional status bits can be appended to the end of each conversion result. The status bits allow the digital host to check the state of the input overvoltage protection circuit and verify that the ADC features are configured correctly without interrupting conversions. The status bits are enabled when the status bits enable bit in the configuration register is set to 1 (see Configuration Register Details section). Table 15 shows a description of each status bit.

When enabled, the status bits are clocked out MSB first starting on the SCK falling edge immediately following the LSB of the conversion result. The SDO line returns to high impedance after the sixth status bit is clocked out (except in daisy-chain mode). The user is not required to clock out all status bits to start the next conversion. For example, if the digital host needs to monitor the $\overline{OV}$ clamp flag but also needs to minimize the SCK frequency, the remaining status bits can be ignored to limit the number of SCK pulses required per conversion period. When using multiple AD4020/AD4021/AD4022 devices in daisy-chain mode, however, all six status bits must be clocked out for each connected device.

Figure 52 shows the serial interface timing for $\overline{CS}$ mode, 3-wire without busy indicator with all six status bits, Bits[5:0] (see Figure 52), clocked out.

Table 15. Status Bits Descriptions

Bit	Bit Name	Description
5	$\overline{OV}$ clamp flag	Indicates the state of the $\overline{OV}$ clamp flag in the configuration register.
4	Span compression	Indicates the state of the span compression enable bit in the configuration register.
3	High-Z mode	Indicates the state of the High-Z mode enable bit in the configuration register.
2	Turbo mode	Indicates the state of the turbo mode enable bit in the configuration register.
[1:0]	Reserved	Reserved.

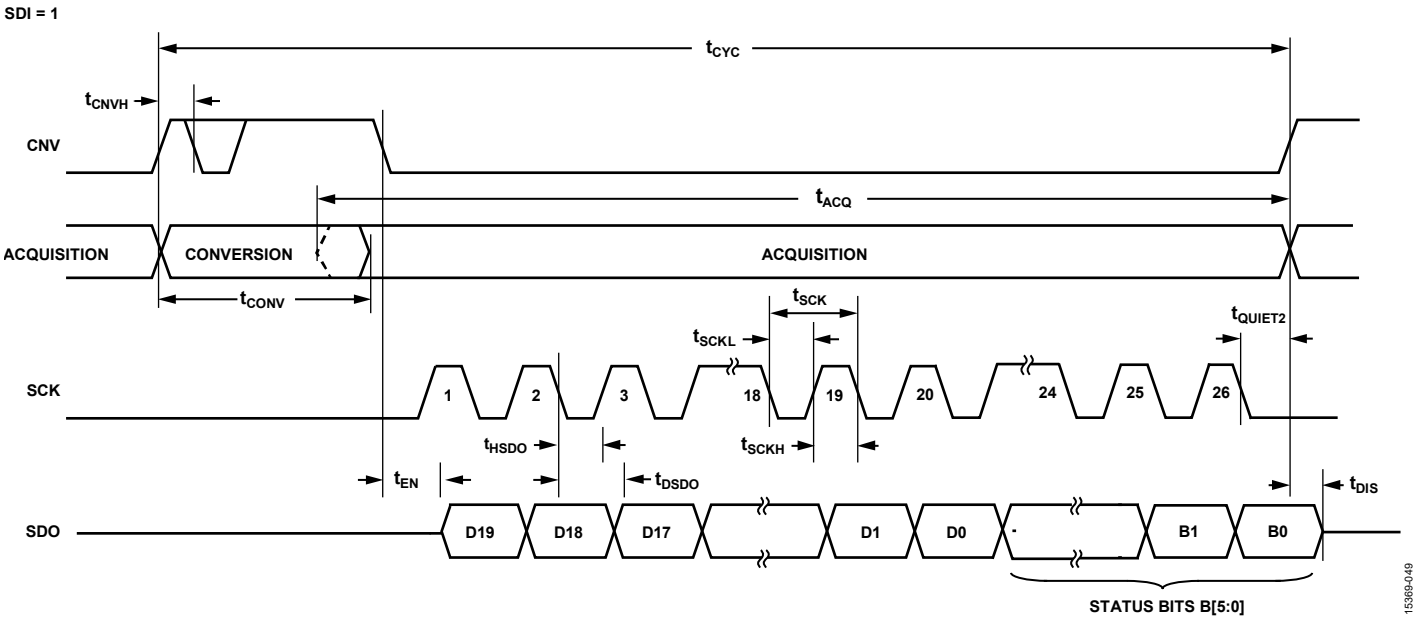


Figure 52. $\overline{CS}$ Mode, 3-Wire Without Busy Indicator Serial Interface Timing Diagram Including Status Bits

$\overline{CS}$ MODE, 3-WIRE TURBO MODE

This mode is typically used when a single AD4020/AD4021/AD4022 device is connected to an SPI-compatible digital host. Turbo mode allows lower SCK frequencies by increasing the time that the ADC conversion result can be clocked out. The AD4020 can achieve a throughput rate of 1.8 MSPS only when turbo mode is enabled and using a minimum SCK rate of 71 MHz (see the Serial Clock Frequency Requirements section). The connection diagram is shown in Figure 53, and the corresponding timing diagram is shown in Figure 54.

To enable turbo mode, set the turbo mode enable bit in the configuration register to 1 (see Table 12). This mode replaces the 3-wire with busy indicator mode when turbo mode is enabled. Writing to the user configuration register requires SDI to be connected to the digital host (see the Register Read/Write Functionality section). When turbo mode is enabled, the conversion result read on SDO corresponds to the result of the previous conversion.

When performing conversions in this mode, SDI must be held high, a CNV rising edge initiates a conversion and forces SDO to high impedance. The user must wait t_{QUIET1} time after the CNV rising edge before bringing CNV low to clock out the previous conversion result. When the conversion is complete (after t_{CONV}), the AD4020/AD4021/AD4022 enter the acquisition phase and power down.

When CNV goes low, the MSB is output to SDO. The remaining data bits are clocked by subsequent SCK falling edges. The data is valid on both SCK edges. Although the rising edge can capture the data, a digital host using the SCK falling edge allows a faster reading rate, provided it has an acceptable hold time, as dictated by t_{HSDO} (see Table 2). If the status bits are not enabled, SDO returns to high impedance after the 16th SCK falling edge. If the status bits are enabled, they are shifted out on SDO on the 17th through the 22nd SCK falling edges (see the Status Bits section). SDO returns to high impedance after the final SCK falling edge, or when CNV goes high (whichever occurs first). The user must also provide a delay of t_{QUIET2} between the final SCK falling edge and the next CNV rising edge to ensure specified performance.

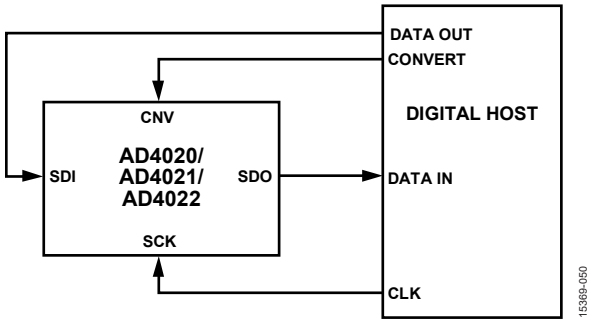


Figure 53. $\overline{CS}$ Mode, 3-Wire Turbo Mode Connection Diagram

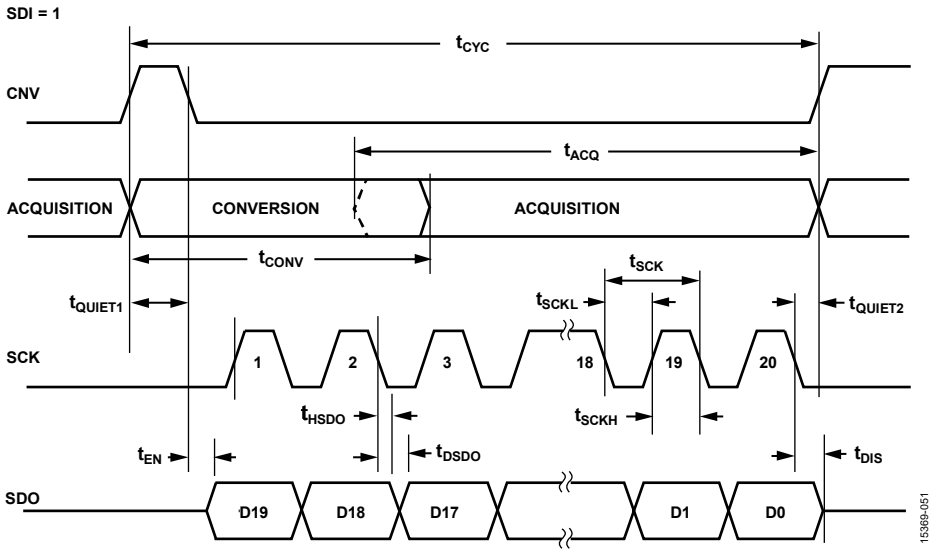


Figure 54. $\overline{CS}$ Mode, 3-Wire Turbo Mode Serial Interface Timing Diagram (Status Bits Not Shown)

$\overline{CS}$ MODE, 3-WIRE WITHOUT THE BUSY INDICATOR

This mode is typically used when a single AD4020/AD4021/AD4022 device is connected to an SPI-compatible digital host. The connection diagram is shown in Figure 55, and the corresponding timing diagram is shown in Figure 56.

Turbo mode must be disabled to use this mode. To disable turbo mode, set the turbo mode enable bit in the configuration register to 0 (see Table 12). Turbo mode is disabled by default.

When performing conversions in this mode, SDI must be held high. SDI can be connected to VIO if register reading and writing is not required. A rising edge on CNV initiates a conversion and forces SDO to high impedance. After a conversion is initiated, it continues until completion, irrespective of the state of CNV. This feature can be useful when bringing CNV low to select other SPI devices, such as analog multiplexers. However, CNV must be returned high before the minimum conversion time (t_{CONV}) elapses and then held high for the maximum possible conversion time to avoid generating the busy signal indicator. When the conversion is complete, the AD4020/AD4021/AD4022 enter the acquisition phase and power down. There must not be any digital activity on SCK during the conversion.

When CNV goes low, the MSB is output onto SDO. The remaining data bits are clocked out on SDO by subsequent SCK falling edges. The data is valid on both SCK edges. Although the rising edge can capture the data, a digital host using the SCK falling edge allows a faster reading rate, provided it has an acceptable hold time, as dictated by t_{HSDO} (see Table 2). If the status bits are not enabled, SDO returns to high impedance after the 20th SCK falling edge. If the status bits are enabled, they are shifted out on SDO on the 21st through the 26th SCK falling edges (see the Status Bits section). SDO returns to high impedance after the final SCK falling edge, or when CNV goes high (whichever occurs first).

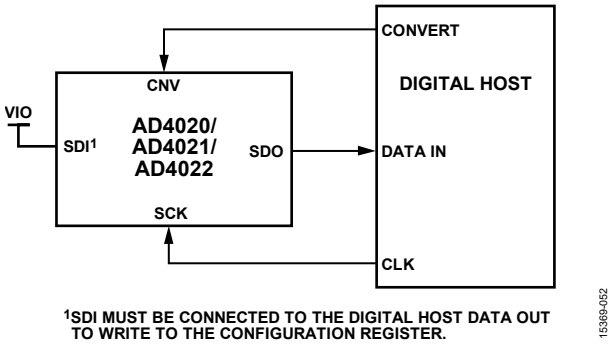


Figure 55. $\overline{CS}$ Mode, 3-Wire Without Busy Indicator Connection Diagram

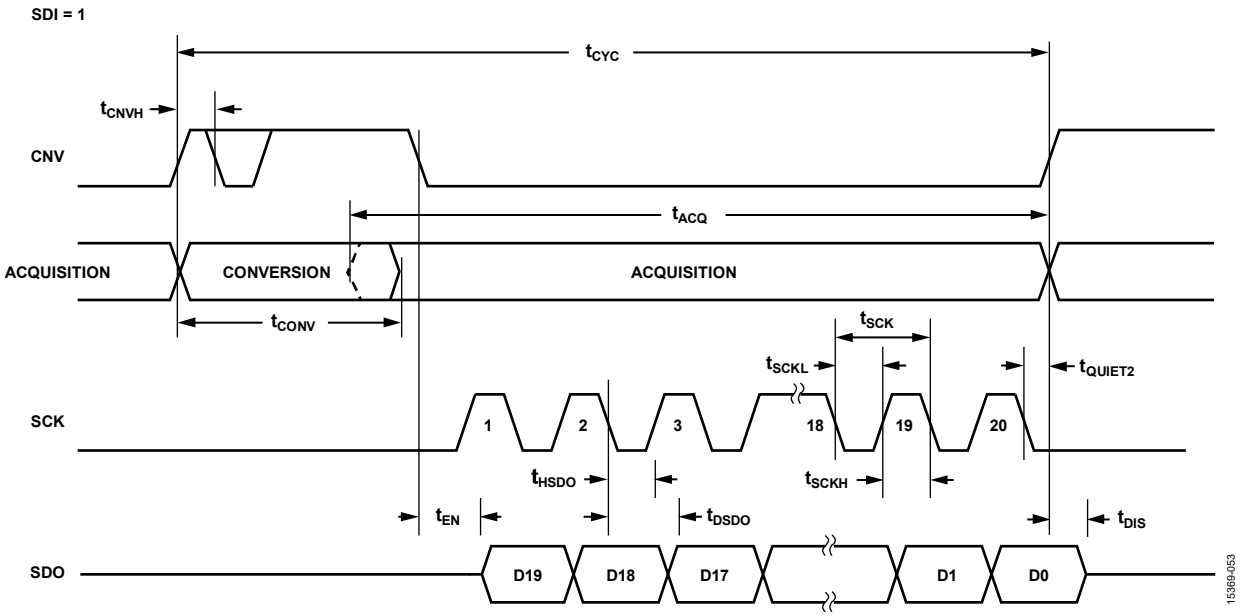


Figure 56. $\overline{CS}$ Mode, 3-Wire Without the Busy Indicator Serial Interface Timing Diagram (Status Bits Not Shown)

$\overline{CS}$ MODE, 3-WIRE WITH THE BUSY INDICATOR

This mode is typically used when a single AD4020/AD4021/AD4022 device is connected to an SPI-compatible digital host with an interrupt input ($\overline{IRQ}$). The connection diagram is shown in Figure 57, and the corresponding timing diagram is shown in Figure 58.

Turbo mode must be disabled to use this mode. To disable turbo mode, set the turbo mode enable bit in the configuration register to 0 (see Table 12). Turbo mode is disabled by default.

When performing conversions in this mode, SDI must be held high. SDI can be connected to VIO if register reading and writing is not required. A rising edge on CNV initiates a conversion and forces SDO to high impedance. SDO remains high impedance until the completion of the conversion, irrespective of the state of CNV. Prior to the minimum conversion time, CNV can select other SPI devices, such as analog multiplexers. However, CNV must be returned low before the minimum conversion time (t_{CONV}) elapses and then held low for the maximum possible conversion time to guarantee generating the busy signal indicator. When the conversion is complete, the AD4020/AD4021/AD4022 then enter the acquisition phase and power down. There must not be any digital activity on the SCK during the conversion.

When the conversion is complete, SDO is driven low. With a pull-up resistor (for example, 1 kΩ) on the SDO line, this transition can be used as an interrupt signal to initiate the data reading controlled by the digital host. The data bits are then clocked out MSB first on SDO by subsequent SCK falling edges. The data is valid on both SCK edges. Although the rising edge can capture the data, a digital host using the SCK falling edge allows a faster reading rate, provided it has an acceptable hold time, as dictated by t_{HSDO} (see Table 2). The conversion result is clocked out on SDO on the first 20 SCK falling edges. If the status bits are enabled, they are clocked out on SDO on the 21st through the 26th SCK falling edges (see the Status Bits section). SDO returns to high impedance after an optional additional SCK falling edge or the next CNV rising edge (whichever occurs first).

If multiple AD4020/AD4021/AD4022 devices are selected at the same time, the SDO output pin handles this contention without damage or induced latch-up. It is recommended to keep this contention as short as possible to limit extra power dissipation.

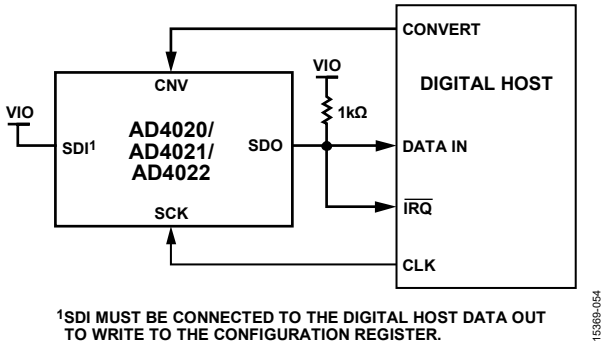


Figure 57. $\overline{CS}$ Mode, 3-Wire with Busy Indicator Connection Diagram

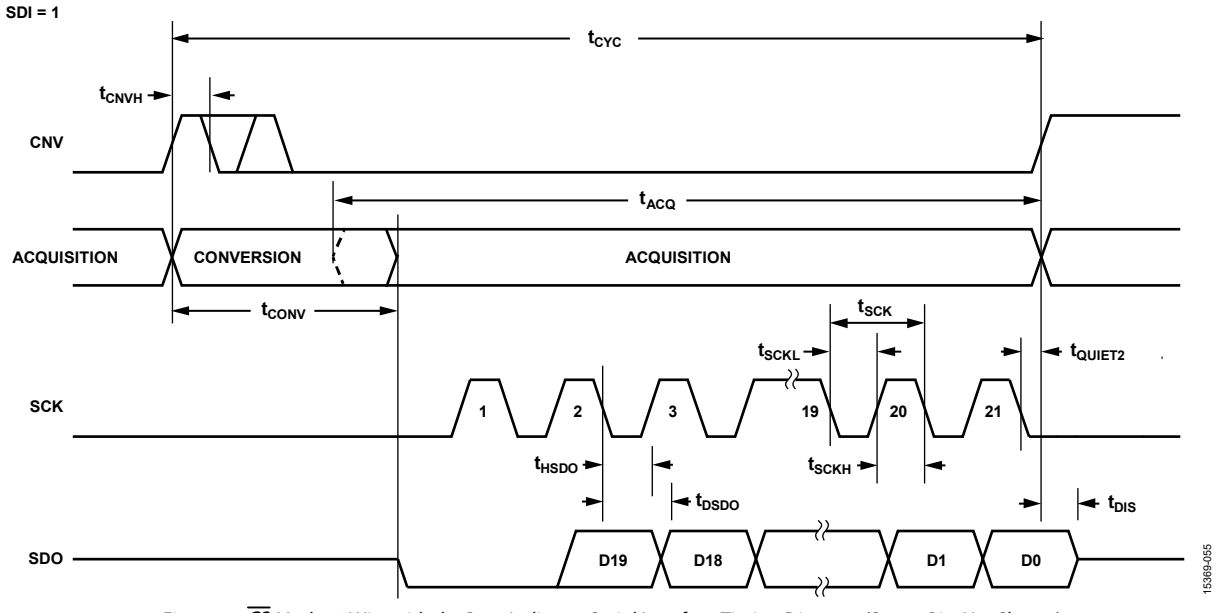


Figure 58. $\overline{CS}$ Mode, 3-Wire with the Busy Indicator Serial Interface Timing Diagram (Status Bits Not Shown)

$\overline{CS}$ MODE, 4-WIRE TURBO MODE

This mode is typically used when a single AD4020/4021/4022 device is connected to an SPI-compatible digital host. Turbo mode allows lower SCK frequencies by increasing the time that the ADC conversion result can be clocked out. The AD4020 can achieve a throughput rate of 1.8 MSPS only when turbo mode is enabled and using a minimum SCK frequency of 71 MHz (see the Serial Clock Frequency Requirements section). The connection diagram is shown in Figure 59, and the corresponding timing diagram is shown in Figure 60.

To enable turbo mode, set the turbo mode enable bit in the configuration register to 1 (see Table 12). This mode replaces the 4-wire with busy indicator mode when turbo mode is enabled. The digital host must be able to write data over SDI to perform register reads and writes (see the Register Read/Write Functionality section). When turbo mode is enabled, the conversion result read on SDO corresponds to the result of the previous conversion.

A rising edge on CNV initiates a conversion and forces SDO to high impedance. CNV must be held high throughout the conversion and data readback phase. When performing conversions in this mode, SDI must be high during the CNV rising edge. The user must wait t_{QUIET1} time after the CNV rising edge before bringing SDI low to clock out the previous conversion result. When the conversion is complete (after t_{CONV}), the AD4020/AD4021/AD4022 enter the acquisition phase and power down.

SDI is analogous to a chip select input, and bringing SDI low outputs the MSB of the conversion result on SDO. The remaining data bits are clocked out on SDO by subsequent SCK falling edges. The data is valid on both SCK edges. Although the rising edge can capture the data, a digital host using the SCK falling edge allows a faster reading rate, provided it has an acceptable hold time, as dictated by t_{HSDO} (see Table 2). The conversion result is clocked out on SDO on the first 20 SCK falling edges. If the status bits are enabled, they are shifted out on SDO on the 21st through the 26th SCK falling edges (see the Status Bits section). SDO returns to high impedance after the final SCK falling edge, or when CNV goes high (whichever occurs first). The user must also provide a delay of t_{QUIET2} between the final SCK falling edge and the next CNV rising edge to ensure specified performance.

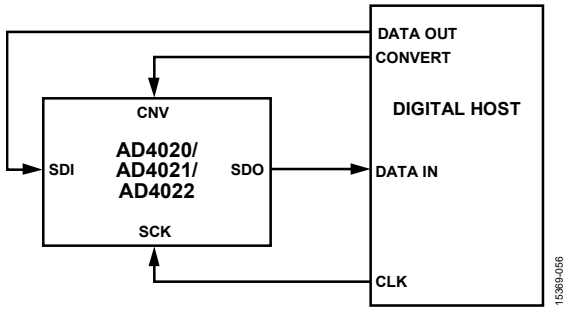


Figure 59. $\overline{CS}$ Mode, 4-Wire Turbo Mode Connection Diagram

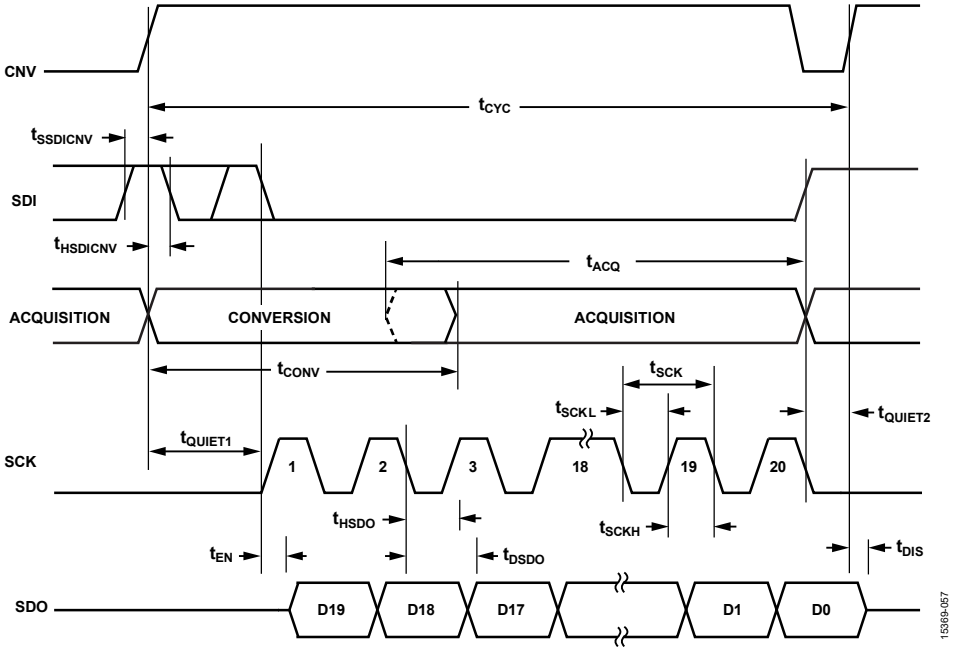


Figure 60. $\overline{CS}$ Mode, 4-Wire Turbo Mode Timing Diagram (Status Bits Not Shown)

$\overline{CS}$ MODE, 4-WIRE WITHOUT THE BUSY INDICATOR

This mode is typically used when multiple AD4020/AD4021/AD4022 devices are connected to an SPI-compatible digital host. A connection diagram using two AD4020/AD4021/AD4022 devices is shown in Figure 61, and the corresponding timing diagram is shown in Figure 62.

Turbo mode must be disabled to use this mode. To disable turbo mode, set the turbo mode enable bit in the configuration register to 0 (see Table 12). Turbo mode is disabled by default.

A rising edge on CNV initiates a conversion and forces SDO to high impedance. When performing conversions in this mode, SDI must be high during the CNV rising edge. CNV must be held high throughout the conversion and data readback phase. When performing conversions in this mode, SDI must be high during the CNV rising edge. Prior to the minimum conversion time (t_{CONV}), SDI can select other SPI devices, such as analog multiplexers. However, SDI must be returned high before the minimum conversion time elapses and then held high for the maximum possible conversion time to avoid generating the busy signal indicator. When the conversion is complete, the AD4020/AD4021/AD4022 enter the acquisition phase and power down. There must not be any digital activity on SCK during the conversion.

SDI is analogous to a chip select input and each ADC result can be read by bringing the corresponding SDI input low. Bringing SDI low on each device outputs the MSB of the conversion result on the corresponding SDO pin. The remaining data bits are clocked out on SDO by subsequent SCK falling edges. The data is valid on both SCK edges. The conversion result is clocked out on SDO on the first 20 SCK falling edges. If the status bits are enabled, they are shifted out on SDO on the 21st through the 26th SCK falling edges (see the Status Bits section). SDO returns to high impedance after the final SCK falling edge, or when SDI goes high (whichever occurs first). If the SDO of each device is tied together, ensure SDI is only low for one device at a time. The user must also provide a delay of t_{QUIET2} between the final SCK falling edge and the next CNV rising edge to ensure specified performance.

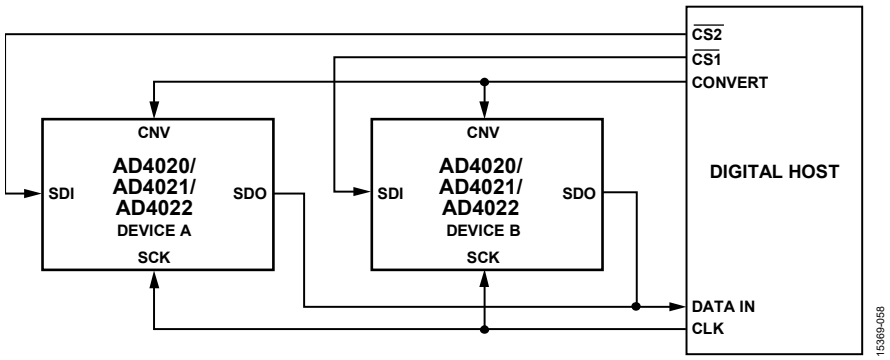


Figure 61. $\overline{CS}$ Mode, 4-Wire Without Busy Indicator Connection Diagram

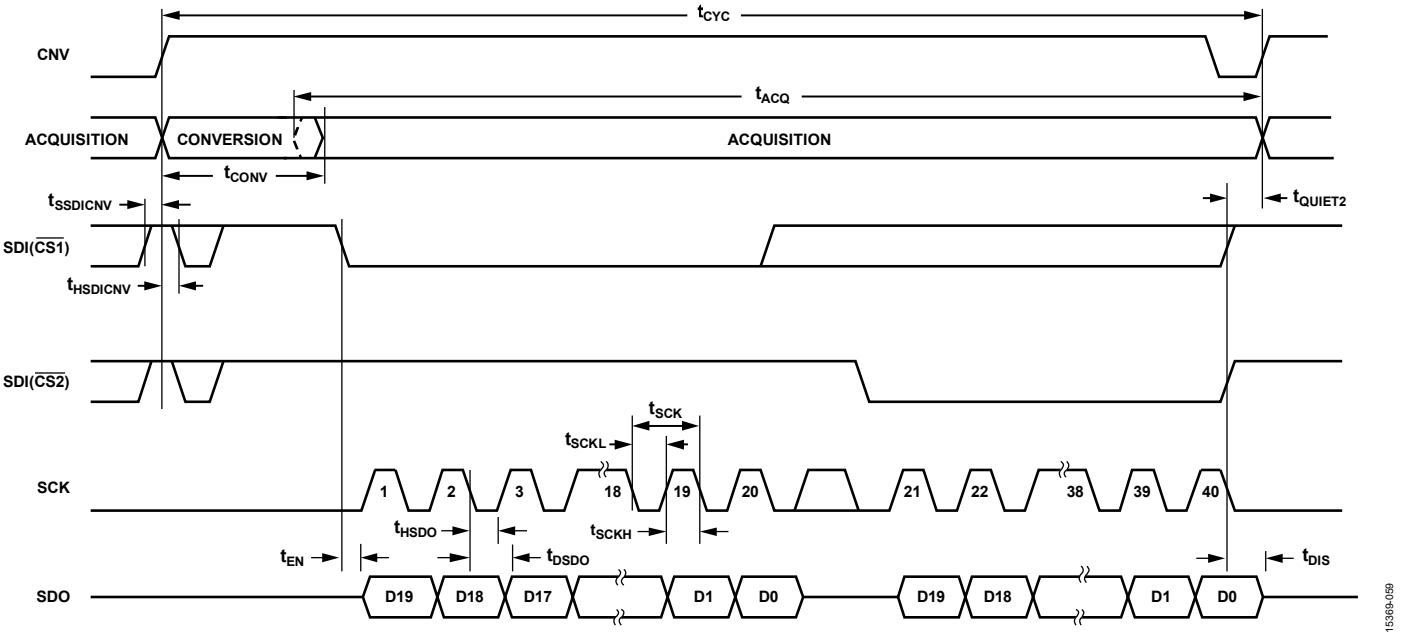


Figure 62. $\overline{CS}$ Mode, 4-Wire Without the Busy Indicator Serial Interface Timing Diagram (Status Bits Not Shown)

$\overline{CS}$ MODE, 4-WIRE WITH THE BUSY INDICATOR

This mode is typically used when a single AD4020/AD4021/AD4022 device is connected to an SPI-compatible digital host with an interrupt input ($\overline{IRQ}$), and when CNV, which samples the analog input, is required to be independent of the signal used to select the data reading. This independence is particularly important in applications where low jitter on CNV is desired. The connection diagram is shown in Figure 63, and the corresponding timing is shown in Figure 64.

Turbo mode must be disabled to use this mode. To disable turbo mode, set the turbo mode enable bit in the configuration register to 0 (see Table 12). Turbo mode is disabled by default.

A rising edge on CNV initiates a conversion and forces SDO to high impedance. When performing conversions in this mode, SDI must be high during the CNV rising edge. CNV must be held high throughout the conversion and data readback phase. When performing conversions in this mode, SDI must be high during the CNV rising edge. Prior to the minimum conversion time (t_{CONV}), SDI can select other SPI devices, such as analog multiplexers. However, SDI must be returned low before the minimum conversion time elapses and then held low for the maximum possible conversion time to guarantee generating the busy signal indicator. When the conversion is complete, the AD4020/AD4021/AD4022 enter the acquisition phase and power down. There must not be any digital activity on SCK during the conversion.

When the conversion is complete, SDO is driven low. With a pull-up resistor (for example, 1 kΩ) on the SDO line, this transition can be used as an interrupt signal to initiate the data reading controlled by the digital host. The data bits are then clocked out MSB first on SDO by subsequent SCK falling edges. The data is valid on both SCK edges. Although the rising edge can capture the data, a digital host using the SCK falling edge allows a faster reading rate, provided it has an acceptable hold time, as dictated by t_{HSDO} (see Table 2). The conversion result is clocked out on SDO on the first 20 SCK falling edges. If the status bits are enabled, they are clocked out on SDO on the 21st through the 26th SCK falling edges (see the Status Bits section). SDO returns to high impedance after an optional additional SCK falling edge or the next CNV rising edge (whichever occurs first).

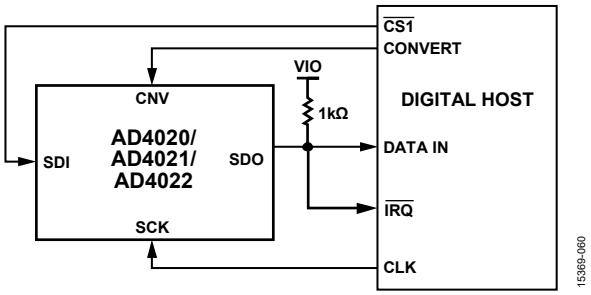


Figure 63. $\overline{CS}$ Mode, 4-Wire with Busy Indicator Connection Diagram

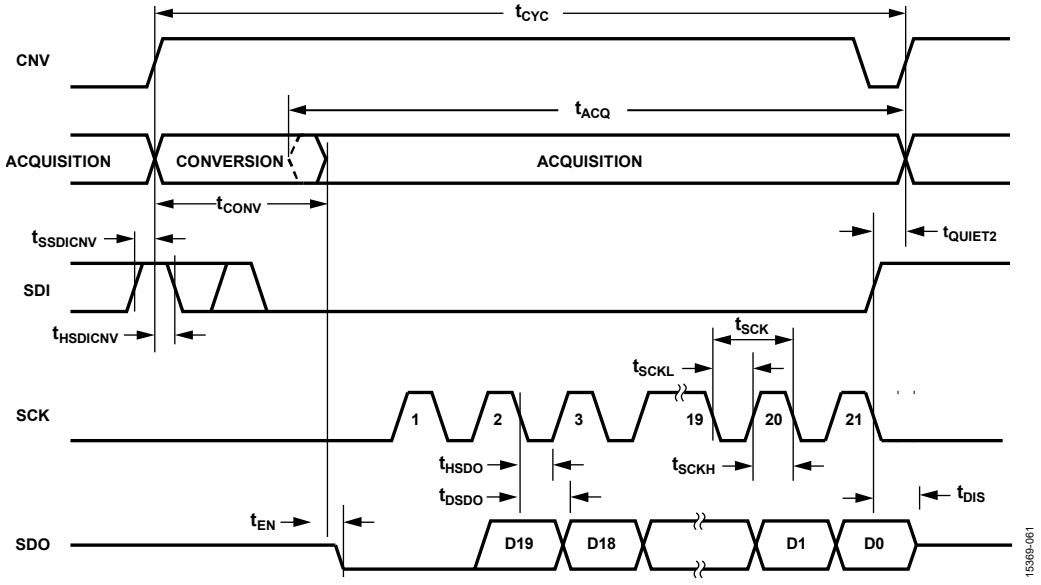


Figure 64. $\overline{CS}$ Mode, 4-Wire with the Busy Indicator Serial Interface Timing Diagram (Status Bits Not Shown)

DAISY-CHAIN MODE

Use this mode to daisy-chain multiple AD4020/AD4021/AD4022 devices on a 3-wire or 4-wire serial interface. This feature is useful for reducing component count and wiring connections such as cases with isolated multiconverter applications or for systems with a limited interfacing capacity. Data readback is analogous to clocking a shift register. A connection diagram example using two AD4020/AD4021/AD4022 devices is shown in Figure 65, and the corresponding timing diagram is shown in Figure 66.

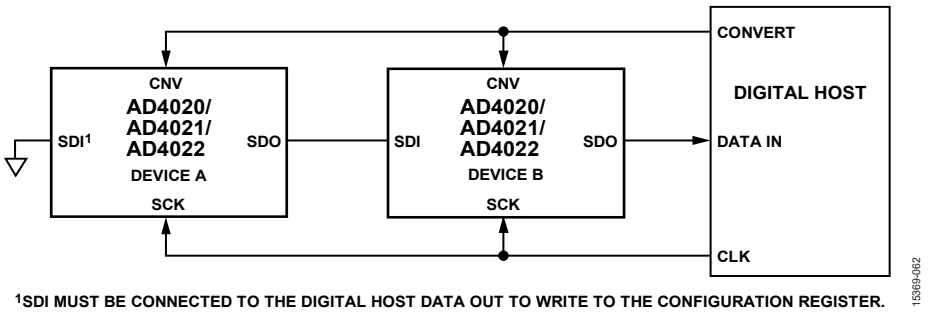
Turbo mode must be disabled to use this mode. To disable turbo mode, set the turbo mode enable bit in the configuration register to 0 (see Table 12). Writing to the user configuration register requires SDI to be connected to the digital host (see the Register Read/Write Functionality section). Turbo mode is disabled by default.

When SDI and CNV are low, SDO is driven low. A rising edge on CNV initiates a conversion and SDO remains low. When performing conversions in this mode, SDI and SCK must be low during the CNV rising edge. CNV must be held high throughout the conversion and data readback phase.

When the conversion is complete, the MSB is output onto SDO of each device, and the AD4020/AD4021/AD4022 enter the acquisition phase and power down. The remaining data bits are clocked out on SDO by subsequent SCK falling edges. For each ADC, SDI feeds the input of the internal shift register and is clocked in on each SCK rising edge. Results are therefore passed through each device until they are all received by the digital host. When the status bits are disabled, 20 × N clocks are required to read back N ADCs. When the status bits are enabled, 26 × N clocks are required to read back the conversion data and status bits for N ADCs. The data is valid on both SCK edges.

The maximum achievable conversion rate when using daisy-chain mode is typically less than when reading a single device because the number of bits to clock out is larger (see the Serial Clock Frequency Requirements section).

It is possible to write to each ADC register in daisy-chain mode. The timing diagram is shown in Figure 51. This mode requires 4-wire operation because data is clocked in on the SDI line with CNV held low. The same command byte and register data can be shifted through the entire chain to program all ADCs in the chain with the same register contents, which requires 8 × (N + 1) clocks for N ADCs. It is possible to write different register contents to each ADC in the chain by first writing to the furthest ADC in the chain first, using 8 × (N + 1) clocks, and then the second furthest ADC with 8 × N clocks, and so forth until reaching the nearest ADC in the chain, which requires 16 clocks for the command and register data. It is not possible to read register contents in daisy-chain mode.



[1]SDI MUST BE CONNECTED TO THE DIGITAL HOST DATA OUT TO WRITE TO THE CONFIGURATION REGISTER.

Figure 65. Daisy-Chain Mode, Connection Diagram

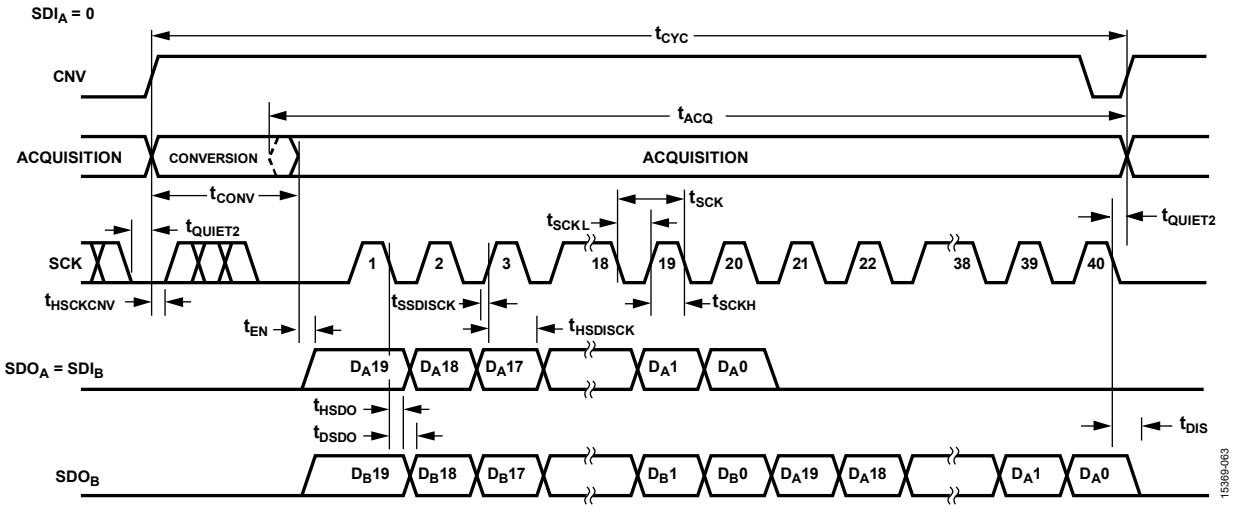


Figure 66. Daisy-Chain Mode Serial Interface Timing Diagram (Status Bits Not Shown)

LAYOUT GUIDELINES

The PCB that houses the AD4020/AD4021/AD4022 must be designed so that the analog and digital sections are physically separated, such as on opposite sides of the device as shown in Figure 67. The pinout of the AD4020/AD4021/AD4022, with the analog signals on the left side and the digital signals on the right side, helps to separate the analog and digital signals.

Avoid running digital lines under the device because they couple noise onto the die, unless a ground plane under the AD4020/AD4021/AD4022 is used as a shield. Fast switching signals, such as CNV or clocks, must not run near analog signal paths. Avoid crossover of digital and analog signals.

At least one ground plane must be used. The ground plane can be common or split between the digital and analog sections. In the latter case, join the planes underneath the AD4020/AD4021/AD4022 devices.

The AD4020/AD4021/AD4022 voltage reference input (REF) has a dynamic input impedance. Decouple the REF pin with minimal parasitic inductances by placing the reference decoupling ceramic capacitor close to (ideally right up against) the REF and GND pins, and connect them with wide, low impedance traces.

Finally, decouple the VDD and VIO power supplies of the AD4020/AD4021/AD4022 with ceramic capacitors, typically 0.1 µF, placed close to the AD4020/AD4021/AD4022 and connected using short, wide traces to provide low impedance paths and to reduce the effect of glitches on the power supply lines.

An example of the AD4020 layout following these rules is shown in Figure 67 and Figure 68. Note that the AD4021/AD4022 layout is equivalent to the AD4020 layout.

EVALUATING THE AD4020/AD4021/AD4022 PERFORMANCE

Other recommended layouts for the AD4020/AD4021/AD4022 are outlined in the user guide of the evaluation board for the AD4020 (EVAL-AD4020FMCZ). The evaluation board package includes a fully assembled and tested evaluation board with the AD4020, the UG-1042 user guide, and software for controlling the board from a PC via the EVAL-SDP-CH1Z. The EVAL-AD4020FMCZ can also be used to evaluate the AD4021/AD4022 by limiting the throughput to 1 MSPS and 500 kSPS, respectively, in the software (see UG-1042 for more information).

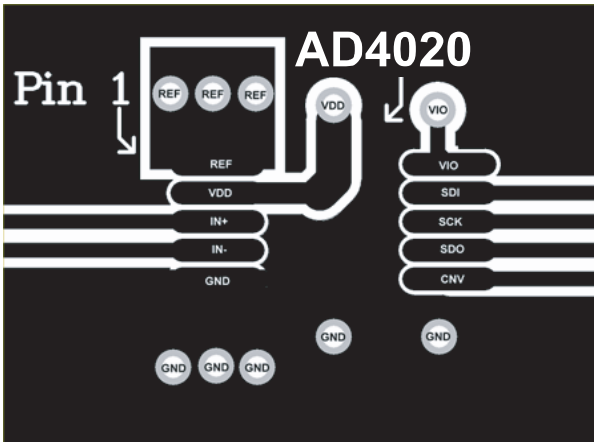


Figure 67. Example Layout of the AD4020 (Top Layer)

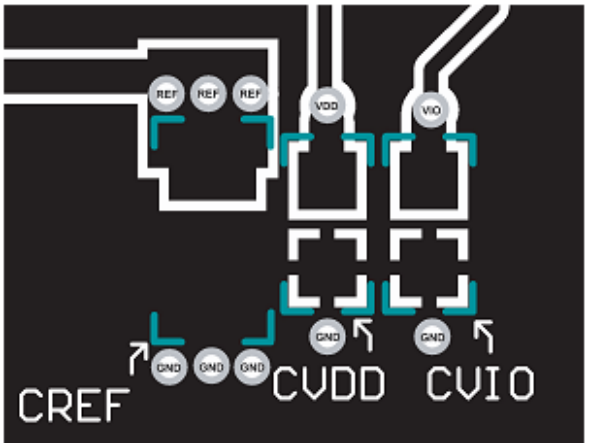


Figure 68. Example Layout of the AD4020 (Bottom Layer)

OUTLINE DIMENSIONS

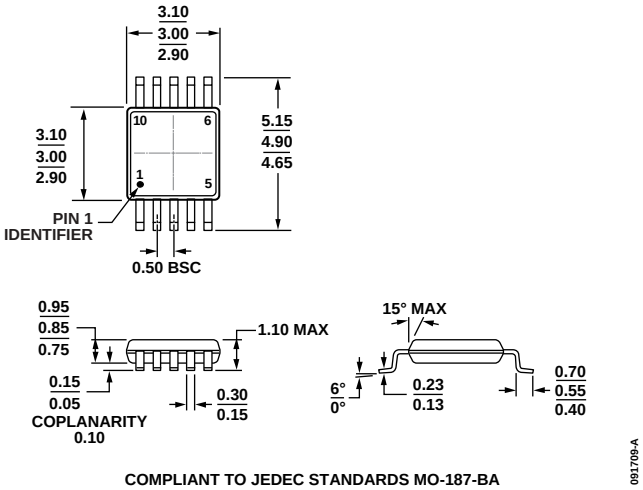


Figure 69. 10-Lead Mini Small Outline Package [MSOP]
(RM-10)
Dimensions shown in millimeters

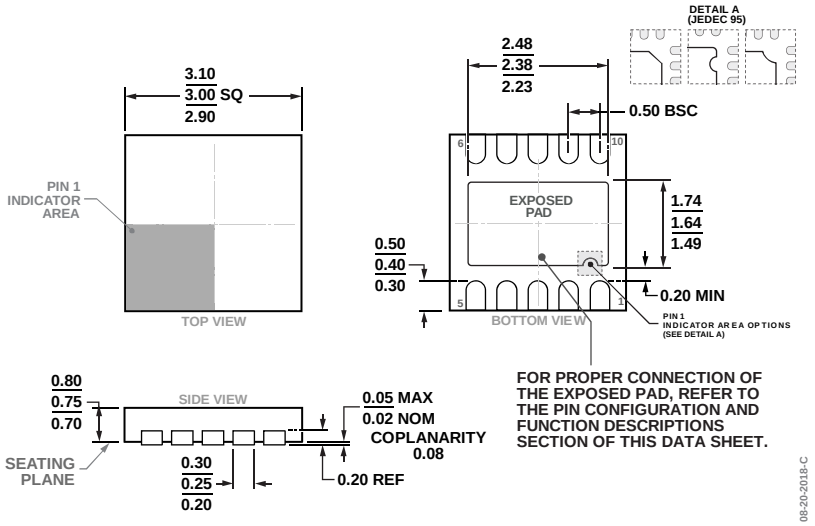


Figure 70. 10-Lead Lead Frame Chip Scale Package [LFCSP]
3 mm × 3 mm Body and 0.75 mm Package Height
(CP-10-9)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2]	Integral Nonlinearity (INL)	Temperature Range	Package Description	Ordering Quantity	Package Option	Marking Code
AD4020BRMZ	±3.1 ppm	−40°C to +125°C	10-Lead MSOP, Tube	50	RM-10	C8L
AD4020BRMZ-RL7	±3.1 ppm	−40°C to +125°C	10-Lead MSOP, Reel	1000	RM-10	C8L
AD4020BCPZ-R2	±3.1 ppm	−40°C to +125°C	10-Lead LFCSP, Reel	250	CP-10-9	C8L
AD4020BCPZ-RL7	±3.1 ppm	−40°C to +125°C	10-Lead LFCSP, Reel	1500	CP-10-9	C8L
AD4021BRMZ	±3.1 ppm	−40°C to +125°C	10-Lead MSOP, Tube	50	RM-10	CAD
AD4021BRMZ-RL7	±3.1 ppm	−40°C to +125°C	10-Lead MSOP, Reel	1000	RM-10	CAD
AD4021BCPZ-R2	±3.1 ppm	−40°C to +125°C	10-Lead LFCSP, Reel	250	CP-10-9	CAC
AD4021BCPZ-RL7	±3.1 ppm	−40°C to +125°C	10-Lead LFCSP, Reel	1500	CP-10-9	CAC
AD4022BRMZ	±3.1 ppm	−40°C to +125°C	10-Lead MSOP, Tube	50	RM-10	CAF
AD4022BRMZ-RL7	±3.1 ppm	−40°C to +125°C	10-Lead MSOP, Reel	1000	RM-10	CAF
AD4022BCPZ-R2	±3.1 ppm	−40°C to +125°C	10-Lead LFCSP, Reel	250	CP-10-9	CAE
AD4022BCPZ-RL7	±3.1 ppm	−40°C to +125°C	10-Lead LFCSP, Reel	1500	CP-10-9	CAE
EVAL-AD4020FMCZ			AD4020 Evaluation Board Compatible with EVAL-SDP-CH1Z			

[1] Z = RoHS Compliant Part.
[2] The EVAL-AD4020FMCZ can evaluate the AD4021 and AD4022 by setting the throughput to 1 MSPS and 500 kSPS in its software, respectively (see the UG-1042).

D15369-0-11/19(B)

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Analog Devices Inc.:

AD4020BCPZ-RL7 AD4020BRMZ-RL7 AD4020BRMZ EVAL-AD4020FMCZ EV-AD4020-REF-DGNZ AD4022BCPZ-R2 AD4022BCPZ-RL7 AD4021BCPZ-R2 AD4021BCPZ-RL7 AD4021BRMZ-RL7 AD4021BRMZ AD4022BRMZ-RL7 AD4022BRMZ