

74HC1G32; 74HCT1G32

2-input OR gate

Rev. 6 — 18 January 2022

Product data sheet

1. General description

The 74HC1G32; 74HCT1G32 is a single 2-input OR gate. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC} .

2. Features and benefits

- Wide supply voltage range from 2.0 V to 6.0 V
- Symmetrical output impedance
- High noise immunity
- CMOS low power dissipation
- Balanced propagation delays
- Latch-up performance exceeds 100 mA per JESD78 Class II Level B
- Input levels:
 - For 74HC1G32: CMOS level
 - For 74HCT1G32: TTL level
- Complies with JEDEC standards:
 - JESD8C (2.7 V to 3.6 V)
 - JESD7A (2.0 V to 6.0 V)
- ESD protection
 - HBM JESD22-A114-A exceeds 2000 V
 - MM JESD22-A115-A exceeds 200 V
- Specified from -40°C to $+85^{\circ}\text{C}$ and from -40°C to $+125^{\circ}\text{C}$

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC1G32GW	-40°C to $+125^{\circ}\text{C}$	TSSOP5	plastic thin shrink small outline package; 5 leads; body width 1.25 mm	SOT353-1
74HCT1G32GW				
74HC1G32GV	-40°C to $+125^{\circ}\text{C}$	SC-74A	plastic surface-mounted package; 5 leads	SOT753
74HCT1G32GV				

4. Marking

Table 2. Marking codes

Type number	Marking code[1]
74HC1G32GW	HG
74HCT1G32GW	TG
74HC1G32GV	H32
74HCT1G32GV	T32

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

5. Functional diagram

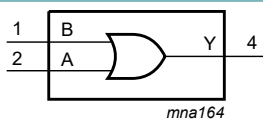


Fig. 1. Logic symbol

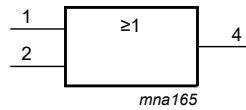


Fig. 2. IEC logic symbol

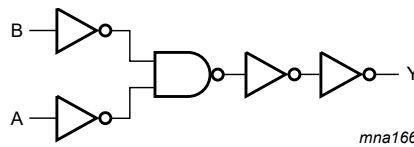


Fig. 3. Logic diagram

6. Pinning information

6.1. Pinning

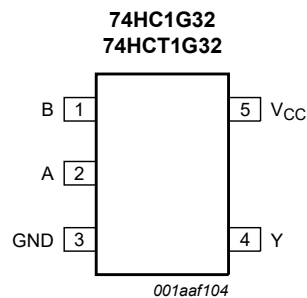


Fig. 4. Pin configuration for SOT353-1 (TSSOP5) and SOT753 (SC-74A)

6.2. Pin description

Table 3. Pin description

Symbol	Pin	Description
B	1	data input B
A	2	data input A
GND	3	ground (0 V)
Y	4	data output Y
V _{CC}	5	supply voltage

7. Functional description

Table 4. Function table

H = HIGH voltage level; L = LOW voltage level

Inputs		Output
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	H

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+7.0	V
I _{IK}	input clamping current	V _I < -0.5 V or V _I > V _{CC} + 0.5 V	-	±20	mA
I _{OK}	output clamping current	V _O < -0.5 V or V _O > V _{CC} + 0.5 V	-	±20	mA
I _O	output current	-0.5 V < V _O < V _{CC} + 0.5 V	[1]	±12.5	mA
I _{CC}	supply current		-	25	mA
I _{GND}	ground current		-25	-	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	T _{amb} = -40 °C to +125 °C	[2]	250	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SOT353-1 (TSSOP5) package: P_{tot} derates linearly with 3.3 mW/K above 74 °C.
For SOT753 (SC-74A) package: P_{tot} derates linearly with 3.8 mW/K above 85 °C.

9. Recommended operating conditions

Table 6. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	74HC1G32			74HCT1G32			Unit
			Min	Typ	Max	Min	Typ	Max	
V _{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V _I	input voltage		0	-	V _{CC}	0	-	V _{CC}	V
V _O	output voltage		0	-	V _{CC}	0	-	V _{CC}	V
T _{amb}	ambient temperature		-40	+25	+125	-40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate	V _{CC} = 2.0 V	-	-	625	-	-	-	ns/V
		V _{CC} = 4.5 V	-	-	139	-	-	139	ns/V
		V _{CC} = 6.0 V	-	-	83	-	-	-	ns/V

10. Static characteristics

Table 7. Static characteristics

Voltages are referenced to GND (ground = 0 V). All typical values are measured at T_{amb} = 25 °C.

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	
74HC1G32								
V _{IH}	HIGH-level input voltage	V _{CC} = 2.0 V	1.5	1.2	-	1.5	-	V
		V _{CC} = 4.5 V	3.15	2.4	-	3.15	-	V
		V _{CC} = 6.0 V	4.2	3.2	-	4.2	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 2.0 V	-	0.8	0.5	-	0.5	V
		V _{CC} = 4.5 V	-	2.1	1.35	-	1.35	V
		V _{CC} = 6.0 V	-	2.8	1.8	-	1.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}						
		I _O = -20 μA; V _{CC} = 2.0 V	1.9	2.0	-	1.9	-	V
		I _O = -20 μA; V _{CC} = 4.5 V	4.4	4.5	-	4.4	-	V
		I _O = -20 μA; V _{CC} = 6.0 V	5.9	6.0	-	5.9	-	V
		I _O = -2.0 mA; V _{CC} = 4.5 V	4.13	4.32	-	3.7	-	V
V _{OL}	LOW-level output voltage	I _O = -2.6 mA; V _{CC} = 6.0 V	5.63	5.81	-	5.2	-	V
		V _I = V _{IH} or V _{IL}						
		I _O = 20 μA; V _{CC} = 2.0 V	-	0	0.1	-	0.1	V
		I _O = 20 μA; V _{CC} = 4.5 V	-	0	0.1	-	0.1	V
		I _O = 20 μA; V _{CC} = 6.0 V	-	0	0.1	-	0.1	V
I _I	input leakage current	I _O = 2.0 mA; V _{CC} = 4.5 V	-	0.15	0.33	-	0.4	V
		I _O = 2.6 mA; V _{CC} = 6.0 V	-	0.16	0.33	-	0.4	V
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 6.0 V	-	-	10	-	20	μA
C _I	input capacitance		-	1.5	-	-	-	pF

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	
74HCT1G32								
V _{IH}	HIGH-level input voltage	V _{CC} = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V						
		I _O = -20 µA	4.4	4.5	-	4.4	-	V
		I _O = -2.0 mA	4.13	4.32	-	3.7	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V						
		I _O = 20 µA	-	0	0.1	-	0.1	V
		I _O = 2.0 mA	-	0.15	0.33	-	0.4	V
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 5.5 V	-	-	1.0	-	1.0	µA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V	-	-	10	-	20	µA
ΔI _{CC}	additional supply current	per input; V _{CC} = 4.5 V to 5.5 V; V _I = V _{CC} - 2.1 V; I _O = 0 A	-	-	500	-	850	µA
C _I	input capacitance		-	1.5	-	-	-	pF

11. Dynamic characteristics

Table 8. Dynamic characteristics

GND = 0 V; $t_r = t_f \leq 6.0$ ns. All typical values are measured at $T_{amb} = 25$ °C. For test circuit see Fig. 6

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	
74HC1G32								
t _{pd}	propagation delay	A and B to Y; see Fig. 5 [1]						
		V _{CC} = 2.0 V; C _L = 50 pF	-	18	115	-	135	ns
		V _{CC} = 4.5 V; C _L = 50 pF	-	8	23	-	27	ns
		V _{CC} = 5.0 V; C _L = 15 pF	-	8	-	-	-	ns
		V _{CC} = 6.0 V; C _L = 50 pF	-	7	20	-	23	ns
C _{PD}	power dissipation capacitance	V _I = GND to V _{CC} [2]	-	19	-	-	-	pF
74HCT1G32								
t _{pd}	propagation delay	A and B to Y; see Fig. 5 [1]						
		V _{CC} = 4.5 V; C _L = 50 pF	-	10	24	-	27	ns
		V _{CC} = 5.0 V; C _L = 15 pF	-	10	-	-	-	ns
C _{PD}	power dissipation capacitance	V _I = GND to V _{CC} - 1.5 V [2]	-	20	-	-	-	pF

[1] t_{pd} is the same as t_{PLH} and t_{PHL}.

[2] C_{PD} is used to determine the dynamic power dissipation P_D (µW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz

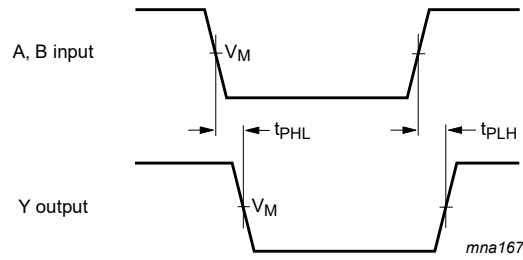
f_o = output frequency in MHz

C_L = output load capacitance in pF

V_{CC} = supply voltage in V

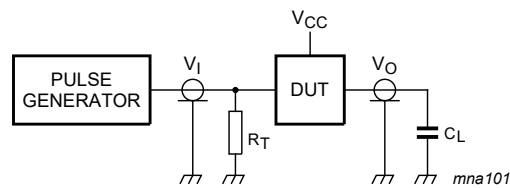
Σ(C_L × V_{CC}² × f_o) = sum of outputs

11.1. Waveforms and test circuit



For 74HC1G32: $V_M = 0.5 \times V_{CC}$; $V_I = \text{GND to } V_{CC}$
 For 74HCT1G32: $V_M = 1.3 \text{ V}$; $V_I = \text{GND to } 3.0 \text{ V}$

Fig. 5. The input (A and B) to output (Y) propagation delays



Measurement points are given in [Table 8](#). Definitions for test circuit:

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

Fig. 6. Test circuit for measuring switching times

12. Package outline

TSSOP5: plastic thin shrink small outline package; 5 leads; body width 1.25 mm

SOT353-1

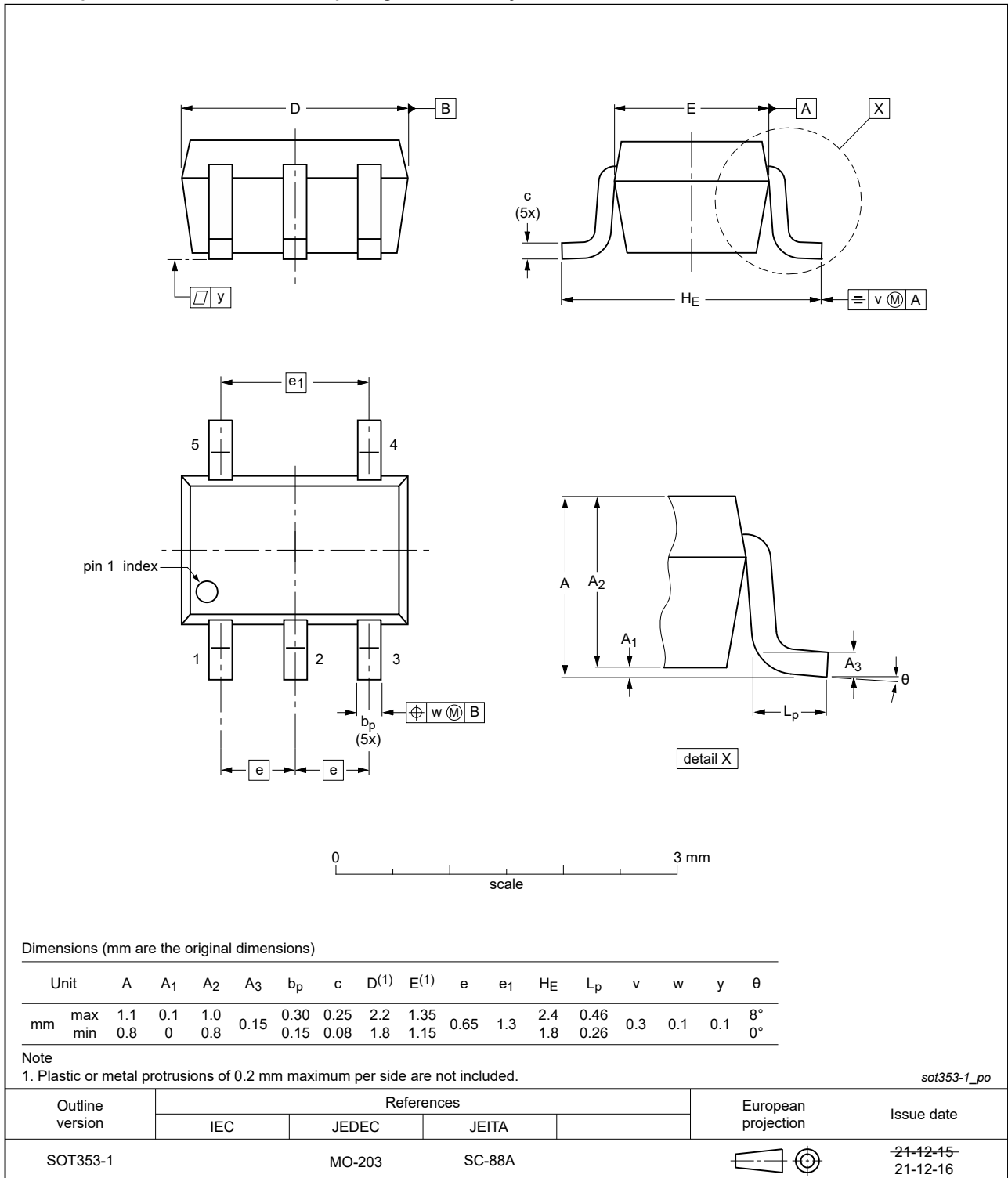


Fig. 7. Package outline SOT353-1 (TSSOP5)

Plastic surface-mounted package; 5 leads

SOT753

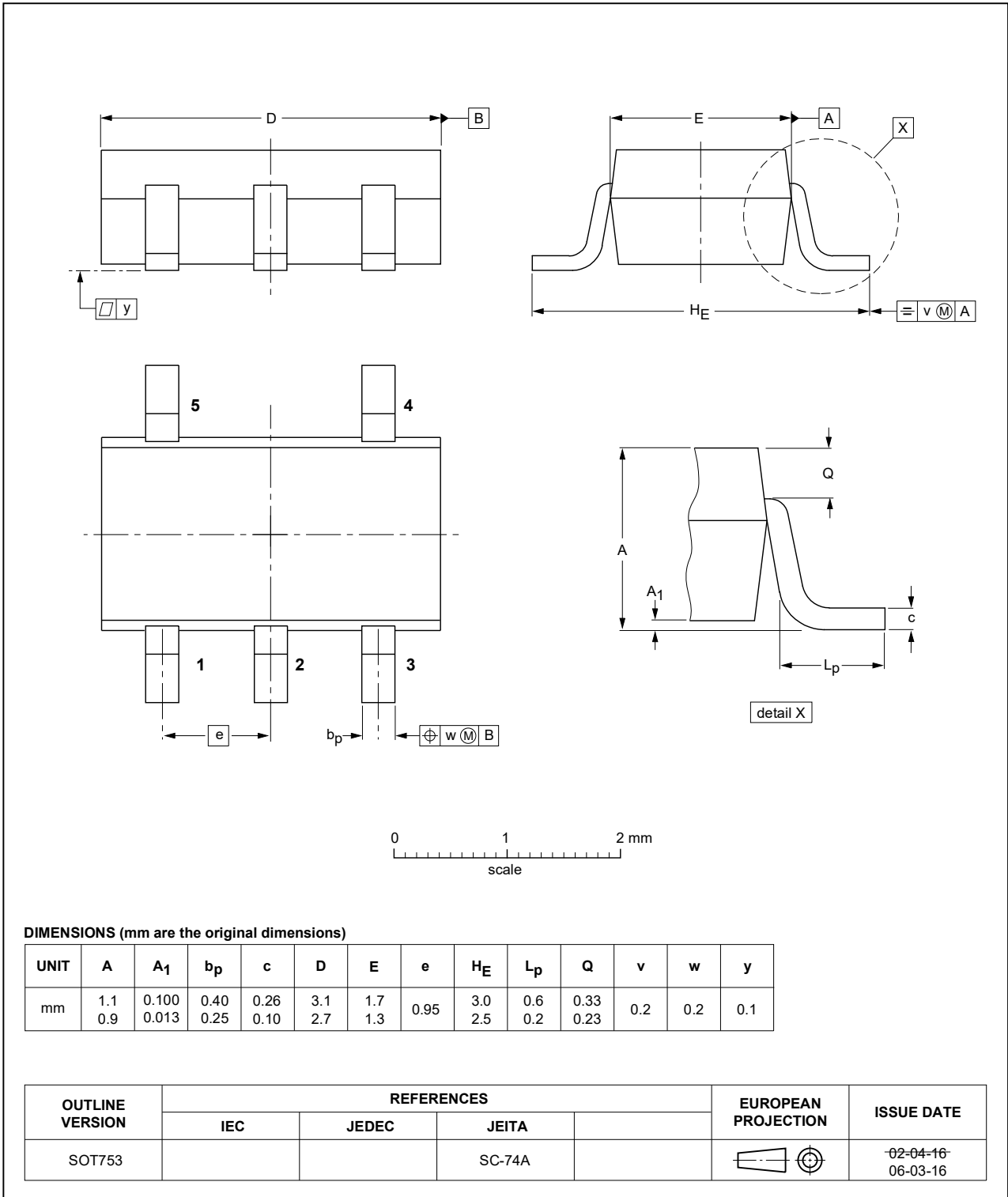


Fig. 8. Package outline SOT753 (SC-74A)

13. Abbreviations

Table 9. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT1G32v.6	20220118	Product data sheet	-	74HC_HCT1G32v.5
Modifications:	<ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. Section 1 and Section 2 updated. Table 5: Derating values for P_{tot} total power dissipation updated. Fig. 7: Package outline drawing for SOT353-1 (TSSOP5) has changed. 			
74HC_HCT1G32v.5	20080314	Product data sheet	-	74HC_HCT1G32v.4
Modifications:	<ul style="list-style-type: none"> Pin description of Pin 4 changed from input to output in Table 3. 			
74HC_HCT1G32v.4	20070514	Product data sheet	-	74HC_HCT1G32v.3
74HC_HCT1G32v.3	20020515	Product specification	-	74HC_HCT1G32v.2
74HC_HCT1G32v.2	20010406	Product specification	-	74HC_HCT1G32
74HC_HCT1G32	19971216	Preliminary specification	-	-

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Document status [1][2]	Product status [3]	Definition
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- [2] The term 'short data sheet' is explained in section "Definitions".
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Contents

1. General description	1
2. Features and benefits	1
3. Ordering information	1
4. Marking	2
5. Functional diagram	2
6. Pinning information	2
6.1. Pinning.....	2
6.2. Pin description.....	3
7. Functional description	3
8. Limiting values	3
9. Recommended operating conditions	4
10. Static characteristics	4
11. Dynamic characteristics	5
11.1. Waveforms and test circuit.....	6
12. Package outline	7
13. Abbreviations	9
14. Revision history	9
15. Legal information	10

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