

74LVT08

3.3 V Quad 2-input AND gate

Rev. 3 — 22 March 2017

Product data sheet

1 General description

The 74LVT08 is a high-performance BiCMOS product designed for V_{CC} operation at 3.3 V.

The 74LVT08 is a quad 2-input AND gate.

2 Features and benefits

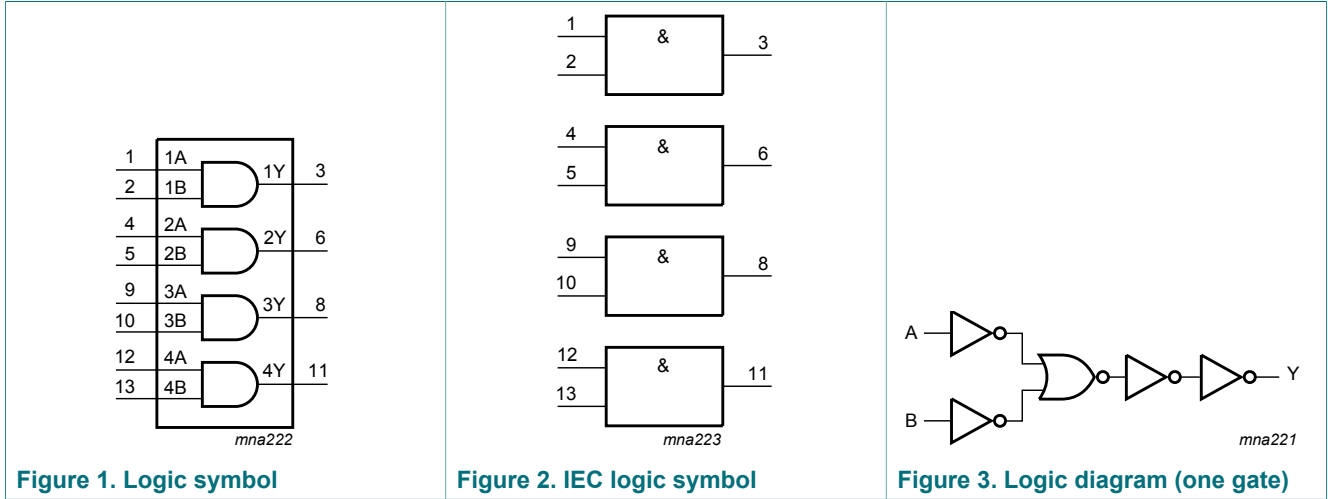
- Wide supply voltage range from 2.7 V to 3.6 V
- Output capability: +64 mA and -32 mA
- TTL input and output switching levels
- Latch-up protection
 - JESD78 Class II exceeds 500 mA
- Complies with JEDEC standards:
 - JESD8C (2.7 V to 3.6 V)
- ESD protection:
 - HBM JESD22-A114E exceeds 2000 V
 - MM JESD22-A115-A exceeds 200 V
- Specified from -40 °C to 85 °C

3 Ordering information

Table 1. Ordering information

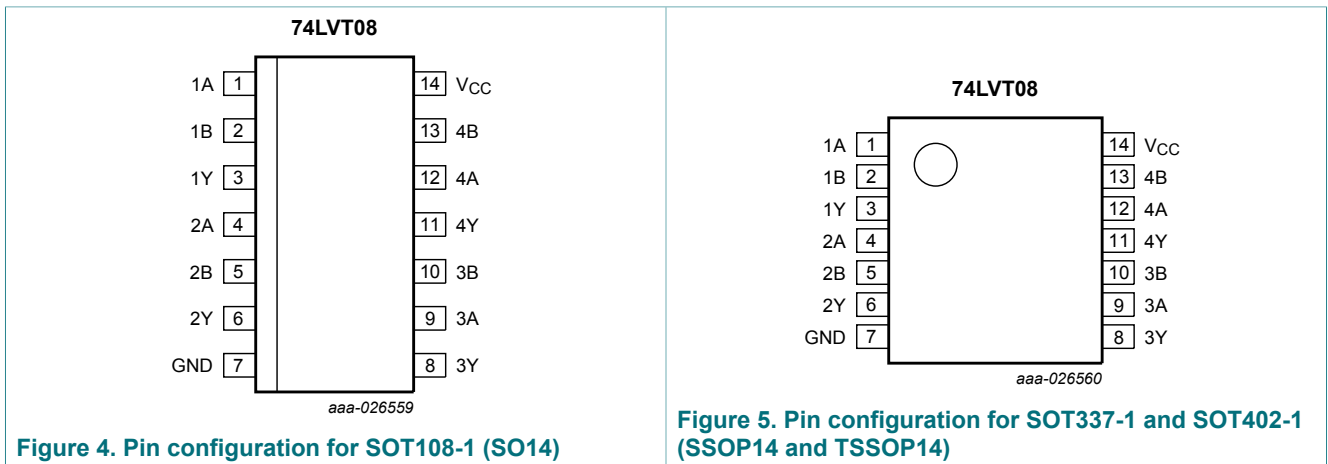
Type number	Package			
	Temperature range	Name	Description	Version
74LVT08D	-40 °C to +85 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74LVT08DB	-40 °C to +85 °C	SSOP14	plastic shrink small outline package; 14 leads; body width 5.3 mm	SOT337-1
74LVT08PW	-40 °C to +85 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1

4 Functional diagram



5 Pinning information

5.1 Pinning



5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
1Y to 4Y	3, 6, 8, 11	data output
1A to 4A	1, 4, 9, 12	data input
1B to 4B	2, 5, 10, 13	data input
GND	7	ground (0 V)
V _{CC}	14	supply voltage

6 Functional description

Table 3. Function table ^[1]

Input		Output
nA	nB	nY
H	H	H
H	L	L
L	H	L
L	L	L

[1] H = HIGH voltage level; L = LOW voltage level

7 Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+4.6	V
V _I	input voltage		[1] -0.5	+7.0	V
V _O	output voltage	output in OFF-state or HIGH-state	[1] -0.5	+7.0	V
I _{IK}	input clamping current	V _I < 0 V	-50	-	mA
I _{OK}	output clamping current	V _O < 0 V	-50	-	mA
I _O	output current	output in LOW-state	-	64	mA
		output in HIGH-state	-32	-	mA
T _{stg}	storage temperature		-65	+150	°C
T _j	junction temperature		[2] -	150	°C
P _{tot}	total power dissipation	T _{amb} = -40 to +85 °C	[3] -	500	mW

[1] The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

[3] For SO14 packages: above 70 °C derate linearly with 8 mW/K.
For SSOP14 and TSSOP14 packages: above 60 °C derate linearly with 5.5 mW/K.

8 Recommended operating conditions

Table 5. Operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{CC}	supply voltage		2.7	-	3.6	V
V _I	input voltage		0	-	5.5	V
I _{OH}	HIGH-level output current		-20	-	-	mA
I _{OL}	LOW-level output current		-	-	32	mA

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb}	ambient temperature	in free-air	-40	-	+85	°C
$\Delta t/\Delta V$	input transition rise and fall rate	outputs enabled	-	-	10	ns/V

9 Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ ^[1]	Max	Unit
$T_{amb} = -40\text{ °C to }+85\text{ °C}$						
V_{IK}	input clamping voltage	$V_{CC} = 2.7\text{ V}; I_{IK} = -18\text{ mA}$	-1.2	-	-	V
V_{IH}	HIGH-level input voltage		2.0	-	-	V
V_{IL}	LOW-level input voltage		-	-	0.8	V
V_{OH}	HIGH-level output voltage	$V_{CC} = 2.7\text{ V to }3.6\text{ V}; I_{OH} = -100\text{ }\mu\text{A}$	$V_{CC} - 0.2$	-	-	V
		$V_{CC} = 2.7\text{ V}; I_{OH} = -6\text{ mA}$	2.4	-	-	V
		$V_{CC} = 3.0\text{ V}; I_{OH} = -20\text{ mA}$	2.0	-	-	V
V_{OL}	LOW-level output voltage	$V_{CC} = 2.7\text{ V}; I_{OL} = 100\text{ }\mu\text{A}$	-	-	0.2	V
		$V_{CC} = 2.7\text{ V}; I_{OL} = 24\text{ mA}$	-	-	0.5	V
		$V_{CC} = 3.0\text{ V}; I_{OL} = 32\text{ mA}$	-	-	0.5	V
I_I	input leakage current	$V_{CC} = 0\text{ V or }3.6\text{ V}; V_I = 5.5\text{ V}$	-	-	10	μA
		$V_{CC} = 3.6\text{ V}; V_I = V_{CC}\text{ or GND}$	-	-	± 1	μA
I_{OFF}	power-off leakage current	$V_{CC} = 0\text{ V}; V_I\text{ or }V_O = 0\text{ V to }4.5\text{ V}$	-	-	± 100	μA
I_{CC}	supply current	$V_{CC} = 3.6\text{ V}; V_I = \text{GND or }V_{CC}; I_O = 0\text{ A}$	-	-	-	-
		output HIGH	-	-	0.02	mA
		output LOW	-	1	2	mA
ΔI_{CC}	additional supply current	per input pin; $V_{CC} = 3.0\text{ V to }3.6\text{ V};$ one input at $V_{CC} - 0.6\text{ V}$ and other inputs at $V_{CC}\text{ or GND}$ ^[2]	-	-	0.2	μA
C_I	input capacitance	$V_I = 0\text{ V or }3.0\text{ V}$	-	4	-	pF
C_O	output capacitance	$V_O = 0\text{ V or }3.0\text{ V}$	-	10	-	pF

[1] Typical values are measured at $T_{amb} = 25\text{ °C}$ and $V_{CC} = 3.3\text{ V}$.

[2] This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND.

10 Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 7](#).

Symbol	Parameter	Conditions	Min	Typ ^[1]	Max	Unit
$T_{amb} = -40\text{ }^{\circ}\text{C to } +85\text{ }^{\circ}\text{C}$						
t_{PLH}	LOW to HIGH propagation delay	nA or nB to nY; see Figure 6				
		$V_{CC} = 2.7\text{ V}$	-	-	4.7	ns
		$V_{CC} = 3.0\text{ V to } 3.6\text{ V}$	1	3.0	3.9	ns
t_{PHL}	HIGH to LOW propagation delay	nA or nB to nY; see Figure 6				
		$V_{CC} = 2.7\text{ V}$	-	-	4.8	ns
		$V_{CC} = 3.0\text{ V to } 3.6\text{ V}$	1	3.4	4.6	ns

[1] Typical values are measured at $V_{CC} = 3.3\text{ V}$ and $T_{amb} = 25\text{ }^{\circ}\text{C}$.

10.1 Waveforms and test circuit

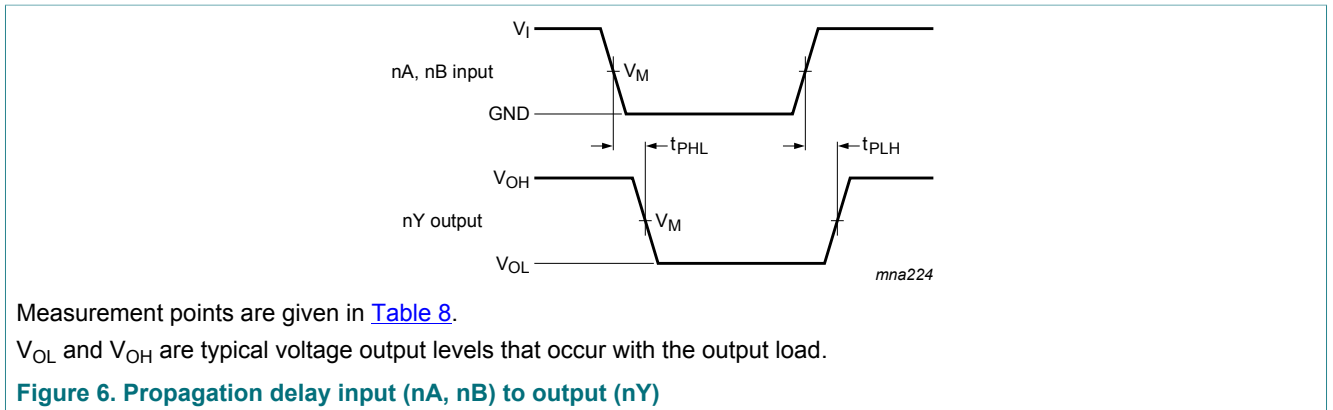
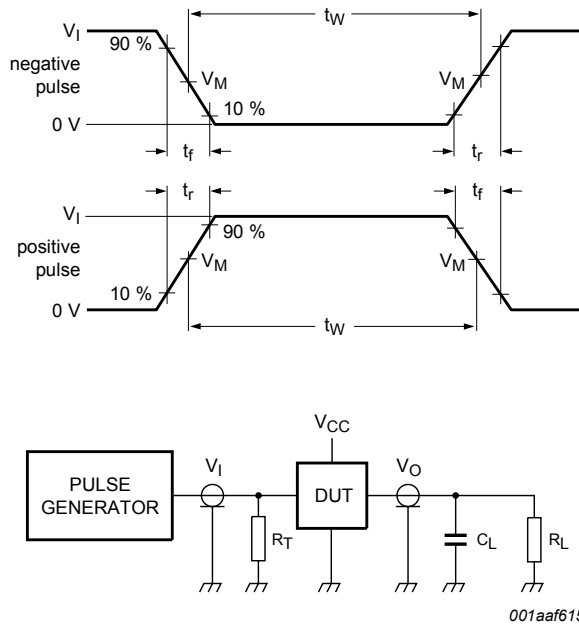


Table 8. Measurement points

Input		Output
V_M	V_I	V_M
1.5 V	2.7 V	1.5 V



Test data is given in [Table 9](#).

Definitions test circuit:

R_T = termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = load capacitance including jig and probe capacitance.

R_L = load resistance.

Figure 7. Test circuit for measuring switching times

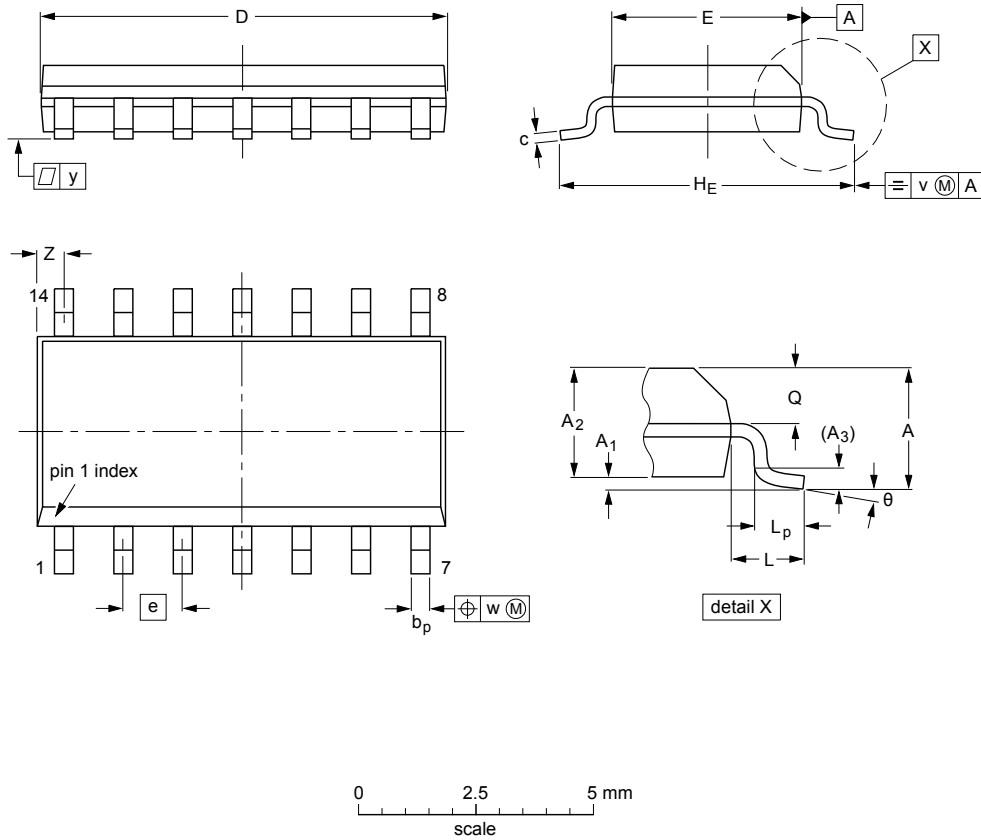
Table 9. Test data

Input				Load		Test
V_I	f_i	t_W	t_r, t_f	C_L	R_L	
2.7 V	≤ 10 MHz	500 ns	≤ 2.5 ns	50 pF	500 Ω	t_{PLH}, t_{PHL}

11 Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	z ⁽¹⁾	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Note

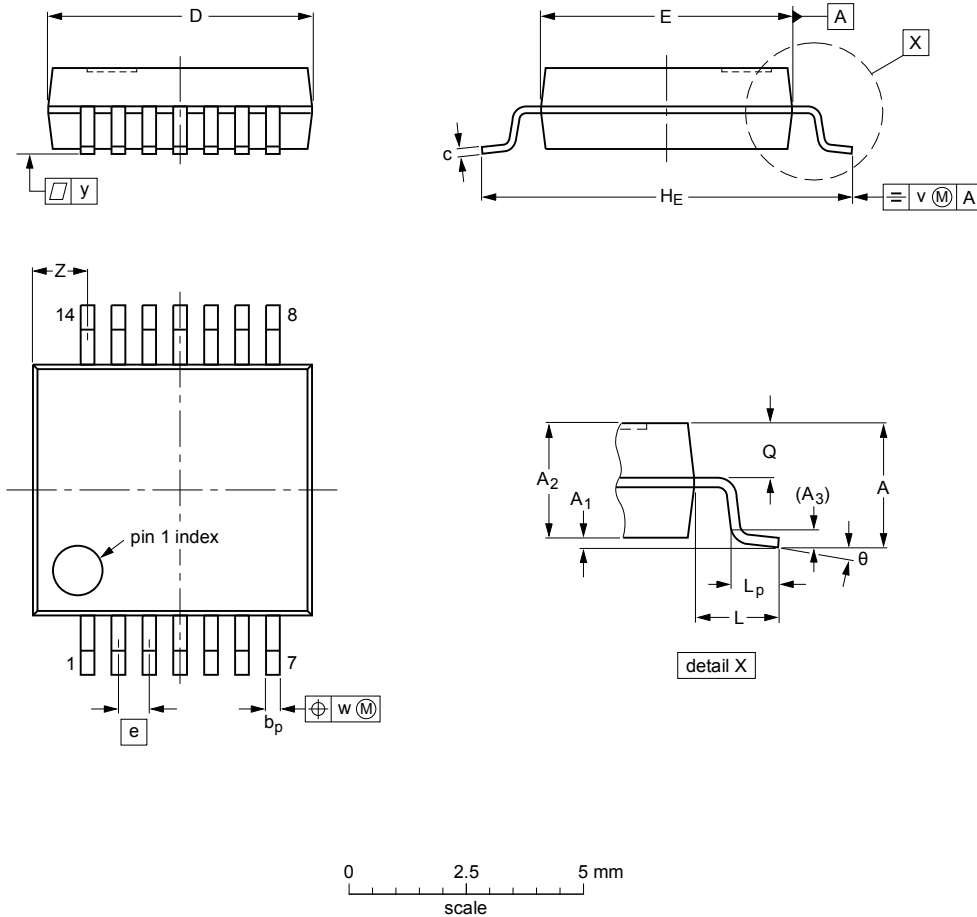
1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT108-1	076E06	MS-012			99-12-27 03-02-19

Figure 8. Package outline SOT108-1 (SO14)

SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm

SOT337-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.4 0.9	8° 0°

Note

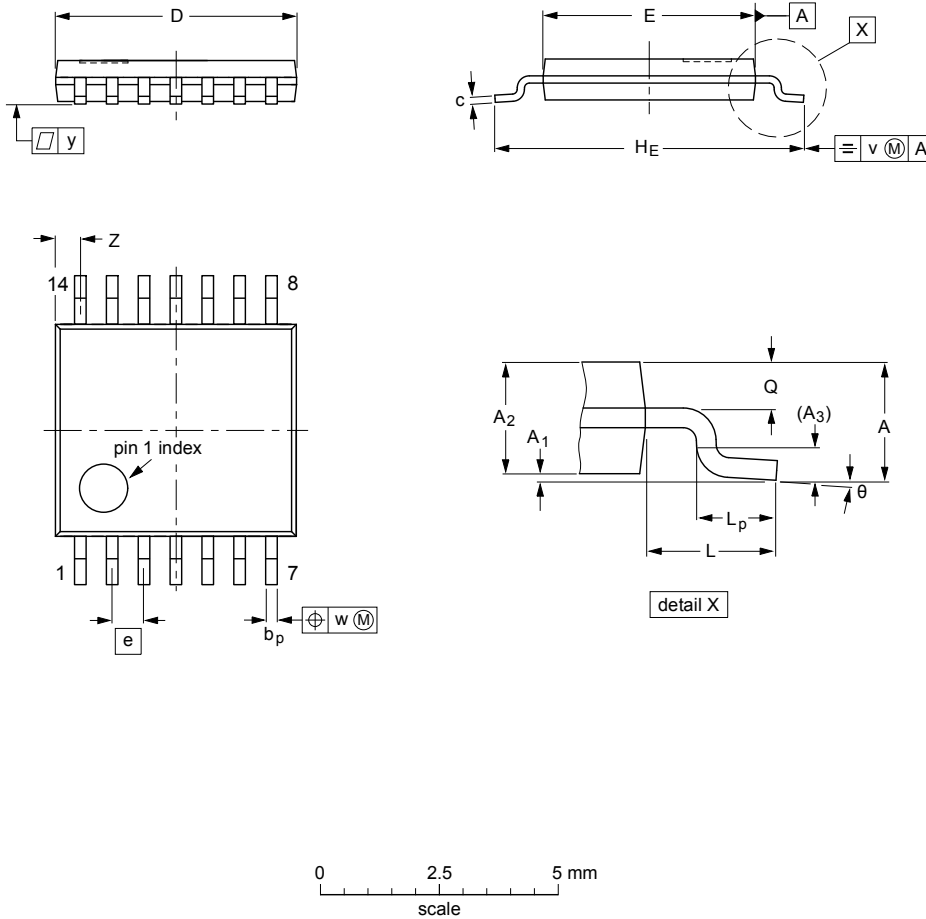
1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT337-1		MO-150				-99-12-27 03-02-19

Figure 9. Package outline SOT337-1 (SSOP14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1



DIMENSIONS (mm are the original dimensions)

UNIT	A _{max.}	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽²⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT402-1		MO-153				-99-12-27 03-02-18

Figure 10. .Package outline SOT402-1 (TSSOP14)

12 Abbreviations

Table 10. Abbreviations

Acronym	Description
BiCMOS	Bipolar Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

13 Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVT08 v.3	20170322	Product data sheet	-	74LVT08 v.2
Modifications:	<ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. 			
74LVT08 v.2	19960529	Product specification	-	74LVT08 v.1

14 Legal information

14.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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