

N-Channel Enhancement Mode Field Effect Transistor

Product Summary

• V_{DS}	60V
• I_D	130A
• I_D (Package limited)	85A
• $R_{DS(ON)}$ (at $V_{GS}=10V$)	<3.0 mohm
• $R_{DS(ON)}$ (at $V_{GS}=4.5V$)	<4.5 mohm
• 100% UIS Tested	
• 100% ∇V_{DS} Tested	

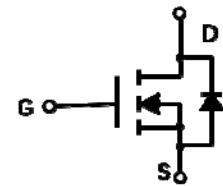
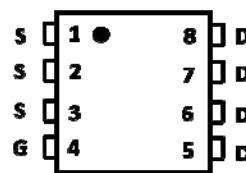
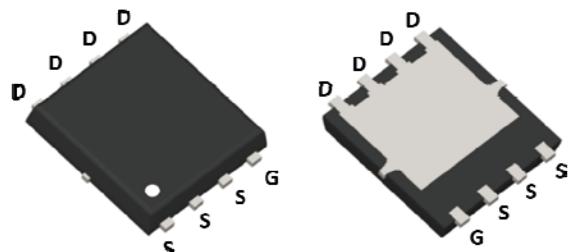
General Description

- Split Gate Trench MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$

Applications

- DC-DC Converters
- Power management functions
- Synchronous-rectification applications

PDFN5060-8L



Absolute Maximum Ratings ($T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-source Voltage	V_{DS}	60	V
Gate-source Voltage	V_{GS}	± 20	V
Drain Current	I_D	130	A
Drain Current ^A	I_D	85	A
$T_C=100^\circ\text{C}$		54	
Pulsed Drain Current ^B	I_{DM}	390	A
Avalanche energy ^C	EAS	270	mJ
Total Power Dissipation ^D	P_D	105	W
Thermal Resistance Junction-to-Case	$R_{\theta JC}$	1.2	$^\circ\text{C} / \text{W}$
Thermal Resistance Junction-to-Ambient ^E	$R_{\theta JA}$	55	
Junction and Storage Temperature Range	T_J, T_{STG}	-55~+150	$^\circ\text{C}$

Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
SKG85G06A	F1	SKG85G06A	5000	10000	50000	13" reel

Electrical Characteristics ($T_J=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{\text{GS}}=0\text{V}, I_{\text{D}}=250\mu\text{A}$	60			V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{\text{DS}}=60\text{V}, V_{\text{GS}}=0\text{V}$			1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{\text{GS}}= \pm 20\text{V}, V_{\text{DS}}=0\text{V}$			± 100	nA
Gate Threshold Voltage	$V_{\text{GS}(\text{th})}$	$V_{\text{DS}}=V_{\text{GS}}, I_{\text{D}}=250\mu\text{A}$	1.0	1.8	2.5	V
Static Drain-Source On-Resistance	$R_{\text{DS}(\text{ON})}$	$V_{\text{GS}}=10\text{V}, I_{\text{D}}=20\text{A}$		2.5	3.0	$\text{m}\Omega$
		$V_{\text{GS}}=4.5\text{V}, I_{\text{D}}=10\text{A}$		3.5	4.5	
Diode Forward Voltage	V_{SD}	$I_{\text{S}}=20\text{A}, V_{\text{GS}}=0\text{V}$			1.2	V
Maximum Body-Diode Continuous Current	I_{S}				85	A
Dynamic Parameters						
Input Capacitance	C_{iss}	$V_{\text{DS}}=30\text{V}, V_{\text{GS}}=0\text{V}, f=1\text{MHz}$		3350		pF
Output Capacitance	C_{oss}			1666		
Reverse Transfer Capacitance	C_{rss}			77.7		
Switching Parameters						
Total Gate Charge	Q_g	$V_{\text{GS}}=10\text{V}, V_{\text{DS}}=30\text{V}, I_{\text{D}}=25\text{A}$		66.1		nC
Gate-Source Charge	Q_{gs}			10.7		
Gate-Drain Charge	Q_{gd}			10.9		
Reverse Recovery Charge	Q_{rr}	$I_{\text{F}}=25\text{A}, \text{di/dt}=100\text{A/us}$		73		ns
Reverse Recovery Time	t_{rr}			68		
Turn-on Delay Time	$t_{\text{d(on)}}$	$V_{\text{GS}}=10\text{V}, V_{\text{DD}}=30\text{V}, I_{\text{D}}=25\text{A}$ $R_{\text{GEN}}=2\Omega$		22.5		ns
Turn-on Rise Time	t_r			6.7		
Turn-off Delay Time	$t_{\text{d(off)}}$			80.3		
Turn-off fall Time	t_f			26.9		

Note:

- The maximum current rating is package limited.
- Repetitive rating; pulse width limited by max. junction temperature.
- $V_{\text{DD}}=50\text{ V}$, $R_{\text{G}}=25\Omega$, $L=0.5\text{ mH}$, starting $T_J=25^\circ\text{C}$.
- P_D is based on max. junction temperature, using junction-case thermal resistance.
- The value of R_{GA} is measured with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with $T_a=25^\circ\text{C}$.

Typical Performance Characteristics

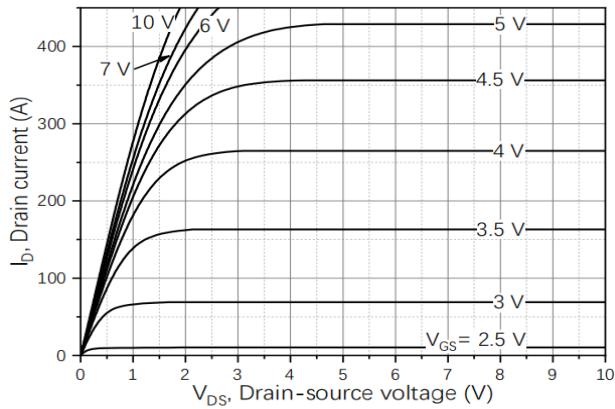


Figure1. Output Characteristics

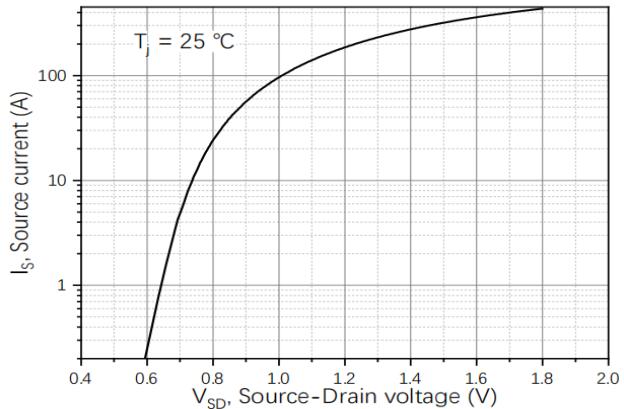


Figure2. Transfer Characteristics

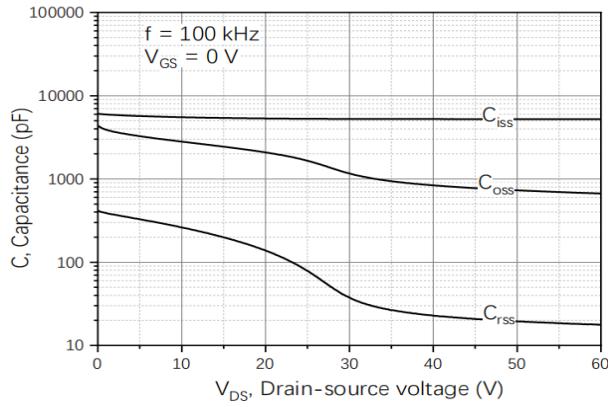


Figure3. Capacitance Characteristics

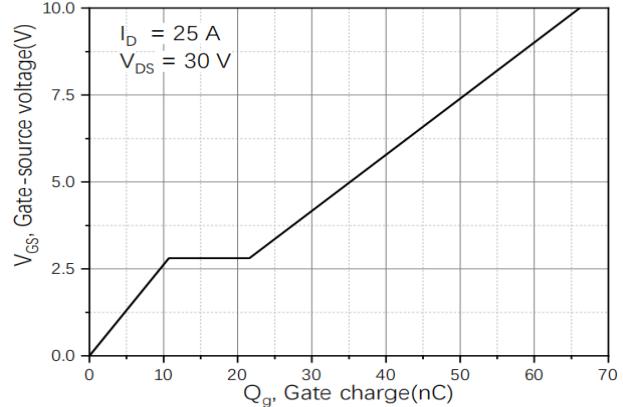


Figure4. Gate Charge

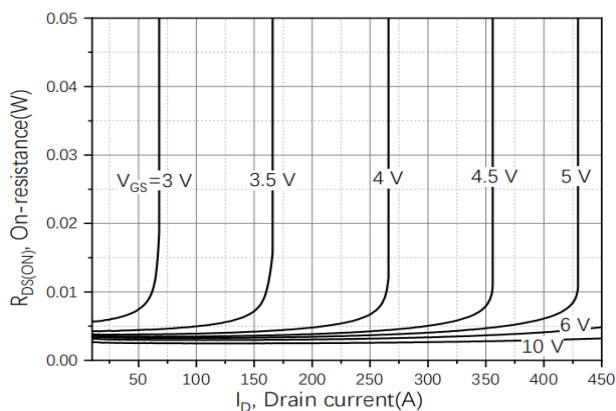


Figure5. Drain-Source on Resistance

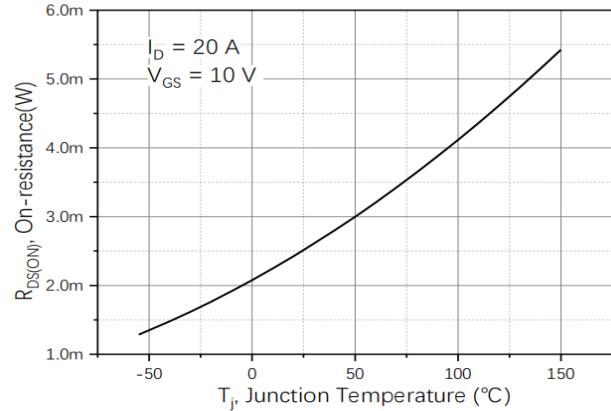


Figure6. Drain-Source on Resistance

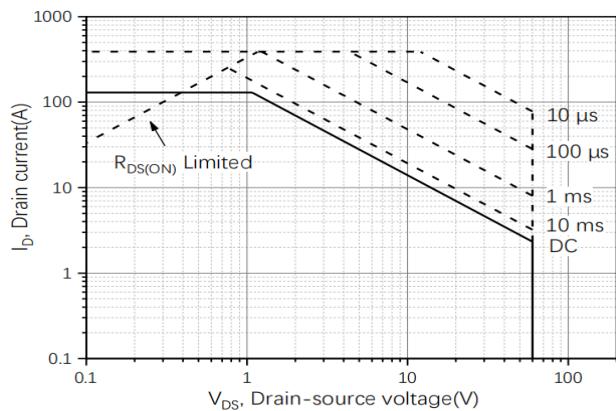


Figure7. Safe Operation Area

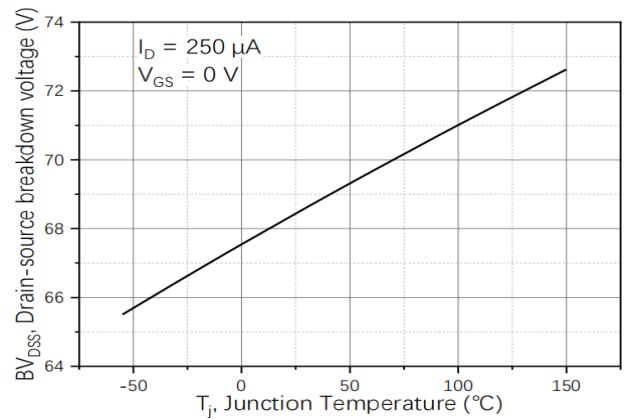
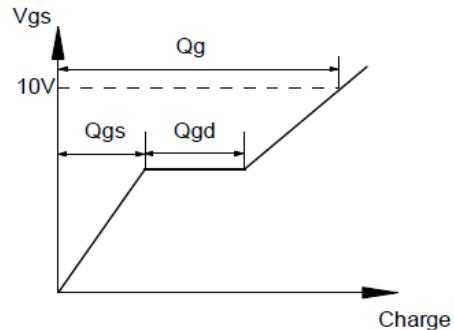
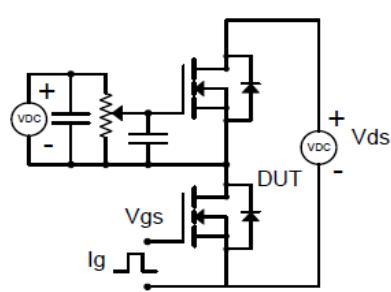
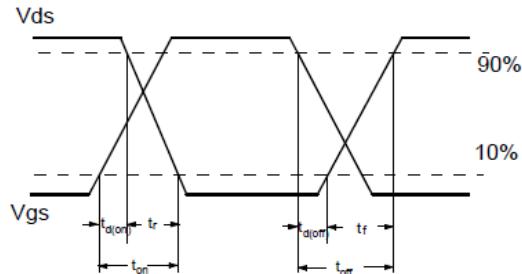
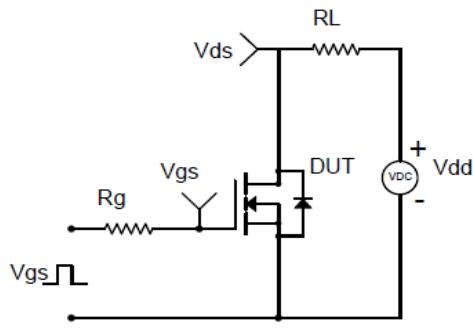
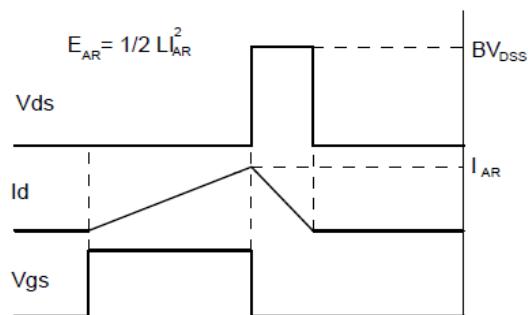
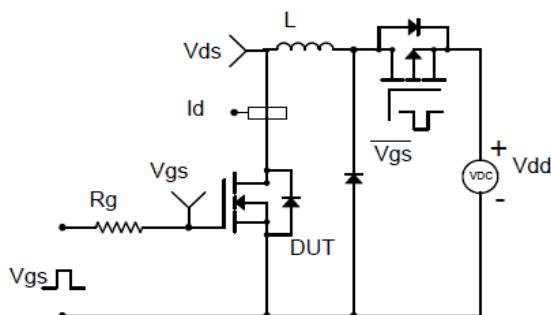
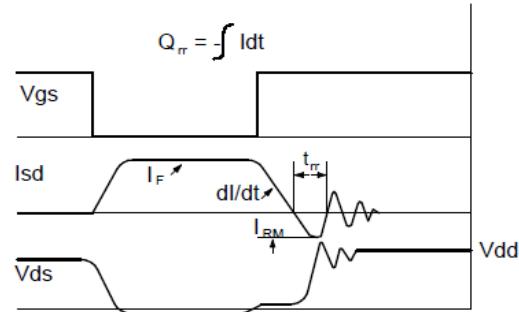
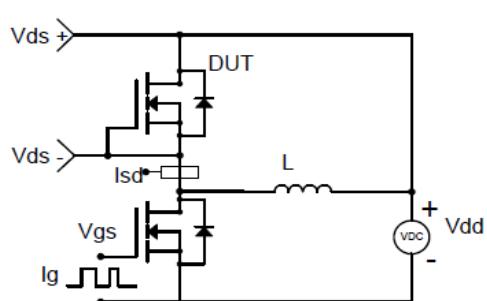


Figure8. Drain-source breakdown voltage

Test circuits and waveforms
Figure A: Gate Charge Test Circuit & Waveforms

Figure B: Resistive Switching Test Circuit & Waveforms

Figure C: Unclamped Inductive Switching (UIS) Test

Figure D: Diode Recovery Test Circuit & Waveforms


PDFN5060-8L Package Information

