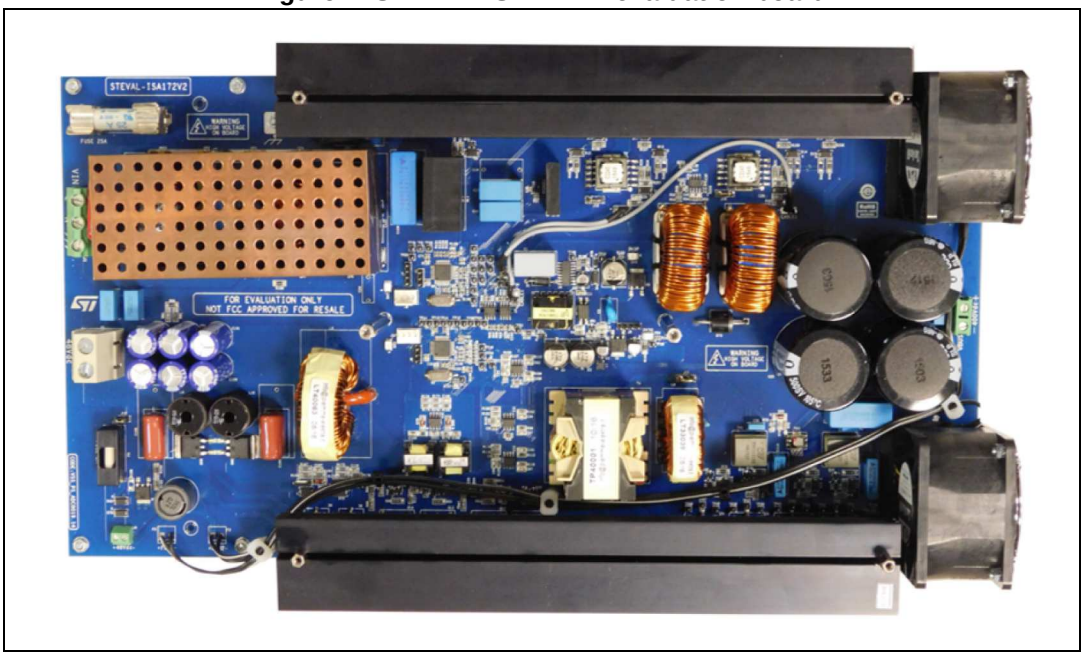
AN4856
Application note

STEVAL-ISA172V2: 2 kW fully digital AC - DC power supply (D-SMPS) evaluation board

Introduction

The STEVAL-ISA172V2 evaluation board is a high power AC-DC converter designed for telecom systems. This type of application requires high efficiency over the entire load range of operation and across the universal mains input voltage range. Given the demand for more efficient, compact solutions, their design is becoming more challenging and new conversion approaches, rather than the standard designs based on analog ICs, have been investigated. In particular, while the standard approach is based on the use of a boost type PFC and a regulation stage, both of which controlled using analog PWM controllers, the new, fully digital approach relies on the use of microcontrollers to control both the PFC and the DC-DC stage. This approach is increasingly being used for high density, high efficiency power electronics systems.

Figure 1. STEVAL-ISA172V2 evaluation board



This application note focuses on the design of a 2 kW AC-DC switch mode power supply with full digital control based on the STM32F334C8 microcontroller. The system consists of two power stages: an input interleaved power factor corrector (PFC), controlled by an STM32F334C8 and a regulation stage implemented with a phase shifted full-bridge with zero-voltage-switching (ZVS) PWM, and synchronous rectification (SR), controlled by a second STM32F334C8 microcontroller. Operating principles, main features and design choices are discussed. Details regarding the main components used for the implementation of both the power and control stages are also provided.

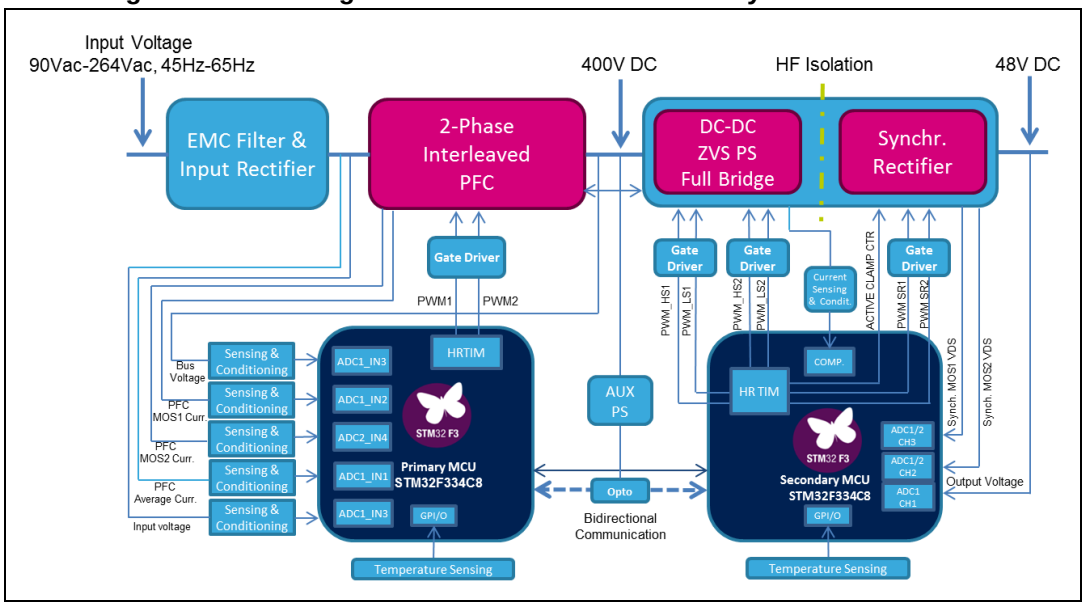
Contents

1 System overview

In *Figure 2* is shown the block diagram of the 2 kW D-SMPS. A two part architecture digitally controlled by two 32-bit STM32F3 microcontrollers has been implemented.

The first one consists of an interleaved PFC while the second one is a DC-DC full bridge phase shifted PWM.

Figure 2. Block diagram of the STEVAL-ISA172V2 system architecture



The main blocks, from left to right, are: the EMC filter and the input rectifier, the 2-phase interleaved PFC and full bridge DC-DC with synchronous rectification.

The double stage EMC filter is connected to input rectifier bridge diodes of the PFC and it is housed in a special shielding case to mitigate electromagnetic interference on the filters.

The front-end stage of this 2 kW AC-DC switched mode power supply (SMPS) consists of an interleaved PFC topology: two parallel boost converters are driven in an interleaved (180° phase shifted) manner in order to split the total current and to reduce the high-frequency ripple of line and DC link capacitor currents. Therefore this topology has the advantage to reduce the volume of input inductor and the size of output filter capacitor increasing the converter power density.

The input stage is typically controlled using an outer voltage loop for bus voltage regulation and an inner control loop to shape the current according to a sinusoidal waveform. The outer loop adjusts the current reference in order to maintain a regulated bus voltage independently from the load or input voltage variations. The output isolation and regulation stage is implemented using a DC-DC zero voltage switching full bridge topology operated with fixed frequency and phase shifted PWM.

The DC-DC stage performs voltage step-down using an HF transformer with a primary-to-secondary turns ratio chosen to maintain good efficiency and regulation in the entire operating range. The transformer is supplied with a voltage whose average value depends on the phase shift of primary side active switches. On the secondary side this voltage waveform is rectified and then smoothed by the output filter. While on the primary side

switching losses are reduced thanks to zero voltage switching (ZVS), on the secondary side synchronous rectification (SR) is used to ensure low conduction losses. The overall effect of these design choices is high system efficiency, in line with the stringent requirements of the power supply industry.

The system is controlled by two STM32F334 microcontrollers: one for the primary side (PFC) and one for the secondary side (DC-DC). Primary microcontroller unit (MCU) controls the first stage by sampling of current of the two MOSFETs, the input AC voltage and the output bus voltage. Two PWM control signals are then generated to drive two power switches with a proper duty cycle given by control loop.

A second STM32F334C8 microcontroller is used to control the DC-DC stage, adjusting the phase shift and ensuring stable operation in the overall load range. Additional PWM signals are used to drive, respectively, the SR and active clamp MOSFETs. Furthermore, two channels of ADCs are used to sample the rising and falling edges of the drain-to-source voltage on the SR MOSFETs.

The two microcontrollers exchange information about the status of the input and output power stage via bidirectional serial communication. Both the power stage and control stage are supplied by an offline flyback circuit based on VIPER27H which provides a suitable regulated voltage to the microcontrollers, the gate drive ICs and signal conditioning circuits.

Table 1 summarizes the main specifications of the 2 kW AC/DC D-SMPS.

Table 1. 2 kW AC/DC D-SMPS converter specifications

Parameter	Value
Input AC voltage	90 V AC up to 264 V AC
Input AC frequency	45 Hz up to 65 Hz
Output voltage	48 V DC
Max output current	42 A
PFC output voltage	400 V DC
Output power	2000 W
PFC switching frequency	60 kHz
DC/DC switching frequency	100 kHz
HF transformer isolation	4 kV
Cooling	Forced air with speed modulation
Input short circuit protection	25 A fuse
Input overload protection	Managed by primary STM32F334C8
Input under/over-voltage	Managed by primary STM32F334C8
Input under/over-frequency	Managed by primary STM32F334C8
Bus DC under/over-voltage	Managed by primary STM32F334C8
Output under/over-voltage	Managed by secondary STM32F334C8
Over-temperature protection	Managed by primary and secondary STM32F334C8
Output over-current protection	Managed by secondary STM32F334C8

The converter accepts universal input voltage and produces a 48 V regulated output. The continuous power rating of the unit is 2 kW.

A cooling fan is activated to provide forced air cooling with air flow modulation depending of the load power. The ambient operating temperature range is from 0 °C to 50 °C.

The intermediate high-voltage DC bus is regulated at 400 V by the PFC which draws sinusoidal input current from the AC input maintaining high power factor and low current total harmonic distortion (THDI%). The DC-DC circuit converts this high DC voltage to low DC voltage providing isolation (4 kV), by means of an HF transformer, and high efficiency thanks to ZVS operation. Protections on input/output current and input/output voltage are also provided together with over-temperature detection.

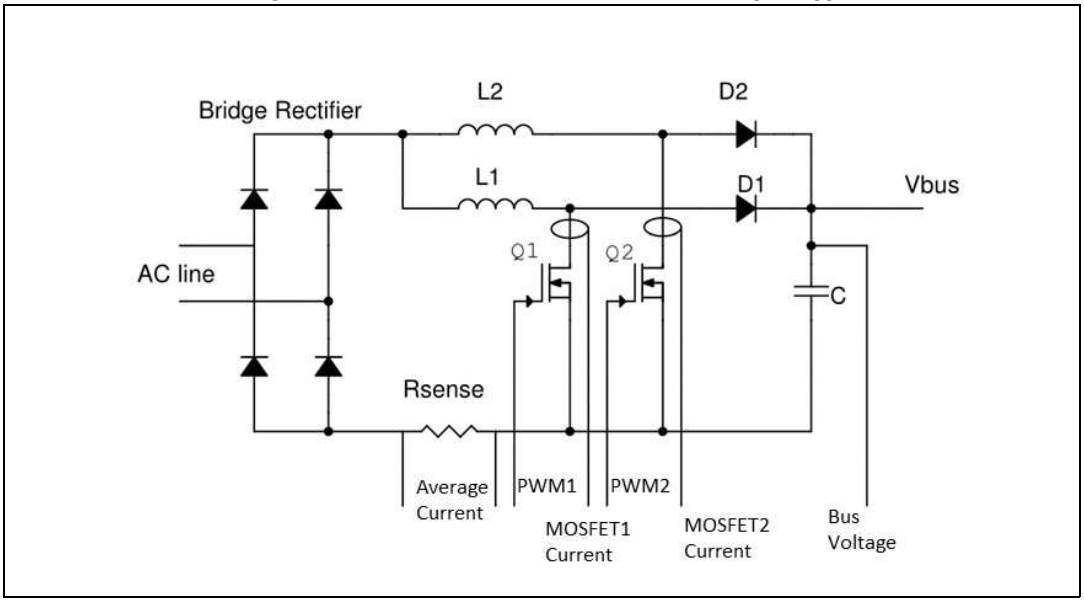
Warning: **Any replacement of switching devices in the evaluation board with other types requires fine tuning of all driving signals. This is true for the PFC as well as for the DC-DC. Do not change any switch device without firmware fine-tuning of the involved signals, as simply replacing devices may cause the board to fail or overheat. Any replacement requires a high level of expertise on the system. For high voltage and high power, always use a Plexiglas protection on the board while avoiding obstruction of the air flow from the fan.**

2 Interleaved PFC

For high power applications such as the 2 kW D-SMPS evaluation board, an interleaved PFC is often used to reduce line current harmonics. The two phase interleaved power factor corrector even allows to reduce the size of input and output capacitors to filter the current ripple as well the inductors, increasing the power density of the converter. This benefit is obtained thanks to the current ripple cancellation using two boost converters in which it is possible to have a larger ripple current for each inductor if compared with a single PFC inductor.

2.1 Interleaved PFC overview

Figure 3. Interleaved PFC main circuit topology



The interleaved PFC circuit includes a line bridge rectifier device and two boost converters as shown in *Figure 3*. This illustration shows also the main measurements sampled and used by the microcontroller in control algorithm for bus voltage and input current regulation.

The complete schematic is shown in *Appendix A: Schematic diagrams*.

The total input current ripple can be considered as the results of a ripple cancellation because Q1 and Q2 in the average PFC control loop are driven with a phase difference of 180°. The cancellation is related to the duty cycle value, and the maximum cancellation for the two phases is obtained when the instantaneous duty is equal to 50% for both devices.

Since the circuit is designed for wide range input lines (90 Vac up to 264 Vac) the maximum line current ripple is obtained in the presence of low line voltage when the highest current is present.

2.2 Interleaved PFC design

The following table reports the main specifications for the PFC converter, while the dimensioning of passive components and power switches are addressed below.

Table 2. PFC design specifications

Parameter	Description	Min.	Typ.	Max.	Unit
V_{IN}	Input voltage	90	120/230	264	V
V_{OUT}	PFC bus voltage	375	400	425	V
F_{IN}	Input voltage frequency	45	50/60	65	Hz
P_{OUT}	Output PFC power			2150	W
F_{SW}	Switching frequency		60000		Hz
$\Delta_{IL\_MAX\%}$	Maximum inductor current ripple		30		%

2.2.1 Boost inductors selection

Starting from specifications reported in *Table 2*, the value of L1 and L2 inductors are calculated as follows.

The minimum instantaneous duty cycle $\delta_{lowline}$ at minimum input voltage peak is:

Equation 1

$$\delta_{lowline} = \frac{V_{out} - V_{in\_lowline}\sqrt{2}}{V_{out}} = \frac{400 - 90\sqrt{2}}{400} = 0.683$$

If we define K(δ) as the ratio between the input current variation and the variation of the current on the single inductor in a two phase interleaved PFC:

Equation 2

$$K(\delta) = \Delta I_{input}/\Delta I_L = (1-2\delta)/(1-\delta) \qquad \text{for } \delta \le 0.5$$

$$K(\delta) = \Delta I_{input}/\Delta I_L = (2\delta-1)/\delta \qquad \text{for } \delta > 0.5$$

We can calculate K at δ=0.683:

K(0.683)=0.53

Assuming as maximum output power of the PFC the nominal output power of the D-SMPS divided by an estimated minimum efficiency of the DC-DC converter (93%), the maximum peak current variation on a single inductor, for a maximum imposed ripple of 30%, is:

Equation 3

$$\Delta I_L = \frac{0.3\ P_{out\_max}\ \sqrt{2}}{V_{in\_lowline}\ \eta\ K} = \frac{0.3 \cdot\ 2150\ \cdot \sqrt{2}}{90 \cdot 0.96 \cdot 0.53} \cong 20A$$

Once the Δ_{IL} is obtained, the minimum inductor value for each boost converter is given by:

Equation 4

$$L1 = L2 > \frac{V_{in\_lowline}\ \delta_{lowline}\sqrt{2}}{\Delta I_L \quad f_{sw}} = \frac{90 \cdot 0.683 \cdot \sqrt{2}}{20 \cdot 60000} = 73\ \mu H$$

A 140 µH Sendust ui60 inductor with 15 A RMS saturation current has been selected. The oversized inductor value has been chosen to ensure the minimum calculated inductance at maximum RMS current according to the diagram in *Figure 4*:

Figure 4. Inductance variation versus RMS current

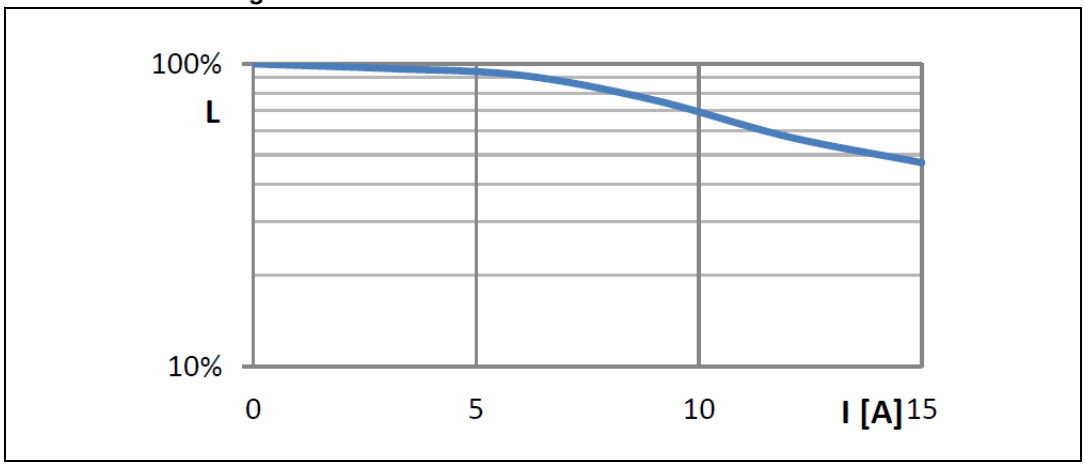
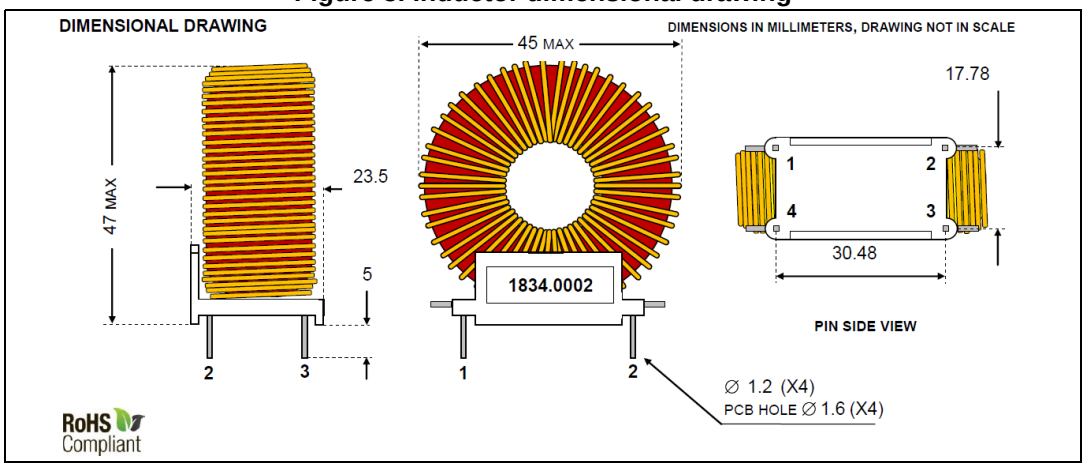


Figure 5. Inductor dimensional drawing



2.2.2 Semiconductor selection

The choice of power semiconductors is fundamental to meet the efficiency requirements of the application. In a boost PFC, when the switch is turned on its current is equal to the inductor current.

The peak inductor current, for the average current mode control, can be calculated using *Equation 5*.

Equation 5

$$I_{Lpeak} = \left(\frac{P_{out}\sqrt{2}}{2\,V_{in\_lowline}\,\eta} + \frac{\Delta I_L}{2}\right)\cdot 1.2 = \left(\frac{2150\sqrt{2}}{2\cdot 90\cdot 0.96} + \frac{20}{2}\right)\cdot 1.2 \cong 33\ A$$

While the RMS value on each switch is given by *Equation 6*

Equation 6

$$I_{DS} = \frac{P_{out}}{2\sqrt{2}\cdot V_{in\_lowline}\cdot\eta}\sqrt{2 - \frac{16\cdot V_{in\_lowline}\sqrt{2}}{3\pi\cdot V_{out}}} = \frac{2150}{2\sqrt{2}\cdot 90\cdot 0.96}\sqrt{2 - \frac{16\cdot 90\cdot\sqrt{2}}{3\pi\cdot 400}} = 10.6\ A_{rms}$$

When the switch is off, the drain-to-source voltage is equal to the output voltage. Therefore, the MOSFET is selected with a rated voltage greater than the output voltage and rated current greater than the maximum inductor current. To minimize conduction losses, it is very important to use a power MOSFET with low drain to-source resistance in order to ensure high efficiency. The output voltage value of the device is chosen according to *Equation 7*:

Equation 7

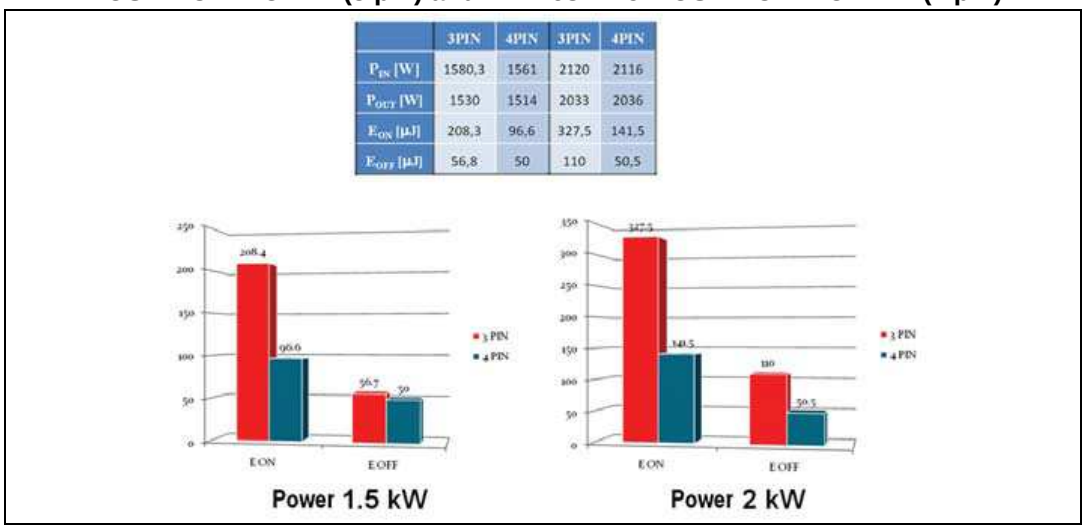
$$V_{DS} \geq 1.3\ V_{OUT} \geq 520\ V$$

To meet the design requirements, two STW48N60M2-4 N-channel power MOSFETs have been selected for Q1 and Q2, respectively. This device is characterized by a minimum breakdown voltage of 650 V and a maximum $R_{DS(on)}$ of 45 mΩ at 25 °C for each switch. The total gate charge is 91 nC @ 52 A and V_{DD} = 480 V.

The equivalent resistor for each couple of switches will be 22.5 mΩ, the parallel of the two switches will decrease the static power loss.

Using a 4-lead technology it is possible to reduce switching losses, especially when the power level and hence the current, are very high. In particular, the reduction of the on-switching loss is always present and increases with the power level, while the drop in the off-switching loss becomes more evident when the power level increases, as shown in *Figure 6*.

Figure 6. Switching energy comparison @ 1.5 kW and 2 kW, for MDmesh M5 MOSFETs in TO-247 (3 pin) and MDmesh M5 MOSFETs in TO247-4 (4 pin)



For further details, refer to application note AN4407.

The average current on diodes D1 and D2 can be calculated as:

Equation 8

$$I_d = \frac{P_{out}}{2 \cdot V_{out}} = \frac{2150}{800} = 2.68\ A$$

Two STPSC1006D 600 V, 18 A RMS, Qc = 12 nC, HV power Schottky SiC diodes are used as boost diodes. The forward voltage drop is V_F < 1 V @ I_F = 2.5 A and T = 175 °C.

2.2.3 Output capacitor

The output capacitor bank value is selected to limit the output voltage ripple to 1.5% of the nominal output voltage. The DC-link voltage can be written as in *Equation 9*.

Equation 9

$$v_0 = V_0 \pm \Delta v_0$$

Where the ripple $\Delta\upsilon_0$ depends on the output capacitor C_{out}, on the output power P_{out} and on the angular mains frequency ω, as specified in the following formula:

Equation 10

$$\Delta v_0 = \frac{P_{out}}{2 \cdot \omega \cdot C_{out} \cdot V_0}$$

Consequently the output capacitor value is:

Equation 11

$$C_{out} = \frac{P_{out}}{2\omega \cdot \Delta v_0 \cdot V_0} = \frac{2150}{2 \cdot 314 \cdot 6 \cdot 400} \geq 1426\mu F$$

Where the angular frequency ω= 2πf = 2*3.14*50 was calculated considering a mains electrical frequency of 50 Hz. Four 450 V, 470 µF electrolytic capacitors have been connected in parallel on the PFC output. In addition, a 470 nF and 10 nF ceramic capacitor with low ESR and ESL are connected in parallel to the DC-bus.

2.2.4 Input filter capacitor

The need for a high power factor introduces a limit on the maximum capacitance that can be placed across the line. The maximum capacitance is a function of the maximum phase shift that can be tolerated. This phase shift angle can be calculated using *Equation 12*:

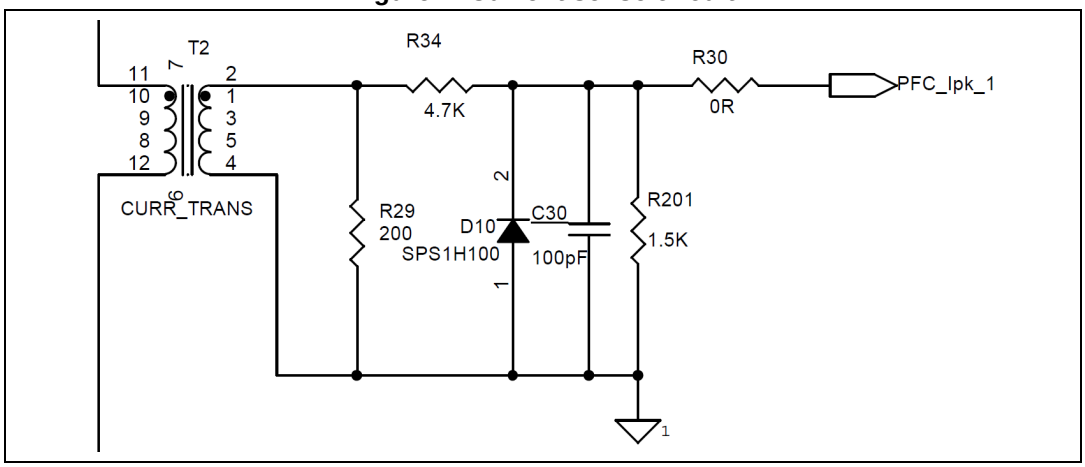
Equation 12

$$\theta = tan^{-1}\left(\frac{\omega \cdot V_{in\_max} \cdot C_{in}}{I_{in}}\right)$$

Choosing a total of C_{in} = 1.7 µF the total displacement is less than 1°, in any case the PFC controller is able to compensate it.

2.2.5 Current sense transformer

Figure 7. Current sense circuit



The PFC is provided by three current sensing circuits: a shunt resistor and two current transformers (CTs). The current flowing across each power switch is sensed by means of CTs. These are placed between each boost inductor and the respective MOSFET. Due to this placement, only the rising part of the inductor current is available to the control algorithm. The current signal is always sampled at the mid-point of the gate control PWM signal to detect the average inductor value, as described in control algorithm section.

The CT must withstand the peak current calculated in *Equation 5*. The selected current sense transformer is the B82801C2245A200 from EPCOS which is characterized by a turns

ratio of 200. The relation between the current of each MOSFET and the respective sensed voltage acquired by microcontroller is given by the *Equation 13*:

Equation 13

$$V_{sense,max} = \frac{R29 \cdot I_{DSmax}}{n_{ratio}} \cdot \frac{R201}{R201 + R34} = \frac{200 \cdot 10.6 \cdot \sqrt{2}}{200} \cdot \frac{1.5}{1.5 + 4.7} = 3.61V$$

If the average control loop is sampled at the mid-point of the gate control PWM corresponding at the mid-point of the sensed current, then $V_{sense,max}/2$ = 1.80 V has to be considered as input on the microcontroller's ADC.

2.3 PFC control algorithm

This section describes the digital interleaved PFC control method designed to work in continuous conduction mode (CCM), that is when the inductor current remains above zero for the full duration of the switching period. The control algorithm continues to work properly even if, due to light load or when the mains voltage is near the zero crossing point, the PFC converter operates in discontinuous conduction mode (DCM), when the inductor current reaches zero before the end of switching period, thanks to the introduction of duty cycle feed-forward control technique. This control method allows a good sinusoidal shape of input current with a low total harmonic distortion (THD) and a power factor (PF) close to one in the entire operating range.

The control algorithm is implemented for the 32-bit STM32F334C8 microcontroller from the STM32 family, which is provided with 2 independent high-speed 12-bit ADCs, 3 ultra-fast comparators and a high resolution timer (HRTIM).

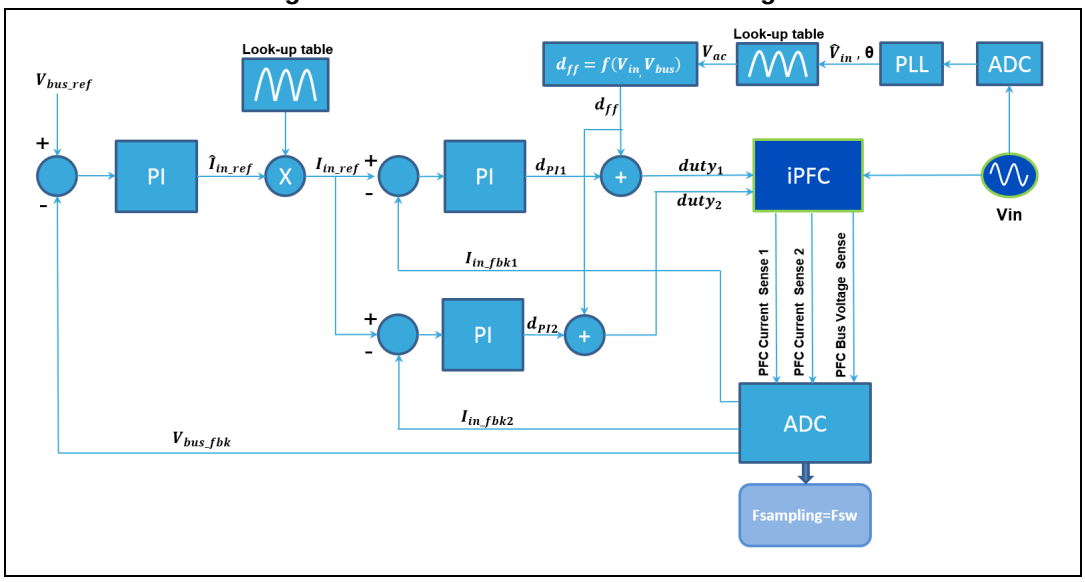
As in the traditional average current control method, there are two different control loops: an outer voltage loop, performed at twice of mains frequency, provides the regulation of bus voltage at the reference value (400 V), setting the proper current reference, and an inner current loop, performed up to 60 kHz that minimizes the error between the average inductor current and its sinusoidal reference in phase with the mains voltage.

To obtain the measurement of average inductor current for each leg of the iPFC converter, two current transformers (CT), placed above each switch, are used. The measurement of interest in CCM is acquired sampling the switch current in the middle point of the PWM on time, while in DCM it can be estimated with a proper correction factor.

With two different current feedback measurements, it is possible to perform an independent current loop for each leg of the converter. Instead of the two CT, is also possible to configure the firmware to use the total current that flows through a shunt resistor, thus performing a unique current loop and driving the switches of the two legs with the same duty cycle.

A block diagram of the control scheme is shown in *Figure 8*.

Figure 8. PFC control scheme block diagram



A phase-locked loop (PLL) in the d-q reference frame was implemented to compute input voltage frequency, amplitude and to assure the synchronization with the input current. The mains voltage, together with the reconstructed 90 degree phase shifted waveform, is transformed to d-q synchronous rotating reference frame using Park transformations with estimated phase angle θ from the PLL output. A PI controller is used to minimize the V_d component, while the mains electrical angle is obtained after a numeric integration and is expressed in 16-bit integer format. The complete control scheme of the PLL is shown in *Figure 9*, while in *Figure 10* the PLL output compared to input voltage is shown.

Figure 9. PLL block diagram

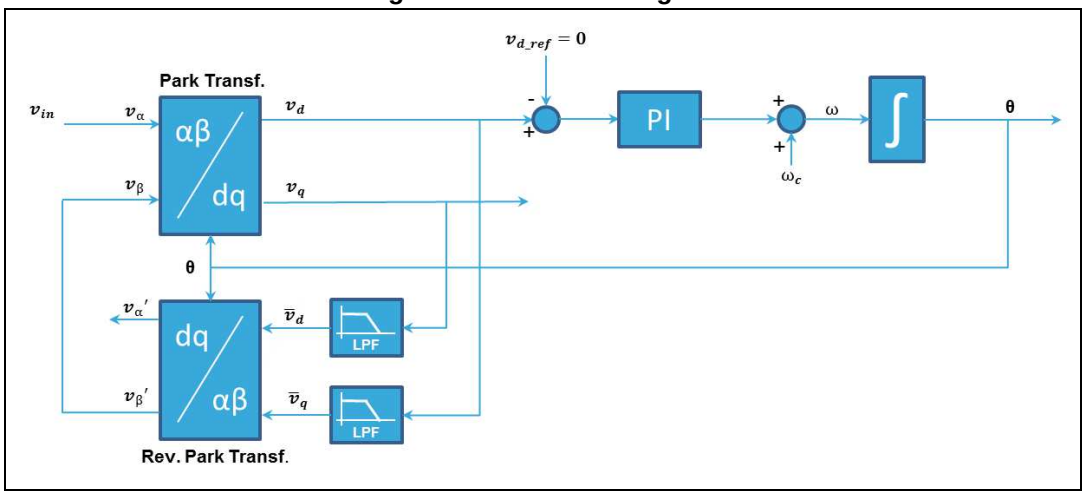
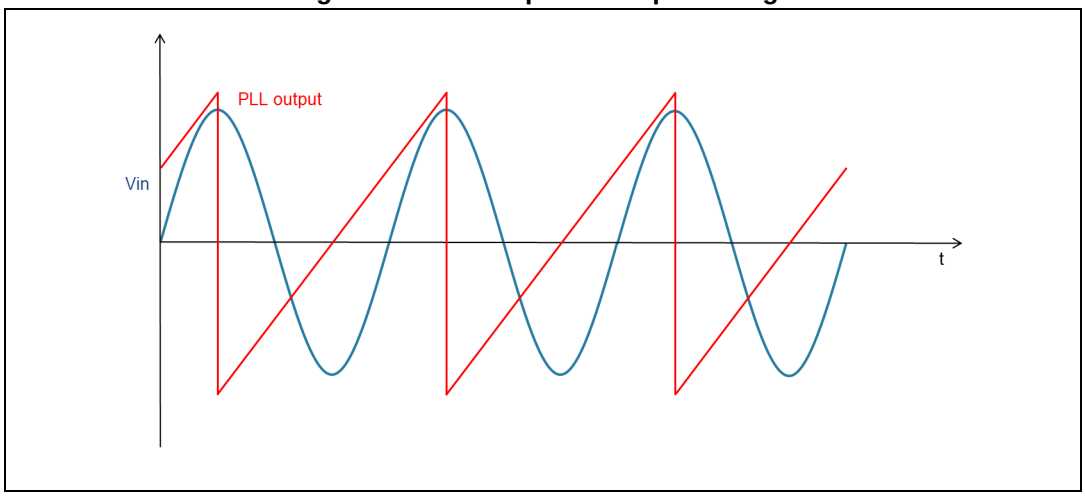


Figure 10. PLL output and input voltage



In the control scheme a linear proportional-integral regulator (PI) is used for voltage control loop. It provides the amplitude of current reference needed to reach the desired DC voltage on bus capacitors. Maximum input current reference is set at 20 Arms, but it can be smaller depending on input voltage and maximum input power set in the firmware (upper limit of the PI voltage regulator is changed according to the input voltage).

The rectified sinusoidal current reference is obtained thanks to a look-up table in which are stored the sinusoidal values in a [0°, 90°] range with 1.15 fixed-point format (1 bit for the integer part and 15 bits for the decimal part). In this manner the current reference does not depend on the input voltage distortion.

Through the implementation of PLL, it is also possible to shift the current reference to compensate sampling delays and achieve a unity power factor.

The inner current loop is based on a PI regulator plus a feed-forward controller. The feed-forward control technique is used to achieve a lower THD and to improve the transient response reducing the output voltage overshoot caused by input voltage changes.

Therefore the total duty cycle applied at the MOSFETs of each leg of the iPFC converter is composed of two terms: a closed loop term, the output of a standard PI regulator, and an open loop, feed-forward term, common for both legs, which depends on the instantaneous input and output voltage values. The input voltage value of the feed-forward term is obtained by means of the same look-up table used to calculate input current reference.

The following describes how the feed-forward duty cycle has been calculated.

For a generic input sinusoid, the expression of the duty cycle for the boost converter in CCM is:

Equation 14

$$d_{CCM}(t) = 1 - \frac{V_{in}|sin\ \omega t|}{V_o}$$

where V_o is the output bus voltage and V_{in} sin ωt is the mains voltage. However, the previous formula, which depends only on open loop parameters of the boost converter, is no longer valid when the converter operates in DCM, in which its behavior changes

significantly, and cannot assure the bus voltage regulation against load changes. The correct expression of the duty cycle when the average inductor current follows its reference is:

Equation 15

$$d_{DCM}(t) = \sqrt{\frac{2L}{T_s} \cdot G_e \cdot \left(1 - \frac{V_{in}|sin\,\omega t|}{V_o}\right)}$$

with $G_e=I_{in\_ref}/V_{in}$ the desired input conductance of the converter, L the value of boost inductance and Ts the switching period. This formula is quite complex, depends on converter's parameters and implies errors due to the inductor tolerance. For this reason only a fraction of the previous open loop duty cycle is applied, while the remaining part is given by the output of the PI controller, with a greater contribution of feed-forward terms for light loads compared to PI output and vice-versa for high loads.

The feed-forward duty cycle term has been calculated using the following expression:

Equation 16

$$d_{ff}(t) = k_{ff} \cdot \left(1 - m \cdot \frac{V_{in}|sin\,\omega t|}{V_o}\right)$$

Where k_{ff} is a gain depending on the load and the input voltage and m is a correction factor to improve THD.

The gain k_{ff} increases with load and decreases with input voltage. Since the output of the PI voltage regulator, which represents the input current reference, depends on the load, the expression chosen for feed-forward duty cycle gain is the following:

Equation 17

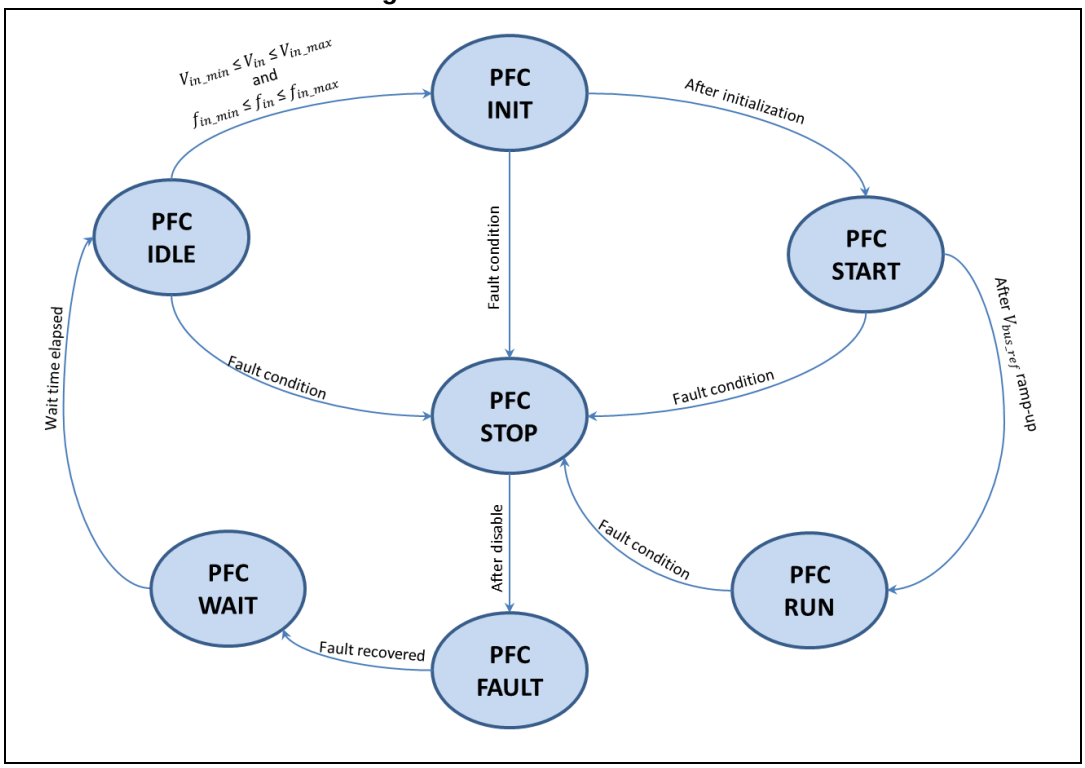
$$k_{ff} = k_g \cdot \frac{I_{in\_ref}}{V_{in}}$$

where V_{in} is the amplitude of the mains voltage, I_{inref} is the amplitude of the current reference and k_g is another gain that varies with input voltage.

2.4 PFC firmware overview

The PFC control firmware allows the regulation of bus voltage and input current. To achieve this aim and design the control logic, a state machine made up of seven states was implemented. The scheme in *Figure 11* shows graphically the architecture of the state machine and the execution of the main tasks.

Figure 11. PFC state machine



At power-on of the system, the HAL (Hardware Abstraction Layer) library is initialized and all the peripherals used, such as Systick, ADC, UART and HRTIM, are configured while the current state is set in PFC_IDLE state. Here the system waits until the input voltage is in the correct range of amplitude and frequency, information given by PLL when it is in steady state. If the previous conditions are satisfied and no faults are detected, after a certain time the NTC used to limit the inrush current is short-circuited by a relay and the new state is PFC_INIT. In this pass-through state, the integral terms of PI regulators are reset, the control variables are reinitialized, the PM8834 gate driver is enabled and PWM outputs are driven at minimum duty cycle. After this, the new state is PFC_START, where the bus voltage reference value is linearly increased from initial value (set at the last sensed measurement in the previous state) up to the reference value of 400 V in a fixed ramp-up time of 3 seconds. When this procedure is completed, a dedicated flag is set and sent, together with PFC status, via serial communication to the secondary microcontroller, so the DC-DC converter can start to regulate the output voltage, while the new value of PFC state variable is PFC_RUN. If in any of the above states a fault condition is verified, the system is forced into PFC_STOP state, where all PWMs are disabled (also for DC-DC that receives a proper serial message), and then it remains in PFC_FAULT state.

The possible faults are:

- Input voltage under/over frequency (f < 45 Hz; f > 65 Hz)
- Input under/over voltage (V_{in} < 90 V AC; V_{in} > 264 V AC)
- Bus DC undervoltage (290 V, only in PFC_RUN state)
- Bus overvoltage (V_{bus} > 450 V)
- Overtemperature (heatsink temperature > 50 °C)

For input voltage frequency and amplitude checks, two buffers of five elements are used to validate the respective last measurements: even if only a buffer value is out of range (with

proper hysteresis), the corresponding fault is set and a user LED blinks a number of times, depending on the type of error that has occurred. This state is maintained until the output is re-enabled by software. When all faults have passed, the system is in PFC_WAIT state for 2 seconds before entering again into a PFC_IDLE state and restarting the entire procedure. In *Table 3* all fault error codes and the respective number of LED blinks are reported.

Table 3. PFC error codes and number of blinks

Fault	Error code	Number of LED blinks
PFC_NO_ERROR	0x0000	-
PFC_BUS_OVER_VOLT	0x0002	2
PFC_BUS_UNDER_VOLT	0x0004	3
PFC_MAIN_OVER_VOLT	0x0008	4
PFC_MAIN_UNDER_VOLT	0x0010	5
PFC_MAIN_OVER_FREQ	0x0020	6
PFC_MAIN_UNDER_FREQ	0x0040	7
PFC_OVER_TEMP	0x0080	8

When the PFC converter operates at light load, or when the load is abruptly disconnected, the bus voltage can increase from its reference value. When it is greater than 430 V, but lower than 450 V (overvoltage threshold), the PFC enters in burst mode: the HRTIM burst mode feature is enabled by software: this means that the PWM outputs are disabled (number of IDLE periods equal to burst repetition rate) until, when the bus voltage is below 400 V, the burst mode is disabled.

As described above, the control firmware performs several tasks, with different timings and priorities to ensure both output voltage regulation and input current regulation. The main tasks and functions are summarized in *Table 4* together with the time scheduling and priority level.

Table 4. Function names and tasks of the PFC firmware

Function	Task	Execution frequency	Priority
HRTIM1_TIMA_IRQHandler()	Current control loop PLL	60 kHz 10 kHz	High
TIM7_DAC2_IRQHandler()	Voltage control loop Update control parameters	2*fmains (90-130 Hz)	Medium
TIM6_DAC1_IRQHandler()	Computing of V_{AC} frequency Computing of V_{AC} amplitude	5 kHz	Medium
TIM15_IRQHandler	Update DAC channels (for debugging only)	4 kHz	Medium
main()	Fault checks State machine Serial communication LED blinking	-	Low

After the initialization of the peripherals and all I/O ports used, the state machine is performed in the main loop. In this loop the fault check function is also performed to ensure that no fault conditions are present. As mentioned above, the last 5 calculated values of voltage frequency and amplitude are checked, together with the bus voltage filtered measurement, in order to verify that the mains parameters are within the converter specified operating window. In this case the state machine can change from one state to another with a timing established by specific counters, the decrease of which is managed by SysTick interrupt every 1 ms. Each 500 ms, a serial communication task is also performed: a message of two bytes is sent to the secondary microcontroller to communicate the PFC status together with a message ID. The PFC status is obtained from error codes in *Table 3* or-ed with a startup complete flag as least significant bit. These tasks have a lower priority level compared to those executed in specific interrupts.

The update event of timer 6 (TIM6) schedules the computation of input voltage amplitude and frequency. The first is calculated digitally filtering the peak values (positive and negative) of input sinusoid detected thanks to PLL, but it can also be calculated as module of input Park components. While, for the second measurement, the electrical angle given by PLL is used to detect the beginning of the positive half-cycle of the mains voltage. For this purpose, a counter is increased every 200 µs until the current sinusoid period ends and then reset. The mains frequency in 0.1 Hz is computed as a ratio between 10 times the frequency of TIM6 (10*5 kHz) and the last value of the counter, obtaining a resolution around 0.5 Hz when the input voltage is at 50 Hz. The calculated value is finally stored in the corresponding buffer. Moreover, the offset value of mains ADC measurement is dynamically adjusted with the average value of acquired measurements inside a single period; this because it can vary slightly changing the input voltage.

The voltage control loop is performed at the update event of timer 7 (TIM7) the frequency of which can be dynamically set at twice of mains frequency (information given by PLL), or set at a constant value. Finally, timer 15 (TIM15) is used to schedule the update of the DAC registers only if the user wants to monitor some normalized variables like current reference, duty cycle, mains electrical angle, etc.

The STM32F334x high resolution timer HRTIM is used to generate the PWM signals to drive MOSFETs of both legs of the converter. The HRTIM is specifically designed to drive power conversion systems. Its modular architecture can generate up to ten digital signals with either independent or coupled waveforms with highly accurate timings (up to 217 ps resolution) and allows control of most conversion topologies.

The HRTIM also has timing measurement capabilities and links to built-in ADC and DAC converters. It features light load management mode and is able to handle various fault schemes for safe shutdown purposes. The HRTIM can be partitioned into several sub modules:

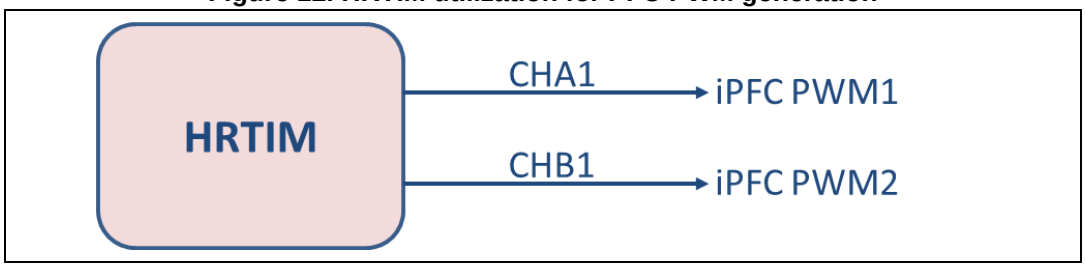
- The master timer
- The timing units (timer A to timer E)
- The output stage
- The burst mode controller
- External event and fault signal conditioning logic
- The system interface

The HRTIM is configured as follows to drive iPFC PWM signals:

- The master timer is used to trigger ADC1 and ADC2 and for synchronization of Timer A and B
- Timer A is used to drive the first leg of the converter
- Timer B is used to drive the second leg of the converter

Timer A output (CHA1) and Timer B output (CHB1) have the same frequency of 60 kHz with 434 ps resolution (maximum possible resolution for a switching frequency lower than 70.3 kHz). However, the two PWM outputs have a different duty cycle, coming from the corresponding current loop (if current transformers are used for current sensing), and are phase-shifted by 180°. The HRTIM utilization for PWM generation is shown in *Figure 12*.

Figure 12. HRTIM utilization for PFC PWM generation



The master timer update event (UE) and master CMP1 register (set at half of the PWM period) triggers two injected acquisition sequences, respectively, for ADC1 and ADC2. The first acquired channels of each sequence are those corresponding to the sensing of two CT currents. In this manner, as mentioned above, it is possible to obtain the average current of each inductor in CCM. The other acquired measurements are the input voltage, the bus voltage, the shunt resistor current and the heatsink temperature. The utilization of the two A/D converters is shown in *Figure 13*, while the HRTIM timing configuration is shown in *Figure 14*.

Figure 13. PFC ADC utilization and acquisition sequence

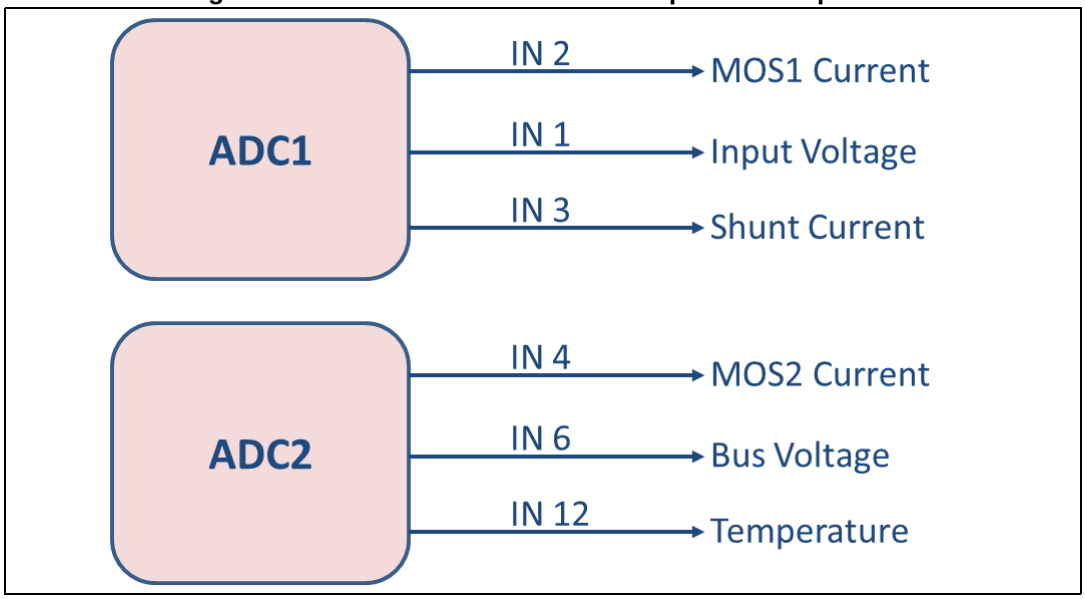
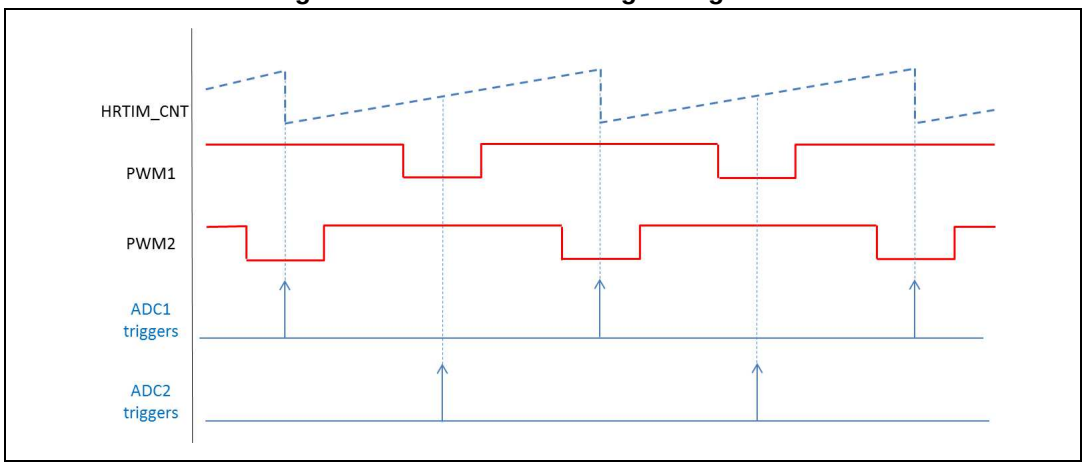


Figure 14. PFC HRTIM timing configuration



2.5 PFC experimental characterization

This section includes the validation results of the interleaved PFC section. It includes the efficiency and power quality test results at different input voltage values and the main waveforms of the PFC.

The power supply efficiency is measured at different mains voltages, namely 120 V AC and 230 V AC with load steps of around 250 W.

The efficiency was measured in the following conditions:

1. The board was supplied with an APS-3000 Adaptive Power System power supply.
2. The PFC output was connected to H&H 800 V/90 A ZS Electronic Load set in continuous current.
3. The input and output voltages were measured directly at the input and output connectors of the PFC section.
4. Input measurements were taken using the Yokogawa WT1010 digital power meter.
5. The power measurements do not take into account the power consumption of the fans.
6. The auxiliary power supply consumption is not included in these measurements (5.1 W for PFC drivers and both microcontrollers), and will be taken into account for DC-DC and overall efficiency measurements.
7. The board was tested at an ambient temperature of 25 °C.
8. For PFC, DPS 2 kW - Primary PFC STM32F334x v2.2 firmware was used.

The testing results are summarized in *Table 5* and *Table 6*.

Table 5. Test results for 120 V AC input operation

V_{IN} (V_{rms})	I_{IN} (A_{rms}	P_{IN} (W)	V_{OUT} (V)	I_{OUT} (A)	P_{OUT} (W)	Efficiency (%)	PF	THD (%)
120.6	2	249	401	0.56	224.56	90.2	0.998	4
120.2	4.15	494	402	1.14	458.28	92.8	0.998	4.29
119.8	6,25	739	402	1.74	699.48	94.7	0.999	4.27
119.2	8.43	1017	402	2.38	956.76	94.1	0.999	3.39

Table 5. Test results for 120 V AC input operation (continued)

V_{IN} (V_{rms})	I_{IN} (A_{rms}	P_{IN} (W)	V_{OUT} (V)	I_{OUT} (A)	P_{OUT} (W)	Efficiency (%)	PF	THD (%)
118.8	10.6	1252	399	2.95	1177.05	94.0	0.999	5
118.3	13	1525	399	3.6	1436.40	94.2	0.999	5
118	14,6	1709	398	4.04	1607.92	94.1	0.999	4.89
117.5	16.77	1949	398	4.59	1826.82	93.7	0.999	4.66

Table 6. Test results for 230 V AC input operation

V_{IN} (V_{rms})	I_{IN} (A_{rms}	P_{IN} (W)	V_{OUT} (V)	I_{OUT} (A)	P_{OUT} (W)	Efficiency (%)	PF	THD (%)
232	1.15	255	405	0.59	238.95	93.7	0.989	6
232	2.22	506	402	1.19	478.38	94.5	0.997	4.54
232	3.4	774	400	1.86	744.00	96.1	0.999	7.32
232	4.4	1002	399	2.42	965.58	96.4	0.999	4.46
231	5.5	1261	399	3.06	1220.94	96.8	0.999	4.11
231	6.6	1502	398	3.65	1452.70	96.7	0.999	7.99
231	7.6	1721	398	4.18	1663.64	96.7	0.999	9.87
230	8.72	1978	399	4.8	1915.20	96.8	0.995	9.45

Figure 15. Input current and voltage at 120 V AC 60 Hz with 50% of load applied

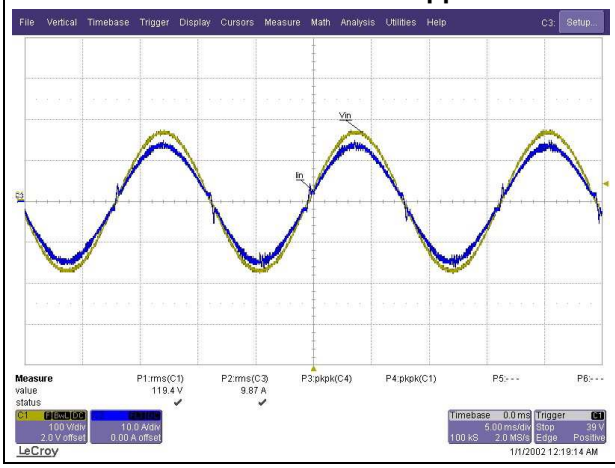
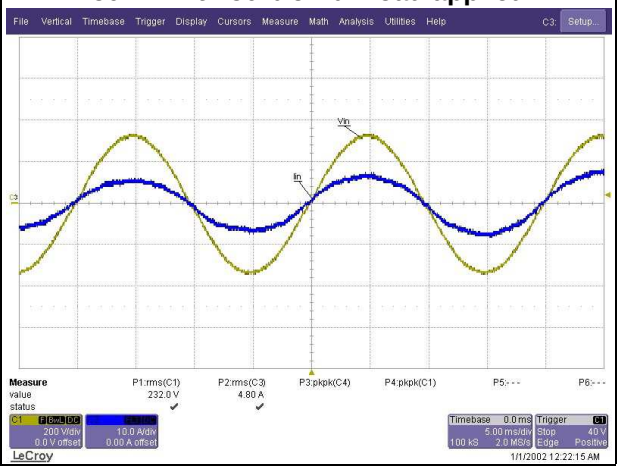


Figure 16. Input current and voltage at 230 V AC 50 Hz with 50% of full load applied



The mains input current together with the input voltage is shown in *Figure 15* and *Figure 16*, respectively at 120 V and 230 V.

The PFC efficiency over the whole operating range is highlighted in *Figure 17* and reaches a maximum value greater than 96%. The power factor for 120 V and 230 V AC input is depicted in *Figure 18* for an output load varying up to 2000 W. In this operating range the power factor is always higher than 0.9.

Figure 17. PFC efficiency

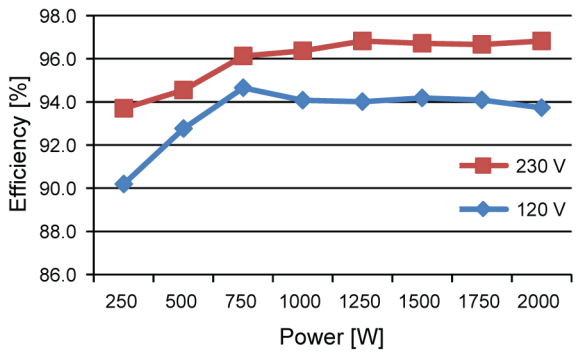


Figure 18. Power factor

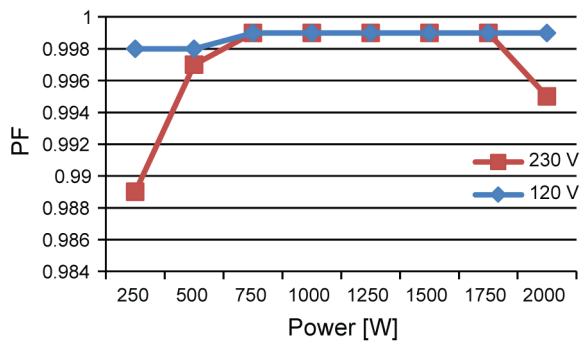


Figure 19. iPFC currents and voltages of boost inductors

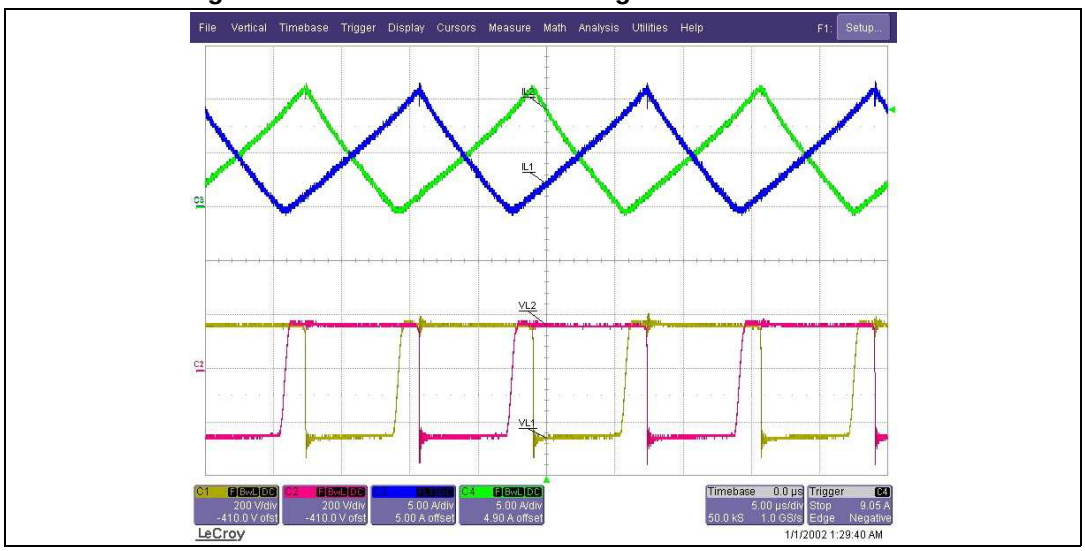


Figure 19 shows the currents of two boost inductors (green and blue traces) with the respective voltage drops (yellow and magenta traces). It can be seen that the input current ripple is minimized thanks to iPFC topology.

3 DC-DC full bridge phase shift converter

3.1 Full bridge phase shift ZVS DC-DC converter overview

The second stage of the 2 kW digital power supply evaluation board consists of a full bridge step-down converter, driven with phase shift modulation, in combination with a push-pull output stage. The purpose of the DC-DC stage is to step down the PFC output voltage from 400 V to 48 V and provide galvanic insulation using an HF transformer. This kind of modulation is used to achieve ZVS (zero voltage switching) and minimize turn-on switching losses, as opposed to classic PWM modulation in which hard switching and considerable power losses are present. For this reason the full bridge phase shifted converter is suited for high power and high frequency applications.

3.2 Description of the topology

Figure 20 shows a basic DC-DC phase shift circuit, only diode rectifier DR1 and DR2 are considered for simplicity to analyze the principle of the converter in the different states. Actually DR1 and DR2 in the STEVAL-ISA172V2 evaluation board are the body diodes of two MOSFETs driven with the synchronous rectification technique, as explained later. An important characteristic of the full bridge phase shift converter is its capability to manage high power, from a few hundred watts to several kilowatts.

Each leg of the converter is driven with a couple of complementary PWM signals with a fixed 50% duty cycle. The modulation is implemented by delaying in phase the two square waves of the lagging-leg (Q3 and Q4) with respect to those of the leading-leg (Q1 and Q2), as shown in *Figure 21*.

Figure 20. Basic circuit of a DC-DC phase shift converter

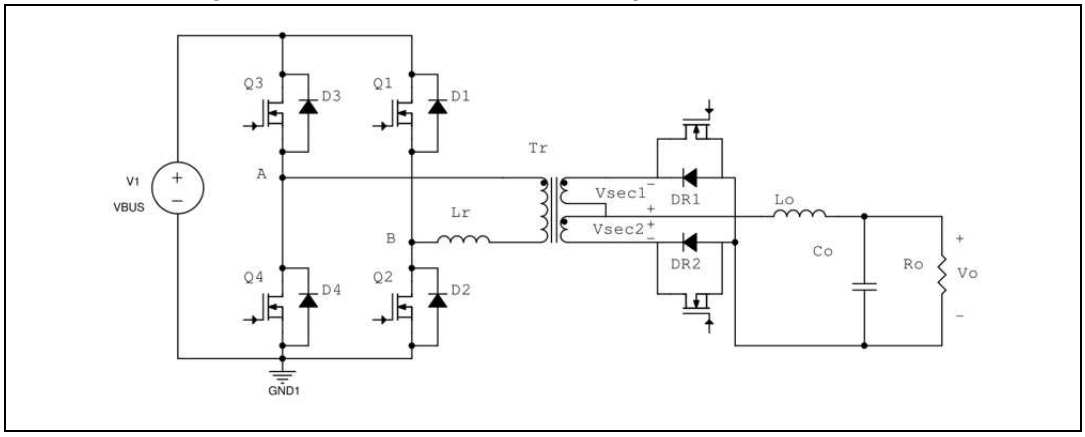
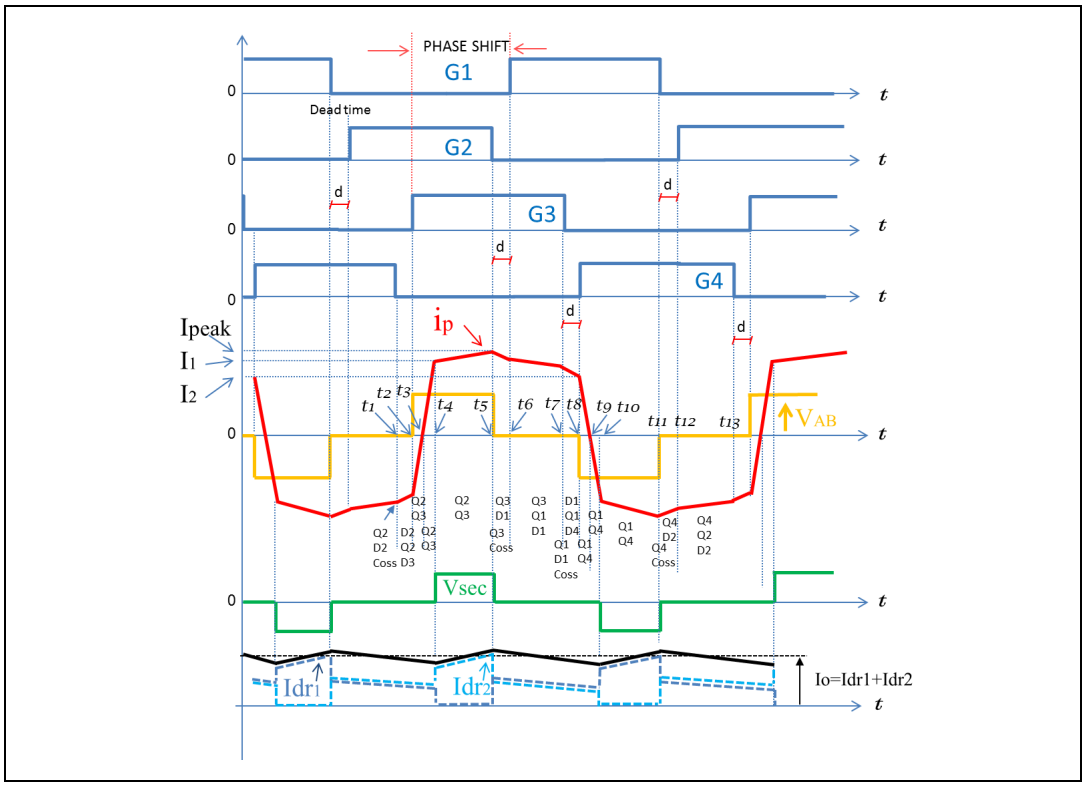


Figure 21. Gate signals, transformer primary current and voltage of the phase shift DC-DC converter



A dead time between the high side and low side driving signals is always necessary to consider, in order to avoid cross conduction between Q1-Q2 and Q3-Q4, as shown in *Figure 21* in which $v_{sec}=v_{sec2} - v_{sec1}$.

In this converter the effect of the parasitic capacitance of the devices is used advantageously to obtain, for all the four switches on the primary side, a soft turn-on, ideally when the drain-to-source voltage reaches zero (ZVS), thanks to the resonance with the transformer's leakage inductance. In this manner the power losses due to the overlap of current and voltage during the turn-on transitions are eliminated.

In contrast to the classic full bridge converter, in which the diagonally opposite switches are turned on simultaneously with a proper duty cycle, the phase shift determines the operating duty cycle of the converter and the square voltage applied on the primary side of the HF transformer. The DC bus voltage is applied to the transformer primary only when two diagonal switches are simultaneously on.

The freewheeling mode is present when the low side or high side switches are on. In this condition the primary side of the transformer is short-circuited (primary voltage is zero).

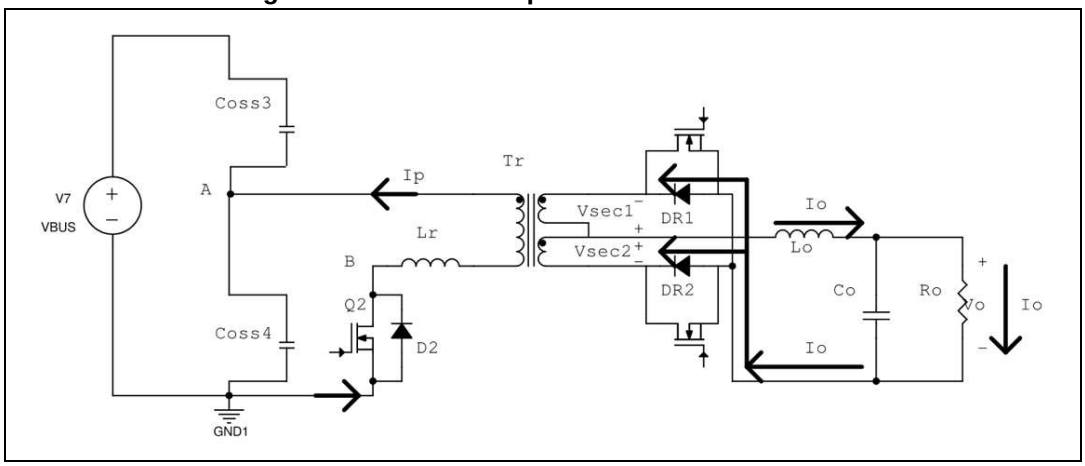
The transformer primary current rising edge slope, as well as the falling edge slope, reduces the duty cycle of the secondary voltage.

This means that more time is needed during the slope for the rising edge and the falling edge on the transformer primary current, and more voltage is loss on the secondary side due to the reduced duty cycle. This effect must be taken into account in the design of the transformer turn ratio, considering the proper resonant inductor L_r and output inductor L_o which determine the slope of the edges.

The following reports the operating modes of the converter depending on the state of the bridge switches.

- Mode 1A: at time t1, Q4 is turning off, Q3 is not yet turned on (dead time), and Q2 is still on:

Figure 22. Mode 1A: Equivalent circuit at time t1



  - The output capacitor C_{oss4} of the MOSFET Q4 starts sinusoidal charging by resonant L_r inductor current (which is relatively low) and the output capacitor C_{oss3} of Q3 starts sinusoidal discharging.
  - The voltages on the primary and secondary (V_{sec}) of the transformer are zero.
  - The output current I_o can free-circulate through the DR1 and DR2 because the voltages V_{sec1} and V_{sec2} are zero and the transformer secondary can be seen as a short circuit.
- Mode 1B: After a certain time interval, before t2 (within the dead time):
  - If there is enough inductive energy, C_{oss3} is completely discharged and C_{oss4} is completely charged.
  - MOSFET body diode D3 is forward biased, which can make Q3 turn on at zero-v
  - The voltages V_{sec1} and V_{sec2} are still zero, DR1 and DR2 are both on and current I_o is split into two parts which flow through the two diodes

Figure 23. Mode 1B: Equivalent circuit before t2

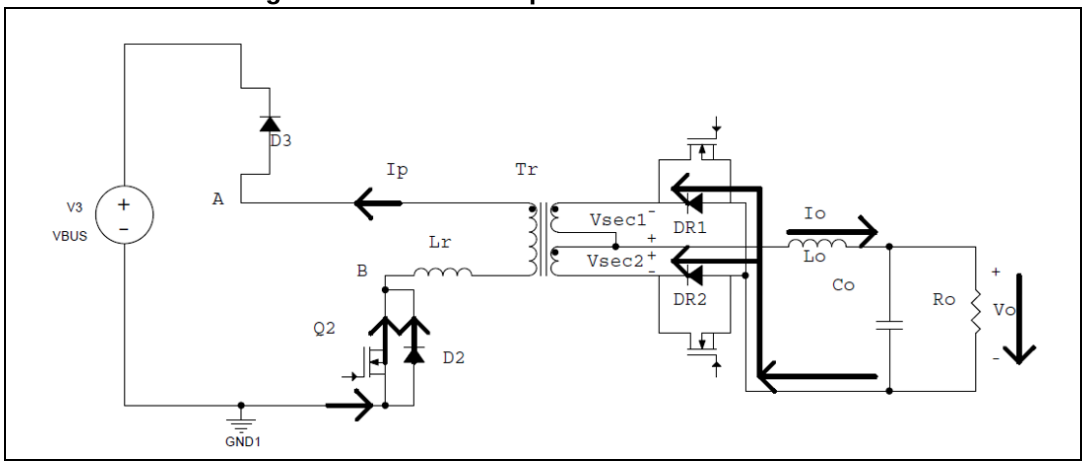
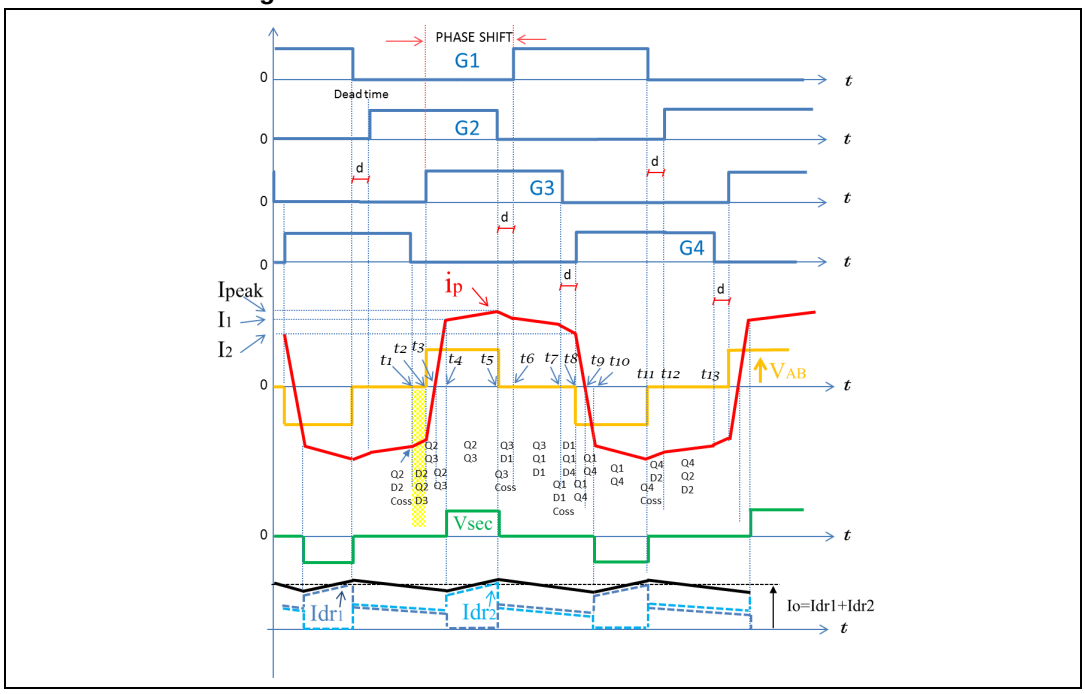


Figure 24. Mode 1: Waveforms between t1 and t2



- Mode 2: between t2 and t3:
  - The primary current I_p (negative) decreases in modulus down to zero with a slope equal to di/dt= V_{bus}/L_r and L_r gets discharged
  - The primary current now flows through Q2 and Q3 (turned on)
  - The output current Io decreases reaching the minimum at t3 and continues to flow through DR1 and DR2
  - V_{sec1} and V_{sec2} voltages are still zero (transformer is still short-circuited).

Figure 25. Mode 2: Equivalent circuit between t2 and t3

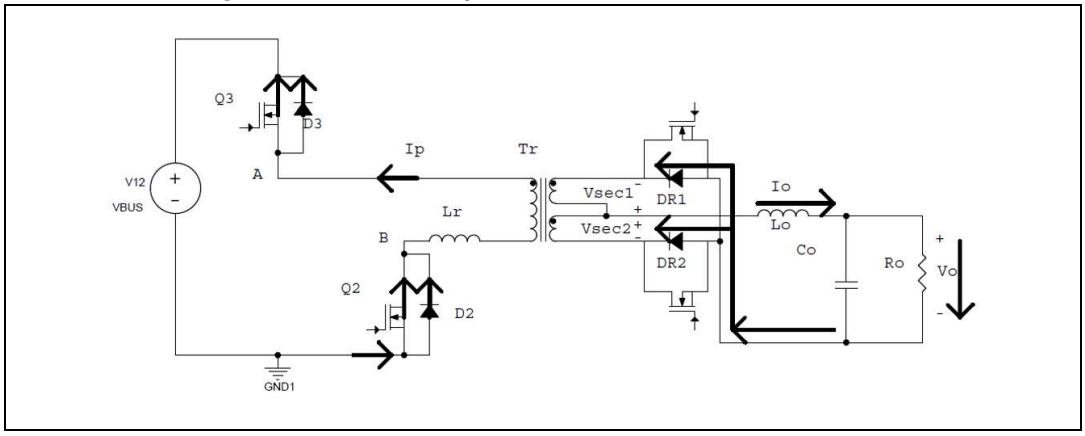
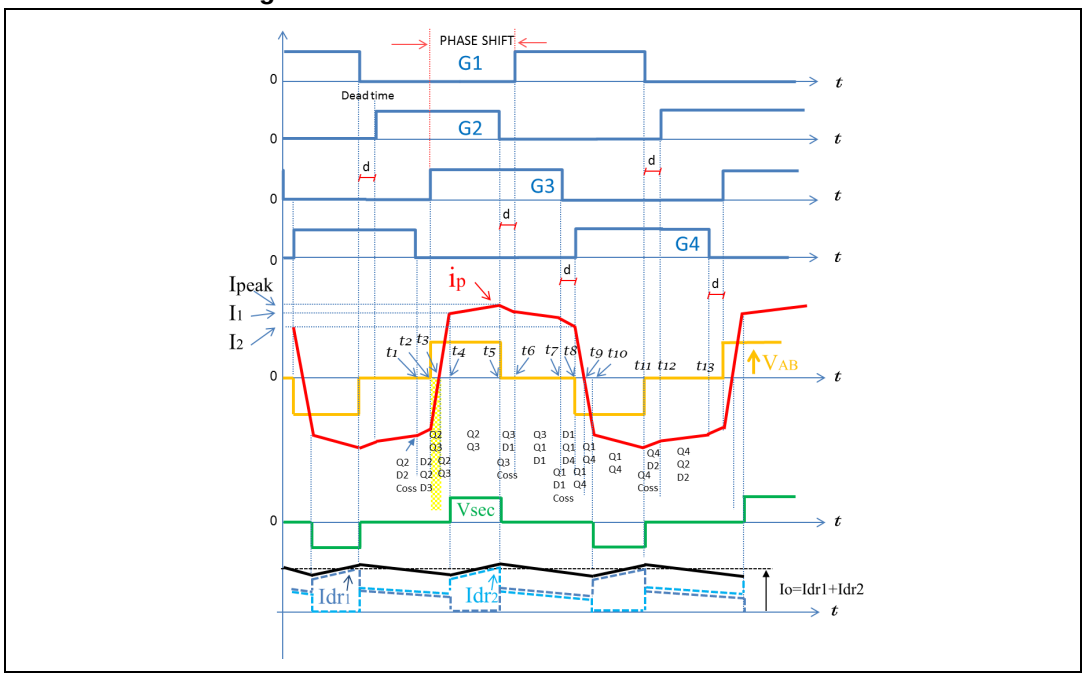


Figure 26. Mode 2: Waveforms between t2 and t3



- Mode 3: between t3 and t4:
  - The primary current Ip increases from zero to reflected output inductor current: I_o*N_S/N_P
  - The primary current continues to flow through Q2 and Q3 (in the opposite direction: D3 and D4 are reverse-biased)
  - L_r is charging
  - Secondary transformer is still short-circuited
  - No power is delivered to output yet (duty cycle loss)

Figure 27. Mode 3: Equivalent circuit between t3 and t4

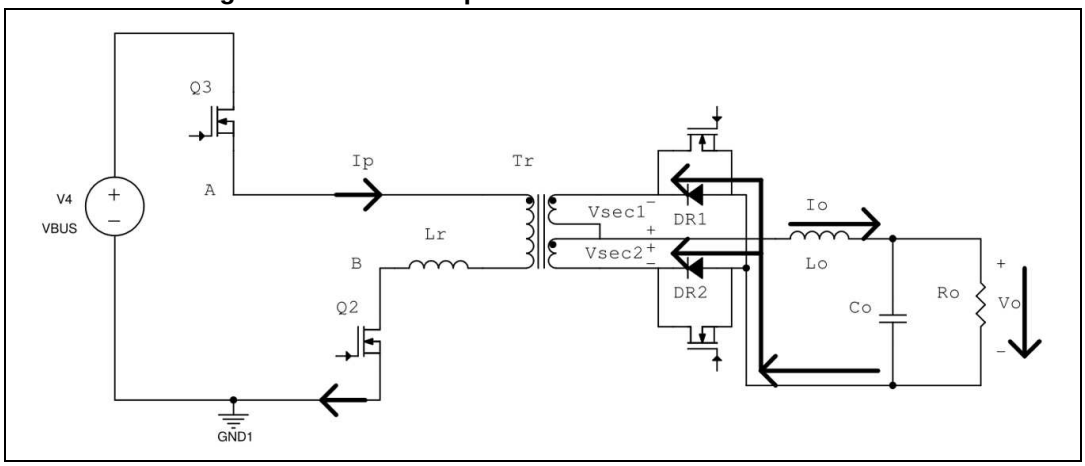
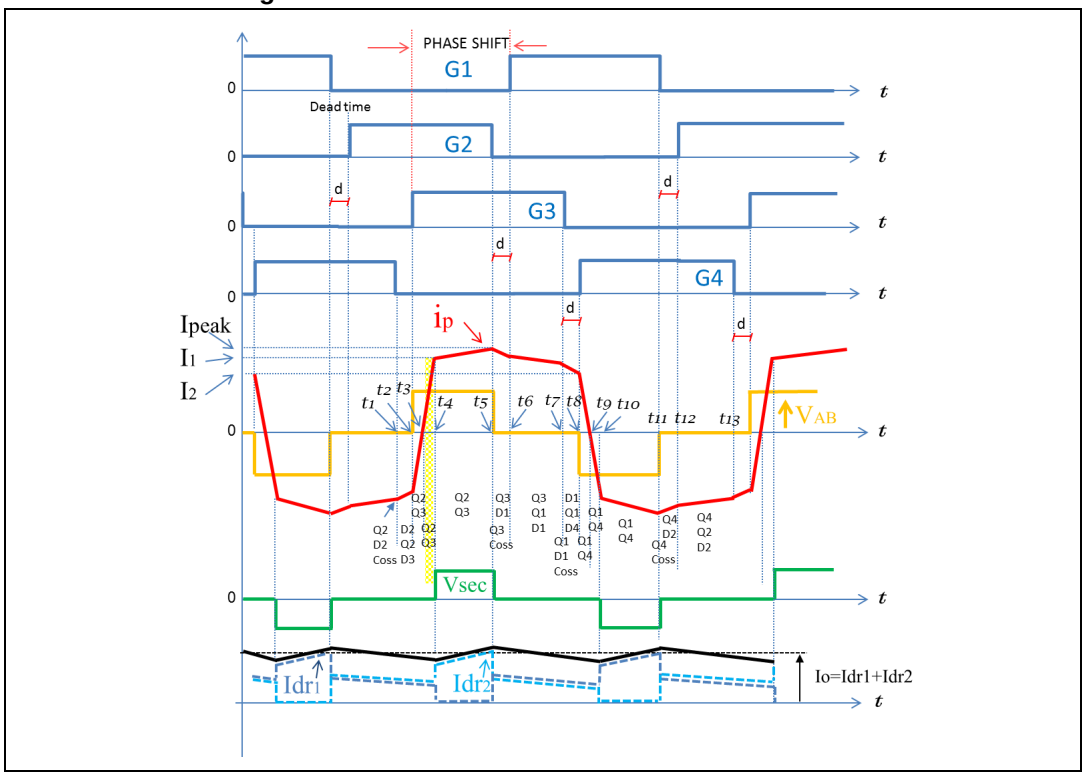
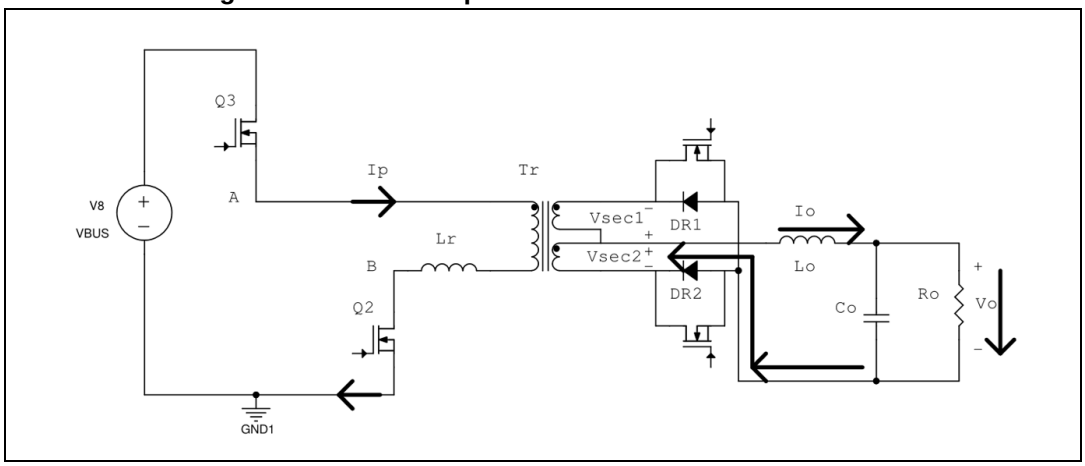


Figure 28. Mode 3: Waveforms between t3 and t4



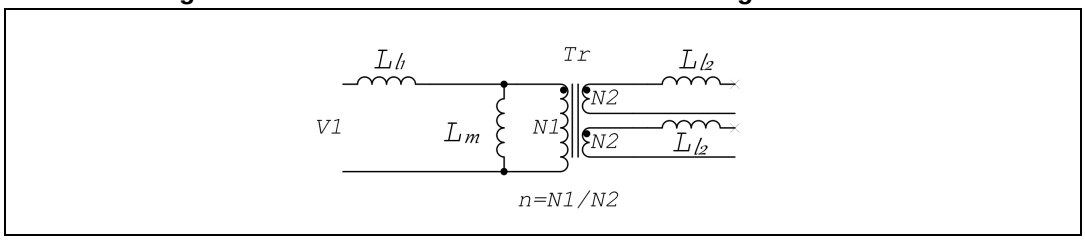
- Mode 4: between t4 and t5:
  - The transformer secondary voltage V_{sec2} is equal to $V_{IN}*N_S/N_P$
  - The inductor L_o starts to get charged
  - I_{DR2} increases while I_{DR1} is zero
  - The energy is transferred from the primary to the output
  - The primary current I_p increases with changed slope

Figure 29. Mode 4: Equivalent circuit between t4 and t5



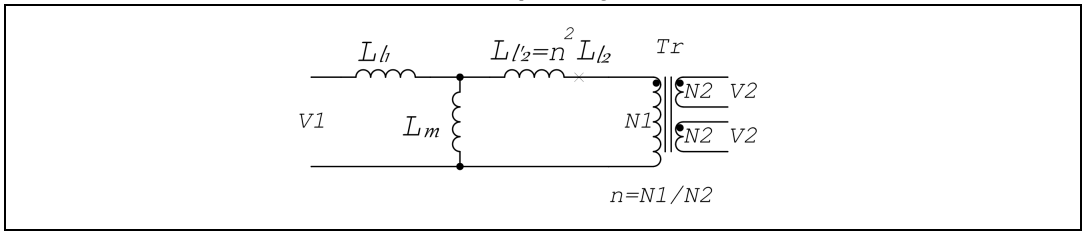
The different slope is due to the reflected L_o inductance to the primary of the transformer, as can be seen in the model shown in the figures that follow.

Figure 30. Model of the transformer with leakage inductances



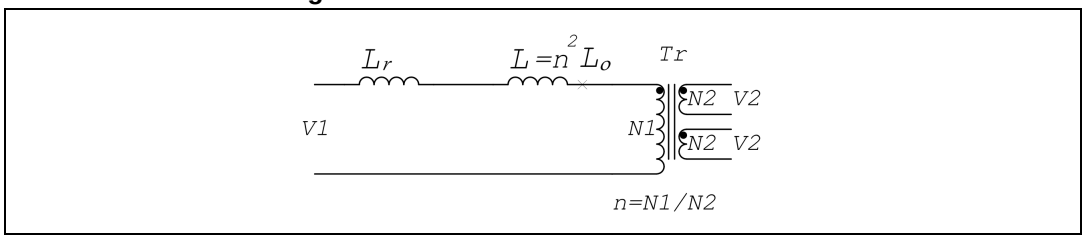
In the model shown in *Figure 30*, for the sake of simplicity resistances are not considered. Secondary leakage inductances can be reported to primary side considering the turns ratio n= N_1/N_2, as shown in *Figure 31*.

Figure 31. Model of the transformer with secondary leakage inductance reflected to the primary



Considering that in practice the reactance $X_{Lm} = \infty$ and considering leakage inductances included in resonance inductor L_r, we can consider the following equivalent circuit:

Figure 32. Final model of the transformer



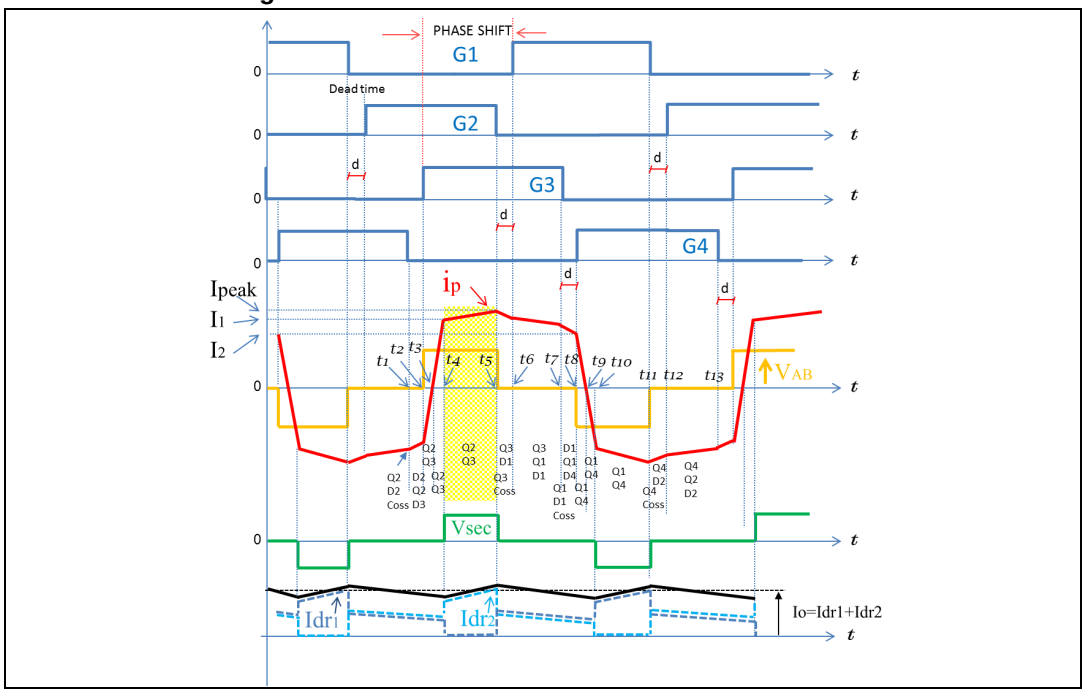
In other words, in mode 4 the total inductance on the primary can be considered as $L_r+n^2L_o$.

The slope of the secondary current I_p in this region depends on the input voltage V_{bus}, output voltage V_o, n transformer ratio, output inductance L_o and L_r:

$$\frac{di}{dt} = \frac{-Vo}{\frac{Lr}{n} + nLo}$$

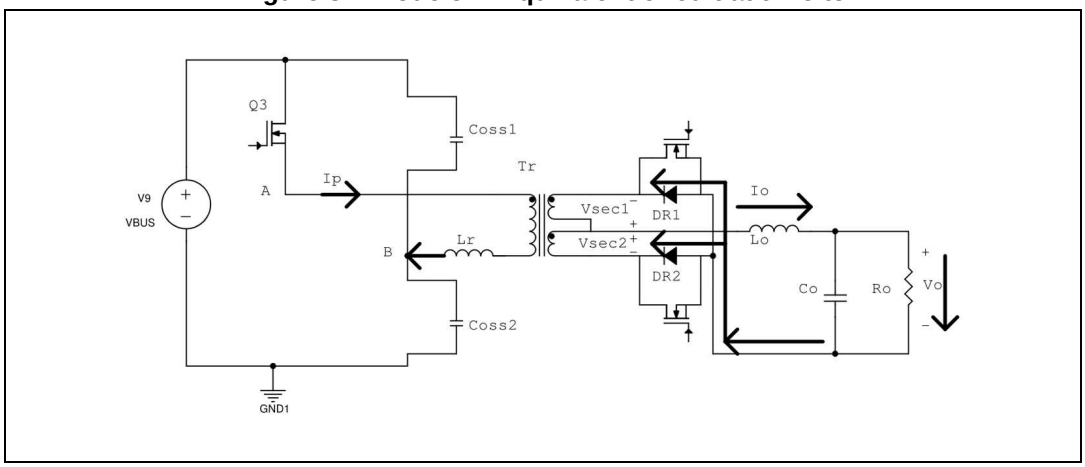
In other words, the equivalent inductance during the interval between t4 and t5 is greater than the initial L_r inductance, and then the primary current slope decreases as shown in the *Figure 33*.

Figure 33. Mode 4: Waveforms between t4 and t5



- Mode 5A: at time t5

Figure 34. Mode 5A: Equivalent circuit at time t5



– Q2 is switched off, Q1 is not yet turned on (dead time) and Q3 is on.

– C_{oss1} starts discharging and C_{oss2} starts charging thanks to the current coming from L_o (which is relatively high). Thus, these two capacitors C_{oss1} and C_{oss2} are

much easier to fully charge and discharge, and Q1 and Q2 (leading leg) are much easier to turn on at zero-voltage condition

  - The output voltage on the transformer V_{sec} falls to zero
  - Diodes DR1 and DR2 are both conducting to support the freewheeling current

- Mode 5B: After a certain time interval, before t6 (within the dead time):
  - The capacitor C_{oss1} is completely discharged and C_{oss2} is completely charged at V_{bus}
  - Dead time is necessary to ensure the charging and discharging process of C_{oss1} and C_{oss2}
  - Body diode of Q1 D1 is in conduction, this permits Q1 to be turned on at zero-voltage
  - V_{sec1} and V_{sec2} are zero and both diodes DR1 and DR2 are conducting

Figure 35. Mode 5B: Equivalent circuit before t_6

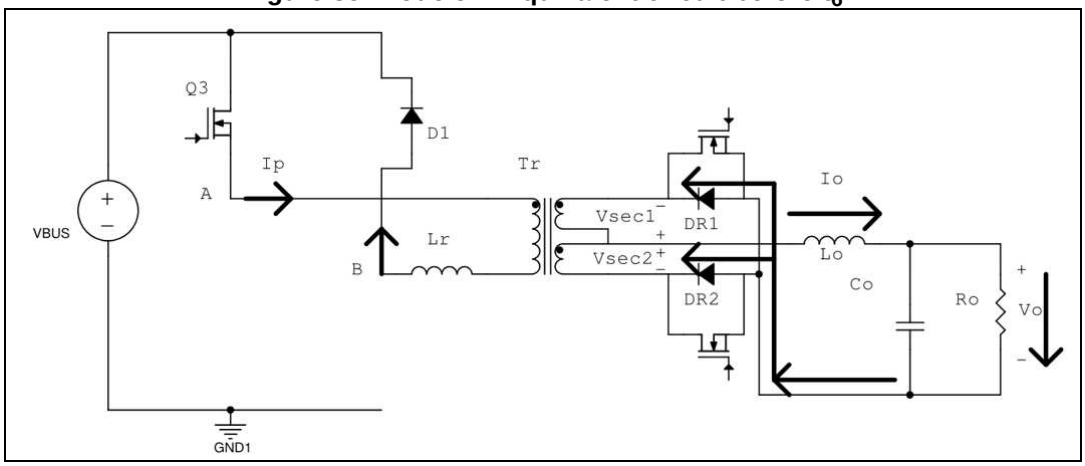
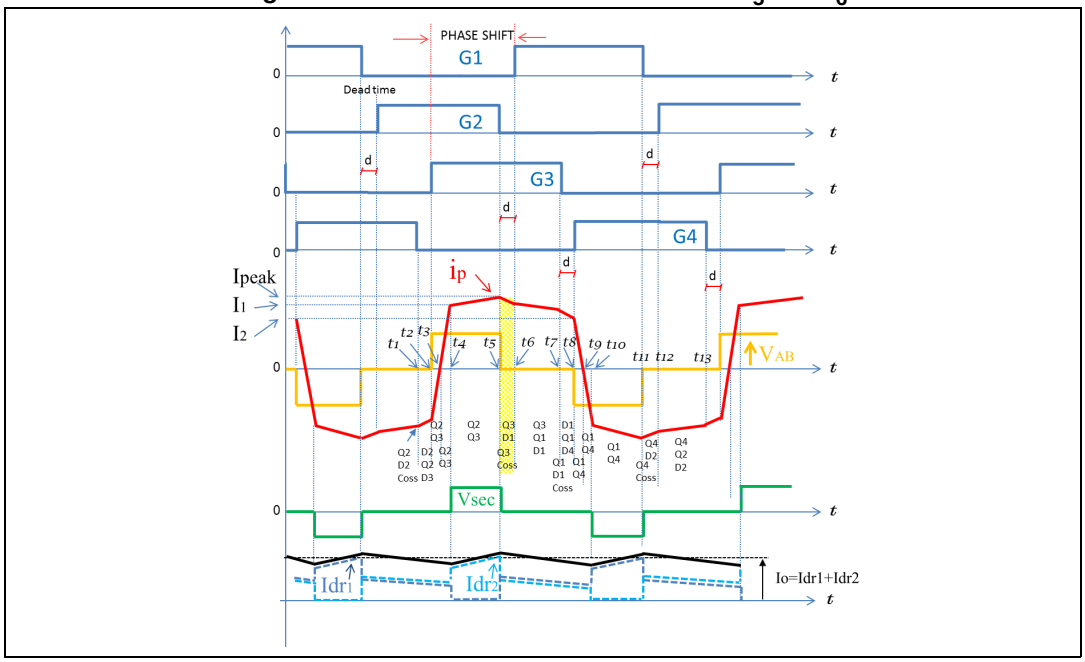


Figure 36. Mode 5: Waveforms between t_5 and t_6



- Mode 6: between t6 and t7:
  - Q2 is off, Q1 is turned on and Q3 is on
  - Both high side switches are turned on and then the primary transformer voltage is zero (freewheeling mode)
  - V_{sec1} and V_{sec2} are zero and both diodes DR1 and DR2 are conducting
  - The slope of the primary transformer current I_p in this region depends on the output voltage V_o, n transformer ratio, and output inductance L_o:

$$\frac{di}{dt} = \frac{-Vo}{\frac{Lr}{n} + nLo}$$

Figure 37. Mode 6: Equivalent circuit between t_6 and t_7

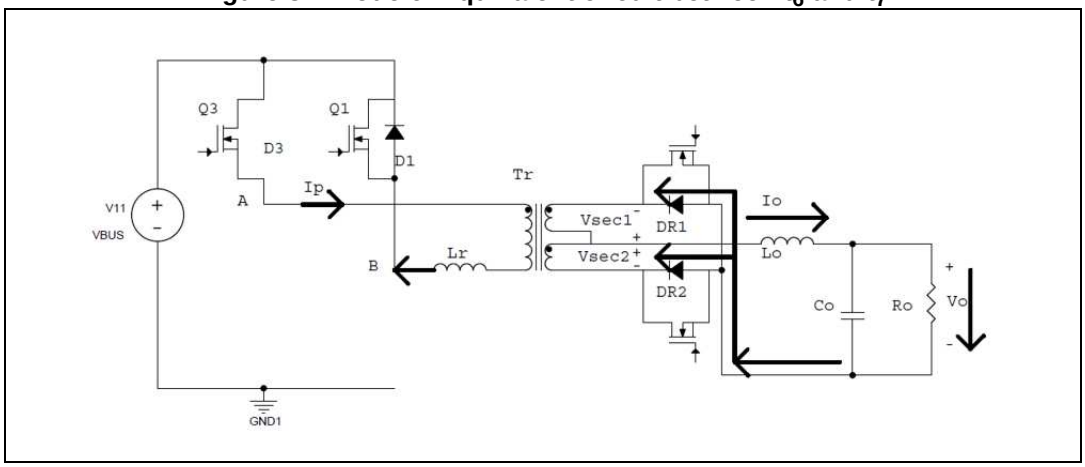
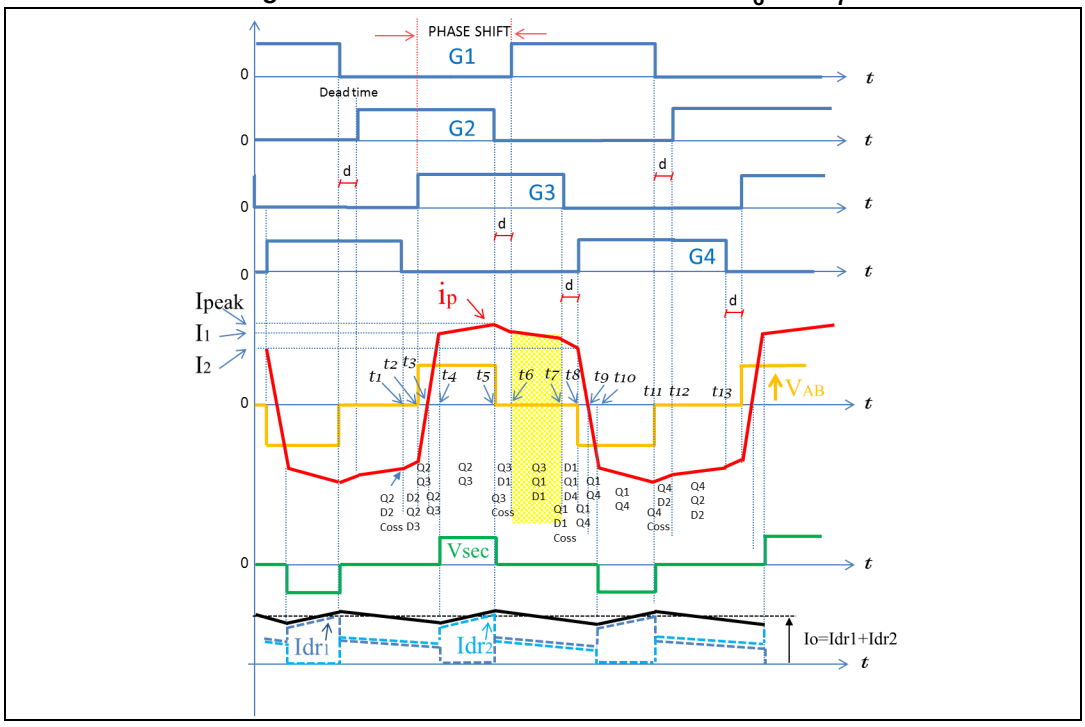


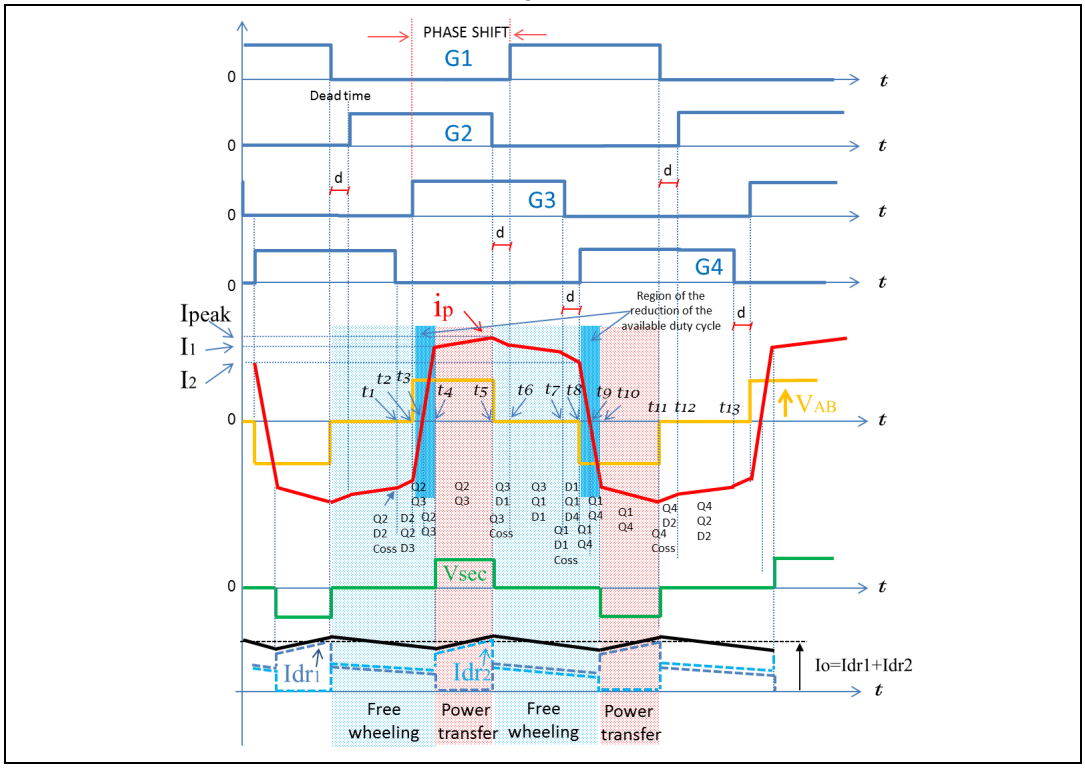
Figure 38. Mode 6: Waveforms between t_6 and t_7



The behavior of the converter in the remaining operating modes is similar to the previous ones, but with different switches involved. Summarizing, we can observe from the diagram below the presence of two free-wheeling and two power transfer regions in one entire switching period.

The region of the reduction of the available duty cycle is also shown (duty cycle loss); it depends on the slope of the transformer primary current inside the free-wheeling zone, which is linked to the bus voltage V_{bus}, and the L_r inductance (the leakage inductance of the transformer is also considered) as V_{bus}/L_r.

Figure 39. Free-wheeling, power transfer and reduction regions of the available duty-cycle



A high value of L_r limits the power transfer capability because it decreases the output available duty cycle (duty cycle loss is increased). On the other hand, a large L_r increases the load range in which the converter works in the ZVS condition (ZVS is reached for smaller loads). For this reason it is important, during the design phase of the converter, to choose a proper resonance inductor value and an adequate transformer turns ratio, in order to assure voltage output regulation even at full load and a large ZVS operating range.

A problem with this topology is that high voltage spikes can be observed on the devices of the push-pull output stage due to the energy stored in the transformer leakage inductance and diode reverse recovery charge.

Using an RCD snubber on this type of converter introduces additional thermal dissipations and decreases the overall efficiency.

Thus the STEVAL-ISA172V2 evaluation board doesn't include a passive snubber, but an active clamp, in order to reverse the extra energy directly to the output, then increase the efficiency, preventing dissipative losses.

Figure 40 shows the acquired voltages on primary and secondary windings together with the primary current of the transformer. It is possible to note that until the primary current reaches the reflected output inductor current, the voltage V_{sec} on the secondary is zero (duty cycle loss), as explained previously.

Figure 40. Full bridge voltage, primary current and secondary voltage on the transformer

3.3 ZVS considerations

To obtain soft turn on of the bridge switches, the stored transformer leakage inductance energy must be greater than the capacitive energy stored in the equivalent output capacitor of the MOSFET, so that when the switch of the same leg is turned off, this capacitance is discharged and zero voltage switching (ZVS) is achieved.

Therefore, to extend the ZVS range also for light loads, a resonance inductor L_r is introduced in series with the primary winding of the transformer, increasing the inductive energy also for small currents.

If the ZVS is not well tuned, the converter works in hard switching, generating a lot of noise and switching losses.

Considering for instance operating Mode 1 described above, to be sure that Q3 turns on with zero voltage, a certain dead time is inserted between Q4 turn off and Q3 turn on.

The equivalent resonant circuit is composed of L_r (which includes the transformer leakage inductance) and the output capacitor C_{eq} seen at the mid point of the leg involved in the ZVS process.

C_{eq} is given by:

Equation 18

$$C_{eq} = C_{oss3} // C_{oss4} // C_{tr} = 2C_{oss} + C_{tr}$$

where C_{oss3} and C_{oss4} are the output MOSFET capacitors and C_{tr} is the input capacitor of the transformer.

This resonance circuit provides a sinusoidal charge/discharge of the capacitors with a period given by:

Equation 19

$$T_r = 2\pi\sqrt{C_{eq} * L_r}$$

The peak of this voltage is after Tr/4 from last device turn off. Dead time plays an important role on the ZVS, to obtain ZVS the condition is that:

Equation 20

$$T_d \geq T_r/4$$

The turn on of the switches should be when the corresponding capacitor is discharged and the body diode of the switch enters in forward conduction: in such way the commutation will occur at zero voltage.

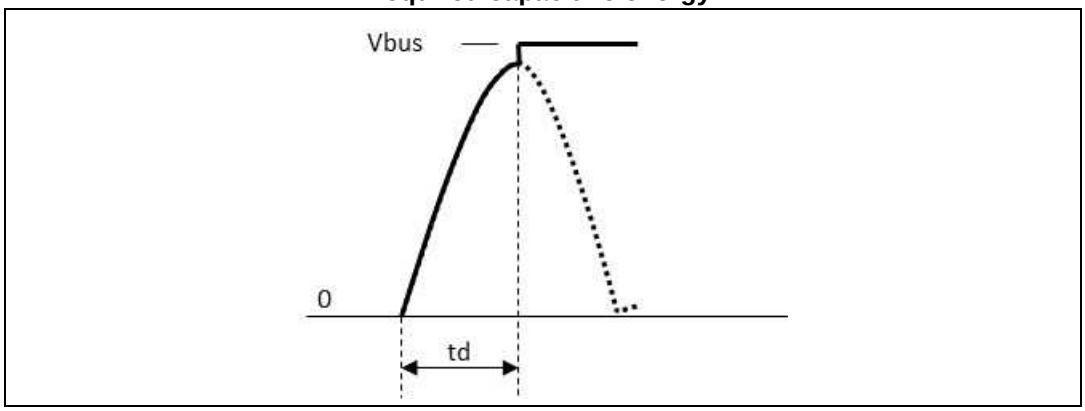
Increasing resonance inductor the ZVS range is extended, but, on the other hand, the resonance frequency is decreased and a greater dead time is required; for this reason it is suitable to choose devices with a low output capacitance such as FDmesh II MOSFET STW35N60DM2.

Since the behavior of the converter is not symmetric for leading and lagging legs, different considerations to achieve ZVS are made for each leg.

3.3.1 ZVS for lagging leg

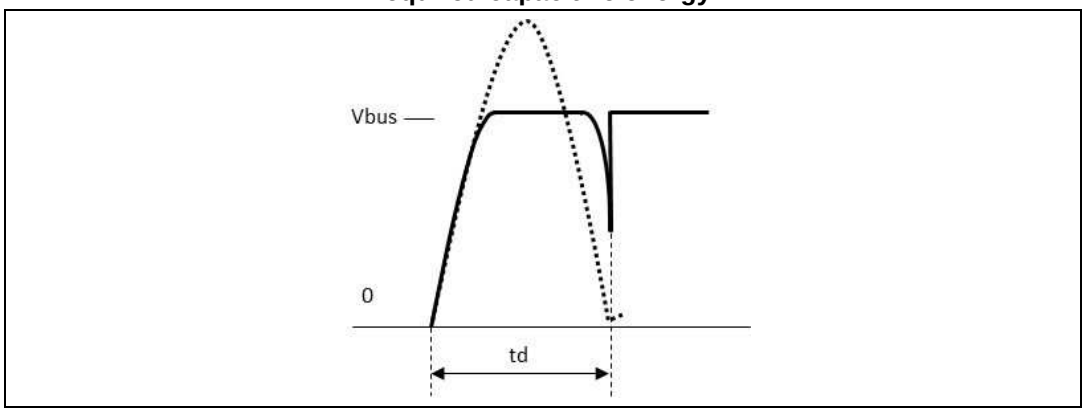
The inductive energy available for ZVS of the lagging leg is relatively small and consists only of the energy stored in resonance inductor and in the transformer leakage inductor. If this energy is not enough to charge or discharge the output capacitor C_{oss}, the switch turns on in hard switching condition, the ZVS is lost with high losses and high EMI (*Figure 41*).

Figure 41. Voltage across the switch when the energy stored in L_r is smaller than required capacitive energy



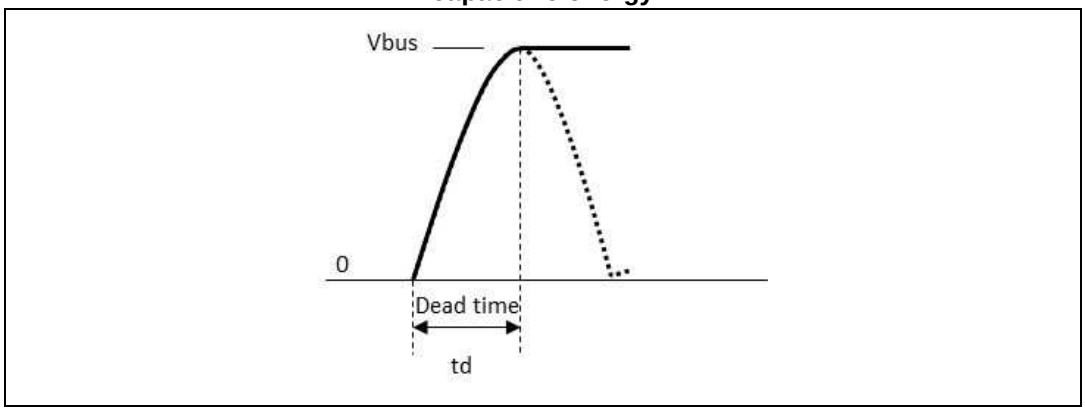
When the energy stored in L_r is larger than the energy required to charge or discharge the output capacitors C_{oss}, they are charged or discharged before one fourth of the resonant period and the voltage is clamped to V_{bus} value, as shown in *Figure 42*.

Figure 42. Voltage across the switch when the energy stored in L_r is greater than required capacitive energy



Finally, when the energy stored on L_r is equal to the energy required to charge or discharge the output capacitors, the voltage across the switch reaches V_{bus} at $T_r/4$ (peak of sinusoid), as shown in *Figure 43*.

Figure 43. Voltage across the switch when the energy stored in L_r is equal to required capacitive energy



The condition for which the ZVS is achieved for lagging leg is:

Equation 21

$$\frac{1}{2} L_r \, {I_1}^2 > \frac{1}{2} (C_{oss3} + C_{oss4}) \, {V_{bus}}^2 + \frac{1}{2} C_{tr} {V_{bus}}^2$$

Where I_1 is the primary transformer current at turn-on/turn-off of Q3 and Q4.

The critical current in which ZVS is lost is:

Equation 22

$$I_{critical} = \sqrt{\frac{(C_{oss3} + C_{oss4}) + C_{tr}}{L_r}} \cdot V_{bus}$$

The choice of L_r inductance is made taking into account the desired minimum load at which the converter starts to work in ZVS (usually 25% of maximum load). When $I_1 \geq I_{critical}$, the ZVS is achieved.

L_r includes also the leakage inductance of the transformer.

3.3.2 ZVS for leading leg

For leading leg the inductive energy available to charge or discharge the output capacitors is greater than that available for lagging leg because the energy stored in output filter inductor L_o is also to be considered.

The condition for which the ZVS is achieved for leading leg is:

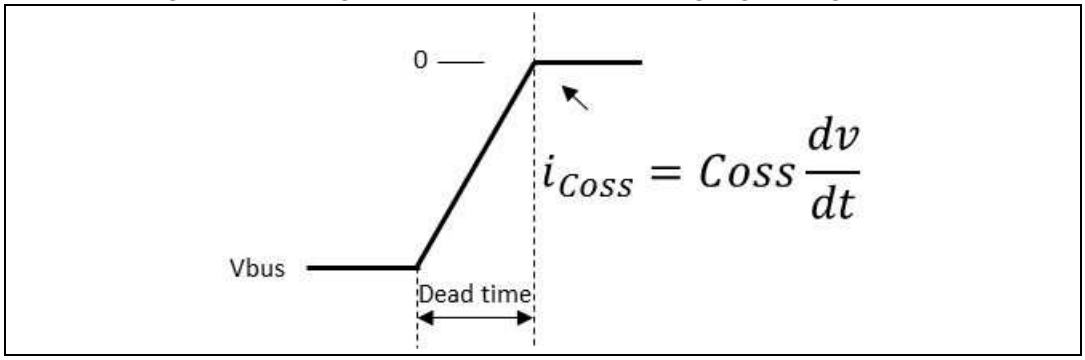
Equation 23

$$\frac{1}{2}(L_r + L_{op})\, {I_2}^2 > \frac{1}{2}(C_{oss1} + C_{oss2})\, {V_{bus}}^2 + \frac{1}{2} C_{tr} {V_{bus}}^2$$

where I_2 is the primary transformer current at turn-off of Q1 or Q2 (peak value of transformer current) and $L_{op}=n^2L_o$ is the output filter inductance referred to the primary.

The inductive energy available when Q1 is turned off is much higher than the energy required to charge and discharge the output capacitors C_{oss1} and C_{oss2} even for low loads, in contrast to that of lagging leg; for this reason the capacitors of the switches are charged or discharged within the dead-time, very quickly, linearly and without oscillations.

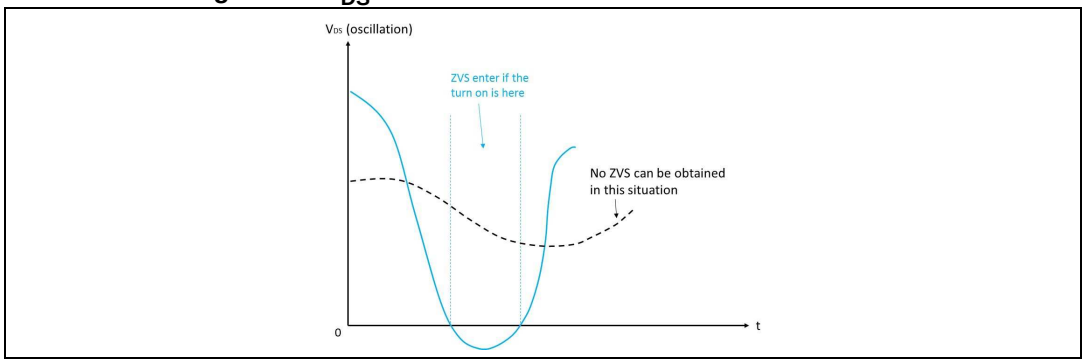
Figure 44. Voltage across a switch of leading leg during turn off



Therefore, the body diode of the devices of leading leg turns on before the complementary MOSFET is turned on, even at light load, and then more energy than the lagging leg is lost as dissipation. In the diagram below the voltage drop across the MOSFET due to resonance during the dead time is shown. A limitation of ZVS will exist at a low primary (or secondary)

current value, so at very low load no ZVS can be obtained and hard switching occurs (see *Figure 45*).

Figure 45. V_{DS} oscillation with and without ZVS reached



3.4 Full bridge ZVS DC-DC converter design

Table 7. DC-DC design specifications

Parameter	Description	Min.	Typ.	Max	Unit
V_{in}	Input voltage	375	400	425	V
V_{out}	Output voltage	45.6	48	50.4	V
P_{out}	Output power			2000	W
I_{out_max}	Maximum output current		42		A
F_{sw}	Switching frequency		100000		Hz
ΔIL_max%	Maximum output inductor current ripple		20		%
ΔVo_max%	Maximum output voltage ripple		5		%

3.4.1 Transformer turns ratio calculation

The transformer turns ratio can be calculated from the equation below:

Equation 24

$$\frac{V_{out}}{V_{in\_min}} = \frac{N_s}{N_p} / \delta_{max}$$

Where N_s is the number of secondary turns, N_p the number of primary turns and δ_{max} is the maximum effective duty cycle of the voltage appearing at the transformer secondary winding within a switching period. In this design, the maximum duty cycle is chosen as δ_{max}=0.8 and takes into account the duty cycle loss, maximum phase shift imposed by control loop and dead time.

N_s/ N_p is calculated as:

Equation 25

$$\frac{N_s}{N_p} = \frac{V_{out}}{V_{in\_min}} \cdot \frac{1}{\delta_{max}} = \frac{48}{375} / 0.80 = 0.16$$

Equation 26

$$n = \frac{N_p}{N_s} \cong 6$$

Where n is the turns ratio of the transformer.

Increasing the transformer turns ratio means to decrease the transformer primary current and the reflected secondary voltage on SR MOSFETs. In practice the n ratio should be chosen considering two important aspects: the first is the minimum primary current at which the ZVS occurs, the second is the maximum power deliverable at minimum input voltage due to the duty cycle loss region.

For the first reason, to extend ZVS range also for light loads, the possibility to choose n = 5, has been evaluated checking the reflected MOSFETs voltage on the synchronous rectification (SR) MOSFETs to be below the breakdown voltage.

The applied voltage on the output devices, when they are in an off state, is two times the reflected voltage on the secondary windings V_{sec}. If we chose n = 5 this voltage is:

Equation 27

$$V_{sec} = 2 \cdot \frac{N_s}{N_p} \cdot V_{in\_max} = 170V$$

From the previous formula, the maximum applied voltage on the (SR) MOSFETs is 170 V, so the chosen device is the N-channel STW75NF20 200V MOSFET in STripFET™ technology with fast recovery diode.

3.4.2 Primary MOSFETs

The power MOSFETs used on the primary side of the phase shifted DC-DC converter is the N-channel STW35N60DM2. It has low Q_g, 600 V breakdown voltage, 0.175 ohm typical drain-source resistance and drain current of 18 A at 25 °C case temperature.

These FDmesh II Plus™ low Q_g power MOSFETs with intrinsic fast-recovery body diode are produced using a new generation of MDmesh™ technology: MDmesh II Plus™ low Q_g. These revolutionary power MOSFETs associate a vertical structure to the company's strip layout to yield one of the world's lowest on-resistance and gate charge. They are therefore suitable for the most demanding high efficiency converters and ideal for bridge topologies and ZVS phase-shift converters.

3.4.3 Resonant inductor L_r calculation

As mentioned before, for the full bridge circuit the STW35N60DM2 MOSFET has been chosen. The equivalent output capacitance of a single device is C_{oss} = 259 pF, so the equivalent capacitance C_{eq} involved in ZVS process (as seen in *Section 3.3*) is:

Equation 28

$$C_{eq} = 2C_{oss} + C_{tr} = 2 * 259 * 10^{-12} + 36 * 10^{-12} = 554pF$$

Where C_{tr} = 36 pF is the transformer input capacitance.

The associated capacitive energy to be removed on the transition can be calculated:

Equation 29

$$W_{Cr} = \frac{1}{2} C_{eq} {V_{bus}}^2$$

To achieve lagging-leg turn on soft switch, the energy stored in L_r must be greater than the energy stored in C_{eq} equivalent capacitor:

Equation 30

$$W_{Lr} = \frac{1}{2} L_r \, {I_1}^2 \geq \frac{1}{2} C_{eq} {V_{bus}}^2 = W_{Cr}$$

Then the value of the resonance inductor depends on the desired minimum current, referred to primary winding of the transformer, at which it is possible to achieve ZVS.

Usually, L_r is chosen to obtain ZVS for loads above a certain percentage of maximum load.

Another method to choose the L_r inductor is dimensioning the resonance tank frequency greater than four times the maximum transition time T_{tr_max} at light load, in order to reach ZVS:

Equation 31

$$T_{tr\_max} = \frac{T_r}{4}$$

In which the resonant period is:

Equation 32

$$T_r = \frac{2\pi}{\omega_r}$$

Where ω_r is the resonant radiant frequency.

Equation 33

$$\omega_r = \frac{1}{\sqrt{C_{eq} * L_r}}$$

Combining *Equation 33* with *Equation 31* and *Equation 32* it is possible to obtain the minimum value for the resonance inductance:

Equation 34

$$L_r = \frac{1}{{\omega_r}^2 * C_{eq}} = \left(\frac{2T_{tr\_max}}{\pi}\right)^2 \frac{1}{Cr}$$

Choosing a 30 µH inductor, experimental results have been shown that ZVS is achieved for loads greater than 35% of maximum load.

The slope of the primary current during δ_{loss} is fixed by L_r:

Equation 35

$$\frac{di}{dt} = \frac{V_{bus}}{L_r} = \frac{400}{30 * 10^{-6}} = 13.33\ A/\mu s$$

And then the critical primary current below which the converter enters hard switching mode is:

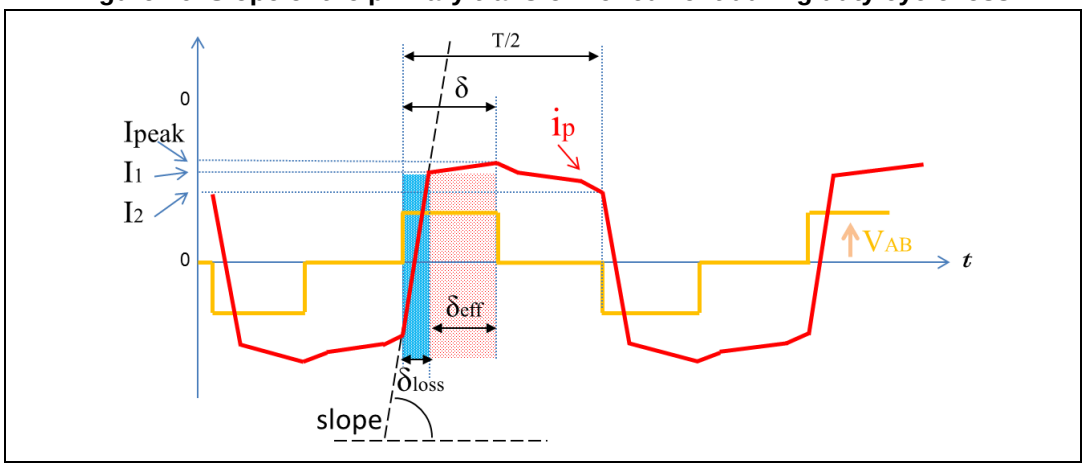
Equation 36

$$I_{critical} = V_{bus}\sqrt{\frac{C_{eq}}{L_r}} = 400\sqrt{\frac{554 * 10^{-12}}{30 * 10^{-6}}} = 1.72A$$

This means that, for primary current above 1.72 A, the converter starts to work in soft switching condition if the dead time is properly tuned, as described in the following paragraph.

The diagram below shows the slope of the primary transformer current, duty cycle loss δ_{loss}, the effective duty cycle δ_{eff} and δ as sum of δ_{loss}+ δ_{eff}.

Figure 46. Slope of the primary transformer current during duty cycle loss



3.4.4 Dead time

A fundamental parameter to set in order to reach ZVS is the dead time inserted in full bridge PWM generation. As explained in *Section 3.3*, the MOSFET should be turned on when the

voltage across the device is zero or almost zero. During the dead time, the devices of the same leg of the full bridge are simultaneously off and the resonant circuit, consisting of L_r and C_{eq}, causes a sinusoidal charge/discharge of output capacitors of the MOSFETs.

As mentioned previously, the period of this oscillation is given by:

Equation 37

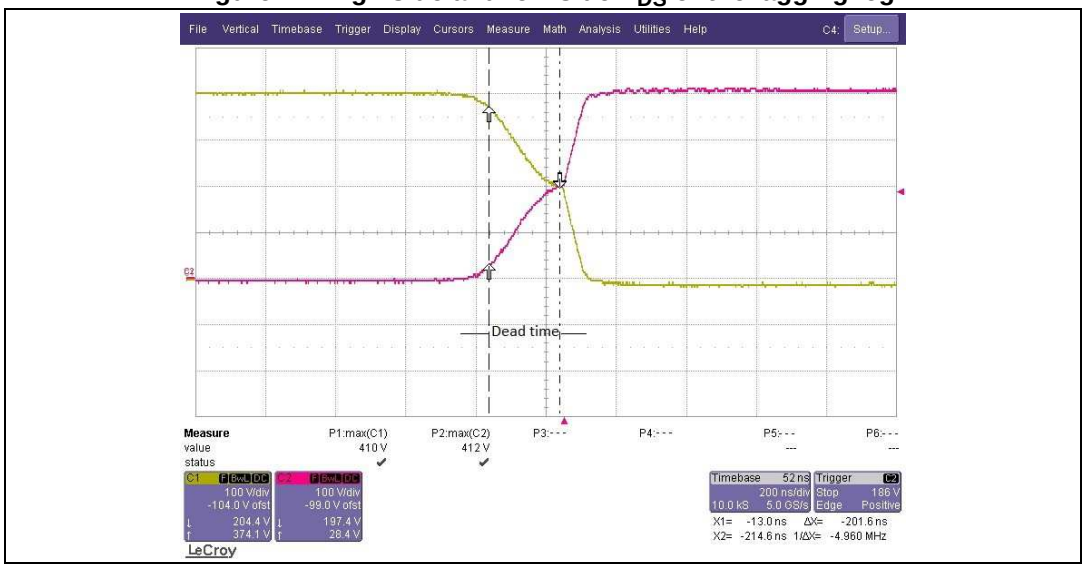
$$T_r = 2\pi\sqrt{C_{eq} * L_r} = 2\pi\sqrt{48 \cdot 10^{-12} * 30 \cdot 10^{-6}} = 805ns$$

The condition to achieve ZVS is to choose $T_d = 1/4T_r$:

Equation 38

$$T_d = \frac{1}{4}T_r = \frac{\pi}{2}\sqrt{C_{eq} * L_r} = 201ns$$

Figure 47. High side and low side V_{DS} of the lagging leg



To minimize switching losses, even if the converter works in hard switching, the dead time was chosen in order to turn on the MOSFETs at the minimum valley of the resonance voltage. In practice, due to the driving circuit delay, the dead time value has been experimentally set in the microcontroller's PWM generation at 450 ns; in this manner the device's commutation occurs in correspondence with the maximum or minimum of the sinusoid, as shown in *Figure 47*, *Figure 48* and *Figure 49*.

Figure 48. V_{DS} at MOSFET turn off

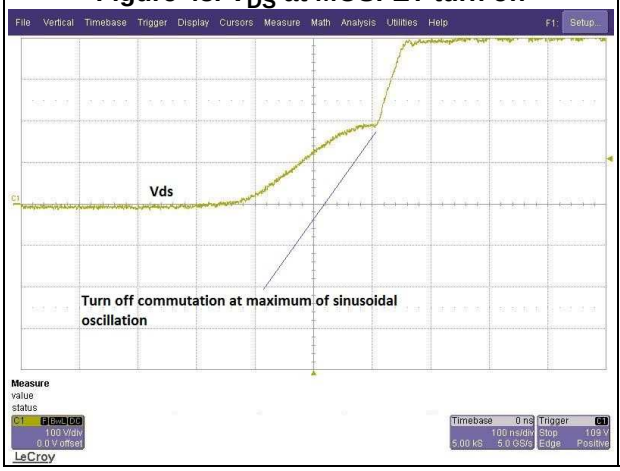


Figure 49. V_{DS} at MOSFET turn on

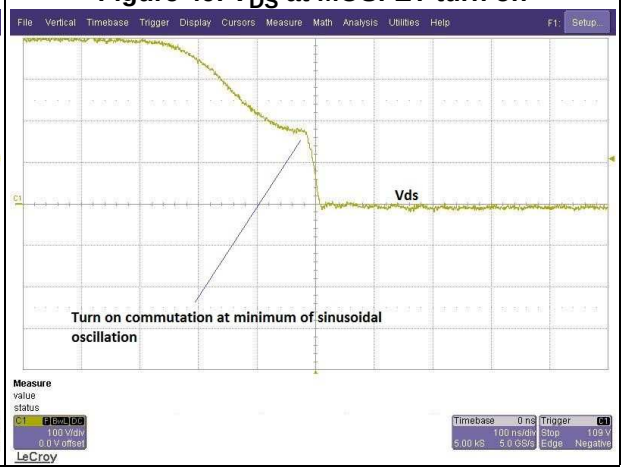
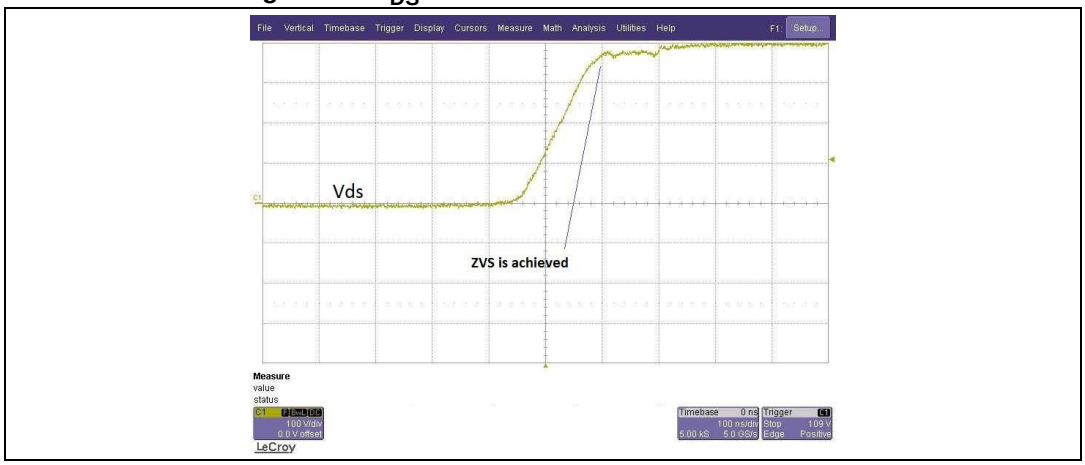


Figure 50 shows the situation in which ZVS is reached: according to experimental measurements, it happens starting from a load of around 35% of maximum load. To reduce this value it would be necessary to increase the resonant inductor L_r, but with the drawback of increasing the duty cycle loss and then the maximum deliverable output power.

Figure 50. V_{DS} at MOSFET turn-off: ZVS reached



3.4.5 Active clamp

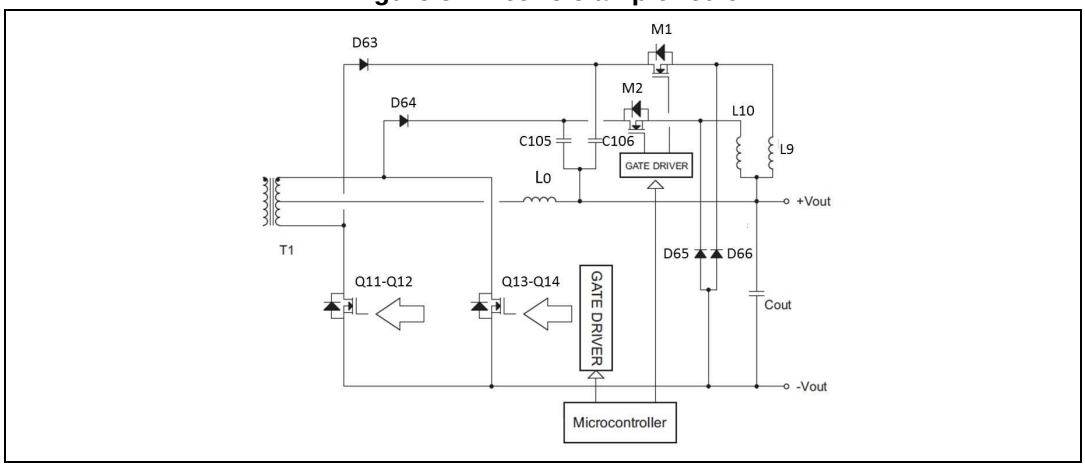
In the full bridge phase shift converter, high voltage spikes are present on synchronous rectification MOSFETs turn off due to the inductive energy stored in the transformer leakage inductor and diode reverse recovery charge of devices. The overvoltage can be greater than the breakdown voltage of the device which therefore has to be protected. These spikes are present and dangerous even when choosing a transformer with a higher turn ratio which reduces the reflected voltage on secondary windings.

As mentioned before, a passive snubber is not applicable without considerably reducing the efficiency of the converter.

Therefore an active resonant clamp, which operates as a buck converter, was introduced to reverse this extra energy to the output stage, maintaining high conversion efficiency.

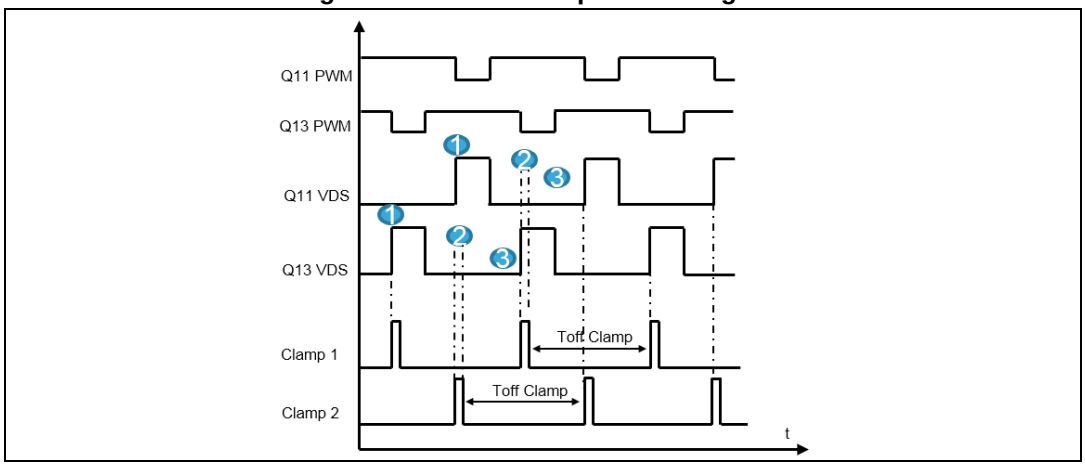
Referring to *Figure 51*, the voltage spikes that are generally observed across the output MOSFETs Q11-Q12 and Q13-Q14 are clamped by capacitors C105 and C106 and then diverted to the output by circuits implemented by M1, L9, D66 and M2, L10, D65, which are in buck configuration. These additional buck converters are designed to work in DCM to reduce the voltage by the desired amount in a single pulse operation.

Figure 51. Active clamp circuit



Therefore the active clamp described avoids dissipating this energy by transferring it to C_{out}, but it needs to be controlled by the microcontroller with two additional signals, as shown in *Figure 52*, to discharge C105 and C106, respectively.

Figure 52. Active clamp control signals



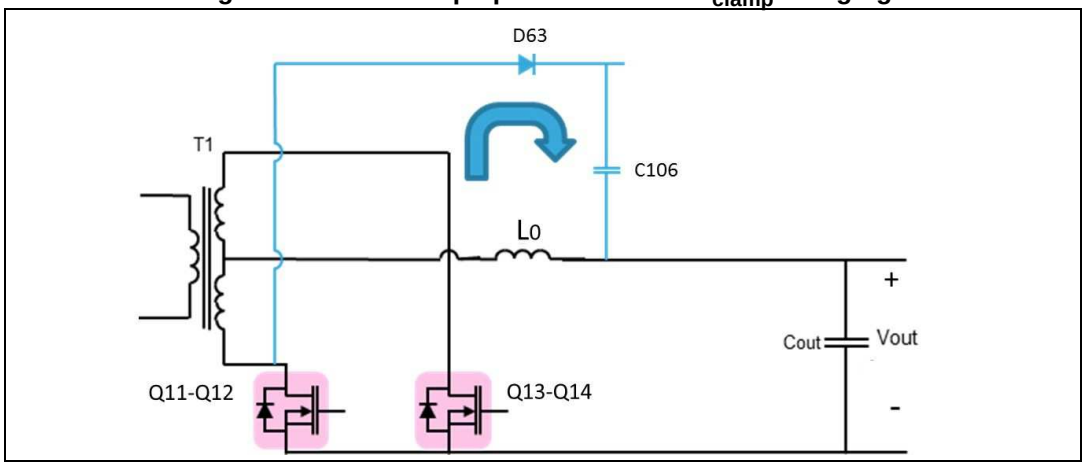
Below it is explained in detail the working principle of the active clamp used in the STEVAL-ISA172V2 evaluation board considering only the first clamp circuit formed by D63, C106, M1, L9 and D66.

The active clamp behavior sequence consists of the following three operation modes:

- Operation mode 1: Clamp capacitor charging

When Q11-Q12 is turned-off, the V_{DS} voltage exceeds the voltage V_{out} + V_{C106}, forward biasing D63 and allowing the energy stored on the leakage inductor to be transferred to the clamping capacitor C106 (*Figure 53*).

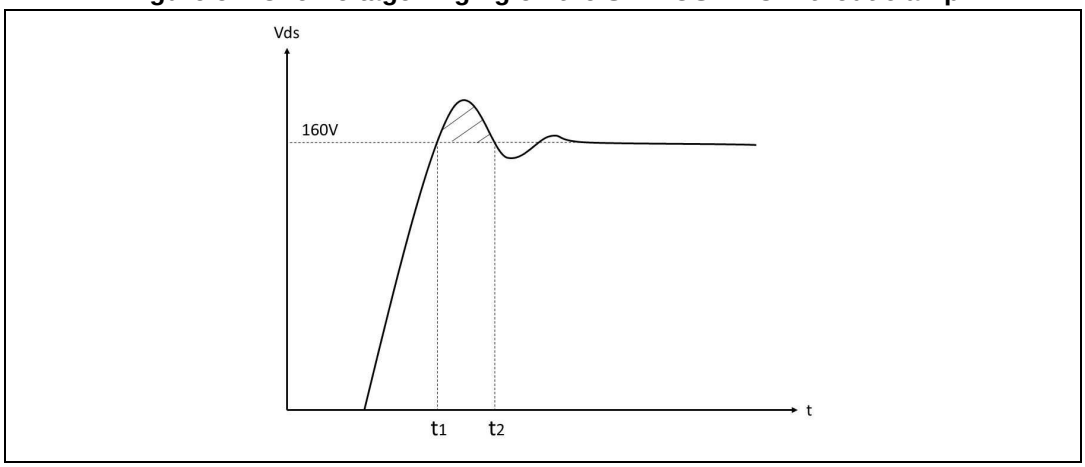
Figure 53. First clamp operation mode: C_{clamp} charging



Without the clamp circuit, the voltage drop across the MOSFETs would increase above the breakdown threshold bringing the device into avalanche mode with a possible failure. Using fast diodes for the output rectification instead of MOSFETs, it could measure a very high overvoltage oscillation (not clamped by internal body-drain diode).

These surges increase with the load current making it impossible to use low voltage MOSFETs for SR without a clamp circuit.

Figure 54. Overvoltage ringing on the SR MOSFETs without clamp

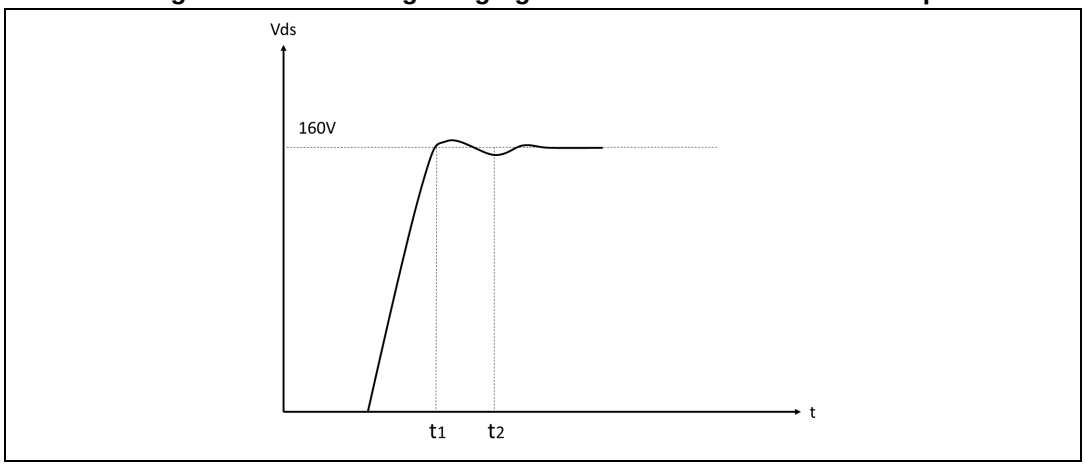


The benefit of this circuit consists of clamping the transformer secondary voltage at a value slightly higher than the reflected V_{sec}, as shown in *Figure 55*.

Equation 39

$$V_{sec} = 2 \cdot \frac{N_s}{N_p} \cdot V_{in} = 160\ V$$

Figure 55. Overvoltage ringing on the SR MOSFETs with clamp



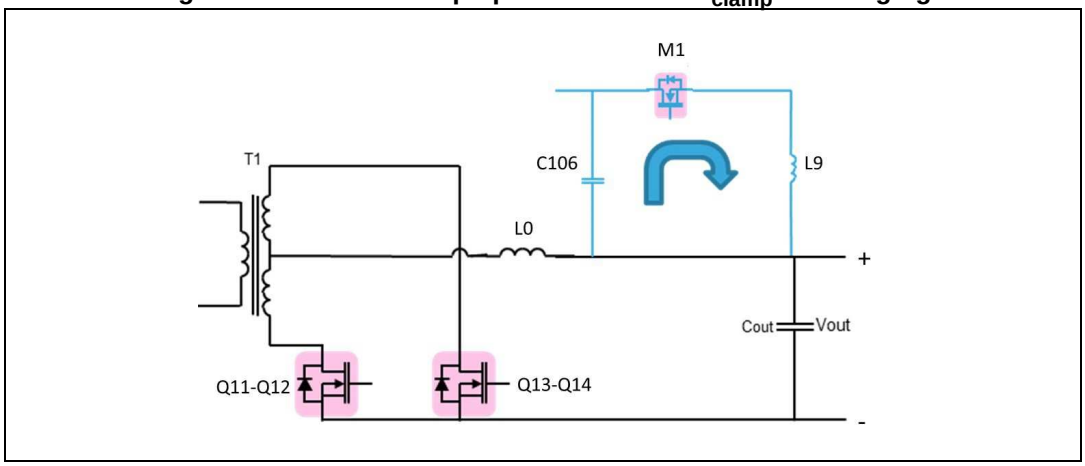
The voltage in the capacitor increases until the maximum value of V_{peak} - V_{out}.

- Operation mode 2: Clamp capacitor discharging and clamp inductor charging

During the previous phase the clamp capacitor was charged at its maximum value. However this capacitor has to be discharged before the next device turn off to clamp the overvoltage also in next PWM period.

During the time interval in which Q11-Q12 is on and V_{DS} is low, M1 is turned on by the PWM signal generated by the microcontroller, partially discharging C106 and transferring energy to L9, as shown in *Figure 56*.

Figure 56. Second clamp operation mode: C_{clamp} discharging



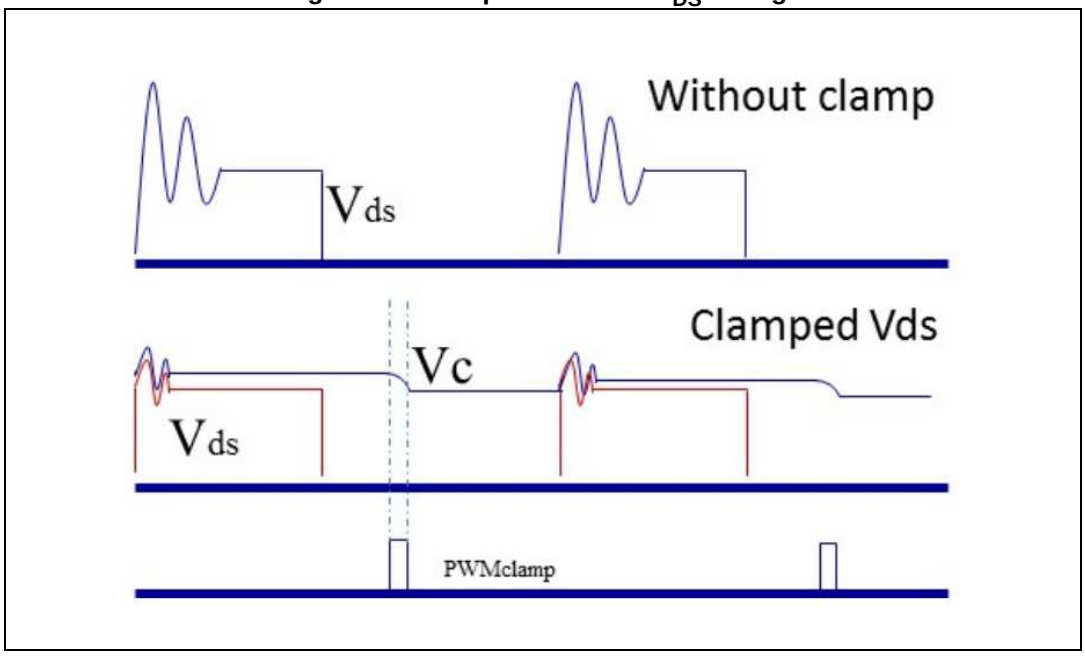
During this phase, capacitor C106 is connected in parallel to L9 forming a resonant circuit. Choosing an inductor of 220 µH and a capacitor of 3.3 µF, the resonant oscillating period is:

Equation 40

$$T_{clamp\_res} = 2\pi\sqrt{L_c C_c} = 2\pi\sqrt{3.3 \cdot 220 \cdot 10^{-12}} = 169\mu s$$

Since $T_{(clamp\_res)}$ >> T_s, where T_s is the switching period of the converter, the charging and discharging of the clamp capacitors can be considered linear. The Figure below shows the MOSFET voltage with and without the clamp circuit, together with the clamp capacitor voltage V_c.

Figure 57. Clamp benefits on V_{DS} voltage

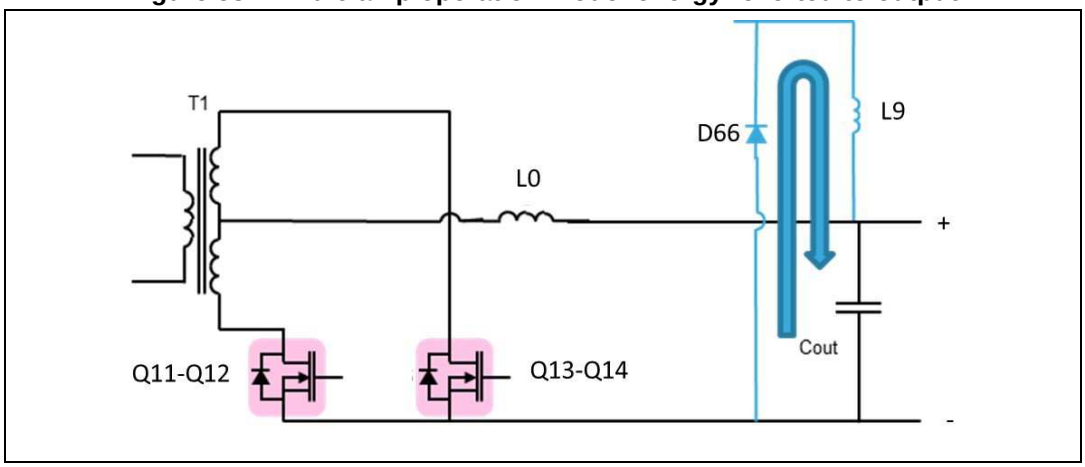


- Operation mode 3: Energy diverting to output capacitor

The voltage across C106 is controlled by the M1 gate pulse duration that is set in order to keep the voltage V_{out} + V_{C106} greater than the transformer reflected voltage V_{sec}.

The energy stored in inductor L9 can be finally diverted on the output capacitor through the D66 diode once the switch M1 is turned off.

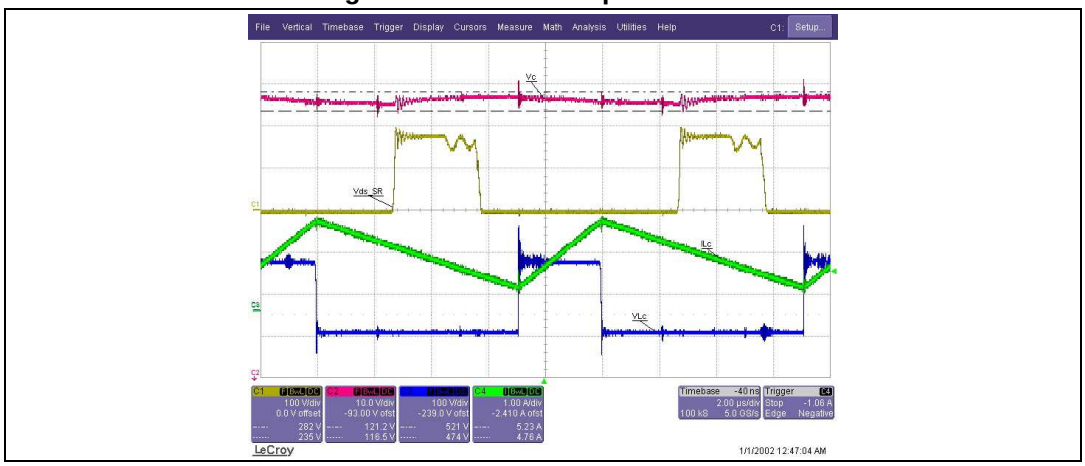
Figure 58. Third clamp operation mode: energy reverted to output



This buck converter can work in continuous or discontinuous conduction mode depending on the energy to deliver to the output before another switching period starts.

Figure 59 shows the main waveforms of interest in the active clamp process at full load.

Figure 59. Active clamp waveforms



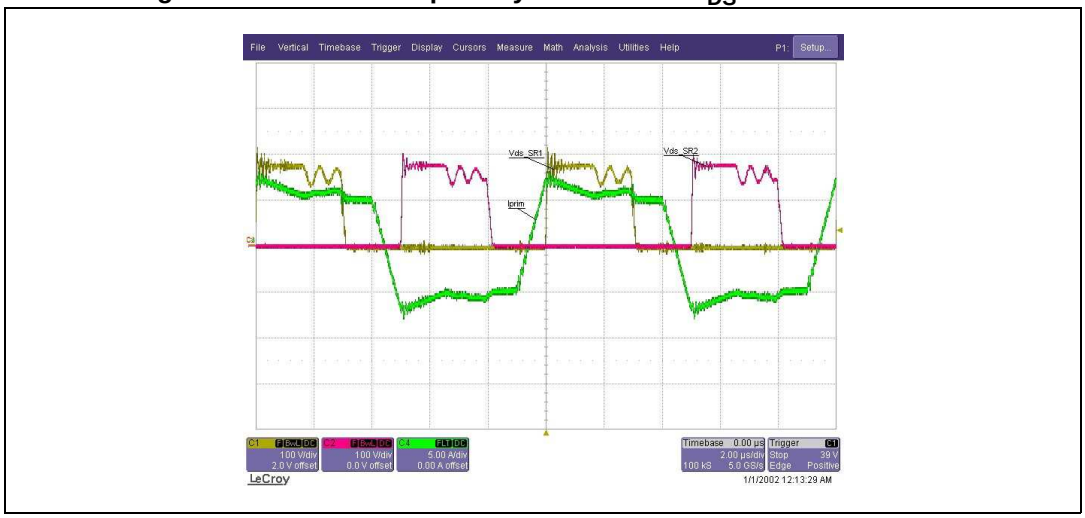
Choosing a T_{on} = 2.9 µs for the clamp MOSFET, we can see a clamp capacitor discharge of around 3.5 V during this time interval (magenta trace). When the corresponding SR MOSFET is turned off; the clamp capacitor, already charged at 121.8 V, limits the V_{DS} overvoltage (yellow trace) charging at a final value of 125.3 V, until the next clamp MOSFET turn on.

The green trace also shows the current of the clamp inductor which is charged during T_{on} of the clamp MOSFET and discharged during the remaining part of switching period.

Furthermore, the presence of the clamping circuits produces a different slope on the primary current with respect to the theory discussed up to now.

Since the clamp circuit operates as a buck converter, a certain amount of energy stored on the clamp capacitors is injected to the 48 V side. For this reason, the primary current, during the power transfer phase, has a slightly flat current shape on top and bottom, instead of positive slope as indicated In *Figure 60* (green trace).

Figure 60. Transformer primary current and V_{DS} on SR MOSFETs



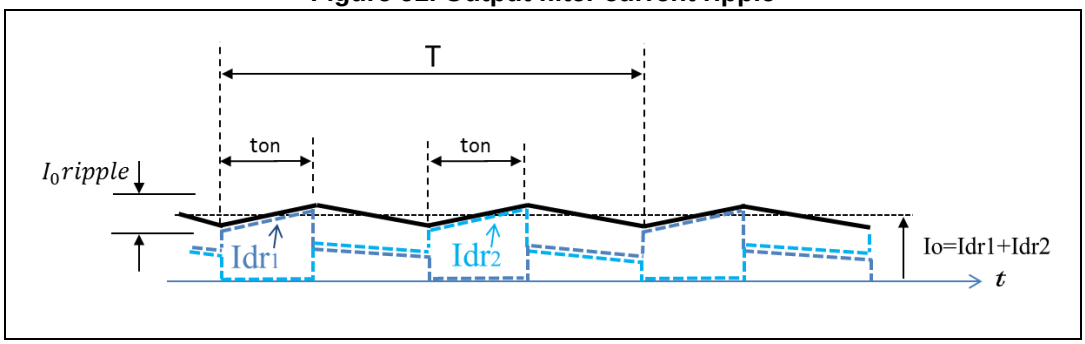
3.4.6 Output choke

Regarding the output choke, it is possible to calculate the minimum inductance L_o to be used, considering a fixed output inductor current ripple of 20%. The output current ripple I_{o_ripple} can be calculated as:

Equation 41

$$I_{o\_ripple} = \frac{P_{out\_max} \cdot ripple}{V_{out\_min}} = \frac{2000 \cdot 0.2}{45.6} = 8.77\ A$$

Figure 61. Output filter current ripple



Equation 42

$$L_{o\_min} = \frac{V_{L\_max}}{I_{o\_ripple}} \cdot t_{on}$$

Where V_{L_max} is the maximum voltage drop on output inductance (*Equation 43*) and t_{on} is the corresponding on-state time (*Equation 44*).

Equation 43

$$V_{L\_max} = \frac{N_s}{N_p} \cdot V_{in\_max} - V_{out\_min} = \left(\frac{425}{5} - 45.6\right) V = 39.4V$$

Equation 44

$$t_{on} = \delta \cdot T_s = \frac{1}{2} \cdot \frac{V_{out\_min}}{V_{in\_max}} \cdot \frac{N_p}{N_s} \cdot T_s = \frac{1}{2} \cdot \frac{45.6}{425} \cdot 5 \cdot 10^{-5} \cong 2.68\mu s$$

Where $\delta = t_{on}/T_S$ with $0<\delta<0.5$.

Substituting *Equation 43* and *Equation 44* in *Equation 42* it is possible to calculate the minimum output inductance value:

Equation 45

$$L_{o\_min} = \frac{V_{L\_max}}{I_{o\_ripple}} \cdot t_{on} \cong 12.05\ \mu H$$

A type R40 AL81 Megaflux FS157060-2 15 µH, ARNOLD CSC powder core inductor has been selected.

3.4.7 Output capacitor

The output capacitor has been designed to satisfy the maximum load transient:

Equation 46

$$t_{transient} = \frac{P_{out} \cdot L_{o\_min} \cdot 0.9}{V_{out\ min}{}^2} = \frac{2000 \cdot 15 \cdot 10^{-6} \cdot 0.9}{45.6^2} = 12.96 \mu S$$

Which represents the time required by the output inductor to change the 90% of the full current variation.

Then the C_{out} is calculated to satisfy the capacitance definition: $I=C\ \Delta V_c/\Delta t$, where Δt is the $t_{transient}$ time, and ΔV_c is considered as 10% of the maximum allowable output ripple:

Equation 47

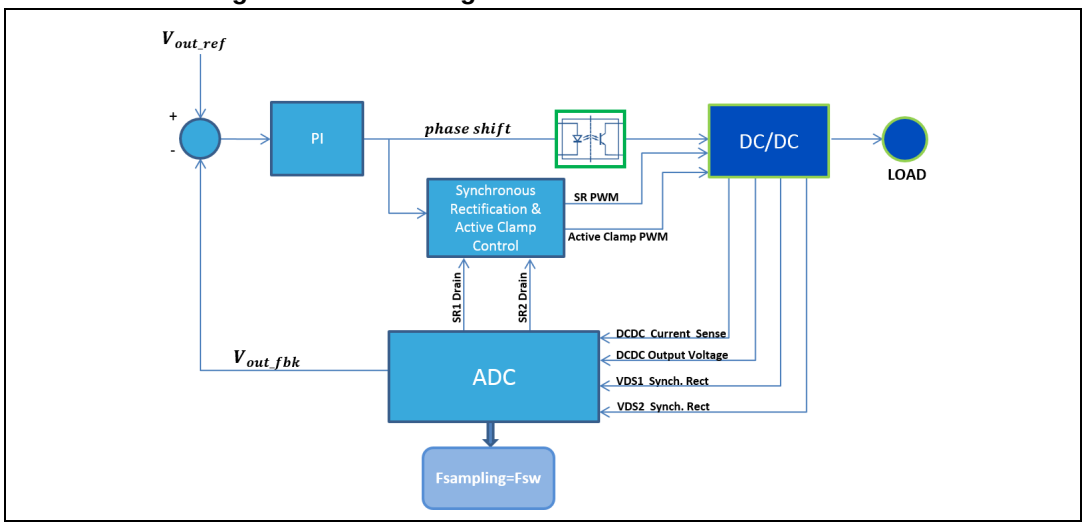
$$C_{out} \geq \frac{\Delta I_c}{10\% \frac{\Delta V_c}{\Delta t}} = \frac{\frac{P_{out} \cdot 0.9}{V_{out\_min}}}{\frac{0.1 \cdot V_{ripple}}{t_{trans}}} = \frac{\frac{2000 \cdot 0.9}{45.6}}{\frac{0.1 \cdot 2.4}{12.96 \cdot 10^{-6}}} = 1957 \mu F$$

Finally six 470 µF, 63 V capacitors have been chosen.

3.5 DC-DC converter firmware and control algorithm overview

The DC-DC control firmware is implemented on the secondary MCU, which is the STM32F334x, and thus the same microcontroller used for iPFC. The chosen switching frequency is 100 kHz. This allows to use the HRTIM with the maximum resolution of 217 ps. The control algorithm is based on a simple voltage loop realized with a traditional PI regulator. The HRTIM drives gate signals for both primary and secondary side MOSFETs in order to regulate the output voltage at 48 V DC. Full bridge topology is controlled with phase-shift modulation achieving ZVS. The two switches of the same leg are driven with two complementary signals with a fixed duty cycle of 50% and a proper dead time, while considering the two high sides (or low sides), the signals are phase shifted by an angle imposed through the control loop executed at 50 kHz. The complete control loop scheme is shown in *Figure 62*.

Figure 62. Block diagram of DC-DC converter control



HRTIM generates PWM signals also for the push-pull stage, in order to implement synchronous rectification (SR) minimizing conduction losses, and for active clamp driving, in order to clamp voltage spikes on the output MOSFETs due to energy stored in transformer leakage inductance during turn-off of switches.

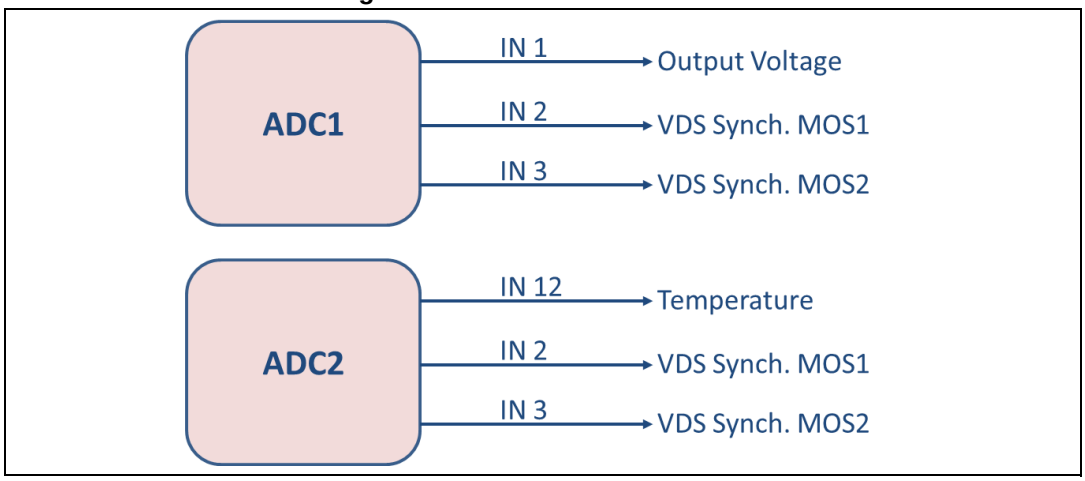
The HRTIM is configured as follows:

- The master timer is used to trigger ADC1 and ADC2 and for synchronization of Timer A, B, C and D
- Timer B and timer C are used for primary full-bridge modulation
- Timer D is used for secondary synchronous rectification
- Timer A is used for active clamp signals

Timer B is configured in half mode driving CHB1 and CHB2 outputs (first leg of full-bridge topology) with a couple of fixed PWMs. Timer C outputs, CHC1 and CHC2, have rising and falling edges phase-shifted compared to CHB1 and CHB2 and drive the second leg of full-bridge topology. Timer D outputs, CHD1 and CHD2, are used to generate the two synchronous rectification MOSFET modulation signals.

The ON and OFF time of these signals depends on the phase shift imposed by the control loop, then rising and falling edges are chosen properly to assure the power-on of the MOSFETs only when the respective diode is conducting. The system is also designed to perform a dynamic variation of these edges depending on the drain-to-source voltage of the synchronous rectification MOSFETs. These voltages can be acquired by two 5 MHz ADC converters, namely ADC1 and ADC2, with one or two injected acquisitions for ADC at each rising or falling edge. Output voltage and heatsink temperature are acquired with two regular acquisitions and DMA transfer. The utilization of the two A/D converters is shown in *Figure 63*.

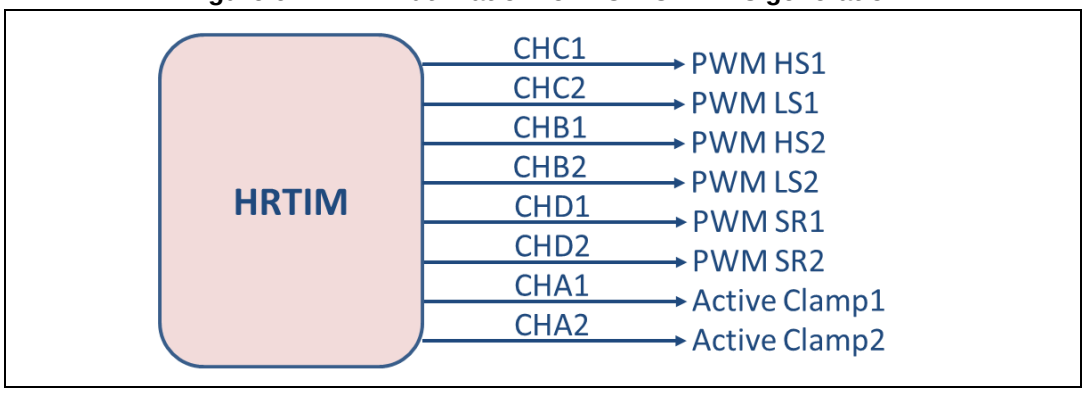
Figure 63. DC-DC ADC utilization



HRTIM also provides pulse signals to drive active clamp MOSFETs in order to partially discharge clamp capacitors diverting this extra energy to the output stage. These pulses have a constant on time and are synchronized with SR signals, discharging the two capacitors when the respective MOSFET is turned on.

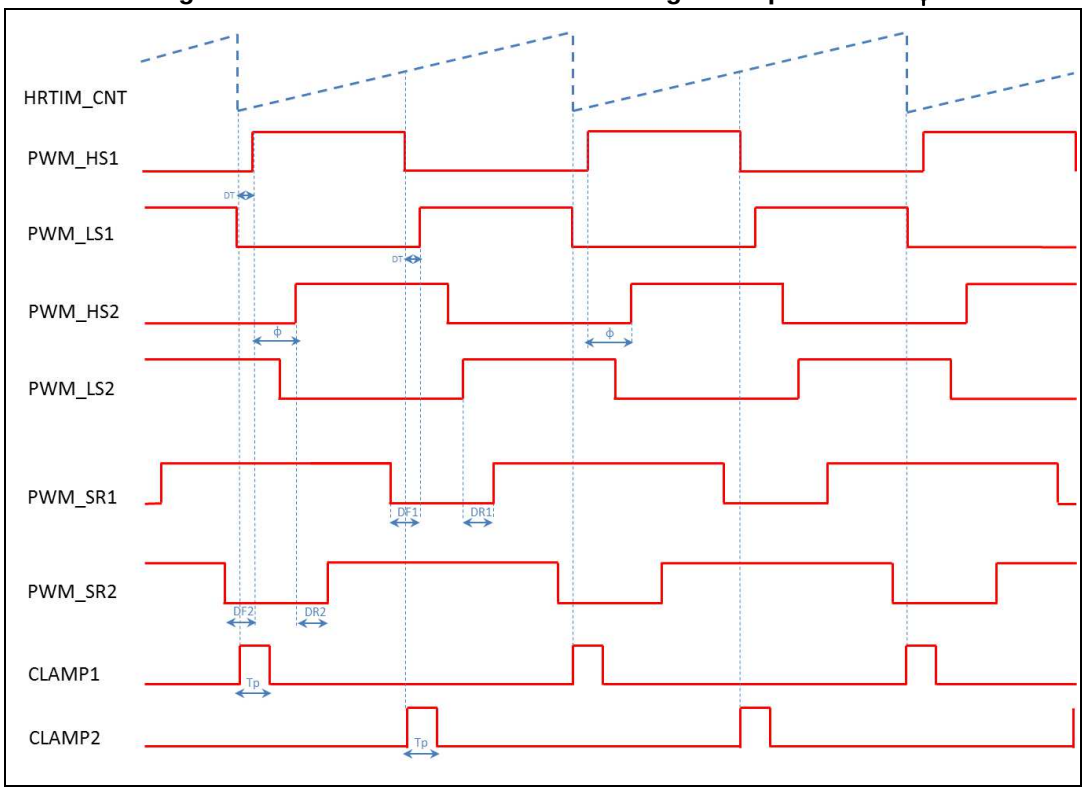
The utilization of HRTIM for PWMs generation is shown in *Figure 64*.

Figure 64. HRTIM utilization for DC-DC PWMs generation



The diagram that follows shows an example of PWM signal generation for a generic phase shift value. This representation includes also SR and active clamp waveforms.

Figure 65. DC-DC PWM waveforms for a generic phase shift φ



The control logic of DC-DC firmware is based on a state machine similar to the PFC one. At power-on of the secondary microcontroller, all peripherals used (HRTIM, ADCs, DAC, UART and COMP) are initialized and the actual state is set at DCDC_IDLE state. When the PFC completes the startup procedure, a specific flag in periodic communication message from the primary to secondary MCU is asserted. As soon as the DC-DC microcontroller receives a message in which the correct regulation of DC bus voltage is confirmed, the DCDC_INIT state is set in which control variables are reinitialized at default values and PWM outputs (full bridge and active clamp) are enabled. Afterwards, in DCDC_START state, a voltage reference ramp-up is performed until the output voltage reaches the reference value of 48 V DC. When this condition is satisfied, the new state is DCDC_RUN until a fault event occurs. During ramp-up or normal operation, the SR is enabled only in presence of a minimum load (phase shift value greater than a default threshold) corresponding at 7 A, and is disabled for loads lower than 4.6 A.

The possible faults for DC-DC are:

- Output undervoltage (short-circuit) (V_{out} < 34 V DC)
- Output overvoltage (V_{out} > 58 V DC)
- Output overcurrent (I_{out} > 43 A)
- Overtemperature (heatsink temperature > 56 °C)

When at least one of these conditions is present, the new state is DCDC_STOP, in which PWM outputs are disabled, and then the new state is DCDC_FAULT.

The output overcurrent protection feature is achieved using internal comparator COMP2. The non-inverting input of comparator is connected to the output of the full bridge sense circuit used to measure DC-DC converter primary current, whereas the inverting input of comparator is internally connected to CH1 of DAC1 in which the overcurrent threshold is

programmed. When the sensed current is higher than the preset threshold, the rising edge of the comparator output triggers the HRTIM fault event and PWM are set in idle state. A specific interrupt is generated to set the state machine in DCDC_STOP state.

In addition to the previous cases, a PFC error (communicated via UART) also causes the DC-DC stop conversion. Like PFC state machine, if all fault conditions disappear, the system is in DCDC_WAIT state for 2 seconds before returning in DCDC_IDLE state and accepting a new restart command from primary MCU. A user LED blinking displays the kind of error occurred with a codification reported in *Table 8*.

Table 8. DC-DC error codes

Fault	Error code	Number of LED blinks
DCDC_NO_ERROR	0x0000	-
DCDC_OUT_OVER_VOLT	0x0002	2
DCDC_SHORT_CIRCUIT	0x0004	3
DCDC_OVER_CURRENT	0x0008	4
DCDC_OVER_TEMP	0x0010	5
DCDC_RECEIVED_ERROR	0x0012	6

The complete DC-DC state machine is shown in *Figure 66*, while main tasks are reported in *Table 9*.

Figure 66. DC-DC state machine

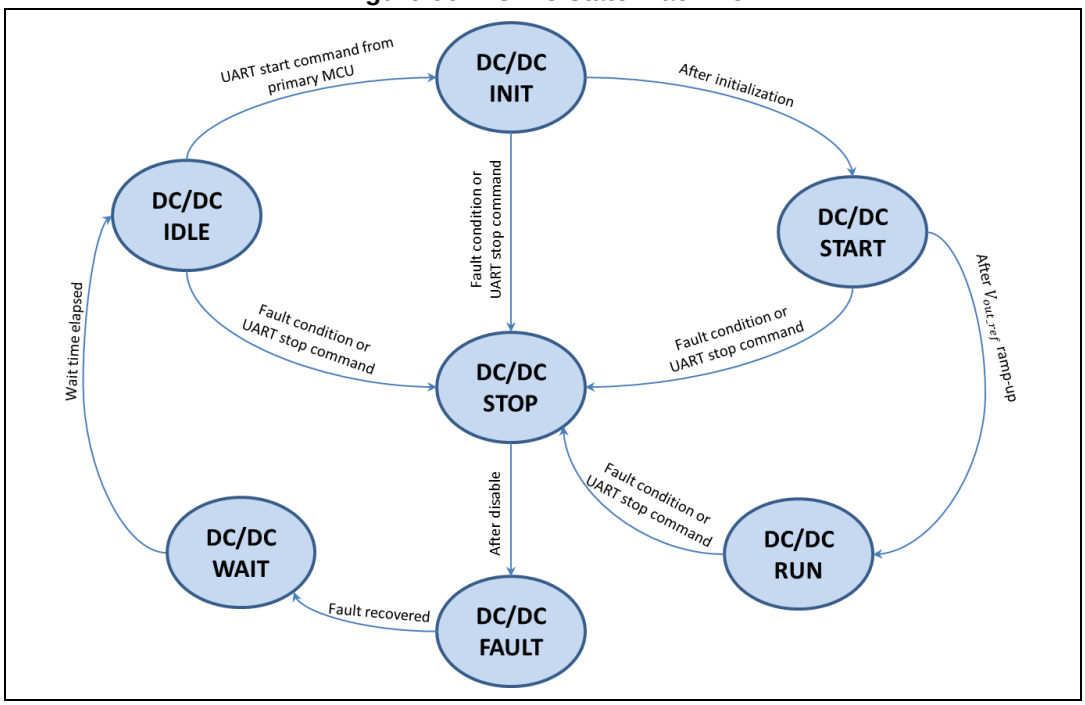


Table 9. Function names and tasks of the DC-DC firmware

Function	Task	Execution frequency	Priority
HRTIM1_TIMC_IRQHandler()	Voltage control loop Synchronous rectification Active clamp Burst mode	50 kHz	High
HRTIM1_FLT_IRQHandler()	Output short-circuit protection	Comparator trigger	Very high
USARTx_DMA_RX_IRQHandler()	Acquisition of PFC status	On acquisition	Medium
main()	Fault checks State machine Serial communication LED	-	Low

As for PFC, also in DC-DC control algorithm burst mode operation is implemented for light load management. When enabled, the HRTIM burst mode controller sets in IDLE state the PWM outputs. The burst mode is disabled when the output voltage is lower than the defined threshold.

3.6 Synchronous rectifier MOSFETs (SR)

The conduction losses of the output rectifier stage contribute significantly to overall efficiency of the DC-DC FB converter.

If simple diodes are used for the output stage, the conduction losses are proportional to the product of the diode voltage drop V_F and the forward conduction current I_F. Therefore, to improve the efficiency of the DC-DC, the synchronous rectification (SR) technique was adopted. It consists of replacing the output diodes with active switches; in this manner, when the switch is on, the current flows through the MOSFET's channel, which offers a low impedance path, instead of the body diode, then the conduction losses are the same of those of a resistance equal to $R_{DS(on)}$.

A drawback of this technique is that the microcontroller has to know when the MOSFET's body diode starts to conduct and then turn on the corresponding switch. To avoid output short-circuit, a delay time has to be considered between the beginning of diode conduction and the command given to the MOSFET gate.

It is important to optimize this delay time, which can be different for rising and falling edges of the two switches, in order to minimize diode conduction and improve efficiency.

A way to perform this optimization is by adopting an adaptive algorithm in which the microcontroller changes these delays recursively considering the acquired measurement of V_{DS} during turn-on and turn-off of the MOSFETs.

Another way to set the proper delays is by measuring the DC-DC efficiency and then increasing or decreasing the MOSFET's on time considering that the edges of the gate signal should not be too close to those of V_{DS} to avoid cross conduction.

This operation should be done at minimum load in which the synchronous rectification is activated (for low loads the V_{DS} of SR MOSFETs presents several oscillations, as shown in *Figure 67*), because the rising edge of V_{DS} shifts in the right direction increasing the load; this means that if the optimization is done at high load value, when the load is decreased a shift of V_{DS} in the left direction will happen causing a V_{GS} and V_{DS} overlap with a possible destruction of device.

Figure 67. V_{DS} of a SR MOSFET for very low loads (device not driven)

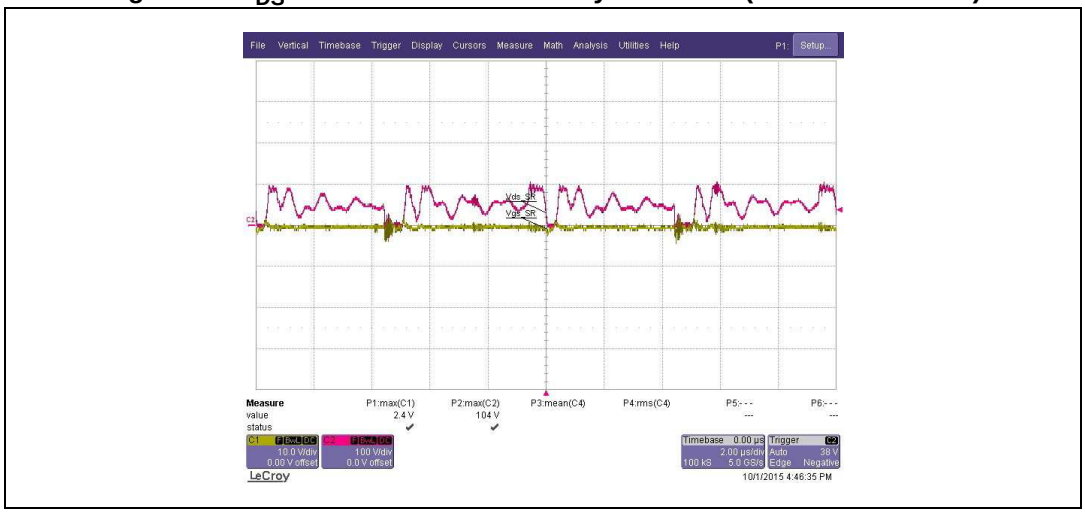


Figure 68 and *Figure 69* show an example in which the delays of SR are not optimized and another in which these delays are optimized.

Figure 68. SR without optimized delays

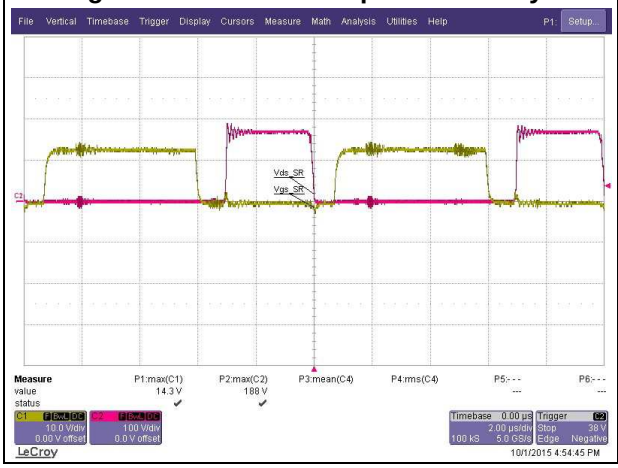
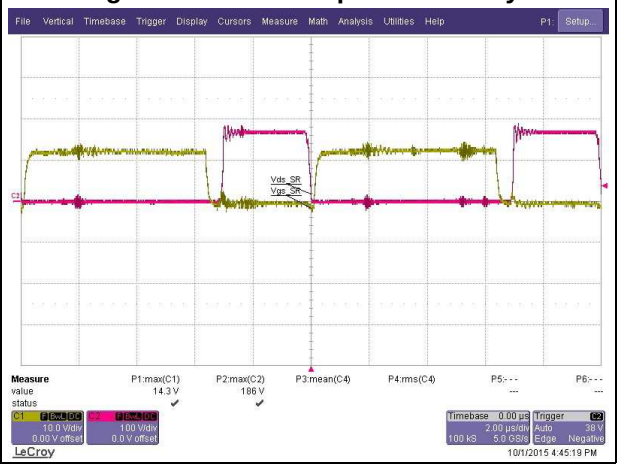


Figure 69. SR with optimized delays



Note: Be careful that if the devices in the full bridge (Q1-Q4) are changed with other types, all the delays for the four edges of SR are to be re-tuned to avoid output short-circuits and to prevent high currents flowing through the switches. The same consideration should be given if the MOSFETs of the SR are changed with other types.

3.7 DC-DC experimental characterization

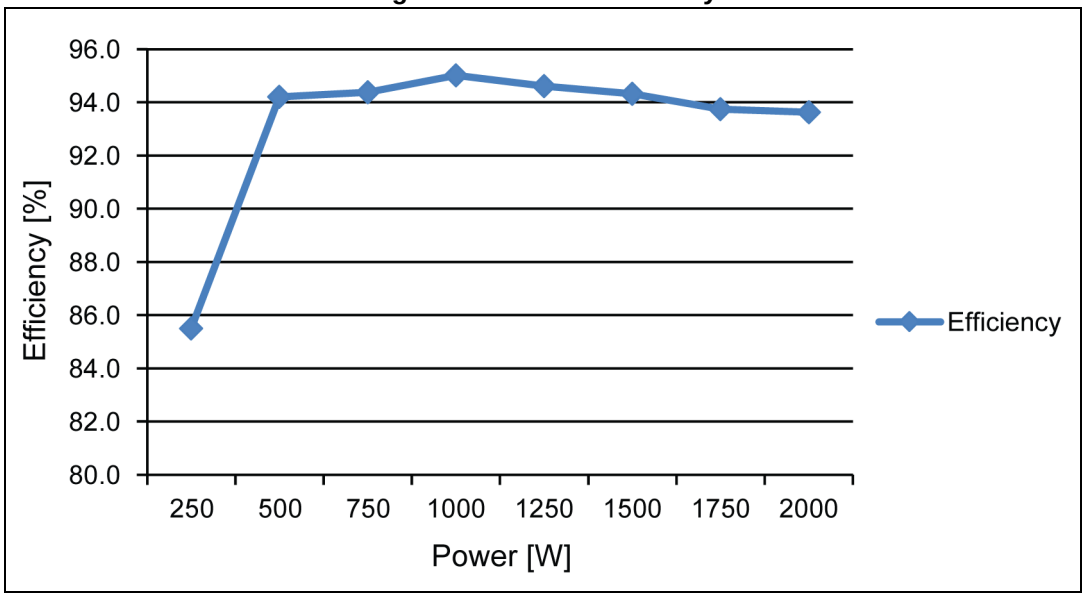
The efficiency was measured in the following conditions:

1. The board was supplied with Magna Power Electronics 600 V/24 A power supply.
2. The DC-DC output was connected to H&H 60 V/750 A ZS Electronic Load set in continuous current.
3. The input and output voltages were measured directly at the input and output connectors of the DC-DC section.
4. The power measurements do not take into account the power consumption of the fans.
5. The auxiliary power supply consumption is included.
6. The board was tested at an ambient temperature of 25 °C.
7. For DC-DC, DPS 2 kW - Secondary DC-DC STM32F334x v2.3 firmware was used.

Table 10. Test results for DC-DC phase shift

V_{IN} (V)	I_{IN} (A)	P_{IN} (W)	V_{OUT} (V)	I_{OUT} (A)	P_{OUT} (W)	Efficiency (%)
401.1	0.66	265	48.16	4.7	226.35	85.5
401	1.49	597	48.11	11.7	562.89	94.2
400.9	1.92	770	48.11	15.1	726.46	94.4
400	2.48	992	48.09	19.6	942.56	95.0
400.7	3.19	1278	47.99	25.2	1209.35	94.6
400.6	3.85	1542	48.01	30.3	1454.70	94.3
400.4	4.82	1930	47.99	37.7	1809.22	93.7
400.4	5.19	2078	47.92	40.6	1945.55	93.6

Figure 70. DC-DC efficiency



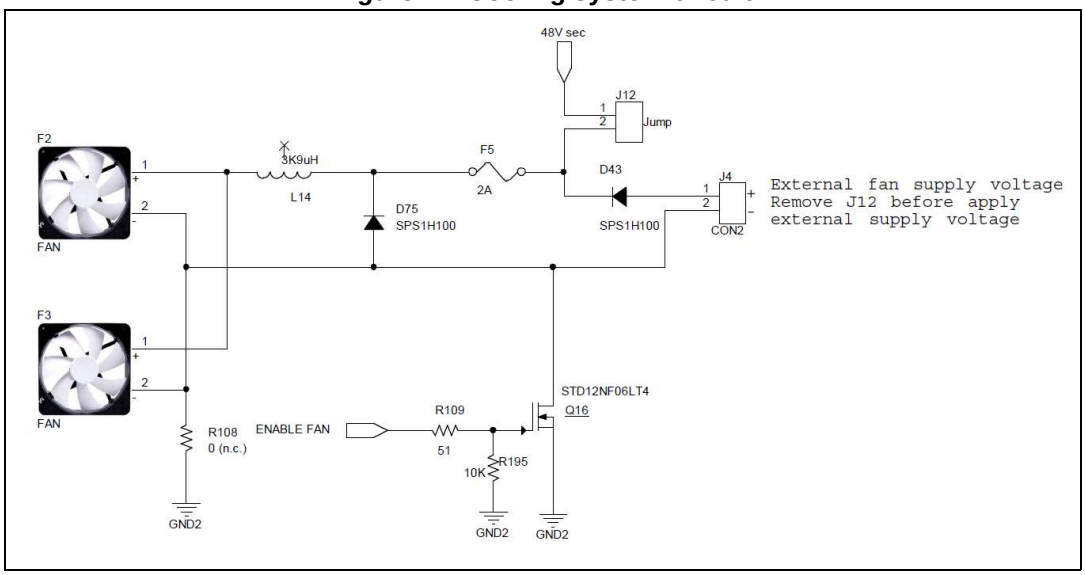
4 Cooling system

The STEVAL-ISA172V2 evaluation board is provided with a forced air cooling system composed of two 48 V fans in order to dissipate the heat from the heatsinks and from the transformer.

The circuit can be supplied directly from 48 V output or externally, excluding the consumption of the fans in efficiency measurements.

To improve system efficiency and reduce acoustical noise at light loads, the speed of the fans is controlled according to the power delivered. A dedicated step-down circuit has been inserted on the board to reduce the voltage applied on the two fans. *Figure 71* shows the driving circuit of the fans.

Figure 71. Cooling system circuit



The speed regulation is obtained by controlling the duty cycle applied to MOSFET Q16 which can assume, with hysteresis control, three different values depending on the output power supplied by the AC-DC converter.

5 Board characterization

The overall efficiency of the board was measured in the following conditions:

1. The board was supplied with Adaptive Power System APS-3000 power supply.
2. The DC-DC output was connected to H&H 60 V/750 A ZS Electronic Load set in continuous current.
3. The input and output voltages and currents were measured directly at the input and output connectors of the board using Voltech PM6000 Universal Power Analyzer power meter.
4. For efficiency computation, measurements of the input and output powers given by the power meter were used directly.
5. The power measurements do not take into account the power consumption of the fans.
6. The auxiliary power supply consumption is included (PFC and DC-DC drivers and both microcontrollers).
7. The board was tested at an ambient temperature of 25 °C.
8. For PFC and DC-DC, the firmware used was DPS 2kW - Primary PFC STM32F334x v2.2 and DPS 2 kW - Secondary DC-DC STM32F334x v2.3, respectively.

Table 11. Board test results for 120 V AC input operation

V_{IN} (Vrms)	I_{IN} (Arms)	P_{IN} (W)	V_{OUT} (V)	I_{OUT} (A)	P_{OUT} (W)	Efficiency (%)	PF
119.33	2.11	245	48	4	192.0	78.4	0.9885
118.86	4.7	560	48	10.2	489.6	87.4	0.9993
118.54	6.4	758	48	14.1	676.8	89.3	0.9971
118	8.67	1016	48	19	912.0	89.8	0.9978
117	10.56	1240	48	23.1	1108.8	89.4	0.9974
117	12.6	1496	47.9	27.9	1336.4	89.3	0.9977
116.7	15	1753	47.9	32.6	1561.5	89.1	0.9983
116.3	17.5	2033	47.8	37.6	1797.3	88.4	0.9999

Table 12. Board test results for 230 V AC input operation

V_{IN} (Vrms)	I_{IN} (Arms)	P_{IN} (W)	V_{OUT} (V)	I_{OUT} (A)	P_{OUT} (W)	Efficiency (%)	PF
229.8	1.11	253	48	4.2	201.6	79.7	0.998
229.5	2.25	517	48	9.6	460.8	89.1	0.998
229.3	3.1	702	48	13.3	638.4	90.9	0.999
229	4.4	1018	48	19.5	936.0	91.9	0.999
228.7	6.24	1432	47.8	27.5	1314.5	91.8	0.999
228.4	7.7	1746	47.9	33.3	1595.1	91.4	0.999

6 Conclusion

This application note describes the design procedure and the working principle of a 2 kW fully digital switch mode power supply evaluation board. The system is based on a two-stage architecture consisting of an interleaved PFC circuit and a DC-DC full-bridge DC-DC stage with synchronous rectification and a special active clamp circuit digitally controlled. The control architecture is designed around two 32-bit MCUs from the STM32 family of microcontrollers. The control algorithm for both the PFC and the DC-DC FB phase shift converters is highlighted throughout the document. The experimental evaluation shows that high efficiency, near unity power factor, and low THD% can be achieved under wide input voltage and load current conditions thanks to the performance of the ST products used and to the implementation of suitable control strategies on high-performance 32-bit F334 microcontrollers.

Appendix A Schematic diagrams

Figure 72. STEVAL-ISA172V2 circuit schematic: input section and EMI filter

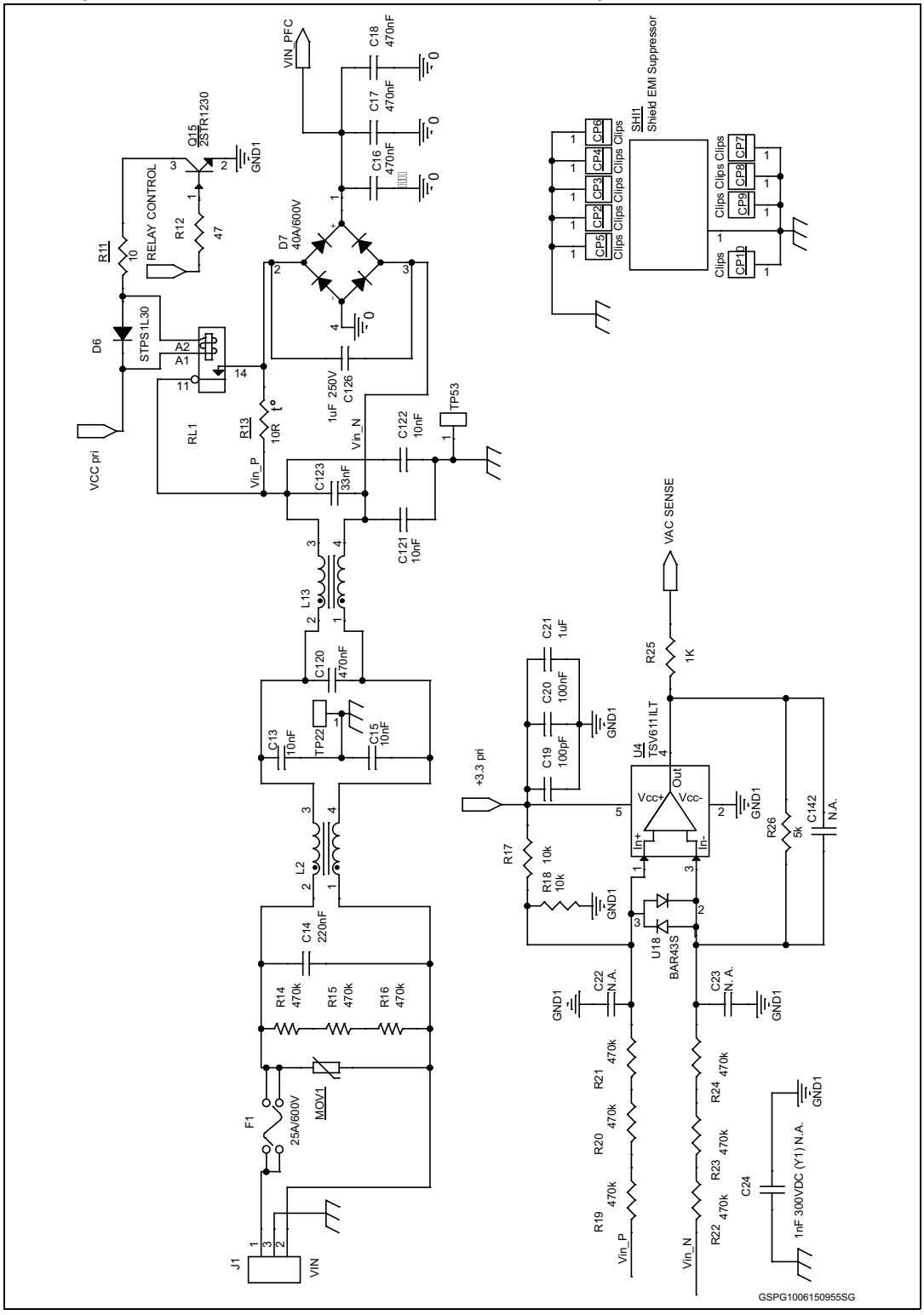


Figure 73. STEVAL-ISA172V2 circuit schematic: interleaved PFC

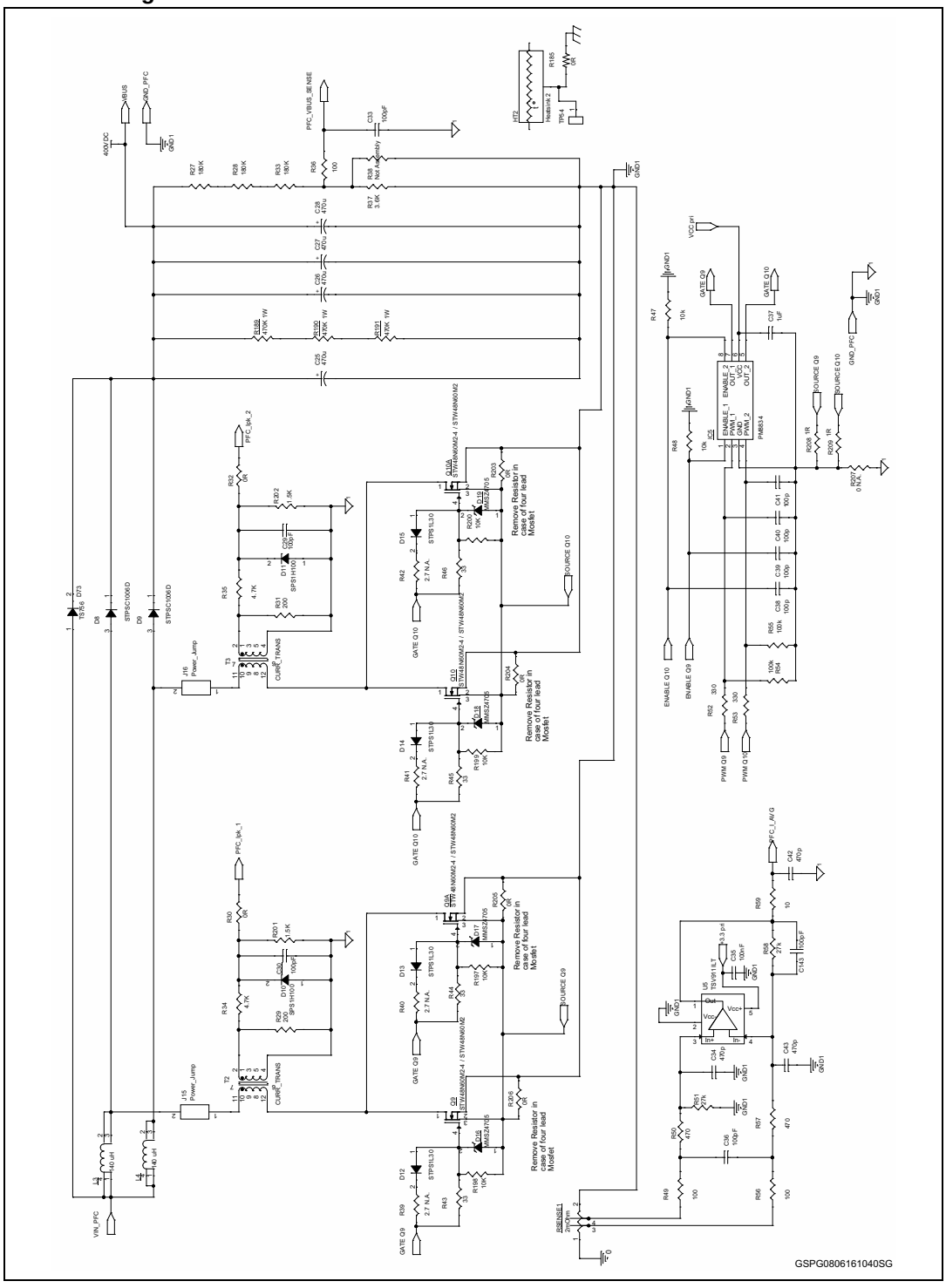


Figure 74. STEVAL-ISA172V2 circuit schematic: phase shift DC-DC converter

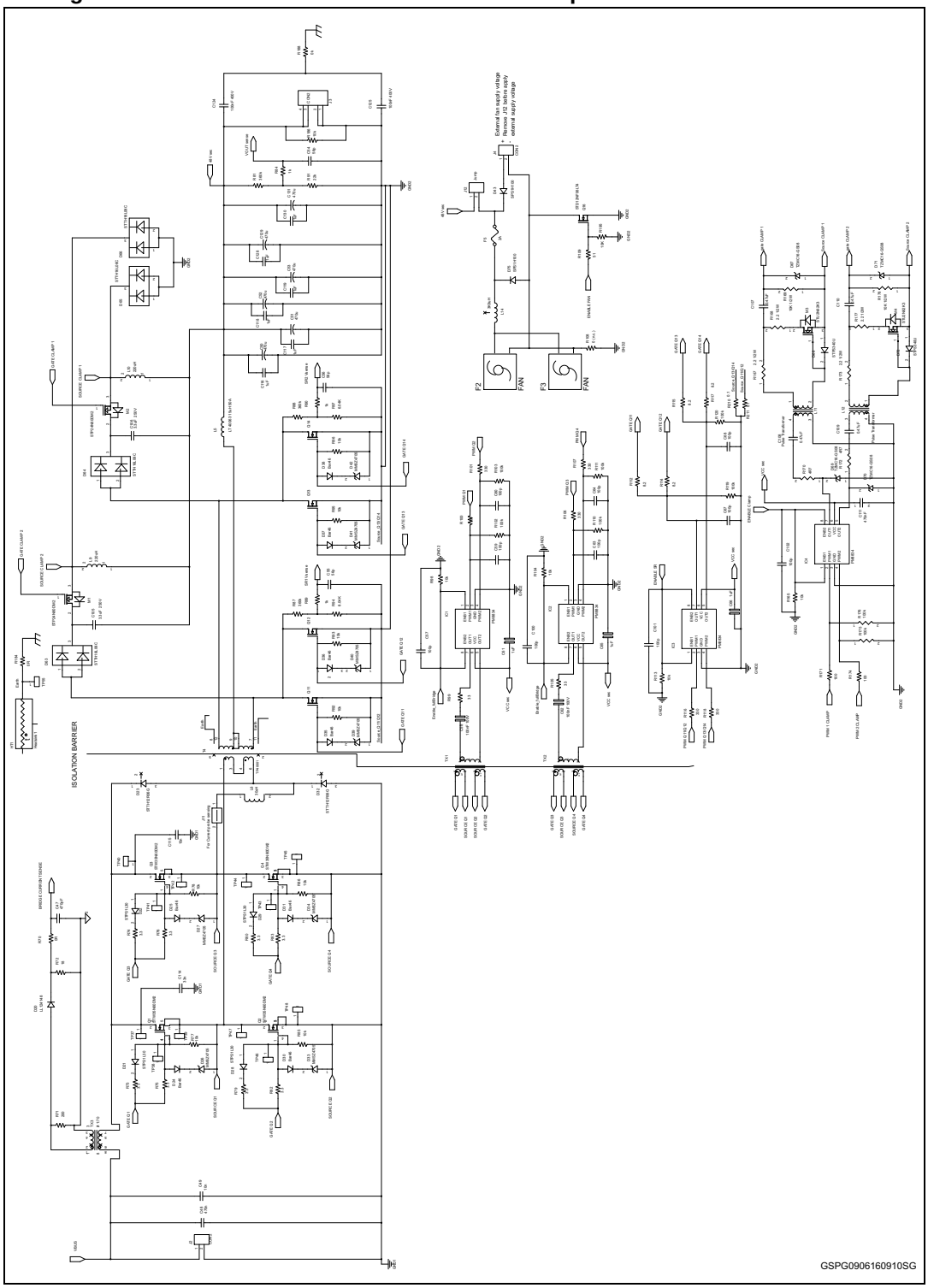


Figure 75. STEVAL-ISA172V2 circuit schematic: primary MCU

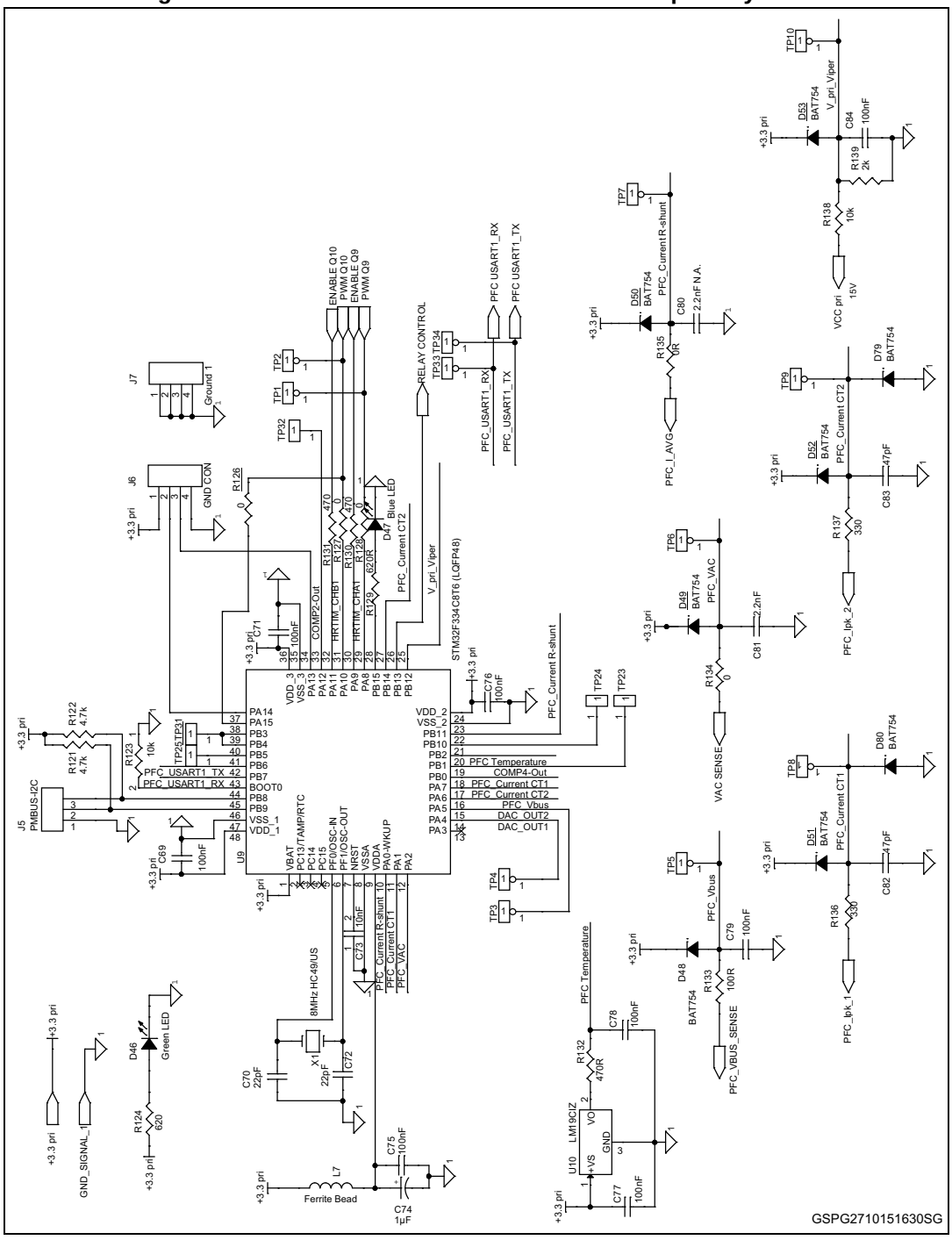


Figure 76. STEVAL-ISA172V2 circuit schematic: secondary MCU

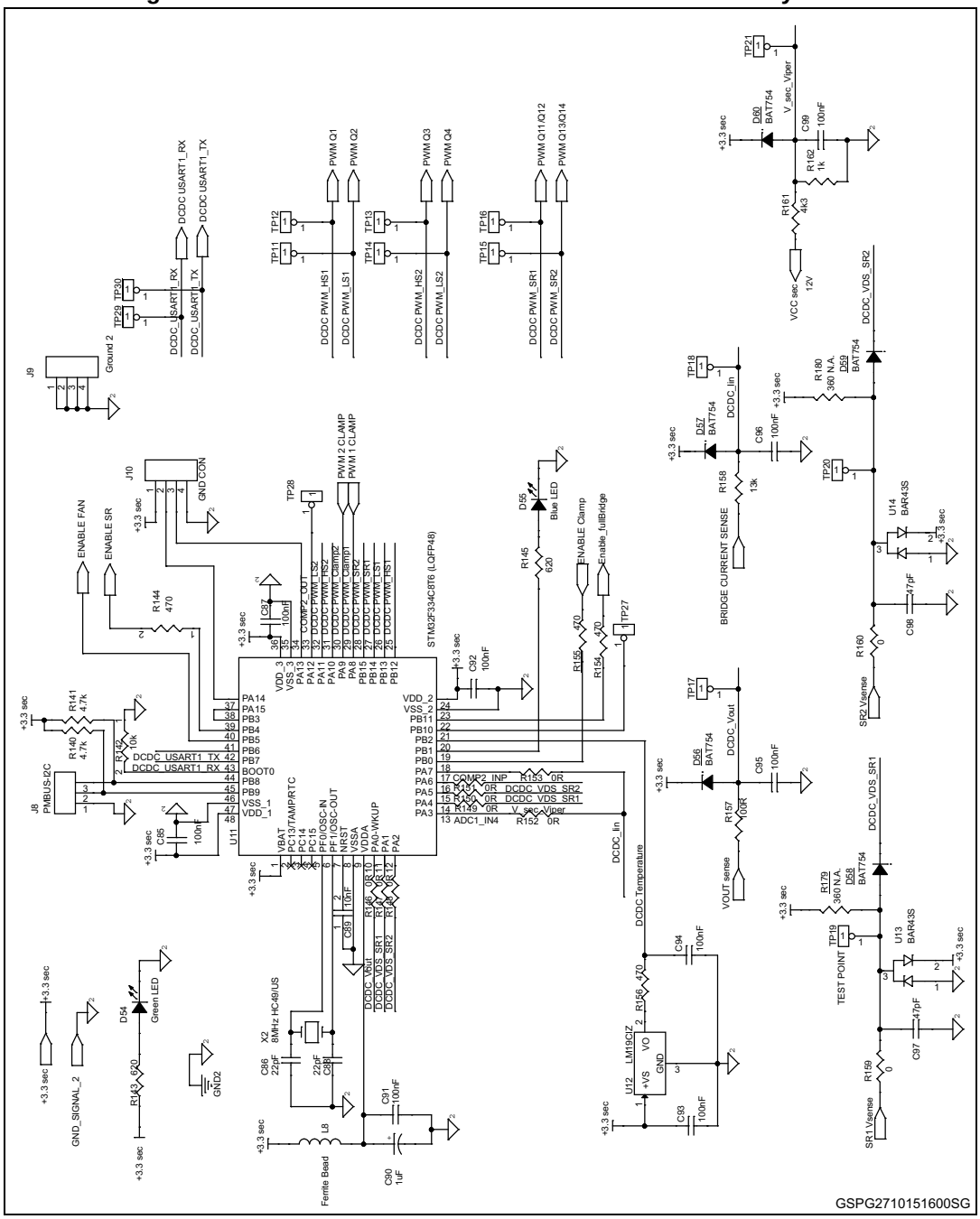


Figure 77. STEVAL-ISA172V2 opto-isolated communications

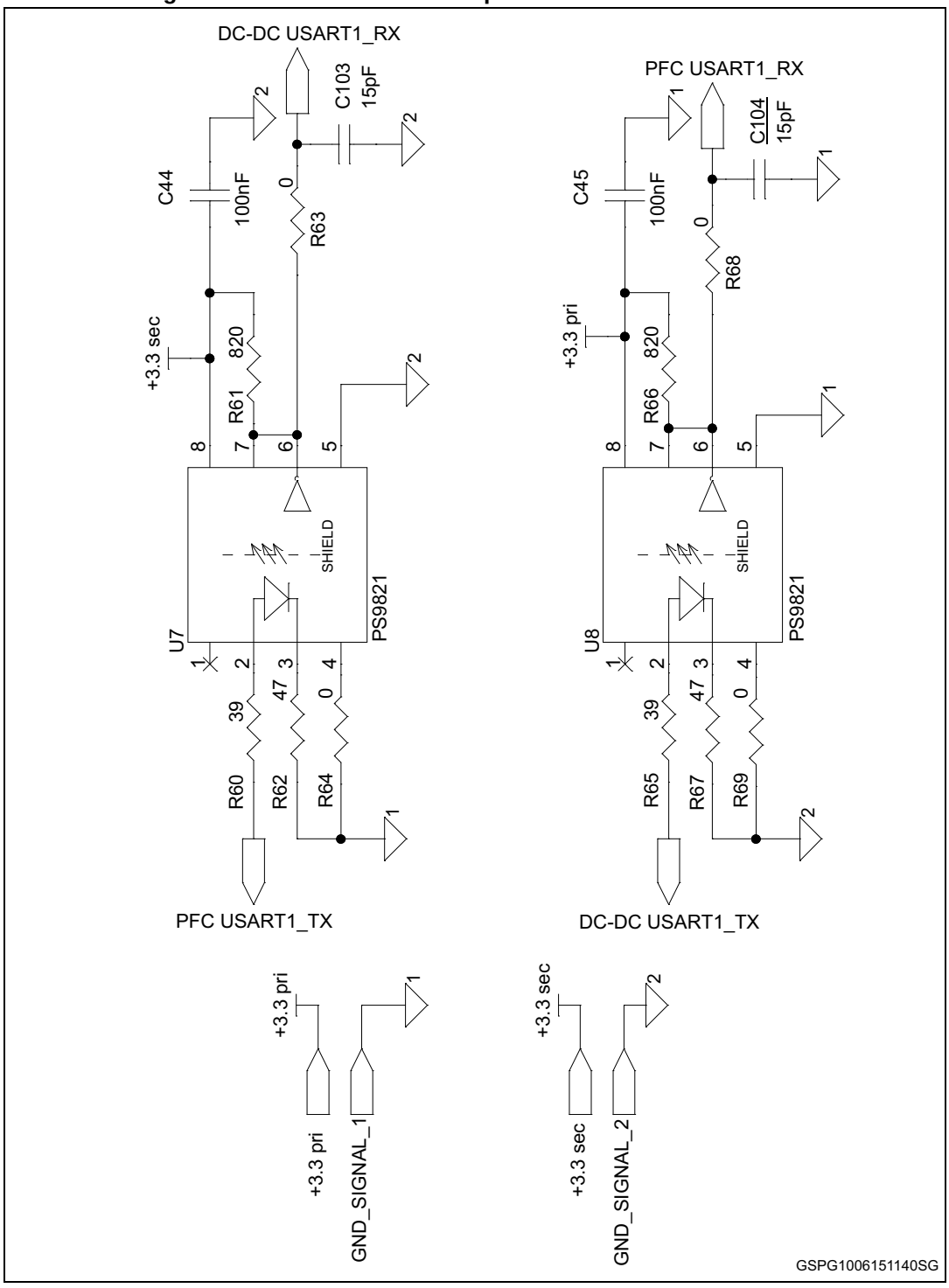
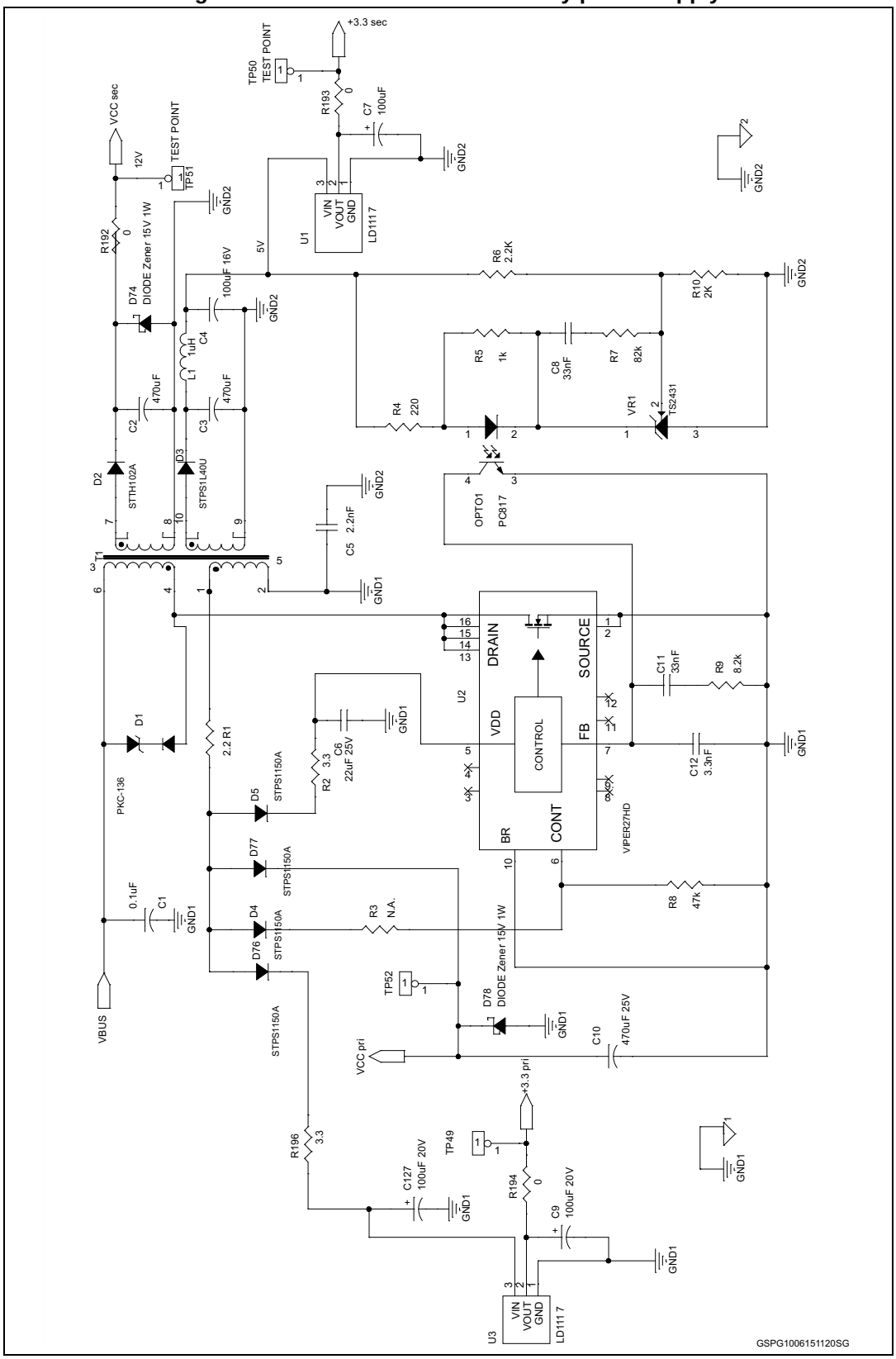


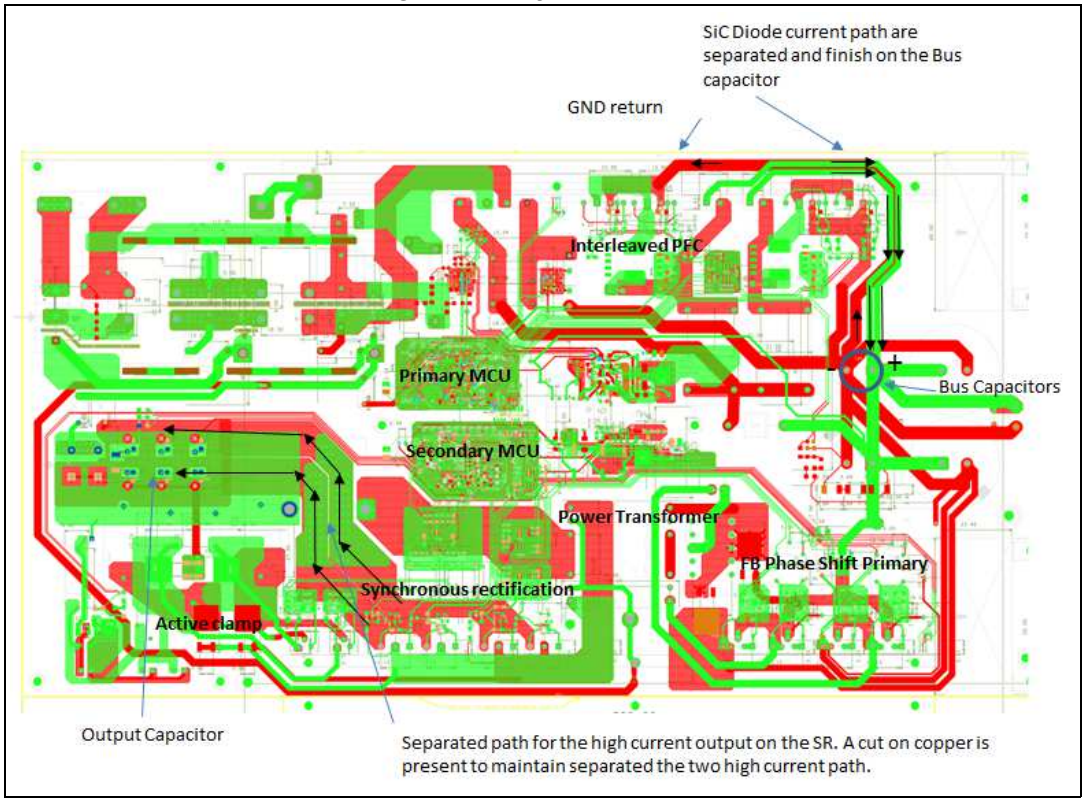
Figure 78. STEVAL-ISA172V2 auxiliary power supply



7 Layout considerations

Special attention and several precautions have been taken during the layout design. The high-current paths have been identified and maintained away from signal paths. A special precaution has been to keep the current paths separate of the two interleaved boost converters (output of the silicon carbide diodes) until the positive pin of the bus capacitors, with the benefit of avoiding shared current between the two diodes. Moreover the send and return PFC path is designed to be on top and bottom copper track to minimize the loop, thus minimizing the parasitic inductance and EMI, as shown in *Figure 79*.

Figure 79. Layout overview



Similarly, the high output current path coming from each synchronous rectification MOSFET is maintained separated individually, minimizing spikes due to the shared current on the SR rectification (*Figure 79* on the left).

Special attention has been given to the sensing signals that reach the primary microcontroller. In particular, on the sensing signals from the two measuring current transformers of the PFC MOSFETs. These two signals being away from the ADC inputs, they can be effected by noise. For this reason, the farther of the two signals is served by a shielded cable up to the microcontroller input, to ensure a clean signal on the input pin.

8 Bill of materials

The bill of materials is available on www.st.com as well as the documentation. Connect to http://www.st.com/web/catalog/tools/FM116/CL2207/SC1079/PF261873 keyword to download it.

9 References

– AN4468 application note: 500 W fully digital AC-DC power supply based on the STM32F334 microcontroller.

– Design Guidelines for Interleaved Single-Phase Boost PFC Circuits Thomas Nussbaumer, Member, IEEE, Klaus Raggl, Member, IEEE, and Johann W. Kolar, Senior Member, IEEE.TRANSACTIONS ON INDUSTRIAL ELECTRONICS, VOL. 56, NO. 7, JULY 2009

10 Warning

The DC-DC converter must be handled very carefully, as high potential (energy) parts could be open during test, assembly phase and can be touched. The user MUST avoid connecting or removing cables during operation, or touching any part of the system when it is connected to the input power supply or battery.

Note: After turning the converter off, the DC-link capacitor may still hold voltage for several minutes.

11 Revision history

Table 13. Document revision history

Date	Revision	Changes
14-Jul-2016	1	Initial release.

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