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SDP Breakout Board User Guide

INTRODUCTION

This user guide is written for system engineers who use the system demonstration platform (SDP); it discusses how to use the SDP breakout board when designing SDP-compatible hardware and software.

The ADZS-BRKOUT-EX3 SDP breakout board from Analog Devices, Inc., can be used in conjunction with SDP controller boards and daughter boards designed on the SDP system. The breakout board allows signals travelling between SDP controller boards and compatible daughter boards to be monitored by the insertion of the breakout board between the SDP controller board and the daughter board.

SDP controller boards are used as part of the evaluation system for many Analog Devices components. The SDP breakout board exposes each of the 120 pins of the SDP controller board's connector allowing users to monitor signals between the controlling board and the attached daughter evaluation board or Circuit from the Lab™ reference circuit board.

This user guide describes the SDP breakout board (ADZS-BRKOUT-EX3). The Getting Started section provides information on how to use the SDP breakout board as a debug tool for the SDP 120-pin connector signals. The Hardware Description section describes the ADZS-BRKOUT-EX3 hardware. This includes details of the connectors on the board and how these signals are exposed. The ADZS-BRKOUT-EX3 schematics are provided in the Schematic section.

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REVISION HISTORY

9/11—Revision 0: Initial Version

PRODUCT OVERVIEW

The SDP breakout board features

- 4-pin × 120-pin small footprint connectors
- Hirose FX8-120P-SV1(91),120-pin header
- Hirose FX8-120S-SV(21), 120-pin receptacle
- ID EEPROM
- 240 through-hole probe points

For more information, go to http://www.analog.com/sdp.

TECHNICAL OR CUSTOMER SUPPORT

You can reach Analog Devices, Inc., Customer Support in the following ways:

- Visit the SDP website at

  http://www.analog.com/sdp
- Email processor questions to

  processor.support@analog.com (worldwide support)

  processor.europe@analog.com (Europe support)

  processor.china@analog.com (China support)
- Phone questions to

  1-800-ANALOGD
- Contact your Analog Devices local sales office or authorized distributor.
- Send questions by mail to:

  Analog Devices, Inc.

  Three Technology Way

  P.O. Box 9106

  Norwood, MA 02062-9106

  USA

PRODUCT INFORMATION

Product information can be obtained from the Analog Devices website.

Analog Devices Website

The Analog Devices website, http://www.analog.com, provides information about a broad range of products—analog integrated circuits, amplifiers, converters, and digital signal processors.

Note that MyAnalog.com is a free feature of the Analog Devices website that allows customization of a web page to display only the latest information about products of interest to you. You can choose to receive weekly email notifications containing updates to the web pages that meet your interests, including documentation errata. MyAnalog.com provides access to books, application notes, data sheets, code examples, and more.

Visit MyAnalog.com to sign up. If you are a registered user, just log on. Your user name is your email address.

REGULATORY COMPLIANCE

The ADZS-BRKOUT-EX3 is designed for use solely in a laboratory environment. The board is not intended for use as a consumer end product or as a portion of a consumer end product. The board is an open system design, which does not include a shielded enclosure and therefore may cause interference to other electrical devices in close proximity. This board should not be used in or near any medical equipment or RF devices. Store unused boards in the protective shipping package.

The ADZS-BRKOUT-EX3board has been certified to comply with the essential requirements of the European EMC directive 89/36/EC, amended by 93/68/EEC, and therefore carries the CE mark.

GETTING STARTED

This section provides specific information to assist you with using the SDP breakout board as part of an SDP system.

The following topics are covered.

- Package contents
- PC configuration
- Breakout board installation

PACKAGE CONTENTS

The ADZS-BRKOUT-EX3 board package contains one ADZS-BRKOUT-EX3 board.

Contact the vendor where you purchased the SDP breakout board or contact Analog Devices if this item is missing.

PC CONFIGURATION

For correct operation of an SDP controller board and SDP breakout board, your computer must have the following minimum configuration:

- Windows XP Service Pack 2 or Windows Vista®
- USB 2.0 port

BREAKOUT BOARD INSTALLATION

When removing the SDP breakout board from the package, handle the board carefully to avoid the discharge of static electricity, which can damage some components.

The SDP breakout board is designed for use with an SDP controller board. The SDP breakout board must be connected to a PC via the SDP controller board and a USB cable.

Figure 1 shows the SDP breakout board connected to an SDP-B controller board and a Circuit from the Lab reference circuit or component evaluation board.

The SDP breakout board exposes each of the 120 pins on the SDP-B board connector. The breakout board has a 120-pin receptacle connector (J1) which attaches to the 120-pin connector on the SDP controller board; it also has a 120-pin header connector (P1) for attaching SDP-compatible daughter boards to the system.

Pin 1 to Pin 30 and Pin 91 to Pin 120 from receptacle J1 are exposed in the P6 set of probe points. Pin 31 to Pin 90 are exposed in the P5 set of probe points. In this way, the SDP breakout board can be used to monitor signals travelling between the SDP controller board and the attached daughter board.

The SDP breakout board can also be used as a proof of concept tool through the insertion of pin headers in the exposed, relevant signal through-hole locations. These pin headers can be connected to existing hardware when building up a mock-up system prior to the design of SDP-specific hardware.

Figure 1. Connecting the SDP Breakout Board

HARDWARE DESCRIPTION

This section describes the hardware design of the ADZS-BRKOUT-EX3 board.

The following topics are covered.

- LEDs—This section describes the SDP breakout board LEDs.
- Through-hole probe points—This section provides layouts of through-hole probe points on the SDP breakout board.
- Connector Pin Assignments—This section details the pin assignments on the 120-pin connectors.

LEDS

There is a single LED located on the SDP breakout board. It is connected to the input power line on the 120-pin header connector on the SDP breakout board. Therefore, when power is provided from an attached daughter board, this LED is on. If there is no power coming through the VIN pin on P1, this LED remains off.

THROUGH-HOLE PROBE POINTS

The SDP breakout board contains 240 through-hole probe points, 2 × 120 pin receptacle connector and 2 × 120 pin header connectors. One of the 120-pin receptacle connectors (J1) can be used to connect to the 120-pin connector on the SDP controller board. One of the 120-pin header connectors (P1), on the back of the SDP board, can be used to connect to a daughter board (P1).

Figure 2 and Figure 3 show both sides of the SDP breakout board; the shading indicates the signal path from the receptacle to the header via the through-hole probe points. Connector J2 and P2 are for use with future Blackfin® EZ-Kit products.

The signal lines between these two connectors are exposed through the probe points on P3 and P4.

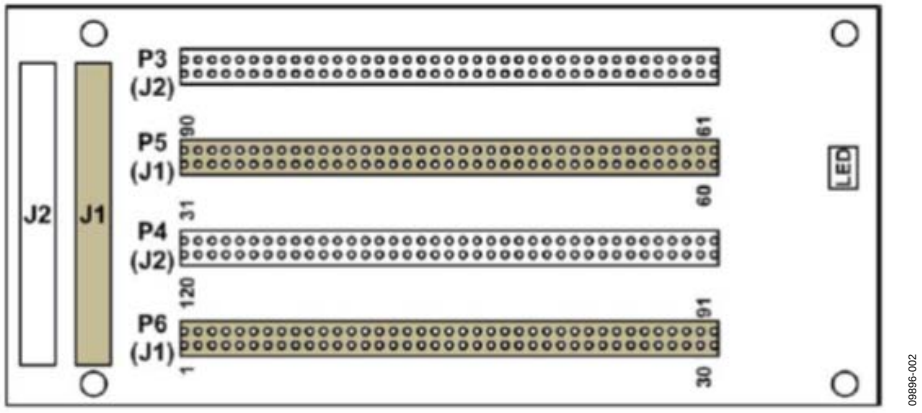

Figure 2. SDP Breakout Board—Top View

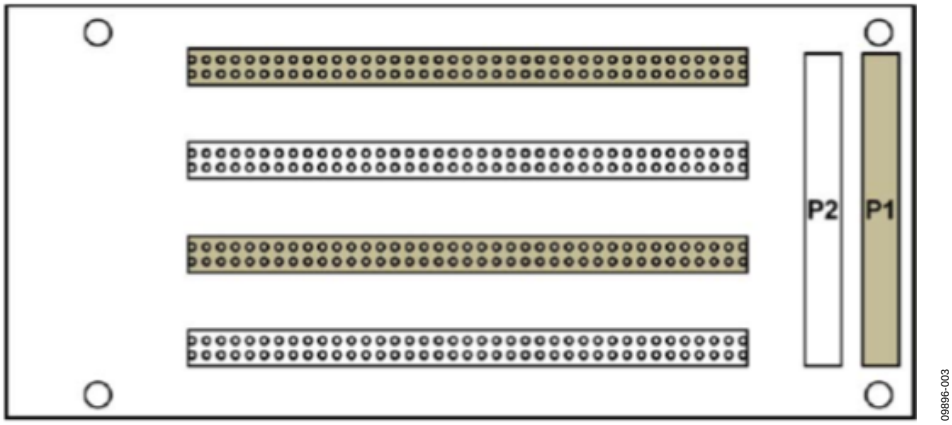

Figure 3. SDP Breakout Board—Bottom View

CONNECTOR PIN ASSIGNMENTS

The SDP breakout board should be connected to an SDP controller board via connector J1 and to an SDP daughter board via connector P1. With this configuration, pin assignments for P6 and P5 through-hole probe points are listed in Table 1.

Table 1. 120-Pin Connector Pin Assignments

Pin No.	Pin Name	Description
1	VIN	Power to SDP Board. Requires 200 mA at 5 V.
2	NC	No Connect. Leave this pin unconnected. Do not ground.
3	GND	Connect to ground plane of board.
4	GND	Connect to ground plane of board.
5	USB_VBUS	Connected directly to the USB +5 V supply.
6	GND	Connect to ground plane of board.
7	PAR_D23	Parallel Data Bus Bit 23. (No connect.)[1]
8	PAR_D21	Parallel Data Bus Bit 21. (No connect.)[1]
9	PAR_D19	Parallel Data Bus Bit 19. (No connect.)[1]
10	PAR_D17	Parallel Data Bus Bit 17. (No connect.)[1]
11	GND	Connect to ground plane of board.
12	PAR_D14	Parallel Data Bus Bit 14.
13	PAR_D13	Parallel Data Bus Bit 13.
14	PAR_D11	Parallel Data Bus Bit 11.
15	PAR_D9	Parallel Data Bus Bit 9.
16	PAR_D7	Parallel Data Bus Bit 7.
17	GND	Connect to ground plane of board.
18	PAR_D5	Parallel Data Bus Bit 5.
19	PAR_D3	Parallel Data Bus Bit 3.
20	PAR_D1	Parallel Data Bus Bit 1.
21	$\overline{\text{PAR\_RD}}$	Asynchronous Parallel Read Strobe.
22	$\overline{\text{PAR\_CS}}$	Asynchronous Parallel Chip Select.
23	GND	Connect to ground plane of board.
24	PAR_A3	Parallel Address Bus Bit 3.
25	PAR_A1	Parallel Address Bus Bit 1.
26	PAR_FS3	Synchronous (PPI) Parallel Frame Sync 3.
27	PAR_FS1	Synchronous (PPI) Parallel Frame Sync 1.
28	GND	Connect to ground plane of board.
29	SPORT_TDV0	SPI Data Line 3. (No connect.)[1]
30	SPORT_TDV1	SPI Data Line 2. (No connect.)[1]
31	SPORT_DR1	SPORT Data Receive 1. Secondary SPORT data into processor.
32	SPORT_DT1	SPORT Data Transmit 1. Secondary SPORT data from processor.
33	SPI_D2	SPORT Data Line. (No connect.)[1]
34	SPI_D3	SPORT Data Line. (No connect.)[1]
35	SERIAL_INT	Serial Interrupt. Used to trigger a nonperiodic serial event.
36	GND	Connect to ground plane of board.
37	$\overline{\text{SPI\_SEL\_B}}$	SPI Chip Select B. Use this to control a second device on the SPI bus.
38	$\overline{\text{SPI\_SEL\_C}}$	SPI Chip Select C. Use this for a third device on the SPI bus.
39	$\overline{\text{SPI\_SEL1/SPI\_SS}}$	SPI Chip Select 1. Used to connect to SPI boot flash, if required. Also used as chip select when Blackfin processor is operating as SPI slave.
40	GND	Connect to ground plane of board.
41	SDA_1	I^2C Data 1.
42	SCL_1	I^2C Data 1.
43	GPIO0	General-Purpose Input/Output.
44	GPIO2	General-Purpose Input/Output.
45	GPIO4	General-Purpose Input/Output.
46	GND	Connect to ground plane of board.

Pin No.	Pin Name	Description
47	GPIO6	General-Purpose Input/Output.
48	TMR_A	Timer A Flag Pin. Use as first timer, if required.
49	TMR_C	Timer C Flag Pin.1 (No connect.)
50	NC	No Connect. Leave this pin unconnected. Do not ground.
51	NC	No Connect. Leave this pin unconnected. Do not ground.
52	GND	Connect to ground plane of board.
53	NC	No Connect. Leave this pin unconnected. Do not ground.
54	NC	No Connect. Leave this pin unconnected. Do not ground.
55	NC	No Connect. Leave this pin unconnected. Do not ground.
56	EEPROM_A0	EEPROM A0. Connect to A0 Address line of the EEPROM.
57	$\overline{\text{RESET\_OUT}}$	Active low reset signal from processor board.
58	GND	Connect to ground plane of board.
59	UART_RX	UART Receive Data.
60	$\overline{\text{RESET\_IN}}$	Active low pin to reset controller board.
61	BMODE1	Boot Mode 1. Pull up with 10 kΩ resistor to set SDP to boot from SPI Flash. Enabled on Connector A only.
62	UART_TX	UART Transmit Data.
63	GND	Connect to ground plane of board.
64	$\overline{\text{SLEEP}}$	Active low sleep from processor board.
65	$\overline{\text{WAKE}}$	External wake up to processor board.
66	NC	No Connect. Leave this pin unconnected. Do not ground.
67	NC	No Connect. Leave this pin unconnected. Do not ground.
68	NC	No Connect. Leave this pin unconnected. Do not ground.
69	GND	Connect to ground plane of board.
70	NC	No Connect. Leave this pin unconnected. Do not ground.
71	CLKOUT	CLKOUT from processor.
72	TMR_D	Timer D Flag Pin.
73	TMR_B	Timer B Flag Pin. Use as second timer, if required.
74	GPIO7	General-Purpose Input/Output.
75	GND	Connect to ground plane of board.
76	GPIO5	General-Purpose Input/Output.
77	GPIO3	General-Purpose Input/Output.
78	GPIO1	General-Purpose Input/Output.
79	SCL_0	I^2C Clock 0. Daughter board EEPROM must be connected to this bus.
80	SDA_0	I^2C Data 0. Daughter board EEPROM must be connected to this bus.
81	GND	Connect to ground plane of board.
82	SPI_CLK	SPI Clock.
83	SPI_MISO	SPI Master In, Slave Out Data.
84	SPI_MOSI	SPI Master Out, Slave In Data.
85	SPI_SEL_A	SPI Chip Select A. Use this to control the first device on the SPI bus.
86	GND	Connect to ground plane of board.
87	SPORT_TSCLK	SPORT Transmit Clock.
88	SPORT_DT0	SPORT Data Transmit 0. Primary SPORT data from processor.
89	SPORT_TFS	SPORT Transmit Frame Sync.
90	SPORT_RFS	SPORT Receive Frame Sync.
91	SPORT_DR0	SPORT Data Receive 0. Primary SPORT data into processor.
92	SPORT_RSCLK	SPORT Receive Clock.
93	GND	Connect to ground plane of board.
94	PAR_CLK	Clock for Synchronous Parallel Interface (PPI).
95	PAR_FS2	Synchronous (PPI) Parallel Frame Sync 2.
96	PAR_A0	Parallel Address Bus Bit 0.
97	PAR_A2	Parallel Address Bus Bit 2.
98	GND	Connect to ground plane of board.
99	PAR_INT	Parallel Interrupt. Used to trigger a nonperiodic parallel event.

Pin No.	Pin Name	Description
100	$\overline{\text{PAR\_WR}}$	Asynchronous Parallel Write Strobe.
101	PAR_D0	Parallel Data Bus Bit 0.
102	PAR_D2	Parallel Data Bus Bit 2.
103	PAR_D4	Parallel Data Bus Bit 4.
104	GND	Connect to ground plane of board.
105	PAR_D6	Parallel Data Bus Bit 6.
106	PAR_D8	Parallel Data Bus Bit 8.
107	PAR_D10	Parallel Data Bus Bit 10.
108	PAR_D12	Parallel Data Bus Bit 12.
109	GND	Connect to ground plane of board.
110	PAR_D15	Parallel Data Bus Bit 15.
111	PAR_D16	Parallel Data Bus Bit 16.1 (No connect.)[1]
112	PAR_D18	Parallel Data Bus Bit 18.1 (No connect.)[1]
113	PAR_D20	Parallel Data Bus Bit 20.1 (No connect.)[1]
114	PAR_D22	Parallel Data Bus Bit 22. (No connect.)[1]
115	GND	Connect to ground plane of board.
116	VIO (+3.3 V)	+3.3 V Output. 20 mA maximum current available to power IO voltage on daughter board.
117	GND	Connect to ground plane of board.
118	GND	Connect to ground plane of board.
119	NC	No Connect. Leave this pin unconnected. Do not ground.
120	NC	No Connect. Leave this pin unconnected. Do not ground.

[1] Functionality not implemented on the SDP board.

Each interface provided by the SDP is available on unique pins of the SDP 120-pin connector. The connector pin numbering scheme is outlined in Figure 4.

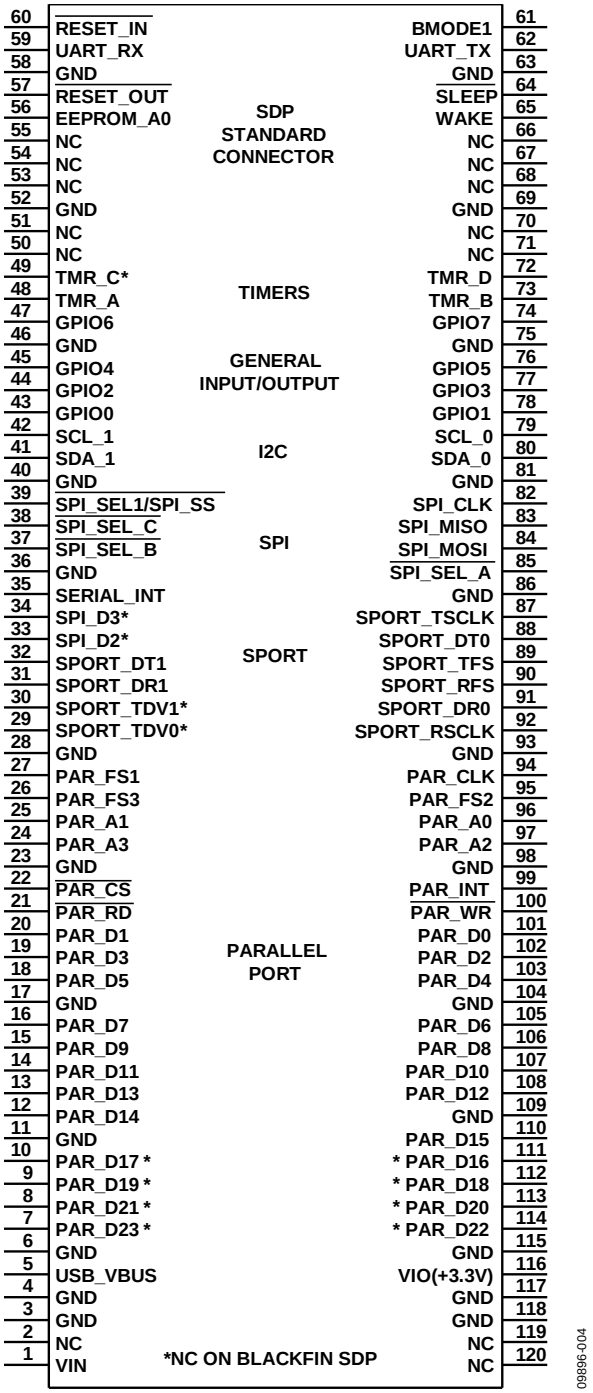

Figure 4. 120-Pin Connector Outline

SCHEMATICS

This section provides the schematic drawings for the ADZS-BRKOUT-EX3 board. The schematic pages include

- SDP breakout board—EI3 connectors
- SDP breakout board—probing connectors
- SDP breakout board—EEPROM and power

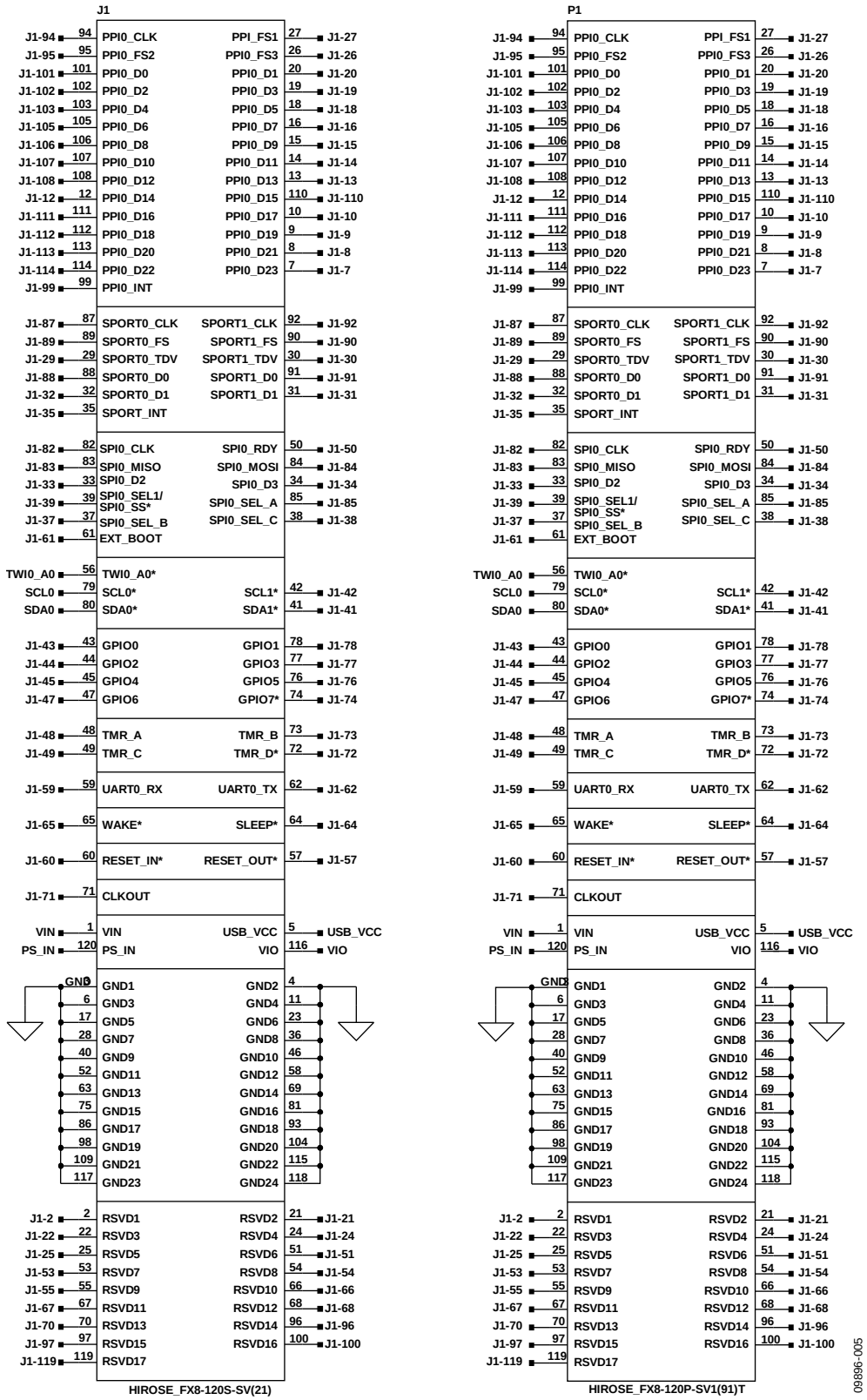

Figure 5. SDP Breakout Board—EI3 Connectors

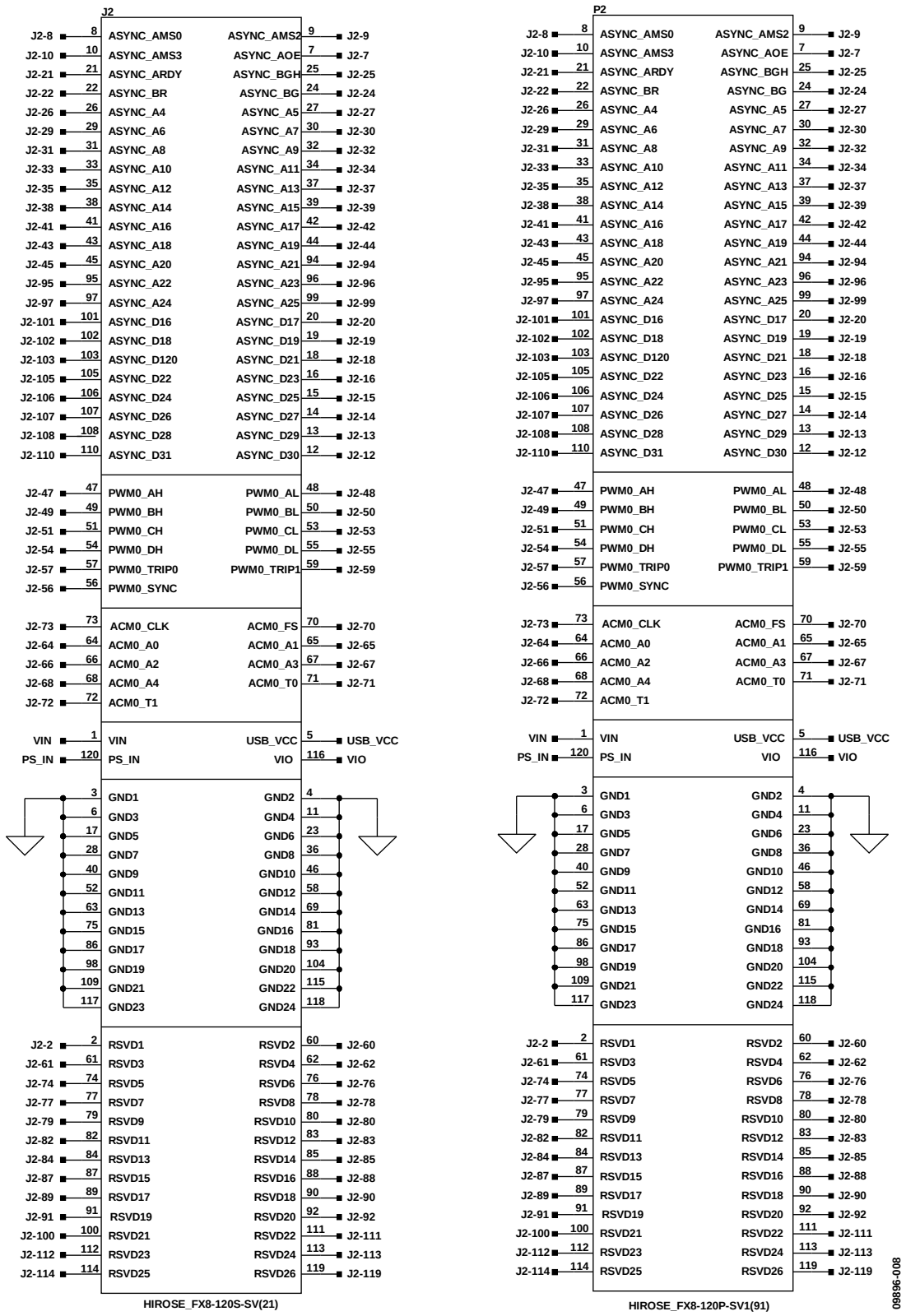

Figure 6. SDP Breakout Board—Probing Connectors

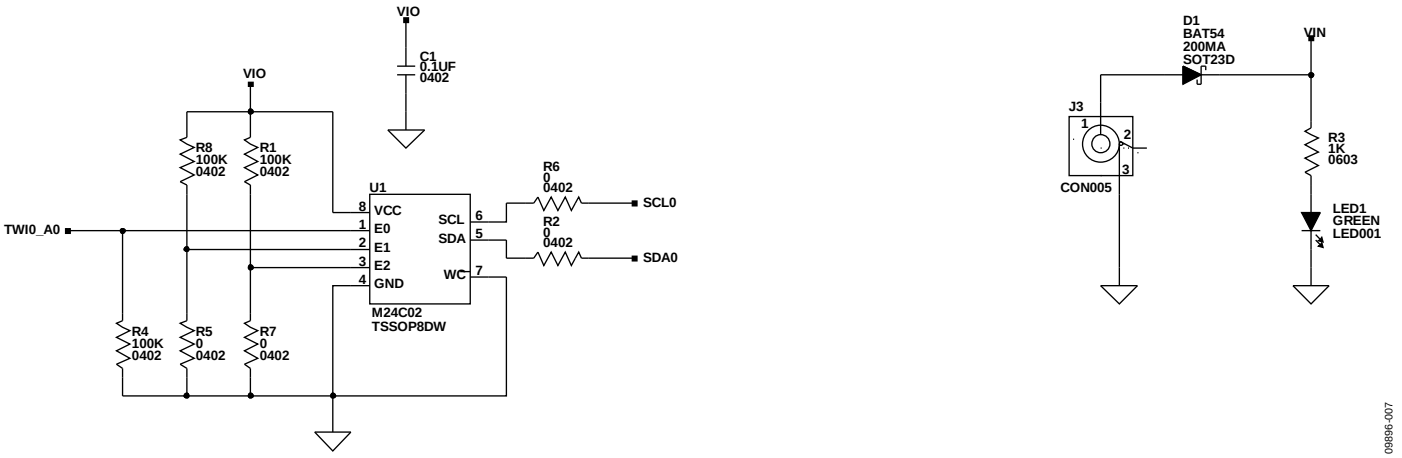

Figure 7. SDP Breakout Board—EEPROM and Power

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ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

UG09896-0-9/11(0)

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