PDM Digital Input, Mono 2.7 W Class-D Audio Amplifier

Data Sheet **SSM2537**

FEATURES

- **Filterless digital Class-D amplifier**
- **Pulse density modulation (PDM) digital input interface**
- **2.7 W into 4 Ω load and 1.4 W into 8 Ω load at 5.0 V supply with <1% total harmonic distortion plus noise (THD + N)**
- **Available in 9-ball, 1.2 mm × 1.2 mm, 0.4 mm pitch WLCSP**
- **93% efficiency into 8 Ω at full scale**
- **Output noise: 25 µV rms at 3.6 V, A-weighted**
- **THD + N: 0.005% at 1 kHz, 100 mW output power**
- **PSRR: 80 dB at 217 Hz, with dither input**
- **Quiescent power consumption: 5.1 mW (VDD = 1.8 V, PVDD = 3.6 V, 8 Ω + 33 µH load)**
- **Pop-and-click suppression**
- **Configurable with PDM pattern inputs**
- **Short-circuit and thermal protection with autorecovery**
- **Smart power-down when PDM stop condition or no clock input detected**
- **64 × f_S or 128 × f_S operation supporting 3 MHz and 6 MHz clocks**
- **DC blocking high-pass filter and static input dc protection**
- **User-selectable ultralow EMI emissions and low latency modes**
- **Power-on reset (POR)**
- **Minimal external passive components**

APPLICATIONS

Mobile handsets

GENERAL DESCRIPTION

The SSM2537 is a PDM digital input Class-D power amplifier that offers higher performance than existing DAC plus Class-D solutions. The SSM2537 is ideal for power sensitive applications where system noise can corrupt the small analog signal sent to the amplifier, such as mobile phones and portable media players.

The SSM2537 combines an audio digital-to-analog converter (DAC), a power amplifier, and a PDM digital interface on a single chip. The integrated DAC plus analog sigma-delta (Σ-Δ) modulator architecture enables extremely low real-world power consumption from digital audio sources with excellent audio performance. Using the SSM2537, audio can be transmitted digitally to the audio amplifier, significantly reducing the effect of noise sources such as GSM interference or other digital signals on the transmitted audio. The SSM2537 is capable of delivering 2.7 W of continuous output power with <1% THD + N driving a 4 Ω load from a 5.0 V supply.

The SSM2537 features a high efficiency, low noise modulation scheme that requires no external LC output filters. The closed-loop, three-level modulator design retains the benefits of an all-digital amplifier, yet enables very good PSRR and audio performance. The modulation continues to provide high efficiency even at low output power and has an SNR of 102 dB PDM input. Spread-spectrum pulse density modulation is used to provide lower EMI-radiated emissions compared with other Class-D architectures.

The SSM2537 has a four-state gain and sample frequency selection pin that can select two different gain settings, optimized for 3.6 V and 5 V operation. This same pin controls the internal digital filtering and clocking, which can be set for a 64 × f_S or 128 × f_S input sample rate to support both 3 MHz and 6 MHz PDM clock rates.

The SSM2537 has a micropower shutdown mode with a typical shutdown current of 1.6 µA for both power supplies. Shutdown is enabled automatically by gating input clock and data signals. A standby mode can be entered by applying a designated PDM stop condition sequence. The device also includes pop-and-click suppression circuitry. This suppression circuitry minimizes voltage glitches at the output when entering or leaving the low power state, reducing audible noises on activation and deactivation.

The SSM2537 is specified over the industrial temperature range of −40°C to +85°C. It has built-in thermal shutdown and output short-circuit protection. It is available in a 9-ball, 1.2 mm × 1.2 mm wafer level chip scale package (WLCSP).

FUNCTIONAL BLOCK DIAGRAM

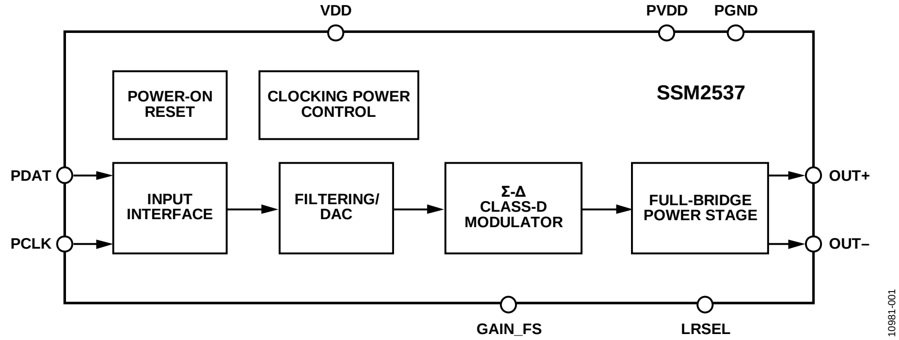

Figure 1.

Rev. 0

Document Feedback

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700

Technical Support **www.analog.com**

TABLE OF CONTENTS

REVISION HISTORY

10/12—Revision 0: Initial Version

SPECIFICATIONS

PVDD = 5.0 V, VDD = 1.8 V, f_S = 128×, T_A = 25°C, R_L = 8 Ω + 33 µH, unless otherwise noted. When f_S = 128×, PDM clock = 6.144 MHz; when f_S = 64×, PDM clock = 3.072 MHz.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
DEVICE CHARACTERISTICS						
Output Power	P_O	f = 1 kHz, BW = 20 kHz				
		R_L = 4 Ω, THD = 1%, PVDD = 5.0 V		2.7		W
		R_L = 8 Ω, THD = 1%, PVDD = 5.0 V		1.4		W
		R_L = 4 Ω, THD = 1%, PVDD = 3.6 V		1.35		W
		R_L = 8 Ω, THD = 1%, PVDD = 3.6 V		0.75		W
		R_L = 4 Ω, THD = 1%, PVDD = 2.5 V		0.62		W
		R_L = 8 Ω, THD = 1%, PVDD = 2.5 V		0.35		W
		R_L = 4 Ω, THD = 10%, PVDD = 5.0 V		3.38		W
		R_L = 8 Ω, THD = 10%, PVDD = 5.0 V		1.8		W
		R_L = 4 Ω, THD = 10%, PVDD = 3.6 V		1.7		W
		R_L = 8 Ω, THD = 10%, PVDD = 3.6 V		0.93		W
		R_L = 4 Ω, THD = 10%, PVDD = 2.5 V		0.78		W
		R_L = 8 Ω, THD = 10%, PVDD = 2.5 V		0.44		W
Total Harmonic Distortion Plus Noise	THD + N	f = 1 kHz				
		P_O = 100 mW into 8 Ω, PVDD = 3.6 V		0.005		%
		P_O = 500 mW into 8 Ω, PVDD = 3.6 V		0.015		%
		P_O = 1 W into 8 Ω, PVDD = 5.0 V		0.02		%
Efficiency	η	P_O = 2 W into 4 Ω, PVDD = 5.0 V		88		%
		P_O = 1.4 W into 8 Ω, PVDD = 5.0 V		93		%
Average Switching Frequency	f_{SW}	No input		290		kHz
Closed-Loop Gain	Gain	−6 dBFS PDM input, BTL output, f = 1 kHz				
		Gain = 3.6 V		3.5		V_P
		Gain = 5.0 V		4.78		V_P
Differential Output Offset Voltage	V_{OOS}	Gain = 3.6 V		0.5		mV
Low Power Mode Wake Time	t_{WAKE}				0.5	ms
Input Sampling Frequency	f_S	f_S = 64×	1.84	3.072	3.23	MHz
		f_S = 128×	3.68	6.144	6.46	MHz
Propagation Delay	t_{PD}	f_S = 6.144 MHz, normal operation		35		µs
		f_S = 6.144 MHz, low latency operation		15		µs
POWER SUPPLY						
Supply Voltage Range						
Amplifier Power Supply	PVDD		2.5	3.6	5.5	V
Digital Power Supply	VDD		1.65	1.8	1.95	V
Power Supply Rejection Ratio	PSRR	V_{RIPPLE} = 100 mV at 100 Hz		80		dB
		V_{RIPPLE} = 100 mV at 1 kHz		80		dB
		V_{RIPPLE} = 100 mV at 10 kHz		75		dB
Supply Current, H-Bridge	I_{PVDD}	Dither input, 8 Ω + 33 µH load				
		PVDD = 5.0 V, f_S = 64×		1.4		mA
		PVDD = 5.0 V, f_S = 128×		1.4		mA
		PVDD = 3.6 V, f_S = 64×		1.1		mA
		PVDD = 3.6 V, f_S = 128×		1.2		mA
		PVDD = 2.5 V, f_S = 64×		1.0		mA
		PVDD = 2.5 V, f_S = 128×		1.1		mA
Standby Current		PVDD = 5.0 V		2.5		µA
Power-Down Current				100		nA

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
Supply Current, Modulator	I_{VDD}	Dither input, 8 Ω + 33 μH load				
		VDD = 1.8 V, f_S = 64×		0.3		mA
		VDD = 1.8 V, f_S = 128×		0.6		mA
Standby Current		VDD = 1.8 V, f_S = 64×		37		μA
		VDD = 1.8 V, f_S = 128×		68		μA
Shutdown Current		VDD = 1.8 V		1.6		μA
NOISE PERFORMANCE						
Output Voltage Noise	e_n	Dither input, A-weighted				
		PVDD = 3.6 V, f_S = 64×		25		μV
		PVDD = 3.6 V, f_S = 128×		27		μV
		PVDD = 5.0 V, f_S = 64×		33		μV
		PVDD = 5.0 V, f_S = 128×		30		μV
Signal-to-Noise Ratio	SNR	P_O = 1.4 W, PVDD = 5.0 V, R_L = 8 Ω, A-weighted				
		f_S = 64×		102		dB
		f_S = 128×		102		dB

DIGITAL INPUT/OUTPUT SPECIFICATIONS

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit
INPUT SPECIFICATIONS					
Input Voltage High	V_{IH}				
PCLK, PDAT, LRSEL Pins		0.7 × VDD		3.6	V
Input Voltage Low	V_{IL}				V
PCLK, PDAT, LRSEL Pins		−0.3		0.3 × VDD	V
Input Leakage Current High	I_{IH}				
PDAT, LRSEL Pins				1	μA
PCLK Pin				3	μA
Input Leakage Current Low	I_{IL}				
PDAT, LRSEL Pins				1	μA
PCLK Pin				3	μA
Input Capacitance				5	pF

PDM INTERFACE DIGITAL TIMING SPECIFICATIONS

Table 3.

Parameter	Limit t_{MIN}	Limit t_{MAX}	Unit	Description
t_{CF}		10	ns	Clock fall time
t_{CR}		10	ns	Clock rise time
t_{DS}	10		ns	Data setup time
t_{DH}	7	7	ns	Data hold time

Timing Diagram

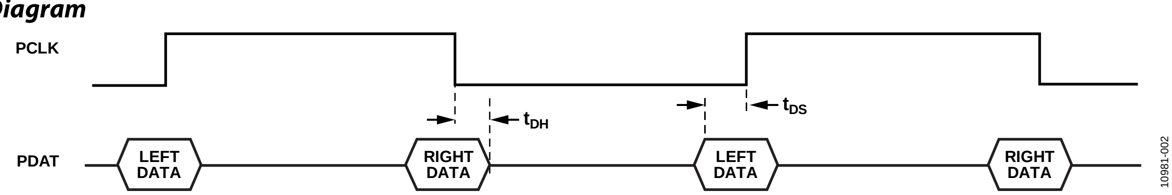

Figure 2. PDM Interface Timing

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings apply at 25°C, unless otherwise noted.

Table 4.

Parameter	Rating
PVDD Supply Voltage	−0.3 V to +6 V
VDD Supply Voltage	−0.3 V to +2 V
Input Voltage (Signal Source)	−0.3 V to +2 V
ESD Susceptibility	4 kV
OUT− and OUT+ Pins	8 kV
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +85°C
Junction Temperature Range	−65°C to +165°C
Lead Temperature (Soldering, 60 sec)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

Junction-to-air thermal resistance (θ_{JA}) is specified for the worst-case conditions, that is, a device soldered in a printed circuit board (PCB) for surface-mount packages. θ_{JA} is determined according to JEDEC JESD51-9 on a 4-layer PCB with natural convection cooling.

Table 5. Thermal Resistance

Package Type	PCB	θ_{JA}	Unit
9-Ball, 1.2 mm × 1.2 mm WLCSP	2S0P	88	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

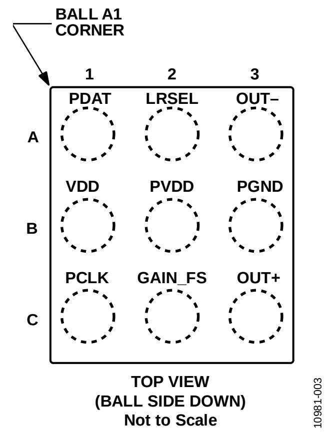

Figure 3. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Function	Description
A1	PDAT	Input	PDM Data Signal.
A2	LRSEL	Input	Left/Right Channel Select. Tie to ground for left channel; pull up to VDD for right channel.
A3	OUT−	Output	Inverting Output.
B1	VDD	Supply	Digital Power, 1.8 V.
B2	PVDD	Supply	Amplifier Power, 2.5 V to 5.5 V.
B3	PGND	Ground	Amplifier Ground.
C1	PCLK	Input	PDM Interface Master Clock.
C2	GAIN_FS	Input	Gain and Sample Rate Selection Pin. (Connect to PVDD for typical operation.)
C3	OUT+	Output	Noninverting Output.

TYPICAL PERFORMANCE CHARACTERISTICS

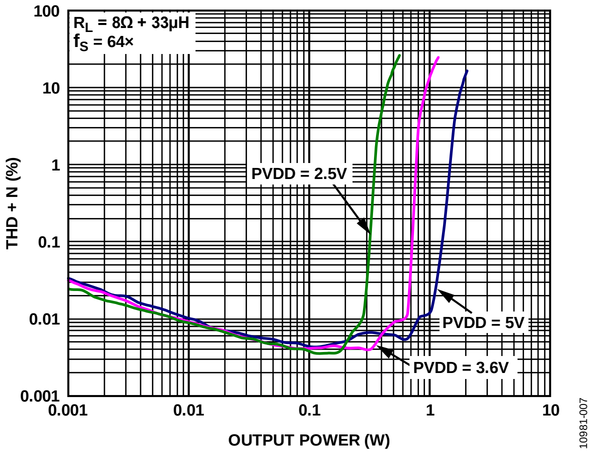

Figure 4. THD + N vs. Output Power into 8 Ω, Gain = 5 V, f_S = 64×

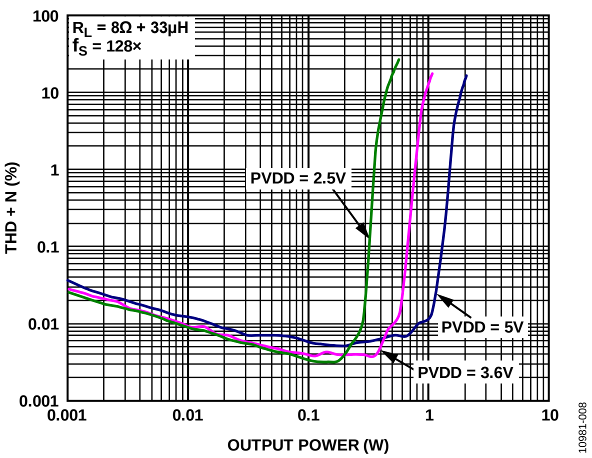

Figure 5. THD + N vs. Output Power into 8 Ω, Gain = 5 V, f_S = 128×

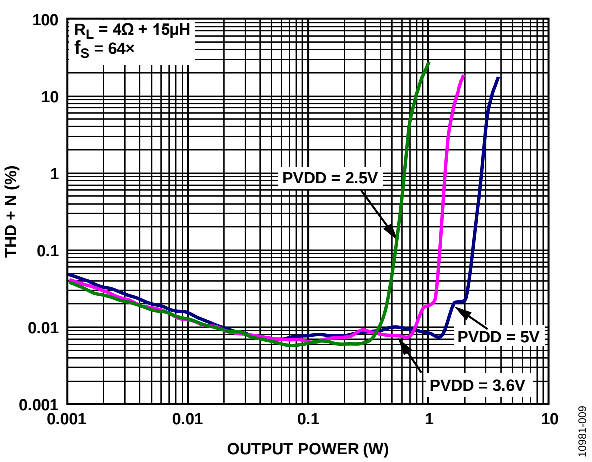

Figure 6. THD + N vs. Output Power into 4 Ω, Gain = 5 V, f_S = 64×

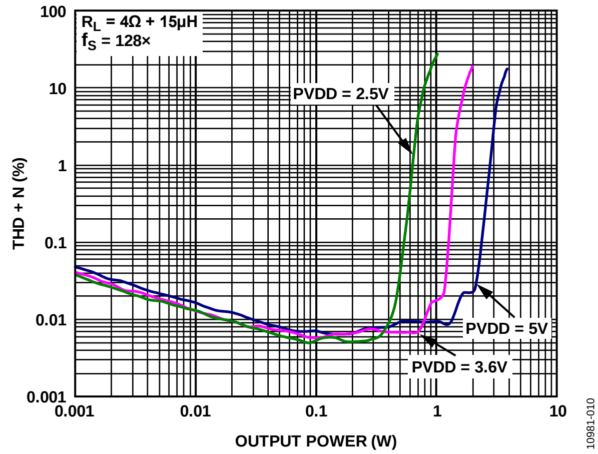

Figure 7. THD + N vs. Output Power into 4 Ω, Gain = 5 V, f_S = 128×

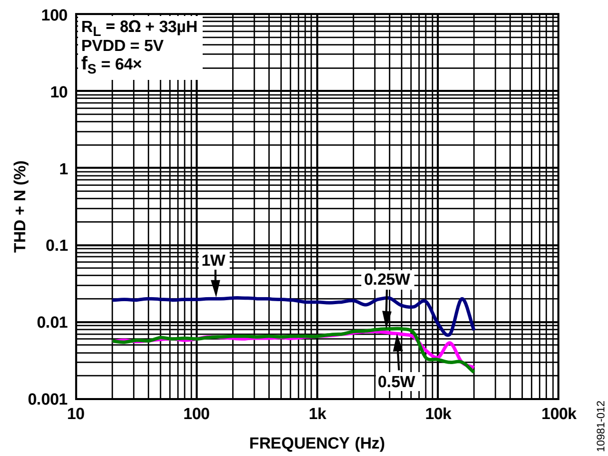

Figure 8. THD + N vs. Frequency, PVDD = 5 V, R_L = 8 Ω, f_S = 64×

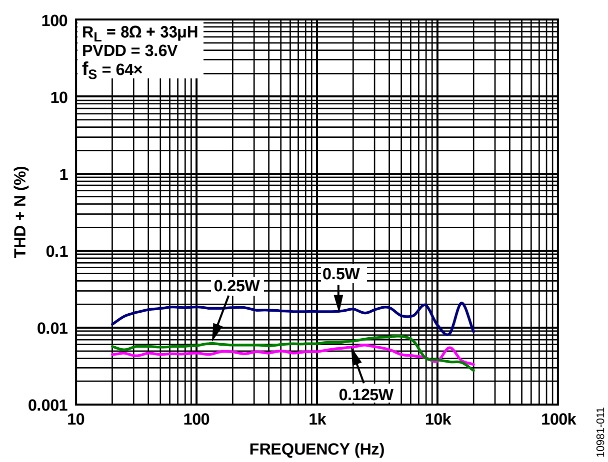

Figure 9. THD + N vs. Frequency, PVDD = 3.6 V, R_L = 8 Ω, f_S = 64×

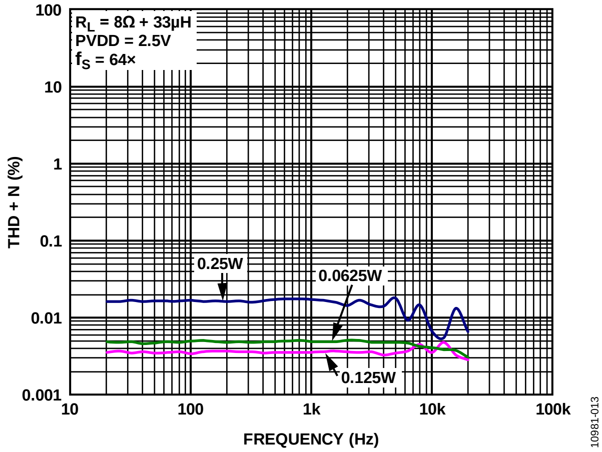

Figure 10. THD + N vs. Frequency, PVDD = 2.5 V, R_L = 8 Ω, f_S = 64×

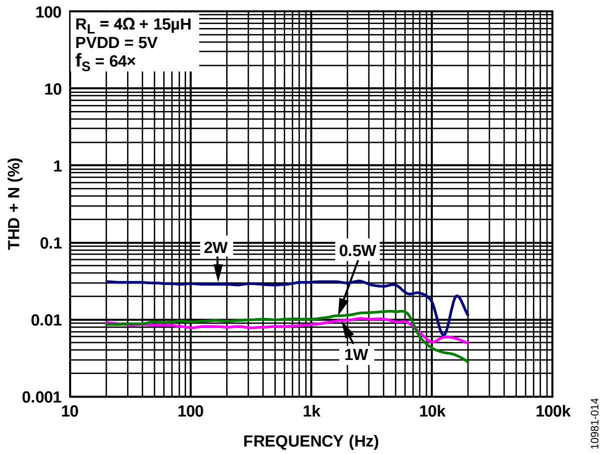

Figure 11. THD + N vs. Frequency, PVDD = 5 V, R_L = 4 Ω, f_S = 64×

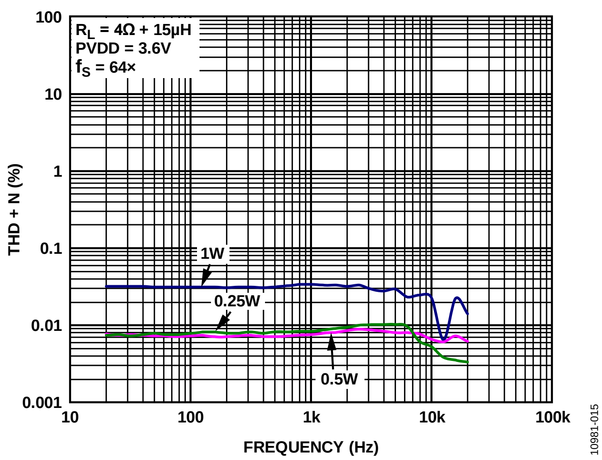

Figure 12. THD + N vs. Frequency, PVDD = 3.6 V, R_L = 4 Ω, f_S = 64×

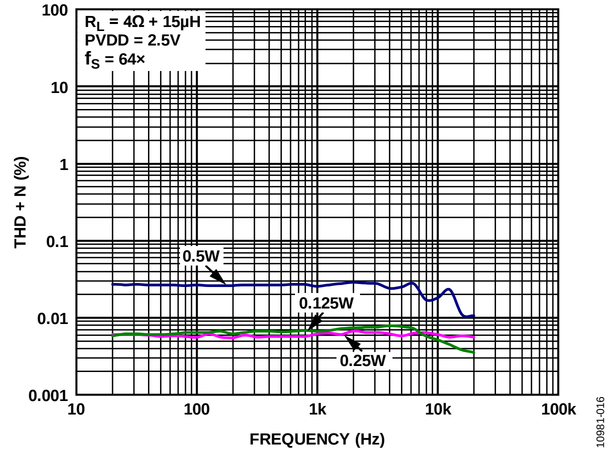

Figure 13. THD + N vs. Frequency, PVDD = 2.5 V, R_L = 4 Ω, f_S = 64×

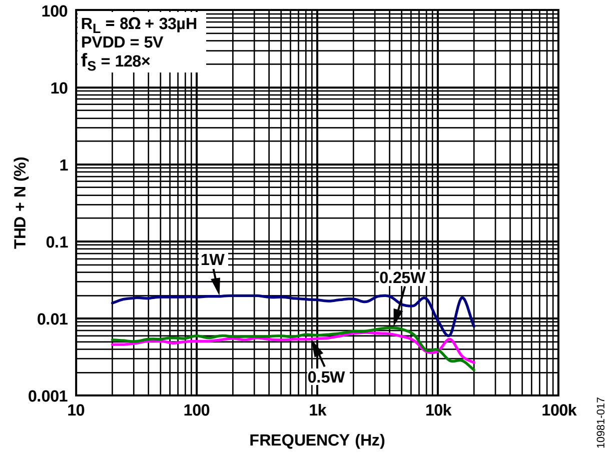

Figure 14. THD + N vs. Frequency, PVDD = 5 V, R_L = 8 Ω, f_S = 128×

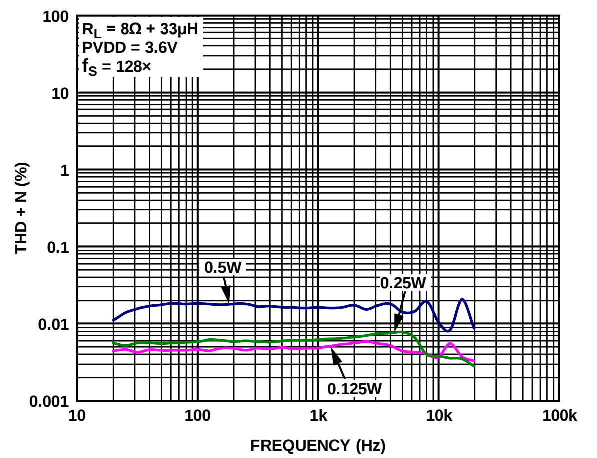

Figure 15. THD + N vs. Frequency, PVDD = 3.6 V, R_L = 8 Ω, f_S = 128×

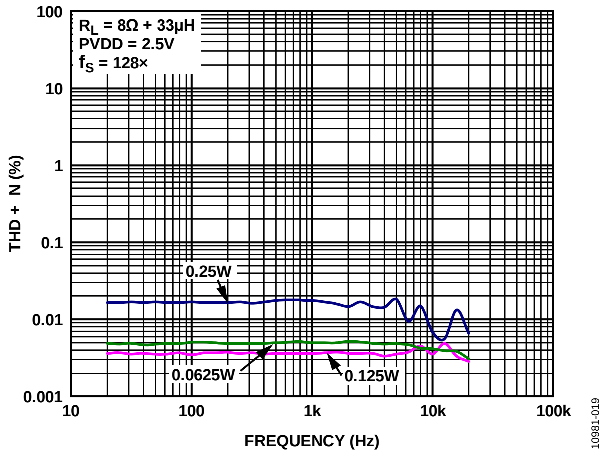

Figure 16. THD + N vs. Frequency, PVDD = 2.5 V, R_L = 8 Ω, f_S = 128×

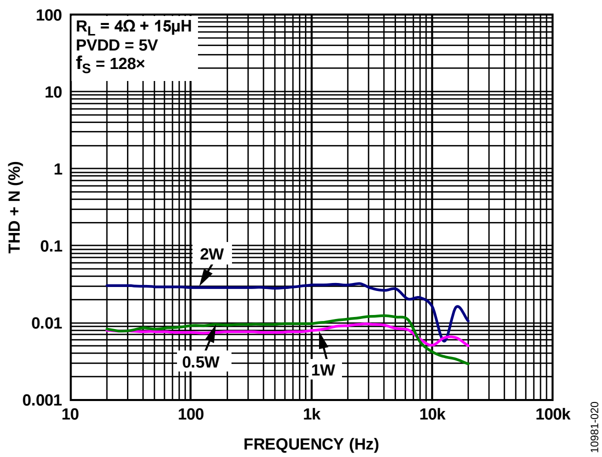

Figure 17. THD + N vs. Frequency, PVDD = 5 V, R_L = 4 Ω, f_S = 128×

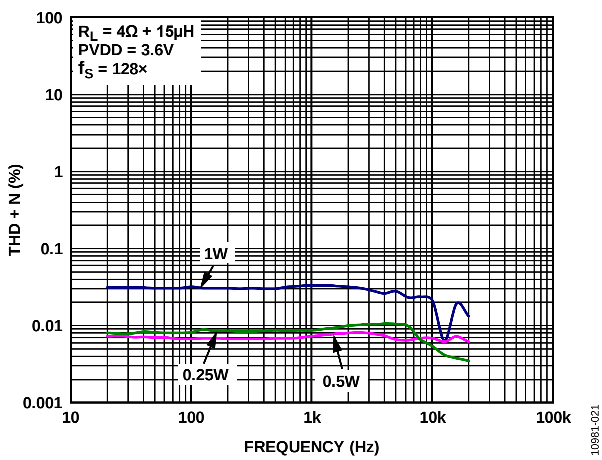

Figure 18. THD + N vs. Frequency, PVDD = 3.6 V, R_L = 4 Ω, f_S = 128×

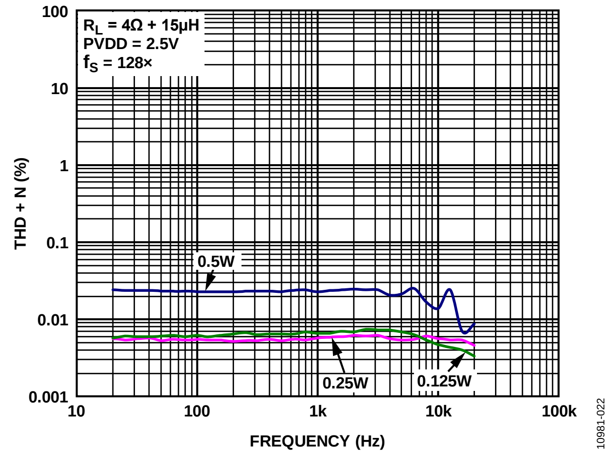

Figure 19. THD + N vs. Frequency, PVDD = 2.5 V, R_L = 4 Ω, f_S = 128×

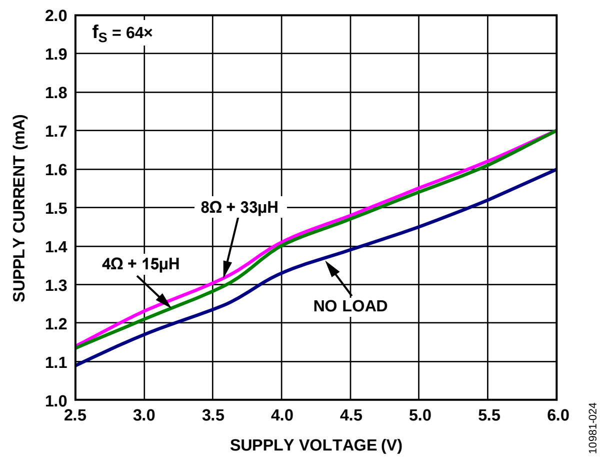

Figure 20. Quiescent Current vs. Supply Voltage, f_S = 64×

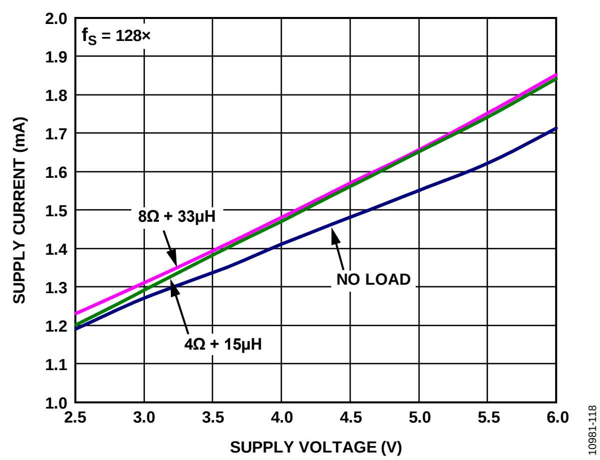

Figure 21. Quiescent Current vs. Supply Voltage, f_S = 128×

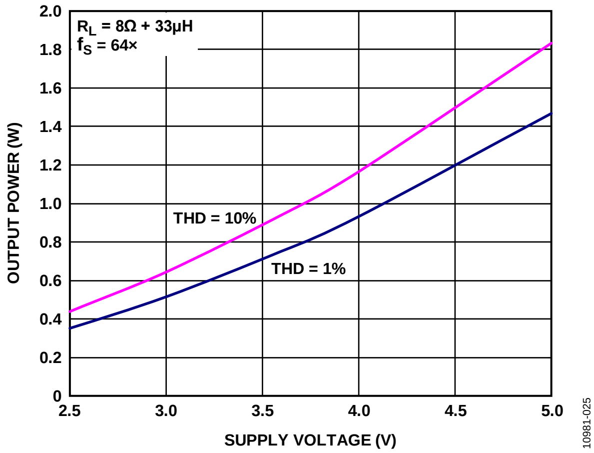

Figure 22. Maximum Output Power vs. Supply Voltage, $R_L = 8\ \Omega$, $f_S = 64\times$

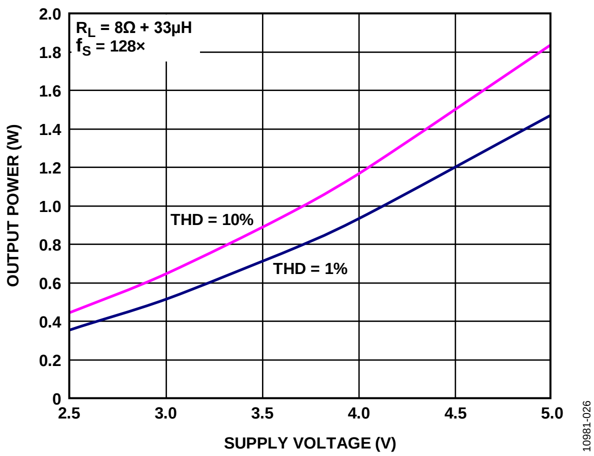

Figure 23. Maximum Output Power vs. Supply Voltage, $R_L = 8\ \Omega$, $f_S = 128\times$

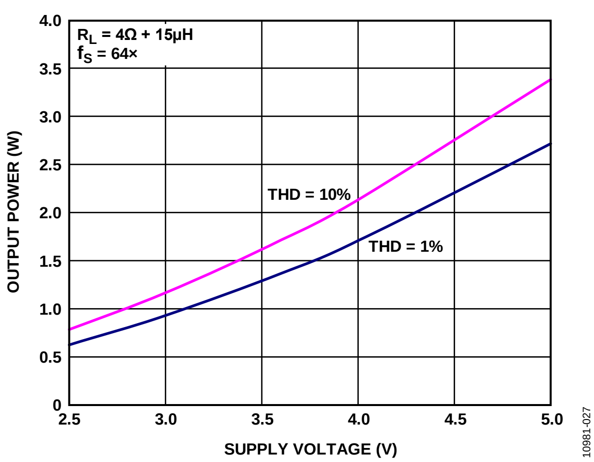

Figure 24. Maximum Output Power vs. Supply Voltage, $R_L = 4\ \Omega$, $f_S = 64\times$

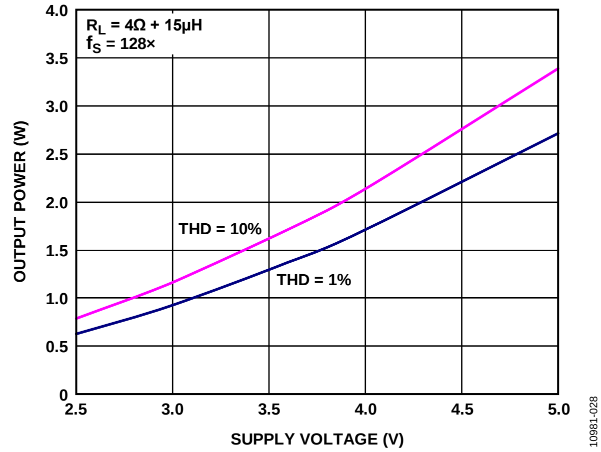

Figure 25. Maximum Output Power vs. Supply Voltage, $R_L = 4\ \Omega$, $f_S = 128\times$

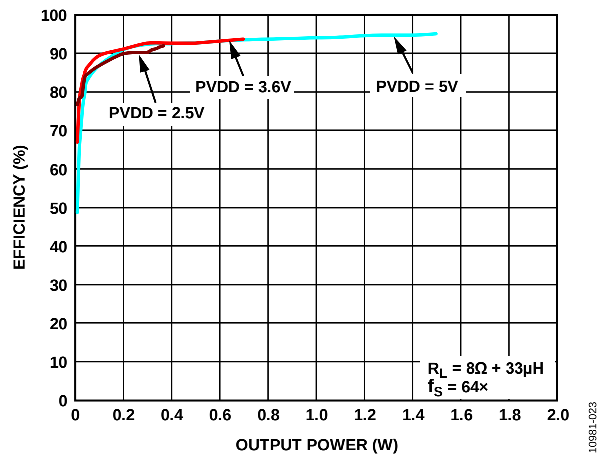

Figure 26. Efficiency vs. Output Power into $8\ \Omega$, $f_S = 64\times$

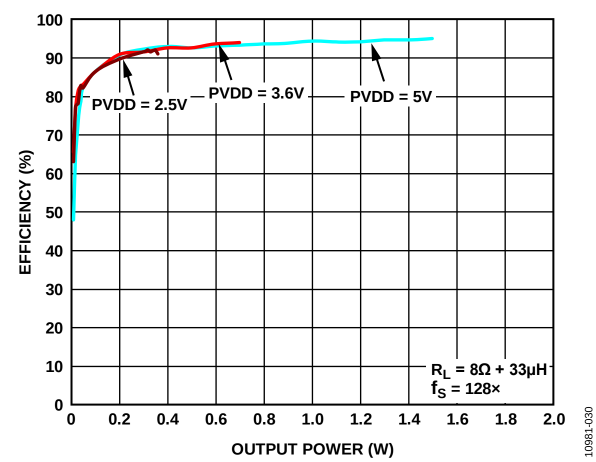

Figure 27. Efficiency vs. Output Power into $8\ \Omega$, $f_S = 128\times$

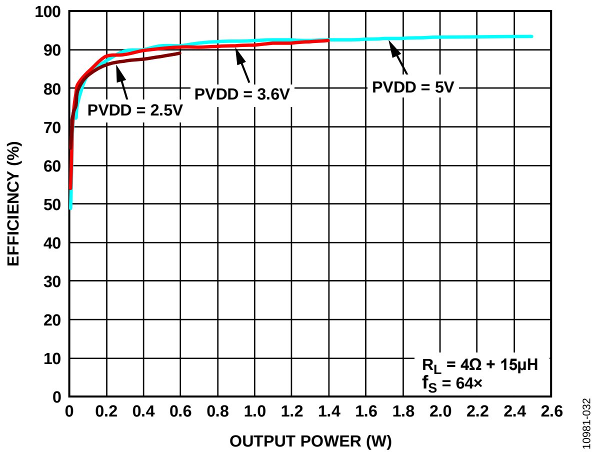

Figure 28. Efficiency vs. Output Power into 4 Ω, f_S = 64×

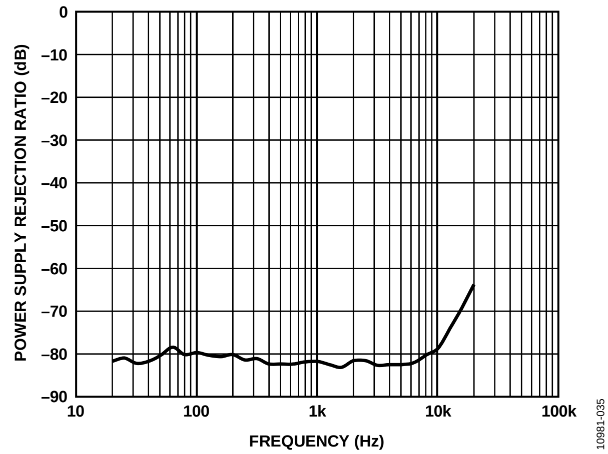

Figure 31. Power Supply Rejection Ratio (PSRR) vs. Frequency

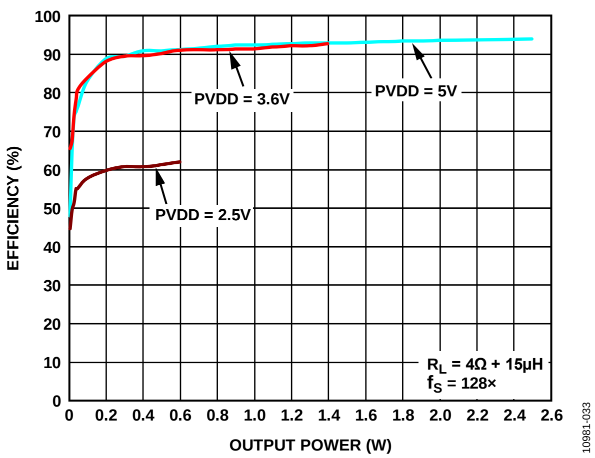

Figure 29. Efficiency vs. Output Power into 4 Ω, f_S = 128×

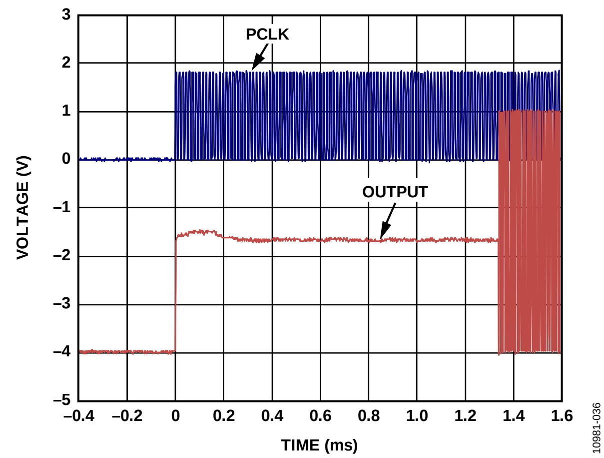

Figure 32. Turn-On Response

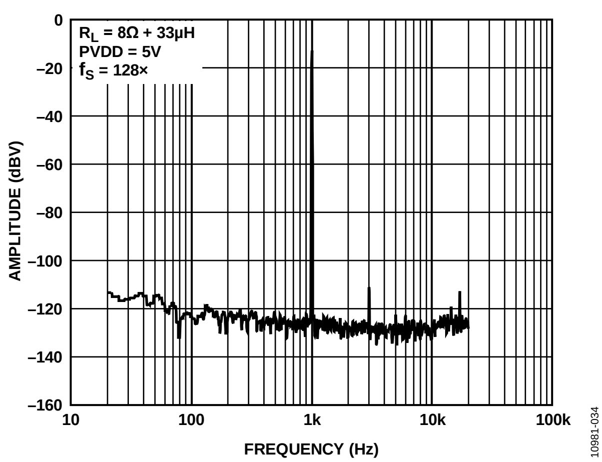

Figure 30. Output Spectrum vs. Frequency

THEORY OF OPERATION

MASTER CLOCK

The SSM2537 requires a clock present at the PCLK input pin to operate. This clock must be fully synchronous with the incoming digital audio on the serial interface. Clock frequencies must fall into one of these ranges: 1.84 MHz to 3.23 MHz or 3.68 MHz to 6.46 MHz.

POWER SUPPLIES

The SSM2537 requires two power supplies: PVDD and VDD.

PVDD

PVDD supplies power to the full-bridge power stage of the MOSFET and its associated drive, control, and protection circuitry. It also supplies power to the digital-to-analog converter (DAC) and to the Class-D PDM modulator. PVDD can operate from 2.5 V to 5.5 V and must be present to obtain audio output. Lowering the supply voltage of PVDD results in lower maximum output power and, therefore, lower power consumption.

VDD

VDD provides power to the digital logic circuitry. VDD can operate from 1.65 V to 1.95 V and must be present to obtain audio output. Lowering the supply voltage of VDD results in lower power consumption but does not affect audio performance.

POWER CONTROL

On device power-up, PVDD must first be applied to the device, which latches in the designated GAIN_FS pin functionality.

The SSM2537 contains a smart power-down feature. When enabled, the smart power-down feature looks at the incoming digital audio and, if it receives the PDM stop condition of at least 129 repeated 0xAC bytes (1024 clock cycles), it places the SSM2537 in standby mode. In standby mode, PCLK can be removed, resulting in a full power-down state. This state is the lowest power condition possible. When PCLK is turned on again and a single non-stop condition input is received, the SSM2537 leaves the full power-down state and resumes normal operation under the default setting as indicated by the GAIN_FS pin state.

POWER-ON RESET/VOLTAGE SUPERVISOR

The SSM2537 includes an internal power-on reset and voltage supervisor circuit. This circuit provides an internal reset to _jj circuitry when PVDD or VDD is substantially below the nominal operating threshold. This simplifies supply sequencing during initial power-on.

The circuit also monitors the power supplies to the IC. If the supply voltages fall below the nominal operating threshold, this circuit stops the output and issues a reset. This is done to ensure that no damage occurs due to low voltage operation and that no pops can occur under nearly any power removal condition.

SYSTEM GAIN/INPUT FREQUENCY

The GAIN_FS pin is used to set the internal gain and filtering configuration for different sample rates of the SSM2537. This pin can be set to one of four states by connecting the pin either to PVDD or to PGND with or without a 47 kΩ resistor (see Table 7). The internal gain and filtering can also be set via PDM pattern control, allowing these settings to be modified during operation (see the PDM Pattern Control section).

The SSM2537 has an internal analog gain control such that when GAIN_FS is tied to PGND or PVDD via a 47 kΩ resistor (5 V gain setting), a −6.02 dBFS PDM input signal results in an amplifier output voltage of 5 V peak. This setting should produce optimal noise performance when PVDD is 5 V.

When the GAIN_FS pin is tied to PVDD or pulled directly to PGND, the gain is adjusted so that a −6.02 dBFS PDM input signal results in an amplifier output voltage of 3.6 V peak. This setting should produce optimal noise performance when PVDD is 3.6 V.

The SSM2537 can handle input sample rates of $64 \times f_S$ (~3 MHz) and $128 \times f_S$ (~6 MHz). Different internal digital filtering is used in each of these cases. Selection of the sample rate is also set via the GAIN_FS pin (see Table 7).

Because the $64 \times f_S$ mode provides better performance with lower power consumption, its use is recommended. The $128 \times f_S$ mode should be used only when overall system noise performance is limited by the source modulator.

Table 7. GAIN_FS Function Descriptions

Device Setting	GAIN_FS Pin Configuration
$f_S = 128 \times$ PCLK, Gain = 5 V	Pull up to PVDD with a 47 kΩ resistor
$f_S = 64 \times$ PCLK, Gain = 5 V	Pull down to PGND with a 47 kΩ resistor
$f_S = 128 \times$ PCLK, Gain = 3.6 V	Pull up to PVDD
$f_S = 64 \times$ PCLK, Gain = 3.6 V	Pull down to PGND

PDM PATTERN CONTROL

The SSM2537 has a simple control mechanism that can set the part for low power states and control functionality. This is accomplished by sending a repeating 8-bit pattern to the device. Different patterns set different functionality (see Table 8).

Any pattern must be repeated a minimum of 129 times. The part is automatically muted when a pattern is detected so that a pattern can be set while the part is operational without a pop/click due to pattern transition.

All functionality set via patterns returns to its default values after a clock-loss power-down.

Table 8. PDM Watermarking Pattern Control Descriptions

Pattern	Control Description
0xD2	Gain optimized for PVDD = 3.6 V operation.
0xD4	Gain optimized for PVDD = 2.5 V operation.
0xD8	Gain optimized for PVDD = 5 V operation.
0xE1	Ultralow EMI mode.
0xE2	Low latency mode with pattern delay (~15 µs latency).
0xE4	f_S set to opposite value determined by GAIN_FS pin.
0xAA	Device reset: Place device into default configuration.
0x66	Mute.
0xAC	Power-down: All blocks off except for PDM interface. Normal start-up time.

EMI NOISE

The SSM2537 uses a proprietary modulation and spread-spectrum technology to minimize EMI emissions from the device. For applications that have difficulty passing FCC Class B emission tests, the SSM2537 includes a modulation select mode (ultralow EMI emissions mode) that significantly reduces the radiated emissions at the Class-D outputs, particularly above 100 MHz. This mode is enabled by activating PDM Watermarking Pattern 0xE1 (see Table 8).

PDM CHANNEL SELECTION

The SSM2537 includes a left/right input select pin, LRSEL (see Table 9), that determines which of the time-multiplexed input streams is routed to the amplifier. To select the left input channel, connect LRSEL to PGND. To select the right channel, connect LRSEL to VDD. At any point during amplifier operation, the logic level applied to LRSEL may be changed and the output will switch the input streams without audible artifacts. No muting, watermarking pattern or synchronizing are necessary to achieve a click/pop free LRSEL transition.

Table 9. LRSEL Pin Function Descriptions

Device Setting	LRSEL Pin Configuration
Right Channel Select	VDD
Left Channel Select	PGND

OUTPUT MODULATION DESCRIPTION

The SSM2537 uses three-level, Σ-Δ output modulation. Each output can swing from PGND to PVDD and vice versa. Ideally, when no input signal is present, the output differential voltage is 0 V because there is no need to generate a pulse. In a real-world situation, there are always noise sources present.

Due to this constant presence of noise, a differential pulse is generated, when required, in response to this stimulus. A small amount of current flows into the inductive load when the differential pulse is generated.

Most of the time, however, the output differential voltage is 0 V, due to the Analog Devices, Inc., three-level, Σ-Δ output modulation. This feature ensures that the current flowing through the inductive load is small.

When the user wants to send an input signal, an output pulse (OUT+ and OUT−) is generated to follow the input voltage. The differential pulse density (VOUT) is increased by raising the input signal level. Figure 33 depicts three-level, Σ-Δ output modulation with and without input stimulus.

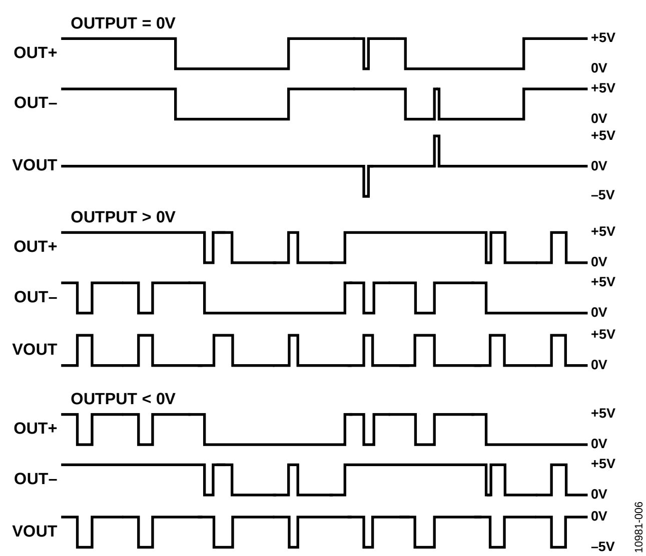

Figure 33. Three-Level, Σ-Δ Output Modulation With and Without Input Stimulus

APPLICATIONS INFORMATION

LAYOUT

As output power increases, take care to lay out PCB traces and wires properly among the amplifier, load, and power supply. A good practice is to use short, wide PCB tracks to decrease voltage drops and minimize inductance. Avoid ground loops where possible to minimize common-mode current associated with separate paths to ground. Ensure that track widths are at least 200 mil per inch of track length for the lowest DCR, and use 1 oz or 2 oz copper PCB traces to further reduce IR drops and inductance. A poor layout increases voltage drops, consequently affecting efficiency. Use large traces for the power supply inputs and amplifier outputs to minimize losses due to parasitic trace resistance.

Proper grounding helps to improve audio performance, minimize crosstalk between channels, and prevent switching noise from coupling into the audio signal. To maintain high output swing and high peak output power, the PCB traces that connect the output pins to the load, as well as the PCB traces to the supply pins, should be as wide as possible to maintain the minimum trace resistances. It is also recommended that a large ground plane be used for minimum impedances.

In addition, good PCB layout isolates critical analog paths from sources of high interference. Separate high frequency circuits (analog and digital) from low frequency circuits.

Properly designed multilayer PCBs can reduce EMI emissions and increase immunity to the RF field by a factor of 10 or more, compared with double-sided boards. A multilayer board allows a complete layer to be used for the ground plane, whereas the ground plane side of a double-sided board is often disrupted by signal crossover.

POWER SUPPLY DECOUPLING

To ensure high efficiency, low total harmonic distortion (THD), and high PSRR, proper power supply decoupling is necessary. Noise transients on the power supply lines are short-duration voltage spikes. These spikes can contain frequency components that extend into the hundreds of megahertz.

The power supply input must be decoupled with a good quality, low ESL, low ESR capacitor, with a minimum value of 4.7 μF. This capacitor bypasses low frequency noises to the ground plane. For high frequency transient noises, use a 0.1 μF capacitor as close as possible to the PVDD and VDD pins of the device. Placing the decoupling capacitors as close as possible to the SSM2537 helps to maintain efficient performance.

OUTLINE DIMENSIONS

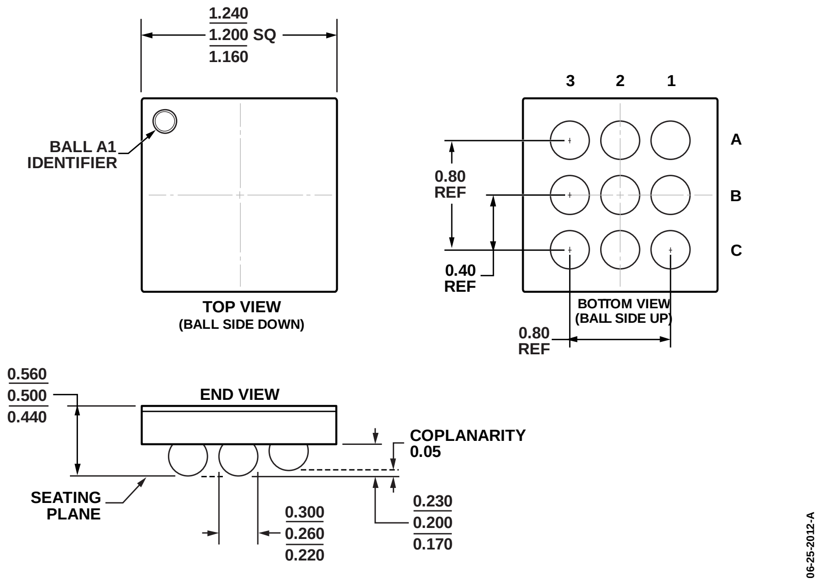

Figure 34. 9-Ball Wafer Level Chip Scale Package [WLCSP]
(CB-9-5)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
SSM2537ACBZ-R7	−40°C to +85°C	9-Ball Wafer Level Chip Scale Package [WLCSP]	CB-9-5
SSM2537ACBZ-RL	−40°C to +85°C	9-Ball Wafer Level Chip Scale Package [WLCSP]	CB-9-5
EVAL-SSM2537Z		Evaluation Board	

[1] Z = RoHS Compliant Part.