SCOPE: CMOS, Serial, 12-Bit D/A Converter

Device Type:	**Generic Number:**
-01	**MX7543S(x)/883B**
-02	**MX7543T(x)/883B**
-03	**MX7543GT(x)/883B**

Case Outline(s).

Outline Letter	Mil-Std-1835	Case Outline	Package Code
Q	GDIP1-T16 or CDIP2-T16	16 Lead CERDIP	J16
E	CQCC1-N20	20-Pin Ceramic LCC	L20

Absolute Maxi mum Ratings: (T_A=+25°C, unless otherwise noted.)

V_{DD} to AGND ..... 0V, +7V
V_{DD} to DGND ..... 0V, +7V
AGND to DGND ..... V_{DD}
DGND to AGND ..... V_{DD}
Digital Input Voltage to DGND ..... -0.3V to +15V
V_{OUT1}, V_{OUT2} to AGND ..... -0.3V to +15V
VREF to AGND ..... -25V to +25V
V_{RFB} to AGND ..... -25V to +25V

Lead Temperature (soldering, 10 seconds) ..... +300°C
Storage Temperature ..... -65°C to +150°C

Continuous Power Dissipation ..... T_A=+70°C
16 pin CERDIP(derate 10mW/°C above +70°C) 800mW
20 pin LCC(derate 9.09mW/°C above +70°C) 727mW
Junction Temperature T_J ..... +150°C
Thermal Resistance, Junction to Case, ΘJC
16 pin CERDIP..... 50°C/W
20 pin LCC ..... 20°C/W
Thermal Resistance, Junction to Ambient, ΘJA:
16 pin CERDIP..... 100°C/W
20 pin LCC ..... 110°C/W

Recommended Operating Conditions

Ambient Operating Range (T_A) ..... -55°C to +125°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TABLE 1. ELECTRICAL TESTS:

TEST	Symbol	CONDITIONS $-55°C \le T_A \le +125°C$ 1/ Unless otherwise specified	GROUP A Subgroup	Device type	Limits Min	Limits Max	Units
Resolution	RES	Guaranteed but not tested		All	12		Bits
Relative Accuracy	RA		All	01 02,03	-1 -0.5	1 0.5	LSB
Differential Nonlinearity	DNL	Monotonic to 11-Bit Monotonic to 12-Bit	All	01 02,03	-2 -1	2 1	LSB
Gain Error NOTE 2	AE		1 2,3	01,02	-12.3 -14.5	12.3 14.5	LSB
Gain Error NOTE 2	AE		1 2,3	03	-1 -2	1 2	LSB
Gain Tempco	TC_{AE}	NOTE 3		All	-5	5	ppm/°C
Power-Supply Rejection	PSRR	V_{DD}=±5% ($\Delta Gain/\Delta V_{DD}$)	1 2,3	All	-0.005 -0.01	0.005 0.01	$\%/\%V_{DD}$
OUT1 Leakage Current	I_{OUT1}	DAC register loaded with all 0s	1 2,3	All	-1 -200	1 200	nA
OUT2 Leakage Current	I_{OUT2}	DAC register loaded with all 1s	1 2,3	All	-1 -200	1 200	nA
Output Current Settling Time NOTE 3	t_{SL}	To ±0.5LSB, OUT1 load is 100 Ω in parallel with13pF. Output measured from falling edge of $\overline{LD1}$ and $\overline{LD2}$.		All		2	µs
Feedthrough Error NOTE 3	FTE	VREF=10V, 10kHz sine wave		All		2.5	mVp-p
Reference Input Resistance	R_{IN}		1,2,3	All	8	25	kΩ
Digital Input High Voltage	V_{IH}		1,2,3	All	3.0		V
Digital Input Low Voltage	V_{IL}		1,2,3	All		0.8	V
Digital Input Leakage Current	I_{IN}	V_{IN}=0V or V_{DD}	1,2,3	All	-1	1	µA
Digital Input Capacitance NOTE 3	C_{IN}			All		8	pF
Output Capacitance NOTE 3	C_{OUT1}	Digital inputs at V_{IH}, DAC register loaded with all 1s Digital inputs at V_{IL}, DAC register loaded with all 0s		All		260 75	pF
Output Capacitance NOTE 3	C_{OUT2}	Digital inputs at V_{IH}, DAC register loaded with all 1s Digital inputs at V_{IL}, DAC register loaded with all 0s		All		75 260	pF

TABLE 1. ELECTRICAL TESTS:

TEST	Symbol	CONDITIONS -55°C≤T_A≤+125°C 1/ Unless otherwise specified	GROUP A Subgroup	Device type	Limits Min	Limits Max	Units
Serial Input to Strobe Setup Time NOTE 3	t_{DS1} t_{DS2} t_{DS3} t_{DS4}	STB1 STB2 $\overline{STB3}$ STB4		All	100 40 0 0		ns
Serial Input to Strobe Hold Time NOTE 3	t_{DH1} t_{DH2} t_{DH3} t_{DH4}	STB1 STB2 $\overline{STB3}$ STB4		All	70 200 250 250		ns
SRI Data Pulse Width NOTE 3	t_{SRI}			All	160		ns
Strobe Pulse Width NOTE 3	t_{STB1} t_{STB2} t_{STB3} t_{STB4}	STB1 STB2 $\overline{STB3}$ STB4		All	160 180 230 230		ns
Load Pulse Width NOTE 3	t_{LD1} t_{LD2}			All	300 300		ns
Time Between Strobing LSB into Register A and Loading Register B NOTE 3	t_{ASB}			All	80		ns
CLEAR Pulse Width NOTE 3	t_{CLR}			All	400		ns

NOTE 1: V_{DD}=+5V, V_{OUT1}=V_{OUT2}=0V, VREF=+10V, unless otherwise noted.
NOTE 2: Measured using internal feedback resistor; includes effects of leakage current and gain TC.
NOTE 3: Characteristics supplied for use as a typical design limit but not production tested.

TERMINAL CONNECTIONS:

	MX7543				
	J16	L20		J16	L20
1	OUT1	NC	11	STB4	NC
2	OUT2	OUT1	12	DGND	$\overline{\text{LD2}}$
3	AGND	OUT2	13	$\overline{\text{CLR}}$	STB3
4	STB1	AGND	14	V_{DD}	STB4
5	$\overline{\text{LD1}}$	STB1	15	VREF	DGND
6	NC	NC	16	R_{FB}	NC
7	SRI	$\overline{\text{LD1}}$	17		$\overline{\text{CLR}}$
8	STB2	NC	18		V_{DD}
9	$\overline{\text{LD2}}$	SRI	19		VREF
10	$\overline{\text{STB3}}$	STB2	20		R_{FB}

MODE CONTROL TABLE:

LOGIC INPUTS							OPERATION	NOTES
REGISTER A CONTROL INPUTS				REGISTER B CONTROL INPUTS				
STB4	$\overline{\text{STB3}}$	STB2	STB1	CLR	$\overline{\text{LD2}}$	$\overline{\text{LD1}}$		
0	1	0	↑	X	X	X	Data appearing at SRI strobed into register A	1,2
0	1	↑	0	X	X	X	Same as above	1,2
0	↓	0	0	X	X	X	Same as above	1,2
↑	1	0	0	X	X	X	Same as above	1,2
1	X	X	X				No operation (Register A)	2
X	0	X	X					
X	X	1	X					
X	X	X	1					
				0	X	X	Clear Register B to code all 0s (Asynchronous Operation)	2,3
				1	1	X	No Operation (Register B)	2
				1	X	1		
				1	0	0	Load Register B with contents of Register A	2

NOTE 1: Serial data is loaded into Register A MSB first, on edges as shown in timing diagram in commercial datasheet.
NOTE 2: 0=Logic Low, 1=Logic High, X=Don't care.
NOTE 3: CLR=0 asynchronously resets Register B to all 0s, but has no effect on Register A.

ORDERING INFORMATION:

01	J16	MX7543SQ/883B
01	L20	MX7543SE/883B
02	J16	MX7543TQ/883B
02	L20	MX7543TE/883B
03	J16	MX7543GTQ/883B
03	L20	MX7543GTE/883B

QUALITY ASSURANCE

Sampling and inspection procedures shall be in accordance with Mil-Prf-38535, Appendix A as Specified in Mil-Std-883.

Screening shall be in accordance with Method 5004 of Mil-Std-883. Burn-in test Method 1015:

1. Test Condition, A, B, C, or D.
2. T_A = +125°C, minimum.
3. Interim and final electrical test requirements shall be specified in Table 2.

Quality conformance inspection shall be in accordance with Method 5005 of Mil-Std-883, Including Groups A, B, C, and D inspection.

Group A inspection:

1. Tests as specified in Table 2.
2. Selected subgroups in Table 1, Method 5005 of Mil-Std-883 shall be omitted.

Group C and D inspections:

a. End-point electrical parameters shall be specified in Table 1.
b. Steady-state life test, Method 1005 of Mil-Std-883.
   1. Test condition A, B, C, D.
   2. T_A = +125°C, minimum.
   3. Test duration, 1000 hours, except as permitted by Method 1005 of Mil-Std-883.

TABLE 2. ELECTRICAL TEST REQUIREMENTS

Mil-Std-883 Test Requirements	Subgroups Per Method 5005, Table 1
Interim Electric Parameters Method 5004	1
Final Electrical Parameters Method 5005	1*, 2, 3
Group A Test Requirements Method 5005	1, 2, 3
Group C and D End-Point Electrical Parameters Method 5005	1

* PDA applies to Subgroup 1 only.

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Maxim Integrated:

MX7543JCWE+ MX7543JN+ MX7543SQ/883B MX7543GKCWE+ MX7543GKCWE+T MX7543GKEWE+ MX7543GKEWE+T MX7543GKN+ MX7543JCWE+T MX7543JP+ MX7543JP+T MX7543KCWE+ MX7543KCWE+T MX7543KN+ MX7543KP+ MX7543KP+T