500 MSPS Direct Digital Synthesizer with 10-Bit DAC

Data Sheet

AD9911

FEATURES

Patented SpurKiller technology
Multitone generation
Test-tone modulation
Up to 800 Mbps data throughput
Matched latencies for frequency/phase/amplitude changes
Linear frequency/phase/amplitude sweeping capability
Up to 16 levels of FSK, PSK, ASK
Programmable DAC full-scale current
32-bit frequency tuning resolution
14-bit phase offset resolution
10-bit output amplitude-scaling resolution
Software-/hardware-controlled power-down
Multiple device synchronization
Selectable 4× to 20× REF_CLK multiplier (PLL)
Selectable REF_CLK crystal oscillator
56-lead LFCSP

APPLICATIONS

Agile local oscillator
Test and measurement equipment
Commercial and amateur radio exciter
Radar and sonar
Test-tone generation
Fast frequency hopping
Clock generation

GENERAL DESCRIPTION

The AD9911 is a complete direct digital synthesizer (DDS). This device includes a high speed DAC with excellent wideband and narrowband spurious-free dynamic range (SFDR) as well as three auxiliary DDS cores without assigned digital-to-analog converters (DACs). These auxiliary channels are used for spur reduction, multitone generation, or test-tone modulation.

The AD9911 is the first DDS to incorporate SpurKiller technology and multitone generation capability. Multitone mode enables the generation up to four concurrent carriers; frequency, phase and amplitude can be independently programmed. Multitone generation can be used for system tests, such as inter-modulation distortion and receiver blocker sensitivity. SpurKilling enables customers to improve SFDR performance by reducing the magnitude of harmonic components and/or the aliases of those harmonic components.

Test-tone modulation efficiently enables sine wave modulation of amplitude on the output signal using one of the auxiliary DDS cores.

The AD9911 can perform modulation of frequency, phase, or amplitude (FSK, PSK, ASK). Modulation is implemented by storing profiles in the register bank and applying data to the profile pins. In addition, the AD9911 supports linear sweep of frequency, phase, or amplitude for applications such as radar and instrumentation.

(continued on Page 3)

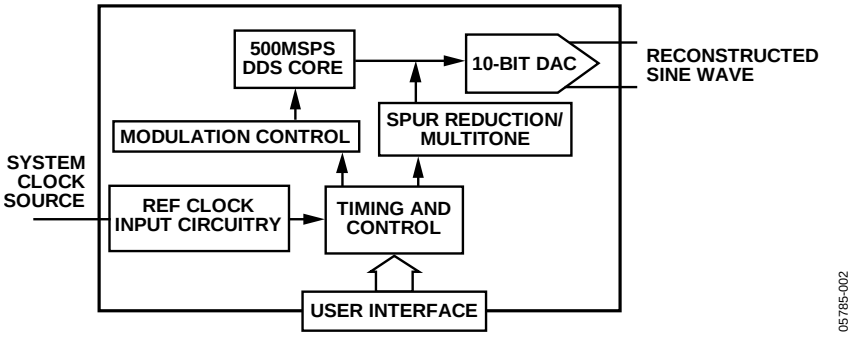

Figure 1. Basic Block Diagram

Rev. A **Document Feedback**

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TABLE OF CONTENTS

REVISION HISTORY

11/2016—Rev. 0 to Rev. A

Changes to Figure 43 Caption ... 25
Updated Outline Dimensions ... 41

5/2006—Revision 0: Initial Version

GENERAL DESCRIPTION

The DDS acts as a high resolution frequency divider with the REF_CLK as the input and the DAC providing the output. The REF_CLK input can be driven directly or used in combination with an integrated REF_CLK multiplier (PLL). The REF_CLK input also features an oscillator circuit to support an external crystal as the REF_CLK source. The crystal can be used in combination with the REF_CLK multiplier.

The AD9911 I/O port offers multiple configurations to provide significant flexibility. The I/O port offers an SPI-compatible mode of operation that is virtually identical to the SPI operation found in earlier Analog Devices DDS products.

Flexibility is provided by four data pins (Pin SDIO_0, Pin SDIO_1, Pin SDIO_2, and Pin SDIO_3) that allow four programmable modes of I/O operation.

The DAC output is supply referenced and must be terminated into AVDD by a resistor and an AVDD center-tapped transformer. The DAC has its own programmable reference to enable different full-scale currents.

The DDS core (the AVDD pins and the DVDD pins) is powered by a 1.8 V supply. The digital I/O interface (SPI) operates at 3.3 V and requires that the Pin DVDD_I/O (Pin 49) be connected to 3.3 V.

FUNCTIONAL BLOCK DIAGRAM

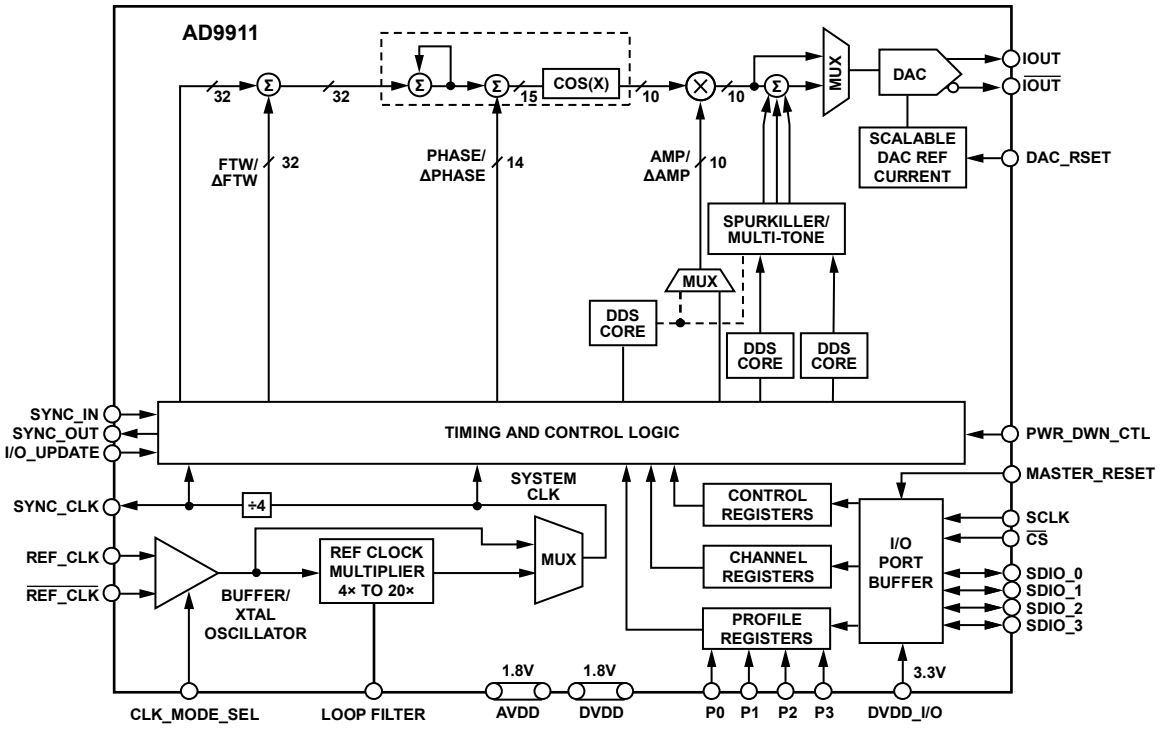


Figure 2. Functional Block Diagram

SPECIFICATIONS

AVDD and DVDD = 1.8 V ± 5%; DVDD_I/O = 3.3 V ± 5%; R_{SET} = 1.91 kΩ; external reference clock frequency = 500 MSPS (REF_CLK multiplier bypassed), unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
REF CLOCK INPUT CHARACTERISTICS					
Frequency Range					
REF_CLK Multiplier Bypassed	1		500	MHz	
REF_CLK Multiplier Enabled	10		125	MHz	
Internal VCO Output Frequency Range VCO Gain Bit Set[1]	255		500	MHz	
Internal VCO Output Frequency Range VCO Gain Bit Cleared	100		160	MHz	
Crystal REF_CLK Source Range	20		30	MHz	
Input Power Sensitivity	−5		+3	dBm	Measured at the pin (single-ended)
Input Voltage Bias Level		1.15		V	
Input Capacitance		2		pF	
Input Impedance		1500		Ω	
Duty Cycle with REF_CLK Multiplier Bypassed	45		55	%	
Duty Cycle with REF_CLK Multiplier Enabled	35		65	%	
CLK Mode Select (Pin 24) Logic 1 V	1.25		1.8	V	1.8 V digital input logic
CLK Mode Select (Pin 24) Logic 0 V			0.5	V	1.8 V digital input logic
DAC OUTPUT CHARACTERISTICS					Must be referenced to AVDD
Full-Scale Output Current		10		mA	10 mA is set by R_{SET} = 1.91 kΩ
Gain Error	−10		+10	%FS	
Output Current Offset		1	25	μA	
Differential Nonlinearity		±0.5		LSB	
Integral Nonlinearity		±1.0		LSB	
Output Capacitance		3		pF	
Voltage Compliance Range	AVDD – 0.50		AVDD + 0.50	V	
WIDEBAND SFDR					The frequency range for wideband SFDR is defined as dc to Nyquist
1 MHz to 20 MHz Analog Output		−65		dBc	
20 MHz to 60 MHz Analog Output		−62		dBc	
60 MHz to 100 MHz Analog Output		−59		dBc	
100 MHz to 150 MHz Analog Output		−56		dBc	
150 t MHz to 200 MHz Analog Output		−53		dBc	
WIDEBAND SFDR Improvement Spur Reduction Enabled					Programs devices on an individual basis to enable spur reduction. See the SpurKiller/Multitone Mode section.
60 MHz to 100 MHz Analog Output		8		dBc	
100 MHz to 150 MHz Analog Output		15		dBc	
150 MHz to 200 MHz Analog Output		12		dBc	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
NARROWBAND SFDR					
1.1 MHz Analog Output (±10 kHz)		−90		dBc	
1.1 MHz Analog Output (±50 kHz)		−88		dBc	
1.1 MHz Analog Output (±250 kHz)		−86		dBc	
1.1 MHz Analog Output (±1 MHz)		−85		dBc	
15.1 MHz Analog Output (±10 kHz)		−90		dBc	
15.1 MHz Analog Output (±50 kHz)		−87		dBc	
15.1 MHz Analog Output (±250 kHz)		−85		dBc	
15.1 MHz Analog Output (±1 MHz)		−83		dBc	
40.1 MHz Analog Output (±10 kHz)		−90		dBc	
40.1 MHz Analog Output (±50 kHz)		−87		dBc	
40.1 MHz Analog Output (±250 kHz)		−84		dBc	
40.1 MHz Analog Output (±1 MHz)		−82		dBc	
75.1 MHz Analog Output (±10 kHz)		−87		dBc	
75.1 MHz Analog Output (±50 kHz)		−85		dBc	
75.1 MHz Analog Output (±250 kHz)		−83		dBc	
75.1 MHz Analog Output (±1 MHz)		−82		dBc	
100.3 MHz Analog Output (±10 kHz)		−87		dBc	
100.3 MHz Analog Output (±50 kHz)		−85		dBc	
100.3 MHz Analog Output (±250 kHz)		−83		dBc	
100.3 MHz Analog Output (±1 MHz)		−81		dBc	
200.3 MHz Analog Output (±10 kHz)		−87		dBc	
200.3 MHz Analog Output (±50 kHz)		−85		dBc	
200.3 MHz Analog Output (±250 kHz)		−83		dBc	
200.3 MHz Analog Output (±1 MHz)		−81		dBc	
PHASE NOISE CHARACTERISTICS					
Residual Phase Noise @ 15.1 MHz (f_{OUT})					
1 kHz Offset		−150		dBc/Hz	
10 kHz Offset		−159		dBc/Hz	
100 kHz Offset		−165		dBc/Hz	
1 MHz Offset		−165		dBc/Hz	
Residual Phase Noise @ 40.1 MHz (f_{OUT})					
1 kHz Offset		−142		dBc/Hz	
10 kHz Offset		−151		dBc/Hz	
100 kHz Offset		−160		dBc/Hz	
1 MHz Offset		−162		dBc/Hz	
Residual Phase Noise @ 75.1 MHz (f_{OUT})					
1 kHz Offset		−135		dBc/Hz	
10 kHz Offset		−146		dBc/Hz	
100 kHz Offset		−154		dBc/Hz	
1 MHz Offset		−157		dBc/Hz	
Residual Phase Noise @ 100.3 MHz (f_{OUT})					
1 kHz Offset		−134		dBc/Hz	
10 kHz Offset		−144		dBc/Hz	
100 kHz Offset		−152		dBc/Hz	
1 MHz Offset		−154		dBc/Hz	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Residual Phase Noise @ 15.1 MHz (f_{OUT}) with REF_CLK Multiplier Enabled 5×					
1 kHz Offset		–139		dBc/Hz	
10 kHz Offset		–149		dBc/Hz	
100 kHz Offset		–153		dBc/Hz	
1 MHz Offset		–148		dBc/Hz	
Residual Phase Noise @ 40.1 MHz (f_{OUT}) with REF_CLK Multiplier Enabled 5×					
1 kHz Offset		–130		dBc/Hz	
10 kHz Offset		–140		dBc/Hz	
100 kHz Offset		–145		dBc/Hz	
1 MHz Offset		–139		dBc/Hz	
Residual Phase Noise @ 75.1 MHz (f_{OUT}) with REF_CLK Multiplier Enabled 5×					
1 kHz Offset		–123		dBc/Hz	
10 kHz Offset		–134		dBc/Hz	
100 kHz Offset		–138		dBc/Hz	
1 MHz Offset		–132		dBc/Hz	
Residual Phase Noise @ 100.3 MHz(f_{OUT}) with REF_CLK Multiplier Enabled 5×					
1 kHz Offset		–120		dBc/Hz	
10 kHz Offset		–130		dBc/Hz	
100 kHz Offset		–135		dBc/Hz	
1 MHz Offset		–129		dBc/Hz	
Residual Phase Noise @ 15.1 MHz (f_{OUT}) with REF_CLK Multiplier Enabled 20×					
1 kHz Offset		–127		dBc/Hz	
10 kHz Offset		–136		dBc/Hz	
100 kHz Offset		–139		dBc/Hz	
1 MHz Offset		–138		dBc/Hz	
Residual Phase Noise @ 40.1 MHz (f_{OUT}) with REF_CLK Multiplier Enabled 20×					
1 kHz Offset		–117		dBc/Hz	
10 kHz Offset		–128		dBc/Hz	
100 kHz Offset		–132		dBc/Hz	
1 MHz Offset		–130		dBc/Hz	
Residual Phase Noise @ 75.1 MHz (f_{OUT}) with REF_CLK Multiplier Enabled 20×					
1 kHz Offset		–110		dBc/Hz	
10 kHz Offset		–121		dBc/Hz	
100 kHz Offset		–125		dBc/Hz	
1 MHz Offset		–123		dBc/Hz	
Residual Phase Noise @ 100.3 MHz (f_{OUT}) with REF_CLK Multiplier Enabled 20×					
1 kHz Offset		–107		dBc/Hz	
10 kHz Offset		–119		dBc/Hz	
100 kHz Offset		–121		dBc/Hz	
1 MHz Offset		–119		dBc/Hz	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
I/O PORT TIMING CHARACTERISTICS					
Maximum Frequency Clock (SCLK)			200	MHz	
Minimum SCLK Pulse Width Low (t_{PWL})	1.6			ns	
Minimum SCLK Pulse Width High (t_{PWH})	2.2			ns	
Minimum Data Set-Up Time (t_{DS})	2.2			ns	
Minimum Data Hold Time	0			ns	
Minimum CSB Set-Up Time (t_{PRE})	1.0			ns	
Minimum Data Valid Time for Read Operation	12			ns	
MISCELLANEOUS TIMING CHARACTERISTICS					
Master_Reset Minimum Pulse Width	1				Minimum pulse width = 1 sync clock period
I/O_Update Minimum Pulse Width	1				Minimum pulse width = 1 sync clock period
Minimum Set-Up Time (I/O_Update to SYNC_CLK)	4.8			ns	Rising edge to rising edge
Minimum Hold Time (I/O_Update to SYNC_CLK)	0			ns	Rising edge to rising edge
Minimum Set-Up Time (Profile Inputs to SYNC_CLK)	5.4			ns	
Minimum Hold Time (Profile Inputs to SYNC_CLK)	0			ns	
Minimum Set-Up Time (SDIO Inputs to SYNC_CLK)	2.5			ns	
Minimum Hold Time (SDIO Inputs to SYNC_CLK)	0			ns	
Propagation Delay Between REF_CLK and SYNC_CLK	2.25	3.5	5.5	ns	
CMOS LOGIC INPUT					
V_{IH}	2.0			V	
V_{IL}			0.8	V	
Logic 1 Current		3	12	µA	
Logic 0 Current		−12		µA	
Input Capacitance		2		pF	
CMOS LOGIC OUTPUTS (1 mA Load)					
V_{OH}	2.7			V	
V_{OL}			0.4	V	
POWER SUPPLY					
Total Power Dissipation—Single-Tone Mode		241		mW	Dominated by supply variation
Total Power Dissipation—With Sweep Accumulator		241		mW	Dominated by supply variation
Total Power Dissipation—3 Spur Reduction/Multitone Channels Active		351		mW	Dominated by supply variation
Total Power Dissipation—Test-Tone Modulation		264		mW	Dominated by supply variation
Total Power Dissipation—Full Power Down		1.8		mW	
IAVDD—Single-Tone Mode		73		mA	
IAVDD— Sweep Accumulator, REF_CLK Multiplier, and 10-Bit Output Scalar Enabled		73		mA	
IDVDD—Single-Tone Mode		50		mA	
IDVDD—Sweep Accumulator, REF_CLK Multiplier, and 10-Bit Output Scalar Enabled		50		mA	
IDVDD_I/O		40		mA	IDVDD = read
IDVDD_I/O		30		mA	IDVDD = write
IAVDD Power-Down Mode		0.7		mA	
IDVDD Power-Down Mode		1.1		mA	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DATA LATENCY (PIPELINE DELAY) SINGLE-TONE MODE[2, 3]					
Frequency, Phase, and Amplitude Words to DAC Output with Matched Latency Enabled	29			SYSCLK cycles	
Frequency Word to DAC Output with Matched Latency Disabled	29			SYSCLK cycles	
Phase Offset Word to DAC Output with Matched Latency Disabled	25			SYSCLK cycles	
Amplitude Word to DAC Output with Matched Latency Disabled	17			SYSCLK cycles	
DATA LATENCY (PIPELINE DELAY) MODULATION MODE[4]					
Frequency Word to DAC Output	34			SYSCLK Cycles	
Phase Offset Word to DAC Output	29			SYSCLK Cycles	
Amplitude Word to DAC Output	21			SYSCLK Cycles	
DATA LATENCY (PIPELINE DELAY) LINEAR SWEEP MODE[4]					
Frequency Rising/Falling Delta Tuning Word to DAC Output	41			SYSCLK Cycles	
Phase Offset Rising/Falling Delta Tuning Word to DAC Output	37			SYSCLK Cycles	
Amplitude Rising/Falling Delta Tuning Word to DAC Output	29			SYSCLK Cycles	

[1] For the VCO frequency range of 160 MHz to 255 MHz, the appropriate setting for the VCO gain bit is dependent upon supply, temperature and process. Therefore, in a production environment this frequency band must be avoided.
[2] Data latency is reference to the I/O_UPDATE pin.
[3] Data latency is fixed and the units are system clock (SYSCLK) cycles
[4] Data latency is referenced to a profile change.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Maximum Junction Temperature	150°C
DVDD_I/O (Pin 49)	4 V
AVDD, DVDD	2 V
Digital Input Voltage (DVDD_I/O = 3.3 V)	−0.7 V to +4 V
Digital Output Current	5 mA
Storage Temperature	−65°C to +150°C
Operating Temperature	−40°C to +85°C
Lead Temperature (10 sec Soldering)	300°C
θ_{JA}	21°C/W
θ_{JC}	2°C/W

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

EQUIVALENT INPUT AND OUTPUT CIRCUITS

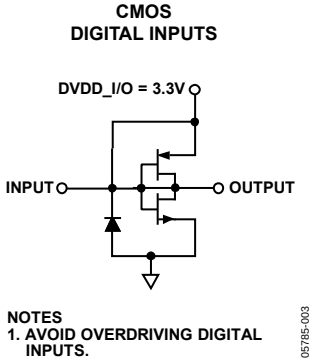


Figure 3. CMOS Digital Inputs

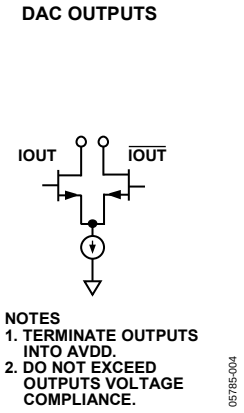


Figure 4. DAC Outputs

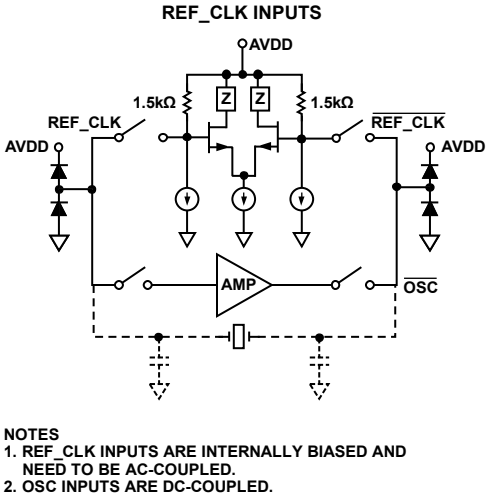


Figure 5. REF_CLK Inputs

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

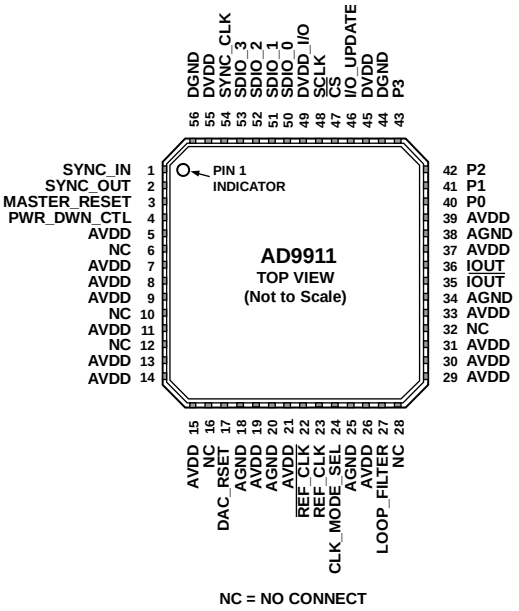


Figure 6. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	I/O	Description
1	SYNC_IN	I	Synchronizes Multiple AD9911 Devices. Connects to the SYNC_OUT pin of the master AD9911 device.
2	SYNC_OUT	O	Synchronizes Multiple AD9911 Devices. Connects to the SYNC_IN pin of the slave AD9911 device.
3	MASTER_RESET	I	Active High Reset Pin. Asserting this pin forces the internal registers to the default state shown in the Register Map section.
4	PWR_DWN_CTL	I	External Power-Down Control. See the Power Down Functions section for details.
5, 7, 8, 9, 11, 13, 14, 15, 19, 21, 26, 29, 30, 31, 33, 37, 39	AVDD	I	Analog Power Supply Pins (1.8 V).
18, 20, 25, 34, 38	AGND	I	Analog Ground Pins.
45, 55	DVDD	I	Digital Power Supply Pins (1.8 V).
44, 56	DGND	I	Digital Power Ground Pins.
35	$\overline{\text{IOUT}}$	O	Complementary DAC Output. Terminates into AVDD.
36	IOUT	O	True DAC Output. Terminates into AVDD.
17	DAC_RSET	I	Establishes the Reference Current for the DAC. A 1.91 kΩ resistor (nominal) is connected from Pin 17 to AGND.
22	$\overline{\text{REF\_CLK}}$	I	Complementary Reference Clock/Oscillator Input. When the REF_CLK is operated in single-ended mode, this pin should be decoupled to AVDD or AGND with a 0.1 µF capacitor.
23	REF_CLK	I	Reference Clock/Oscillator Input. When the REF_CLK operates in single-ended mode, Pin 23 is the input. See the Modes of Operation section for the reference clock configuration.
24	CLK_MODE_SEL	I	Control Pin for the Oscillator. CAUTION: Do not drive this pin beyond 1.8 V. When high (1.8 V), the oscillator is enabled to accept a crystal as the REF_CLK source. When low, the oscillator is bypassed.
27	LOOP_FILTER	I	Connects to the External Zero Compensation Network of the PLL Loop Filter. Typically, the network consists of a 0 Ω resistor in series with a 680 pF capacitor tied to AVDD.

Pin No.	Mnemonic	I/O	Description
6, 10, 12, 16, 28, 32	NC	N/A	No Connection. Analog Devices recommends leaving these pins floating.
40, 41, 42, 43	P0, P1, P2, P3	I	These data pins are used for modulation (FSK, PSK, ASK), start/stop for the sweep accumulator, and ramping up/down the output amplitude. Any toggle of these data inputs is equivalent to an I/O_UPDATE. The data is synchronous to the SYNC_CLK (Pin 54). The data inputs must meet the set-up and hold time requirements to the SYNC_CLK. This guarantees a fixed pipeline delay of data to the DAC output; otherwise, a ±1 SYNC_CLK period of uncertainty occurs. The functionality of these pins is controlled by profile pin configuration (PPC) bits in Register FR1 <12:14>.
46	I/O_UPDATE	I	A rising edge triggers data transfer from the I/O port buffer to active registers. I/O_UPDATE is synchronous to the SYNC_CLK (Pin 54). I/O_UPDATE must meet the set-up and hold time requirements to the SYNC_CLK to guarantee a fixed pipeline delay of data to DAC output. If not, a ±1 SYNC_CLK period of uncertainty occurs. The minimum pulse width is one SYNC_CLK period.
47	$\overline{CS}$	I	The active low chip select allows multiple devices to share a common I/O bus (SPI).
48	SCLK	I	Data Clock for I/O Operations. Data bits are written on the rising edge of SCLK and read on the falling edge of SCLK.
49	DVDD_I/O	I	3.3 V Digital Power Supply for SPI Port and Digital I/O.
50	SDIO_0	I/O	Data pin SDIO_0 is dedicated to the I/O port only.
51, 52, 53	SDIO_1, SDIO_2, SDIO_3	I/O	Data pins SDIO_1:3 can be used for the I/O port or to initiate a ramp up/ramp down (RU/RD) of the DAC output amplitude.
54	SYNC_CLK	O	The SYNC_CLK, which runs at ¼ the system clock rate, can be disabled. I/O_UPDATE and profile changes (Pin 40 to Pin 43) are synchronous to the SYNC_CLK. To guarantee a fixed pipeline delay of data to DAC output, I/O_UPDATE and profile changes (Pin 40 to Pin 43) must meet the set-up and hold time requirements to the rising edge of SYNC_CLK. If not, a ±1 SYNC_CLK period of uncertainty exists.

TYPICAL PERFORMANCE CHARACTERISTICS

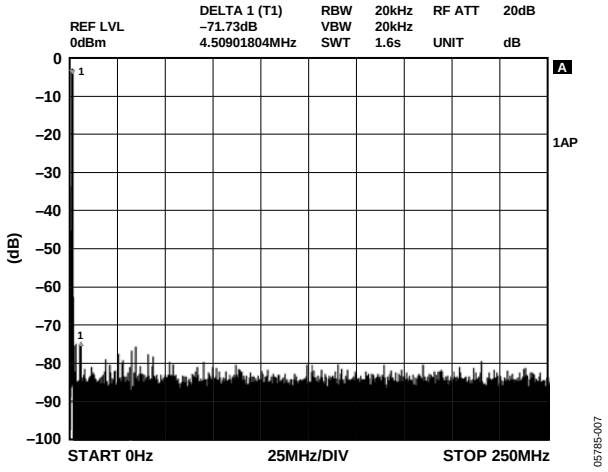


Figure 7. f_{OUT} = 1.1 MHz, f_{CLK} = 500 MSPS, Wideband SFDR

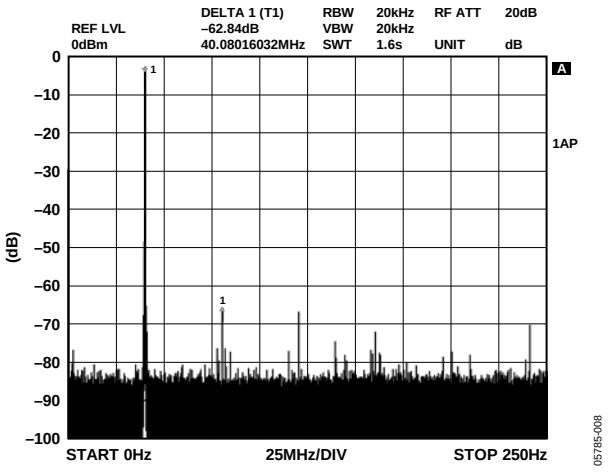


Figure 8. f_{OUT} = 40.1 MHz, f_{CLK} = 500 MSPS, Wideband SFDR

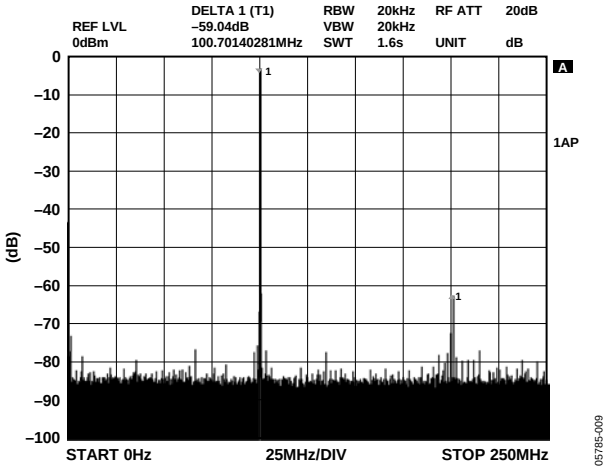


Figure 9. f_{OUT} = 100.3 MHz, f_{CLK} = 500 MSPS, Wideband SFDR

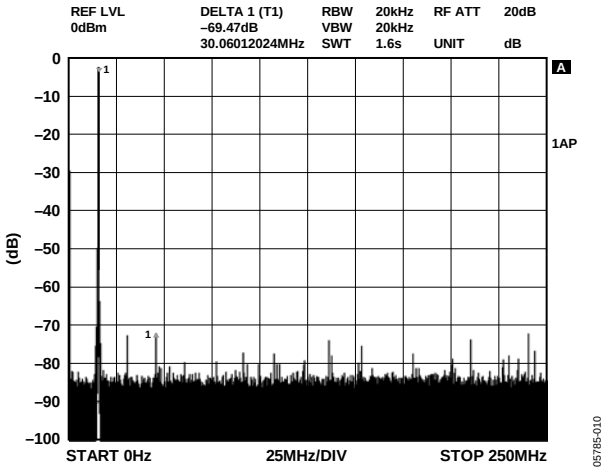


Figure 10. f_{OUT} = 15.1 MHz, f_{CLK} = 500 MSPS, Wideband SFDR

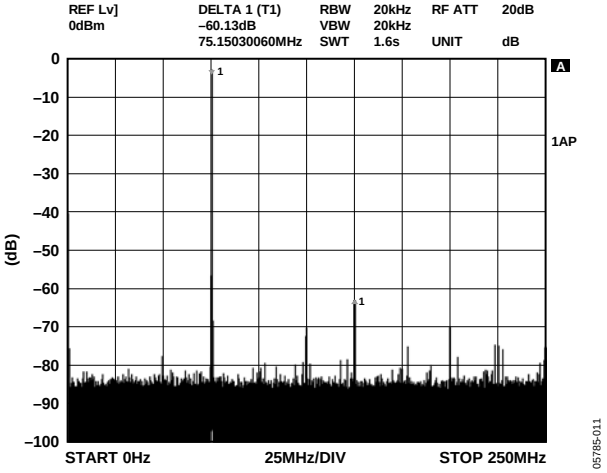


Figure 11. f_{OUT} = 75.1 MHz, f_{CLK} = 500 MSPS, Wideband SFDR

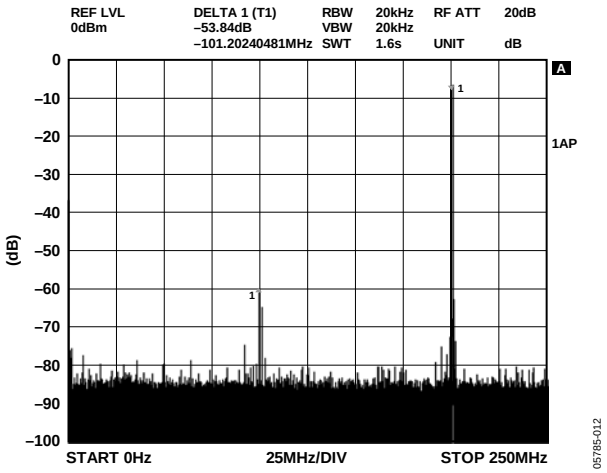


Figure 12. f_{OUT} = 200.3 MHz, f_{CLK} = 500 MSPS, Wideband SFDR

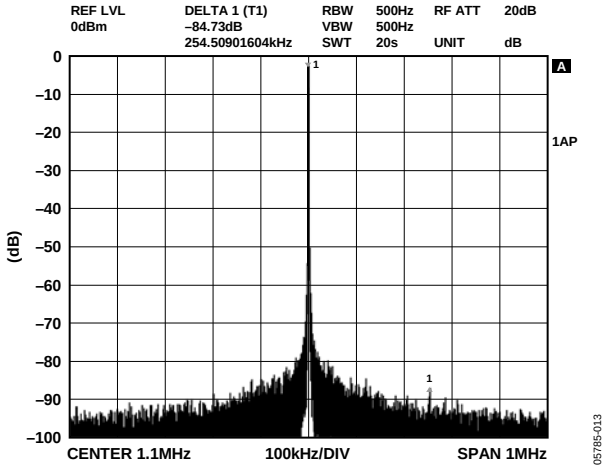


Figure 13. f_{OUT} = 1.1 MHz, f_{CLK} = 500 MSPS, NBSFDR, ±1 MHz

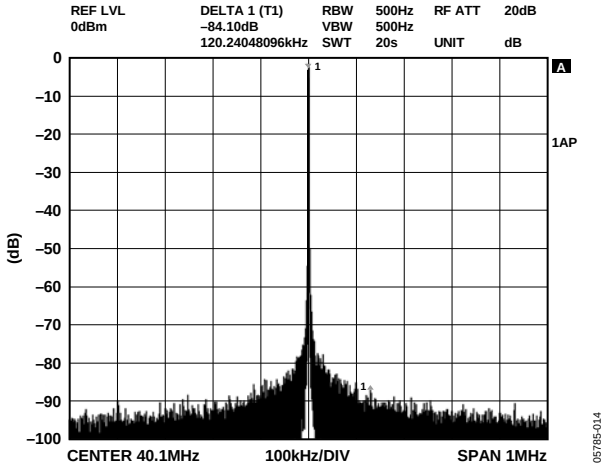


Figure 14. f_{OUT} = 40.1 MHz, f_{CLK} = 500 MSPS, NBSFDR, ±1 MHz

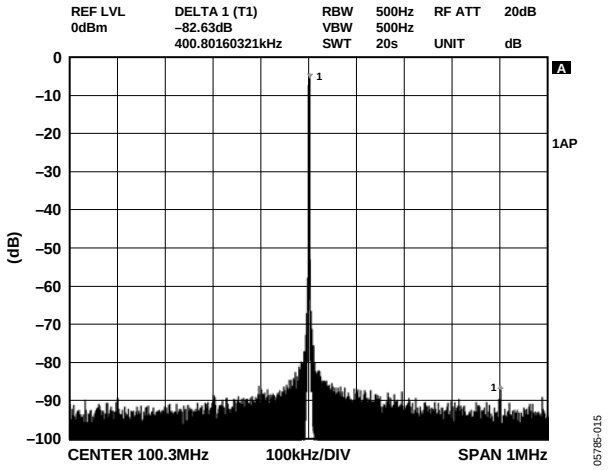


Figure 15. f_{OUT} = 100.3 MHz, f_{CLK} = 500 MSPS, NBSFDR, ±1 MHz

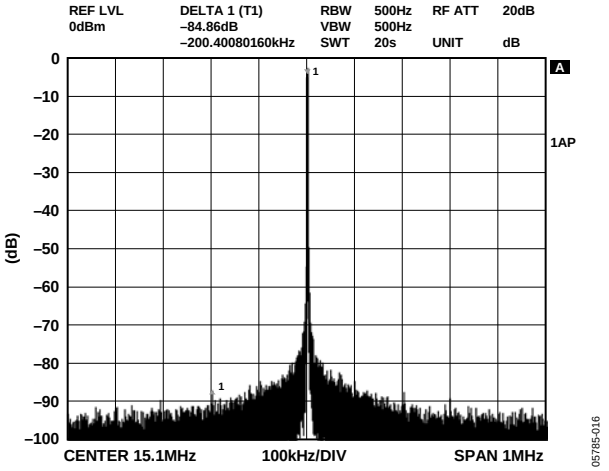


Figure 16. f_{OUT} = 15.1 MHz, f_{CLK} = 500 MSPS, NBSFDR, ±1 MHz

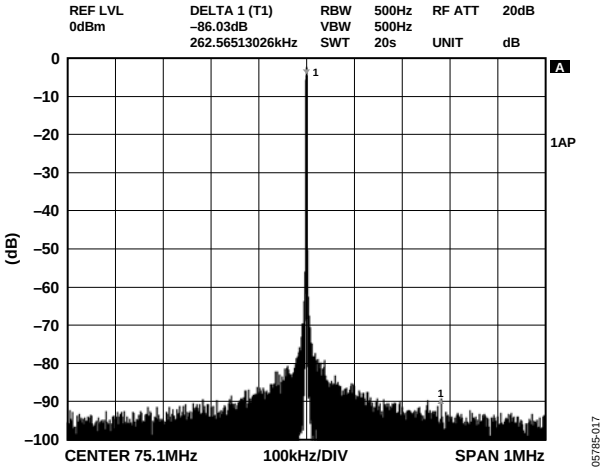


Figure 17. f_{OUT} = 75.1 MHz, f_{CLK} = 500 MSPS, NBSFDR, ±1 MHz

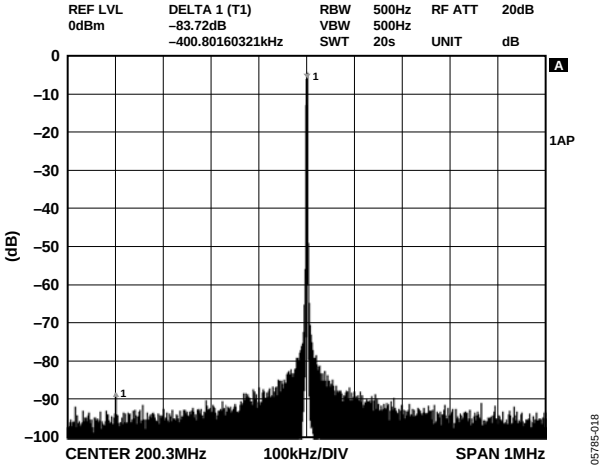


Figure 18. f_{OUT} = 200.3MHz, f_{CLK} = 500 MSPS, NBSFDR, ±1 MHz

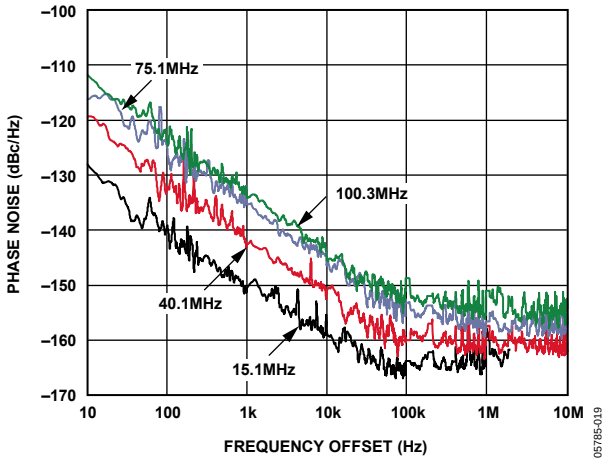


Figure 19. Residual Phase Noise (SSB) with f_{OUT} = 15.1 MHz, 40.1 MHz, 75.1 MHz, 100.3 MHz, f_{CLK} = 500 MHz with REF_CLK Multiplier Bypassed

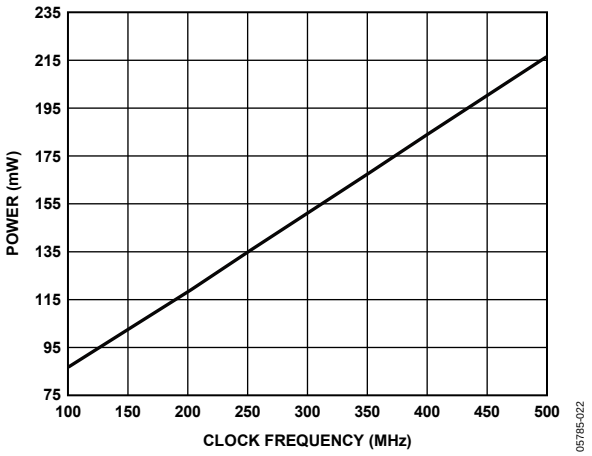


Figure 22. Power vs. System Clock Frequency

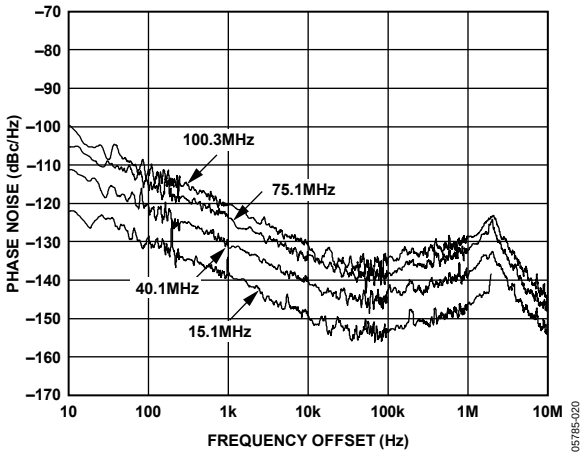


Figure 20. Residual Phase Noise (SSB) with f_{OUT} = 15.1 MHz, 40.1 MHz, 75.1 MHz, 100.3 MHz, f_{CLK} = 500 MHz with REF_CLK Multiplier = 5×

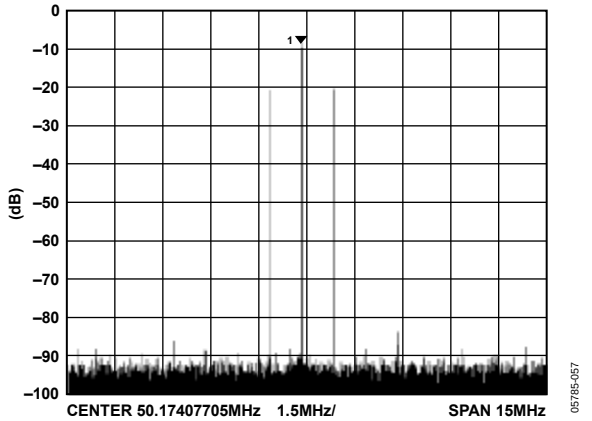


Figure 23. Amplitude Modulation Using Primary Channel (CH1 = 50 MHz) and One Auxiliary Channel (CH0 = 1 MHz)

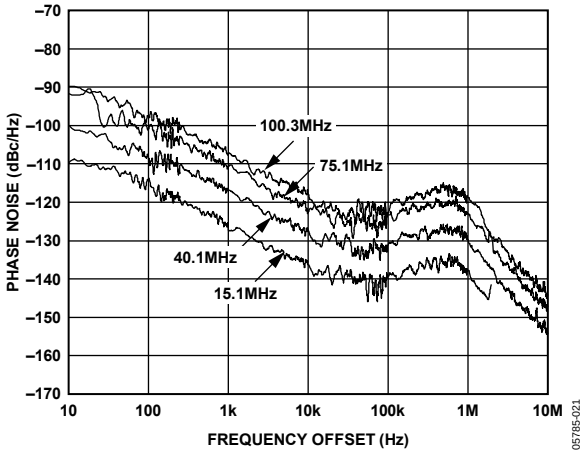


Figure 21. Residual Phase Noise(SSB) with f_{OUT} = 15.1 MHz, 40.1 MHz, 75.1 MHz, 100.3 MHz, f_{CLK} = 500 MHz with REF_CLK Multiplier = 20×

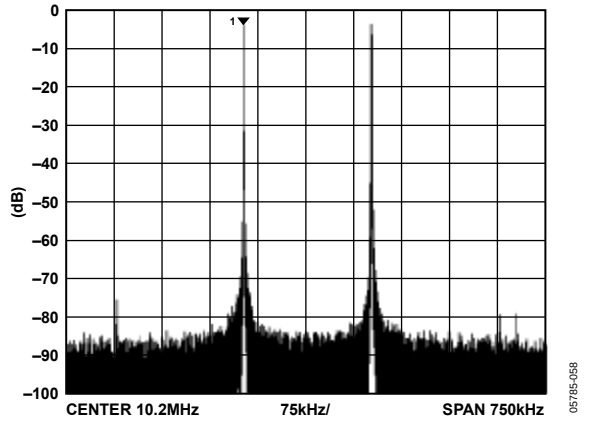


Figure 24. Two-Tone Generation Using Primary Channel (CH1 = 10.1 MHz) and One Auxiliary Channel (CH0 = 10.3 MHz)

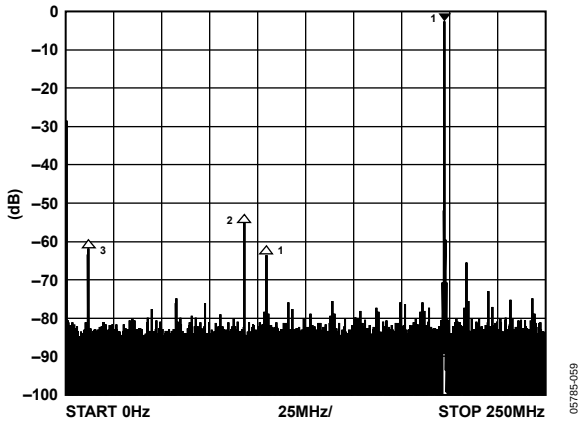


Figure 25. SpurKiller Disabled and Three Spurs Identified

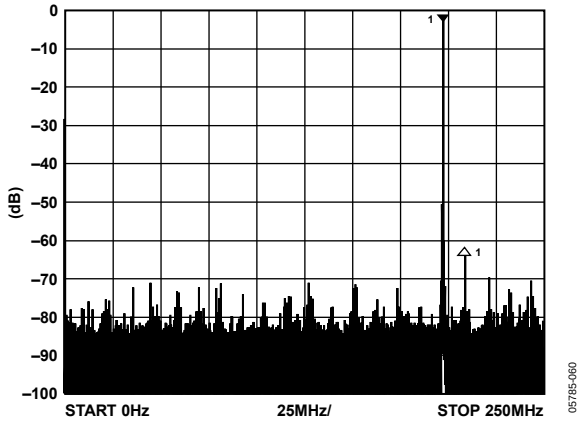


Figure 26. SpurKiller Enabled with Three Spurs Reduced (see Figure 25)

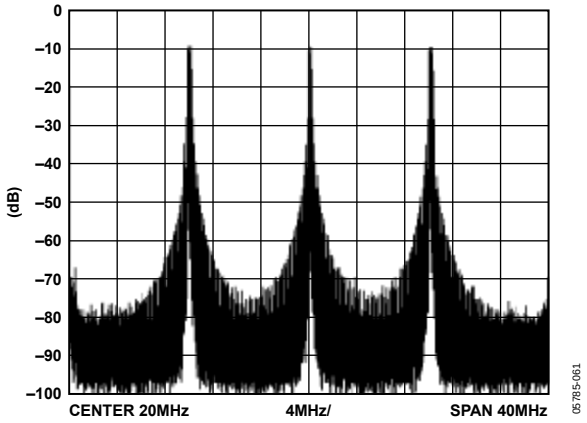


Figure 27. Three Auxiliary Channels Perform Two-Level FSK with Profile Pins. The three carriers are set to 10 MHz, 20 MHz, and 30 MHz using all three auxiliary channels.

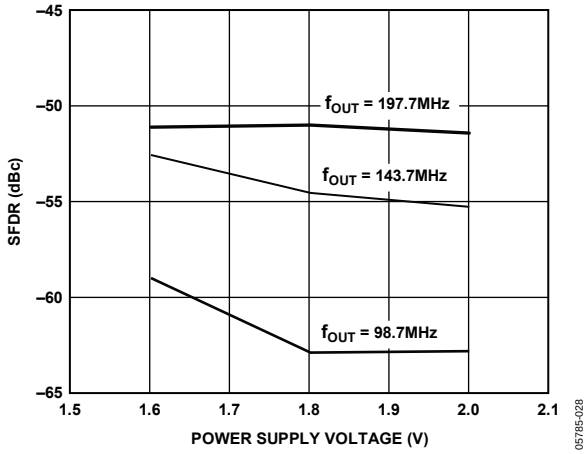


Figure 28. SFDR vs. Supply Voltage (AVDD)

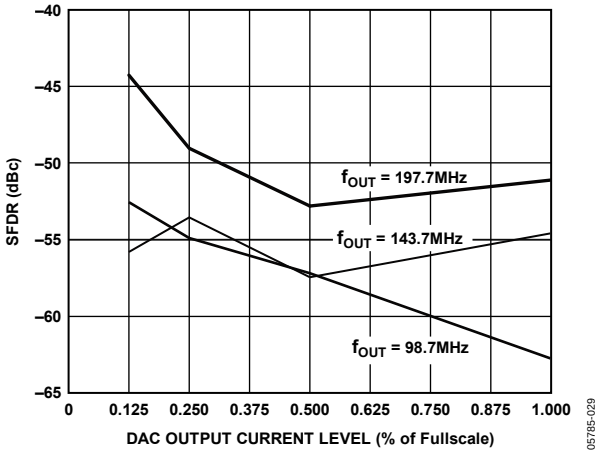


Figure 29. SFDR vs. DAC Output Current

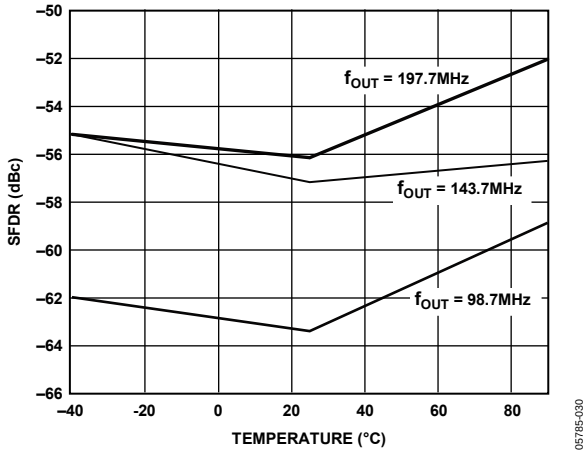


Figure 30. SFDR vs. Temperature

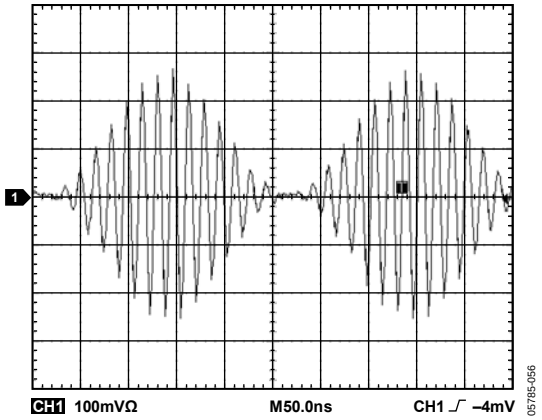


Figure 31. Primary Channel (62 MHz) 100% Amplitude Modulated by CH0 (4 MHz)

APPLICATION CIRCUITS

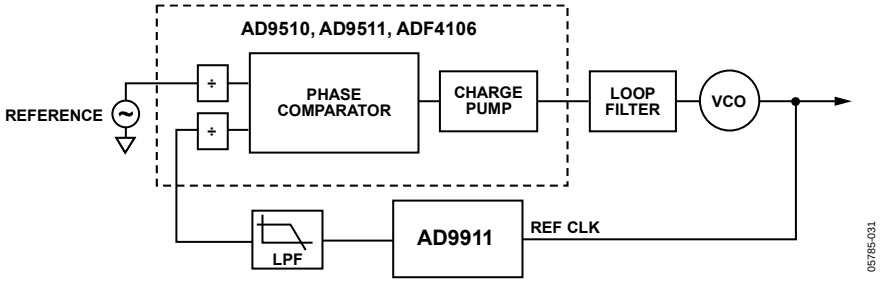


Figure 32. DDS in PLL Feedback Locking to Reference Offering Fine Frequency and Delay Adjust Tuning

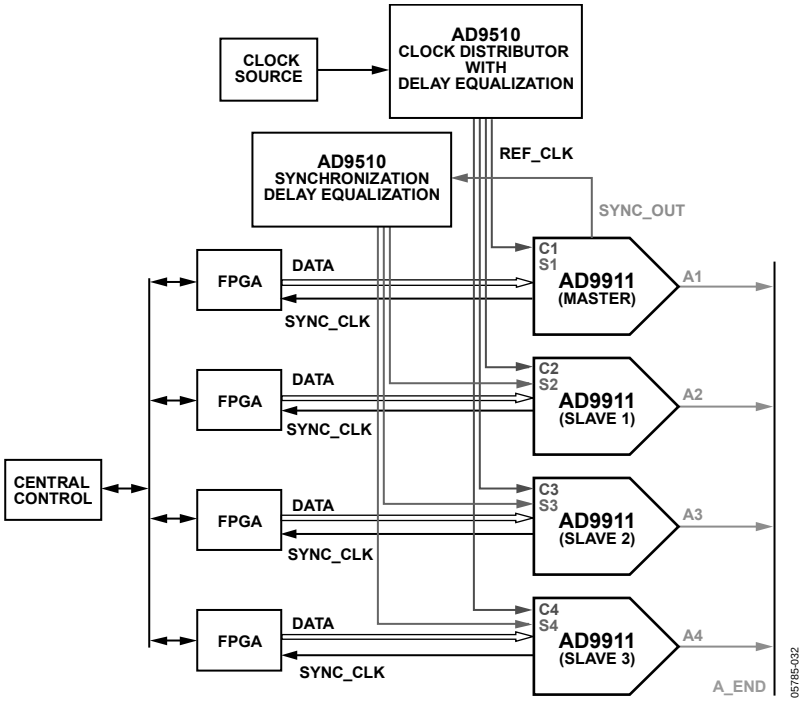


Figure 33. Synchronizing Multiple Devices to Increase Channel Capacity Using the AD9510 as a Clock Distributor for the Reference and SYNC Clock

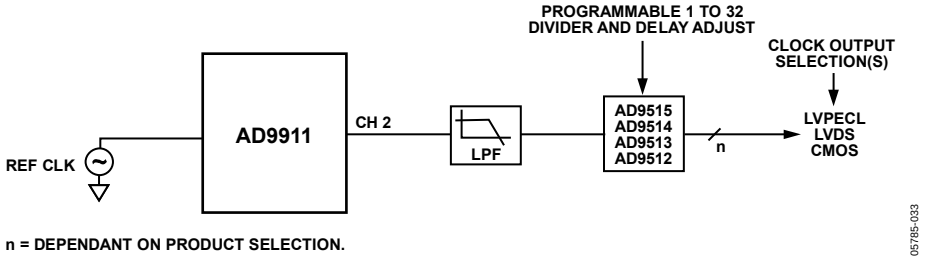


Figure 34. Clock Generation Circuit Using the AD951x Series of Clock Distribution Chips

THEORY OF OPERATION

PRIMARY DDS CORE

The AD9911 has one complete DDS (Channel 1) that consists of a 32-bit phase accumulator, a phase-to-amplitude converter, and 10-bit DAC. Together, these digital blocks generate a sine wave when the phase accumulator is clocked and the phase increment value (frequency tuning word) is greater than 0. The phase-to-amplitude converter translates phase information to amplitude information by a cos (θ) operation.

The output frequency (f_O) of the DDS is a function of the rollover rate of the phase accumulator. The exact relationship is shown in the following equation:

$$f_O = \frac{(FTW)(f_S)}{2^{32}} \; with \; 0 \le FTW \le 2^{31}$$

where:
f_S = the system clock rate.
FTW = the frequency tuning word.
2^{32} represents the capacity of the phase accumulator'.

The DDS core architecture also supports the capability to phase offset the output signal. This is performed by the channel phase offset word (CPOW). The CPOW is a 14-bit register that stores a phase offset value. This value is added to the output of the phase accumulator to offset the current phase of the output signal. The exact value of phase offset is given by the following equation:

$$\Phi = \left(\frac{CPOW}{2^{14}} \right) \times 360°$$

SPURKILLER/MULTITONE MODE AND TEST-TONE MODULATION

The AD9911 is equipped with three auxiliary DDS cores (Channel 0, Channel 2, and Channel 3). Because these channels do not have a DAC, there is no direct output. Instead, these channels are designed to implement either spur reduction/ multiple tones or test-tone modulation on the output spectrum for Channel 1.

When using multitone mode, the device can output up to four distinct carriers concurrently. This is possible via the summing node for all four DDS cores. The frequency, phase and amplitude of each tone is adjustable. The maximum amplitude of the auxiliary channels is −12 db below the primary channel's maximum amplitude to prevent overdriving the DAC input. The primary channel's amplitude can be adjusted down to achieve equal amplitude for all carriers.

When using SpurKiller mode, up to three spurs in the output spectrum for Channel 1 are reducible (one per auxiliary channel). To match an exact frequency using the three channels, the spur must be harmonically related to the fundamental frequency or the tuning word for Channel 1. A nonharmonic spur may be impossible to match frequency.

Spur reduction is not as effective at lower fundamental frequencies where SFDR performance is already very good. The benefits of SpurKiller channels are virtually nonexistent when the output frequency is less than 20% of the sampling frequency.

Test-tone modulation is similar to amplitude modulation options of a signal generator. For test-tone modulation, auxiliary DDS Channel 0 is assigned to implement amplitude sinusoidal modulated waveforms of the primary channel. This function is programmed using internal registers.

D/A CONVERTER

The AD9911 incorporates a 10-bit current output DAC. The DAC converts a digital code (amplitude) into a discrete analog quantity. The DAC current outputs can be modeled as a current source with high output impedance (typically 100 kΩ). Unlike many DACs, these current outputs require termination into AVDD via a resistor or a center-tapped transformer for expected current flow.

The DAC has complementary outputs that provide a combined full-scale output current (I_{OUT} + I_{OUTB}). The outputs always sink current.

The full-scale current is controlled by means of an external resistor (R_{SET}) and the scalable DAC current control bits discussed in the Modes of Operation section. The Resistor R_{SET} is connected between the DAC_RSET pin and analog ground (AGND). The full-scale current is inversely proportional to the resistor value as follows:

$$I_{OUT} = \frac{18.91}{R_{SET}}$$

Limiting the output to 10 mA with an R_{SET} of 1.9 kΩ provides optimal spurious-free dynamic range (SFDR) performance. The DAC output voltage compliance range is AVDD + 0.5 V to AVDD − 0.5 V. Voltages developed beyond this range can cause excessive harmonic distortion. Proper attention should be paid to the load termination to keep the output voltage within its compliance range. Exceeding this range could damage the DAC output circuitry.

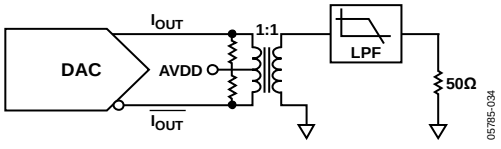


Figure 35. Typical DAC Output Termination Configuration

MODES OF OPERATION

SINGLE-TONE MODE

To configure the AD9911 in single-tone mode, the auxiliary DDS cores (CH0, CH2, and CH3) must be disabled by using the channel enable bits and digital powering down (CSR bit <7>) the three auxiliary DDS cores. Only CH1 remains enabled. See the Register Maps section for a description of the channel enable bits in the channel select register or CSR (Register 0x00). The channel enable bits are enabled or disabled immediately after the CSR data byte is written. An I/O_UPDATE is not required for channel enable bits.

The two main registers used in this mode, Register 0x04 and Register 0x05, contain the frequency tuning word and the phase offset word for CH1. The following is a basic protocol to program a frequency tuning word and/or phase offset word for CH1.

1. Power up the AD9911 and issue a master reset. A master reset places the part in single-bit mode for serial programming operations (refer to the I/O Modes of Operation section). The frequency tuning word and phase offset word for CH1 defaults to 0.
2. Disable CH0, CH2, CH3 and enable CH1 using the channel enable bits in Register 0x00.
3. Using the I/O port, program the desired frequency tuning word (Register 0x04) and/or the phase offset word (Register 0x05) for CH1.
4. Send an I/O update signal. CH1 should output its programmed frequency and/or phase offset value, after a pipeline delay (see Table 1).

Single-Tone Mode—Matched Pipeline Delay

In single-tone mode, the AD9911 offers matched pipeline delay to the DAC input for all frequency, phase, and amplitude changes. The result is that frequency, phase, and amplitude changes arrive at the DAC input simultaneously. The feature is enabled by asserting the match pipeline delay bit found in the channel function register (CSR) (Register 0x03). This feature is available in single-tone mode only.

SPURKILLER/MULTITONE MODE

For both SpurKiller and multitone mode, the frequency, phase and amplitude settings of the auxiliary channels and the primary channel use Register 0x04 Bits <31:0> for frequency and Register 0x05 Bits <13:0> for phase. Note the channel enable bits in the CSR register must be use to distinguish the content of each channel. See the I/O Port section for details.

For multitone mode, the digital content of the three auxiliary DDS channels are summed with the primary channel. Each tone can be individually programmed for frequency, phase and amplitude as well as individually modulated using the profile pins in shift-keying modulation. See Figure 24 and Figure 27 for examples.

Note the data align bits in Register 0x03 Bits <18:16>, provide a coarse amplitude adjust setting for the auxiliary channels. These bits default to clear; for multitone mode these bit should typically be set.

For SpurKiller mode, the digital contents of the three auxiliary DDS channels are attenuated and summed with the primary channel. In this manner, harmonic spurs from the DAC can be reduced. This is accomplished by matching the frequency of the harmonic component, the amplitude, and the phase (180° offset) of the desired spur on one of the SpurKiller channels.

Bench level observations and manipulation are required to establish the optimal parameter settings for the SpurKiller channel(s). The parameters are dependent on the fundamental frequency and system clock frequency. The repeatability of these settings on a unit-to-unit basis depends directly on the SFDR variation of the DAC. The DAC on the AD9911 has enough part-to-part SFDR variation that using a set of fixed programming values across multiple devices will not consistently improve SFDR.

Spur reduction performance on an individual device is stable over supply and temperature. The SpurKiller/multitone mode configuration is illustrated in Figure 36.

The amplitude of the auxiliary channels uses coarse and fine adjustments to match the amplitude of the targeted spur. The coarse adjust is implemented via the data align bits in Register 0x03 Bits <18:16>. The approximate amplitude of the auxiliary channel is programmable between −60 dB and −12 dB compared to the full-scale fundamental, per the following equation:

$$AMP = -60\ \text{dB} + (D \times 6\ \text{dB})$$

where *AMP* is the amplitude and *D* is the decimal value (0-7) of the data align bits

For fine amplitude adjustments, the 10-bit output scalar (multiplier) of the auxiliary channel in Register 0x06 Bit <0:9> is used. The multiplier is enabled by Register 0x06 Bit <12>.

A single active SpurKiller channel targeting the second harmonic is expressed as

$$f_{OUT} = A \times \cos(\omega t + \Phi_1) + B \times \cos(2\omega t + \Phi_2) + B \times \cos(2\omega t + \Phi_2 + 180°) + (\text{all other spurious components})$$

where $B \times \cos(2\omega t + \Phi_2 + 180°)$ represents the fundamental tone of the SpurKiller channel.

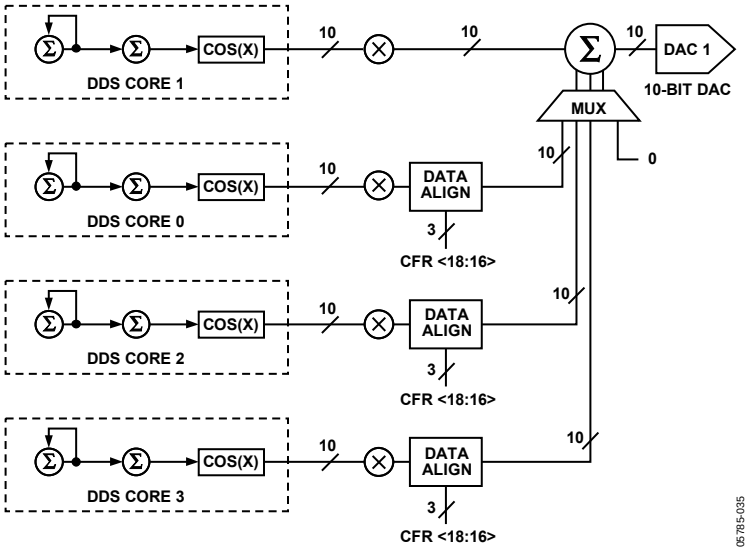


Figure 36. SpurKiller/Multitone Mode Configuration

TEST-TONE MODE

Test-tone mode enables sinusoidal amplitude modulation of the carrier (CH1). Setting Bit 2 in Register 0x01 enables test-tone mode. Auxiliary CH2 and CH3 should both be disabled using the channel enable bits (CSR Bit <7>). The frequency of modulation is set using the frequency tuning word (Register 0x04 Bits <31:0>) of auxiliary CH0. Auxiliary CH0 output scalar (Register 0x06 Bits <0:9>) sets the magnitude of the modulating signal. See Figure 37 for a diagram of the test-tone mode configuration.

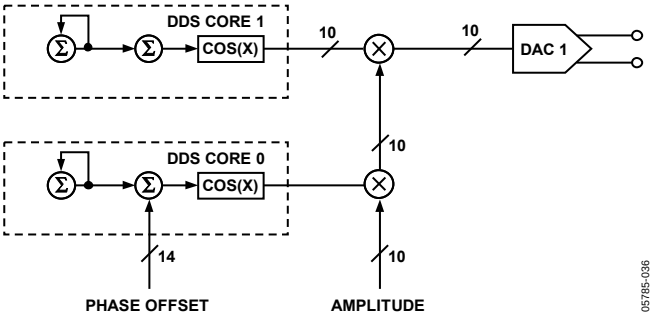


Figure 37. Test-Tone Mode Configuration

REFERENCE CLOCK MODES

The AD9911 supports several methods for generating the internal system clock. An on-chip oscillator circuit is available for initiating the low frequency reference signal by connecting a crystal to the clock input pins. The system clock can also be generated using the internal, PLL-based reference clock multiplier, allowing the part to operate with a low frequency clock source while still providing a high sample rate for the DDS and DAC. For best phase noise performance, a clean, stable clock with a high slew rate is required.

Enabling the PLL allows multiplication of the reference clock frequency from 4× to 20×, in integer steps. The PLL multiplication value is 5-bits located in the Function Register 1 (FR1) Bits <22:18>. For further information, refer to the Register Map section.

When FR1 <22:18> is programmed with values ranging from 4 to 20 (decimal), the clock multiplier is enabled. The integer value in the register represents the multiplication factor. The system clock rate with the clock multiplier enabled is equal to the reference clock rate times the multiplication factor. If FR1 <22:18> is programmed with a value less than 4 or greater than 20, the clock multiplier is disabled. Note that the output frequency of the PLL has a restricted frequency range. There is a VCO gain bit that must be set appropriately. The VCO gain bit (FR1<23>) defines two ranges (low/high) of frequency output. See the Register Map section for configuration directions and defaults.

The charge pump current in the PLL defaults to 75 μA, which typically produces the best phase noise characteristics. Increasing charge pump current typically degrades phase noise, but decreases the lock time and alters the loop bandwidth. The charge pump control bits (FR1 <17:16>) function is described in the Register Map section.

To enable the on-chip oscillator for crystal operation, drive CLK_MODE_SEL (Pin 24) high. The CLKMODESEL pin is considered an analog input, operating on 1.8 V logic. With the on-chip oscillator enabled, connection of an external crystal to the REF_CLK and REF_CLKB inputs is made producing a low frequency reference clock. The crystal frequency must be in the range of 20 MHz to 30 MHz. summarizes the clock mode options. See the Register Maps section for more details.

Table 4.

CLK_MODE_SEL Pin 24	FR1 <22:18> PLL, Bits = M	Oscillator Enabled	System Clock (f_{SYSCLK})	Min/Max Frequency Range (MHz)
High = 1.8 V Logic	4 ≤ M ≤ 20	Yes	$f_{SYSCLK} = f_{OSC} \times M$	$100 < f_{SYSCLK} < 500$
High = 1.8 V Logic	M < 4 or M > 20	Yes	$f_{SYSCLK} = f_{OSC}$	$20 < f_{SYSCLK} < 30$
Low	4 ≤ M ≤ 20	No	$f_{SYSCLK} = f_{REF\ CLK} \times M$	$100 < f_{SYSCLK} < 500$
Low	M < 4 or M > 20	No	$f_{SYSCLK} = f_{REF\ CLK}$	$0 < f_{SYSCLK} < 500$

Reference Clock Input Circuitry

The reference clock input circuitry has two modes of operation. The first mode (logic low) configures the circuitry as an input buffer. In this mode, the reference clock must be ac-coupled to the input due to internal dc biasing. This mode supports either differential or single-ended configurations. If single-ended mode is desired, the complementary reference clock input (Pin 23) should be decoupled to AVDD or AGND via a 0.1 µF capacitor. The following three figures exemplify common reference clock configurations for the AD9911.

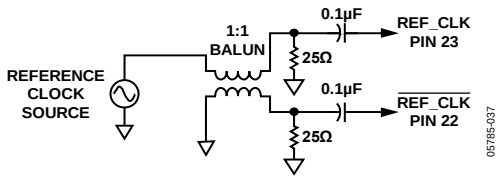


Figure 38. Typical Reference Clock Configuration for Sine Wave Source

The reference clock inputs can also support an LVPECL or PECL driver as the reference clock source.

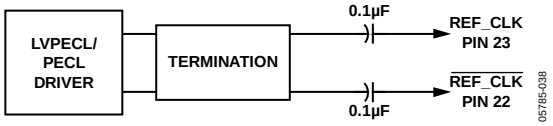


Figure 39. Typical Reference Clock Configuration for LVPECL/PECL Source

For external crystal operation, both clock inputs must be dc-coupled via the crystal leads and bypassed. Figure 40 shows the configuration when a crystal is used.

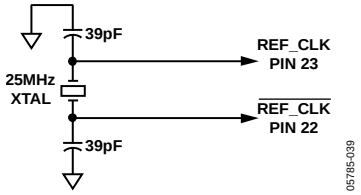


Figure 40. Crystal Configuration for Reference Clock Source

SCALABLE DAC REFERENCE CURRENT CONTROL MODE

Set the full-scale output current using bits CFR <9:8>, as shown in Table 5.

Table 5.

CFR <9:8>		LSB Current State
1	1	Full-scale
0	1	Half-scale
1	0	Quarter-scale
0	0	Eighth-scale

POWER-DOWN FUNCTIONS

The AD9911 supports pin-controlled power-down plus numerous software selectable power-down modes. Software controlled power-down allows the input clock circuitry, DAC, and the digital logic (for the primary and auxiliary DDS cores) to be individually powered.

When the PWR_DWN_CTL input pin is high, the AD9911 enters power-down mode based on the FR1 <6> bit. When the PWR_DWN_CTL input pin is low, the individual power-down bits (CFR <7:4>) control the power-down modes of operation. See the Control Register Descriptions section for further details.

SHIFT KEYING MODULATION

The AD9911 can perform 2-/4-/8- or 16-level modulation of frequency, phase, or amplitude (FSK, PSK, ASK) by applying data to the profile pins. SYNC_CLK must be enabled when performing FSK, PSK, or ASK, while the auxiliary DDS cores must be disabled. Digital power down (CSR Bit <7>) of the auxiliary channels is recommended.

In addition, the AD9911 has the ability to ramp up or ramp down the output amplitude before, during, or after a modulation (FSK, PSK only) sequence. This is accomplished by using the 10-bit output scalar. Profile pins or SDIO_1:3 pins can be configured to initiate the ramp up/ramp down (RU/RD) operation. See the Output Amplitude Control section for further details.

In modulation mode, a set of control bits (CFR<23:22>) determines the type (frequency, phase, or amplitude) of modulation. The primary channel (CH1) has 16 profile registers. Register Address 0x0A through Register Address 0x18 are profile registers for modulation of frequency, phase, or amplitude. Register 0x04, Register 0x05, and Register 0x06 are dedicated registers for frequency, phase, and amplitude, respectively.

These registers contain the initial frequency, phase offset and amplitude word. Frequency modulation is 32-bit resolution, phase modulation is 14 bit, and amplitude is 10 bit. When modulating phase or amplitude, the word value must be MSB-aligned in the profile registers; excess bits are ignored. In

modulation mode, bits CFR <23:22> and FR1 <9:8> configure the modulation type and level. See Table 6 and Table 7 for settings. Note that the linear sweep enable bit must be set to Logic 0 in modulation mode.

Table 6.

CFR <23:22>		CFR <14>	Description
0	0	x	Modulation disabled
0	1	0	Amplitude modulation
1	0	0	Frequency modulation
1	1	0	Phase modulation

Table 7.

FR1 <9:8>		Description
0	0	2-level modulation
0	1	4-level modulation
1	0	8-level modulation
1	1	16-level modulation

When both modulation and the RU/RD feature are desired, unused profile pins or SDIO pins can be assigned. SDIO pins can only be used for RU/RD.

Table 8.

RU/RD Bits FR1 <11:10>		Description
0	0	RU/RD disabled.
0	1	Profile Pin 2 and Pin 3 configured for RU/RD operation.
1	0	Profile Pin 3 configured for RU/RD operation.
1	1	SDIO Pin 1, Pin 2, and Pin 3 configured for RU/RD operation. Forces the I/O to be used only in 1-bit mode.

If profile pins are used for RU/RD, Logic 0 sets for ramp up and Logic 1 sets for ramp down.

To support RU/RD flexibility, it is necessary to assign the profile pins and/or SDIO Pin 1 to Pin 3 to CH1 operation. This is controlled by the profile pin configuration (PPC) or PPC bits (FR1 <14:12>). The modulation descriptions that follow include data pin assignment. In the modulation descriptions, an "x" indicates that it does not matter.

2-Level Modulation—No RU/RD

Modulation level bits are set to 00 (2-level). AFP bits are set to the desired modulation. RU/RD bits and the linear sweep bit are disabled. Table 9 displays how the profile pins are assigned.

Table 9. 2-Level Modulation—No RU/RD

Bits FR1<14:12>			P0	P1	P2	P3
x	x	x	N/A	CH1	N/A	N/A

As shown in Table 9, only Profile Pin P1 can be used to modulate CH1. If Pin P1 is Logic 0 and FSK modulation is desired, then Profile Register 0 (Register 0x04) frequency is chosen. If Pin P1 is Logic 1, then Profile Register 1 (Register 0x0A) frequency is chosen.

4-Level Modulation—No RU/RD

Modulation level bits are set to 01 (4-level). AFP bits are set to the desired modulation. RU/RD bits and the linear sweep bit are disabled. Table 10 displays how the profile pins are assigned.

Table 10. 4-Level Modulation—No RU/RD

Profile Pin Configuration (PPC) Bits FR1 <14:12>			P0	P1	P2	P3
0	1	1	CH1	CH1	N/A	N/A

For this condition, the profile register chosen is based on the 2 bit value presented to profile pins <P0:P1>. For example, if PPC = 011 and <P0:P1>= 11, then the contents of Profile Register 3 (Register 0x0C) are presented to CH1 output.

8-Level Modulation—No RU/RD

Modulation level bits are set to 10 (8-level). AFP bits are set to the desired modulation. RU/RD bits and the linear sweep bit are disabled. Table 11 shows the assignment of profile pins and channels.

Table 11. 8-Level Modulation—No RU/RD

Profile Pin Config. Bits FR1 <14:12>			P0	P1	P2	P3
x	0	1	CH1	CH1	CH1	x

For this condition, the profile register (1 of 8) chosen is based on the 3-bit value presented to the Profile Pin P0 to Pin P2. For example, if PPC = x01 and <P0:P2> = 111, then the contents of Profile Register 7 (Register 0x10) are presented to CH1 output.

16-Level Modulation—No RU/RD

Modulation level bits are set to 11 (16-level). AFP bits are set to the desired modulation. RU/RD bits and the linear sweep bit are disabled. Table 12 displays how the profile pins and channels are assigned.

Table 12. 16-Level Modulation—No RU/RD

Profile Pin Config. (PPC) Bits FR1 <14:12>			P0	P1	P2	P3
x	0	1	CH1	CH1	CH1	CH1

For these conditions, the profile register chosen is based on the 4-bit value presented to Profile Pin P0 to Pin P3. For example, if PPC = x01 and <P0:P3>= 1110, then the contents of Profile Register 14 (Register 0x17) are presented to CH1 output.

2-Level Modulation Using Profile Pins for RU/RD

When the RU/RD bits = 01, either Profile Pin P2 or Pin P3 are available for RU/RD. Note that only a modulation level of two is available when RU/RD bits = 01. See Table 13 for available pin assignments.

Table 13. 2-Level Modulation—RU/RD

Profile Pin Config. Bits FR1<14:12>			P0	P1	P2	P3
0	0	0	N/A	CH1	N/A	CH1 RU/RD
0	1	1	CH1	N/A	CH1 RU/RD	N/A

8-Level Modulation Using a Profile Pin for RU/RD

When the RU/RD bits = 10, Profile Pin P3 is available for RU/RD. Note that only a modulation level of eight is available when the RU/RD bits = 10. See Table 14 for available pin assignments.

Table 14. 8-Level Modulation—RU/RD

Profile Pin Config. Bits FR1 <14:12>			P0	P1	P2	P3
x	0	1	CH1	CH1	CH1	CH1 RU/RD

SHIFT KEYING MODULATION USING SDIO PINS FOR RU/RD

For RU/RD bits = 11, SDIO Pin 1, Pin 2, and Pin 3 are available for RU/RD. In this mode, modulation levels of 2, 4, and 16 are available. Note that the I/O port can only be used in 1-bit serial mode.

Table 15. 2-Level Modulation Using SDIO Pins for RU/RD

Profile Pin Config. Bits FR1 <14:12>			P0	P1	P2	P3
x	x	x	N/A	CH1	N/A	N/A

In this case, the SDIO pins can be used for the RU/RD function, as described in Table 16.

Table 16. SDIO Pins

1	2	3	Description
0	1	0	Triggers the ramp-up function for CH1
0	1	1	Triggers the ramp-down function for CH1

4-Level Modulation Using SDIO Pins for RU/RD

For RU/RD = 11 (SDIO Pin 1 and Pin 2 are available for RU/RD), the modulation level is set to four. See Table 17 for pin assignments, including SDIO pin assignments.

Table 17.

Profile Pin Config. Bits (FR1<14:12>)			P0	P1	P2	P3	SDIO_1	SDIO_2	SDIO_3
0	0	0	N/A	N/A	CH1	CH1	N/A	CH1 RU/RD	N/A
0	1	1	CH1	CH1	N/A	N/A	CH1 RU/RD	N/A	N/A

For the configuration shown in Table 17, the profile register is chosen based on the 2-bit value presented to <P0:P1> or <P2:P3>. For example, if PPC = 011, <P0:P1> = 11, then the contents of Profile Register 3 (Register 0x0C) are presented to CH1 output. SDIO Pin 1 and Pin 2 provide the RU/RD function.

16-Level Modulation Using SDIO Pins for RU/RD

RU/RD = 11 (SDIO Pin 1 available for RU/RD) and the level is set to 16. See the pin assignment shown in Table 18.

Table 18.

Profile Pin Config. Bits (FR1<14:12>)			P0	P1	P2	P3	SDIO_1	SDIO_2	SDIO_3
x	0	1	CH1	CH1	CH1	CH1	CH1 RU/RD	N/A	N/A

For the configuration shown in Table 18, the profile register is chosen based on the 4-bit value presented to <P0:P3>. For example, if PPC = x01 and <P0:P3> = 1101, then the contents of Profile Register 13 (Register 0x16) are presented to CH1 output. The SDIO_1 pin provides the RU/RD function.

LINEAR SWEEP (SHAPED) MODULATION MODE

Linear sweep enables the user to sweep frequency, phase, or amplitude from a starting point (S0) to an endpoint (E0). The purpose of linear sweep mode is to provide better bandwidth containment compared to direct modulation mode by enabling more gradual, user-defined changes between S0 and E0. Note that SYNC_CLK must be enabled when using Linear Sweep while the auxiliary DDS cores must be disabled. Digital power down (CSR bit <7>) of the auxiliary channels is recommended. Figure 41 depicts the linear sweep block diagram.

In linear sweep mode, S0 is loaded into Profile Register 0 (Profile 0 is represented by Register 0x04, Register 0x05, or Register 0x06, depending on the parameter being swept) and E0 is always loaded into Profile Register 1 (Register 0x0A). If E0 is configured for frequency sweep, the resolution is 32-bits. For phase sweep, the resolution is 14 bits and for amplitude sweep, the resolution is 10 bits. When sweeping phase or amplitude, the word value must be MSB-aligned in Profile Register 1; unused bits are ignored. Profile Pin1 triggers and controls the direction (up/down) of the linear sweep for frequency, phase, or amplitude.

The AD9911 can be programmed to ramp up or ramp down the output amplitude (using the 10-bit output scalar) before and after a linear sweep. If the RU/RD feature is desired, profile pins or SDIO_1:3 pins can be configured to control the RU/RD operation. For further details, refer to the Output Amplitude Control section. To enable linear sweep mode, AFP bits (CFR <23:22>), modulation level bits (FR1 <9:8>), and the linear sweep enable bit (CFR <14>) must be programmed. The AFP bits determine the type of linear sweep to be performed (see Table 19). The modulation level bits must be set to 00 (2-level).

Table 19.

AFP CFR <23:22>		Linear Sweep Enable CFR <14>	Description
0	0	1	N/A
0	1	1	Amplitude sweep
1	0	1	Frequency sweep
1	1	1	Phase sweep

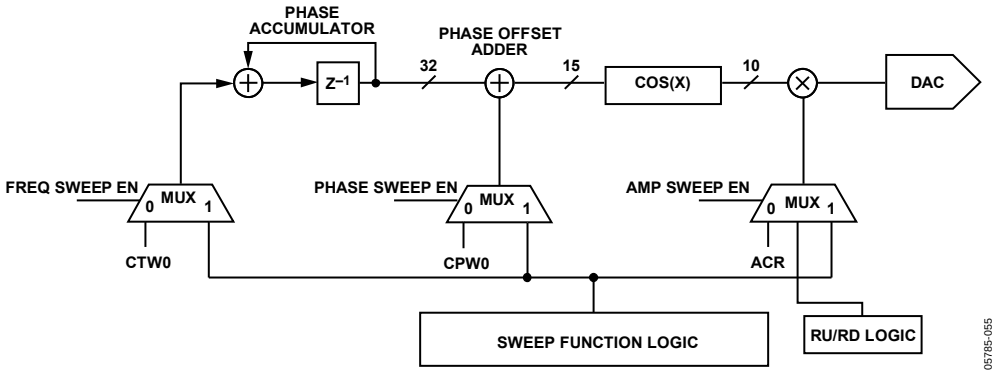


Figure 41. Linear Sweep Capability

Setting the Rate of the Linear Sweep

The rate of the linear sweep is set by the intermediate step size (delta-tuning word) between S0 and E0 (see Figure 42) and the time spent (sweep ramp rate word) at each step. The resolution of the delta-tuning word is 32 bits for frequency, 14 bits for phase, and 10 bits for amplitude. The resolution for the delta ramp rate word is 8 bits.

In linear sweep, the user programs a rising delta word (RDW, Register 0x08) and a rising sweep ramp rate word (RSRR, Register 0x07). These settings apply when sweeping from F0 to E0. The falling delta word (FDW, Register 0x09) and falling sweep ramp rate (FSRR, Register 0x07) apply when sweeping from E0 to S0.

When programming, note that attention is required to prevent overflow of the sweep. If the sweep accumulator is allowed to overflow, an uncontrolled, continuous sweep operation occurs. To avoid this, the magnitude of the rising or falling delta word should be smaller than the difference between full scale and the E0 value (full scale − E0). For a frequency sweep, full scale is $2^{31}-1$. For a phase sweep, full scale is $2^{14}-1$. For an amplitude sweep, full scale is $2^{10}-1$.

The graph in Figure 42 displays a linear sweep up and then down using a profile pin. Note that the no dwell bit is cleared. If the no dwell bit (CFR<15>) is set, the sweep accumulator returns to 0 upon reaching E0. For more information, see the Linear Sweep No Dwell Mode section.

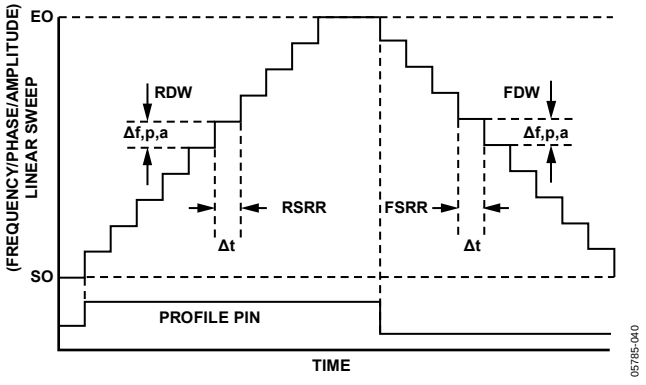


Figure 42. Linear Sweep Mode

For a piecemeal or a nonlinear transition between S0 and E0, the delta tuning words and ramp rate words can be reprogrammed during the transition.

The formulae for calculating the step size of RDW or FDW are

$$\Delta f = \left(\frac{RDW}{2^{32}}\right) \times SYNC\_CLK \quad \text{(Hz)}$$

$$\Delta \Phi = \left(\frac{RDW}{2^{14}}\right) \times 360°$$

$$\Delta a = \left(\frac{RDW}{2^{10}}\right) \times \text{DAC full-scale current}$$

The formula for calculating delta time from RSRR or FSRR is

$$\Delta t = (RSRR) / SYNC\_CLK(Hz)$$

At 500 MSPS operation (SYNC_CLK =125 MHz), the minimum time interval between steps is 1/125 MHz × 1 = 8 ns. The maximum time interval is (1/125 MHz) × 255 = 2.04 µs.

Frequency Linear Sweep Example

This section provides an example of a frequency linear sweep followed by a description.

AFP CFR<23:22> =10, modulation level FR1<9:8> = 00, sweep enable CFR<14> = 1, linear sweep no-dwell CFR<15> = 0.

In linear sweep mode, when the profile pin transitions from low to high, the RDW is applied to the input of the sweep accumulator and the RSRR register is loaded into the sweep rate timer.

The RDW accumulates at the rate given by the ramp rate (RSRR) until the output equals the CTW1 register value. The sweep is then complete and the output held constant in frequency.

When the profile pin transitions from high to low, the FDW is applied to the input of the sweep accumulator and the FSRR register is loaded into the sweep rate timer.

The FDW accumulates at the rate given by the ramp rate (FSRR) until the output equals the CTW0 register value. The sweep is then complete and the output held constant in frequency. See Figure 43 for the linear sweep circuitry. Figure 45 depicts a frequency sweep with no-dwell mode disabled. In this mode, the output follows the state of the profile

pin. A phase or amplitude sweep works in the same manner with fewer bits.

LINEAR SWEEP NO DWELL MODE

To enable linear sweep no dwell mode, set CFR <15>. The rising sweep is started by setting the profile input pin to 1. The frequency, phase or amplitude continues to sweep up at the rate set by the rising sweep ramp rate and the resolution set by the rising delta tuning word, until it reaches E0. The output then reverts to the S0 and stalls until high is detected on the profile pin.

Figure 44 demonstrates the no-dwell mode. The points labeled A indicate where a rising edge is detected on the profile pin. Points labeled B indicate at which points where the AD9911 has determined that the output has reached E0 and reverts to S0.

The falling ramp rate register and the falling delta word are unused in this mode.

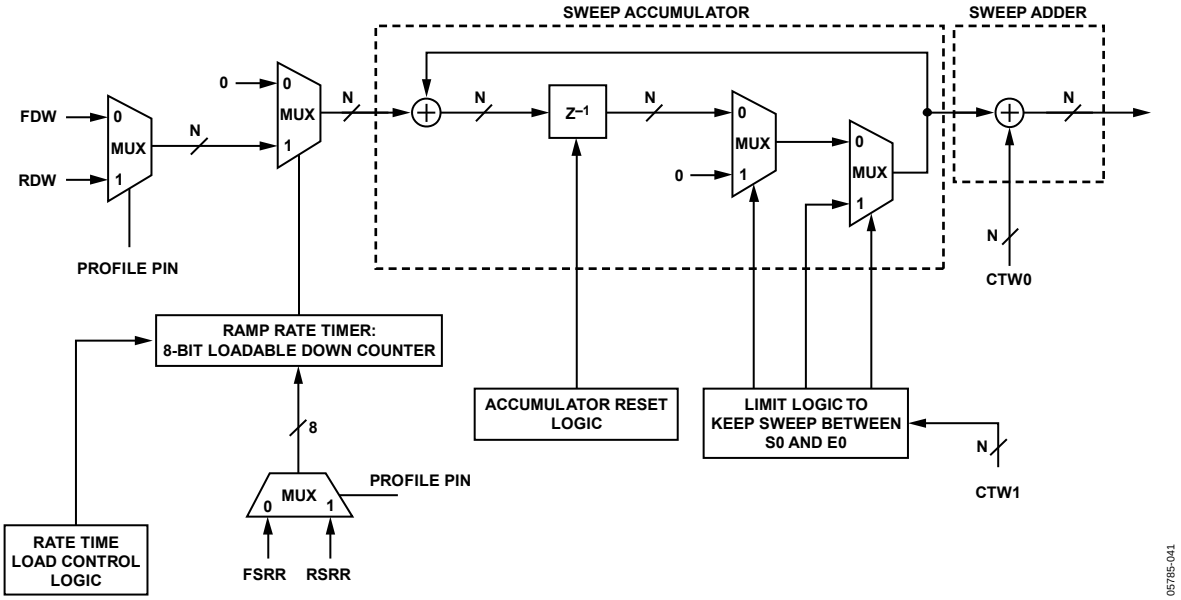


Figure 43. Linear Sweep Block Circuitry (Frequency Sweep)

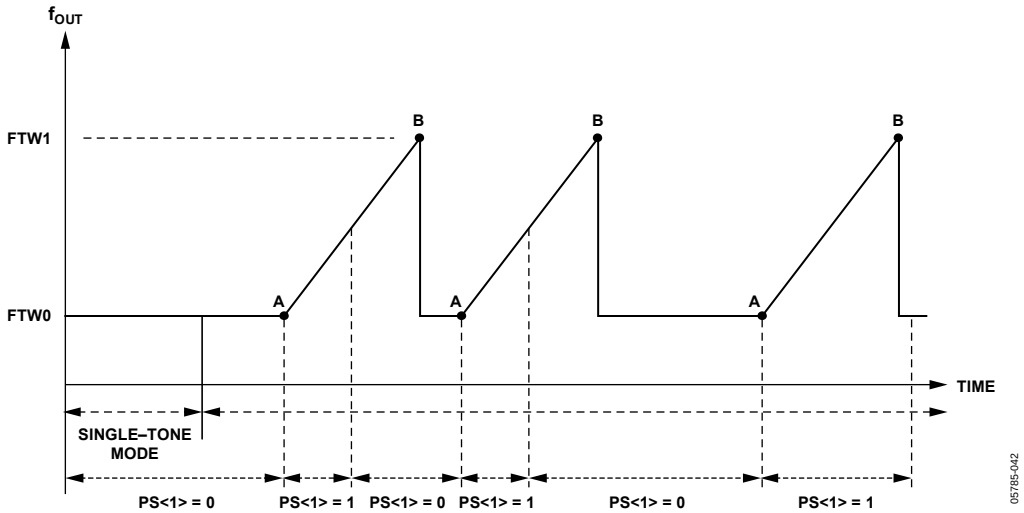


Figure 44. Linear Sweep Mode Enabled—No Dwell Bit Set

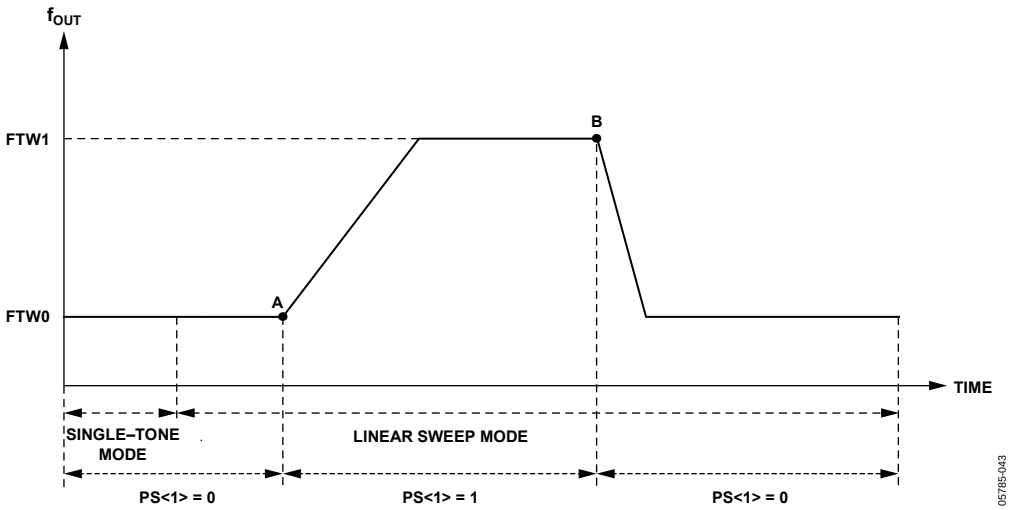


Figure 45. Linear Sweep Enabled-No Dwell Bit Cleared

SWEEP AND PHASE ACCUMULATOR CLEARING FUNCTIONS

The AD9911 provides two different clearing functions. The first function is a continuous zeroing of the sweep logic and phase accumulator (clear and hold). CFR <3> clears the sweep accumulator and CFR <1> clears the phase accumulator

The second function is a clear and release or automatic zeroing function. CFR <4> is the automatic clear sweep accumulator bit and CFR <2> is the automatic clear phase accumulator bit.

Continuous Clear Bits

The continuous clear bits are static control signals that, when high, hold the respective accumulator at 0. When the bit is programmed low, the respective accumulator is released.

Clear and Release Bits

The auto clear sweep accumulator bit, when set, clears and releases the sweep accumulator upon an I/O update or a change in the profile input pins. The auto clear phase accumulator, when set, clears and releases the phase accumulator upon an I/O update or a change in the profile pins. The automatic clearing function is repeated for every subsequent I/O update or change in profile pins until the clear and release bits are cleared via the I/O port.

OUTPUT AMPLITUDE CONTROL

The output amplitude may be controlled via one of four methods. Output amplitude control is implemented by the use of the 10-bit output scale factor (multiplier). See Figure 46 for output amplitude control configurations. For further details on the corresponding methods, see the Shift Keying Modulation section and the Linear Sweep (Shaped) Modulation Mode sections. The remaining methods (Manual and Automatic RU/RD) are described in this section.

The RU/RD feature is used to control an on/off emission from the DAC. This helps reduce the adverse spectral impact of abrupt burst transmissions of digital data. The multiplier can be bypassed by clearing the multiplier enable bit (ACR <12> = 0).

Automatic and manual RU/RD modes are supported. The automatic mode generates a zero to full-scale (10-bits) linear ramp at a rate set using the amplitude ramp rate control register (ACR <23:16>). Ramp initiation and direction (up/down) is controlled using either the profile pins or the SDIO1:3 pins. See Table 21. Manual mode is selected by programming ACR <12:11> = 10. In this mode, the user sets the output amplitude by writing to the amplitude scale factor value in the amplitude control register (Register 0x06 Bits <9:0>).

Automatic RU/RD Mode Operation

The automatic RU/RD mode is entered by setting ACR <12:11> = 11. In this mode, the scale factor is internally generated and applied to the multiplier input port for scaling the output. The scale factor is the output of a 10-bit counter that increments/decrements at a rate set by the 8-bit output ramp rate in Register 0x06 Bits <23:16>. The scale factor increments if the external pin is high and decrements if the pin is low. The scale factor step size is selected using the ACR<15:14>. Table 20 details the step size options available.

Table 20.

Autoscale Factor Step Size ASF <15:14> (Binary)	Increment/Decrement Size
00	1
01	2
10	4
11	8

The amplitude scale factor register allows the device to ramp to a value less than full scale.

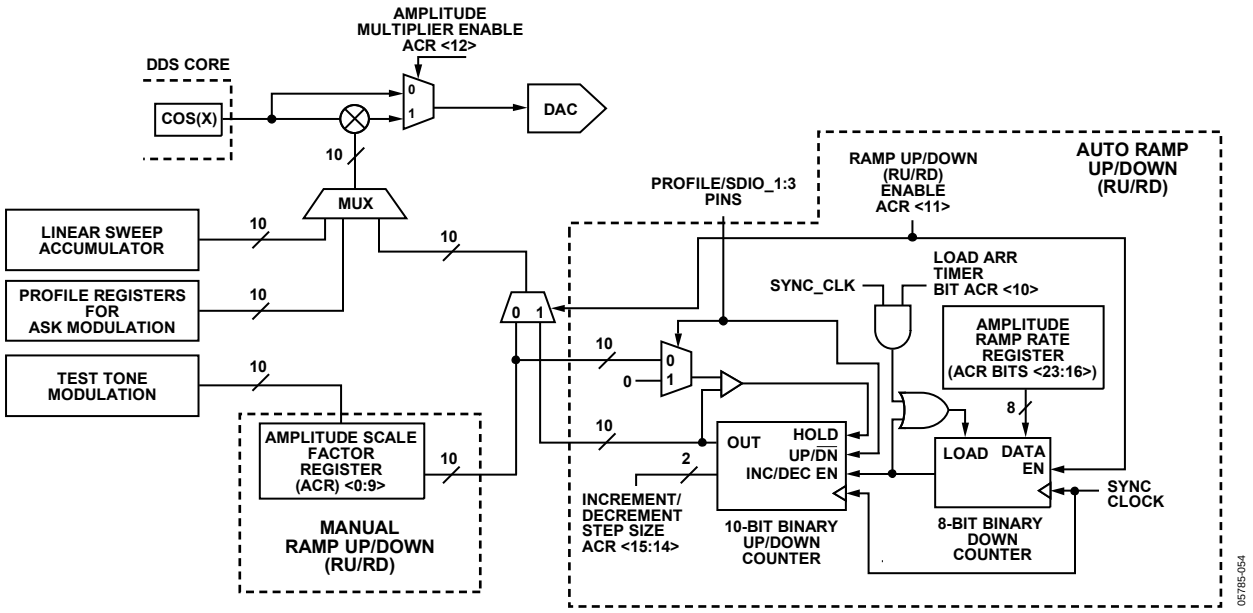


Figure 46. Output Amplitude Control Configurations

Ramp Rate Timer

The ramp rate timer is a loadable 8-bit down counter. It generates the clock signal to the 10-bit counter, which in turn generates the internal scale factor. The formula for calculating the amplitude ramp rate time is

$$\Delta t = (x) / SYNC\_CLK(Hz)$$

Where *x* is the decimal value in Register 00x06 Bits <23:16>.

At 500 MSPS operation (SYNC_CLK =125 MHz), the minimum time interval between steps is 1/125 MHz × 1 = 8 ns. The maximum time interval is (1/125 MHz) × 255 = 2.04 µs.

The ramp rate timer is loaded with the value of the ASF every time the counter reaches 1 (decimal). This load and count down operation continues for as long as the timer is enabled unless the timer is forced to load before reaching a count of 1.

If the load ARR timer bit ACR <10> is set, the ramp rate timer is loaded if any of the following three incidents transpire: an I/O update occurs, a profile pin changes, or the timer reaches a

See through Table 13 through Table 18 for RU/RD pin assignments.

SYNCHRONIZING MULTIPLE AD9911 DEVICES

The AD9911 allows easy synchronization of multiple AD9911 devices. At power-up, the phase of SYNC_CLK may be offset between multiple devices. There are three options (one automatic mode and two manual modes) to compensate for this offset and align the SYNC_CLK edges. These modes force the internal state machines of multiple devices to a common state, which aligns SYNC_CLKs.

Any mismatch in REF_CLK phase between devices results in a corresponding phase mismatch on the SYNC_CLKs.

OPERATION

The first step is to program the master and slave devices for their respective roles. Configure the master device by setting its master enable bit (FR2 <6>). This causes the SYNC_OUT of the master device to output a pulse whose pulse width equals one system clock period and whose frequency equals ¼ of the system clock frequency. Configuring device(s) as slaves is performed by setting the slave enable bit (FR2 <7>).

AUTOMATIC MODE SYNCHRONIZATION

In automatic mode, synchronization is achieved by connecting the SYNC_OUT pin on the master device to the SYNC_IN pin of the slave device(s). Devices are configured as master or slave through programming bits, accessible via the I/O port.

A configuration for synchronizing multiple AD9911 devices in automatic mode is shown in the Application Circuits section. In this configuration, the AD9510 provides coincident REF_CLK and SYNC_IN to all devices.

In this mode, slave devices sample SYNC_OUT pulses from the master device and a comparison of all state machines is made by the auto-synchronization circuitry. If the slave device(s) state machines are not identical to the master, the slave device(s) state machines stall for one system clock cycle. This procedure synchronizes the slave device(s) within three SYNC_CLK periods.

Delay Time Between SYNC_OUT and SYNC_IN

When the delay between SYNC_OUT and SYNC_IN exceeds one system clock period, phase offset bits (FR2 <1:0>) are used to compensate. Without the compensation factor, a phase error of 90°, 180°, or 270° might exist. The default state of these bits is 00, which implies that the SYNC_OUT of the master and the SYNC_IN of the slave have a propagation delay of less than one system clock period.

If the propagation time is greater than one system clock period, the time should be measured and the appropriate offset programmed. Table 21 describes the delays required per system clock offset value.

Table 21.

System Clock Offset Value	SYNC_OUT/SYNC_IN Propagation Delay
00	0 ≤ delay ≤ 1
01	1 ≤ delay ≤ 2
10	2 ≤ delay ≤ 3
11	3 ≤ delay ≤ 4

Automatic Synchronization Status Bit

If a slave device falls out of sync, the sync status bit is set. This bit can be read through the I/O port bit (FR2 <5>). It clears automatically when read. If the device reacquires sync before the bit is read, the alarm will remain high. The bit does not necessarily reflect the current state of the device. The status bit can be masked by writing Logic 1 to the synchronization status mask bit (FR2 <4>). When masked, the bit is held low.

MANUAL SOFTWARE MODE SYNCHRONIZATION

The manual software mode is enabled by setting the manual synchronization bit (FR1 <0>). In this mode, the I/O update that resets the Manual SW synchronization bit stalls the state machine of the clock generator for one system clock cycle. Stalling the clock generation state machine by one cycle changes the phase relationship of SYNC_CLK between devices by one system clock period (90°).

Note that the user may repeat this process until the devices have the corresponding SYNC_CLK signals in the desired phase relationship. The SYNC_IN input can be left floating since this input has an internal pull-up. The SYNC_OUT is not used.

MANUAL HARDWARE MODE SYNCHRONIZATION

Manual hardware mode is enabled by setting the manual SW synchronization bit (FR1 <1>). In this mode, the SYNC_CLK stalls by one system clock cycle each time a rising edge is detected on the SYNC_IN input. Stalling the SYNC_CLK state machine by one cycle changes the phase relationship of SYNC_CLK between devices by one system clock period (90°).

Note that the process can be repeated until the devices have SYNC_CLK signals in the desired phase relationship. The SYNC_IN input can be left floating since this input has an internal pull-up. The SYNC_OUT is not used.

I/O_UPDATE, SYNC_CLK, AND SYSTEM CLOCK RELATIONSHIPS

I/O_UPDATE and SYNC_CLK are used together to transfer data from the I/O buffer to the active registers in the device. Data in the I/O buffer is inactive.

SYNC_CLK is a rising edge active signal. It is derived from the system clock and a divide-by frequency divider of 4. The SYNC_CLK is provided externally to synchronize external hardware to the AD9911 internal clocks.

I/O_UPDATE initiates the start of a buffer transfer. It can be sent synchronously or asynchronously relative to the SYNC_CLK.

If the set-up time between these signals is met, then constant latency (pipeline) to the DAC output exists. For example, if repetitive changes to phase offset via the SPI port is desired, the latency of those changes to the DAC output is constant, otherwise a time uncertainty of one SYNC_CLK period will be present.

The I/O UPDATE is sampled on the rising edge of the SYNC_CLK. Therefore, I/O_UPDATE must have a minimum pulse width greater than one SYNC_CLK period.

The timing diagram shown in Figure 47 depicts when data in the I/O buffer is transferred to the active registers.

The I/O UPDATE is set up and held around the rising edge of SYNC_CLK and has zero hold time and 4.8 ns setup time.

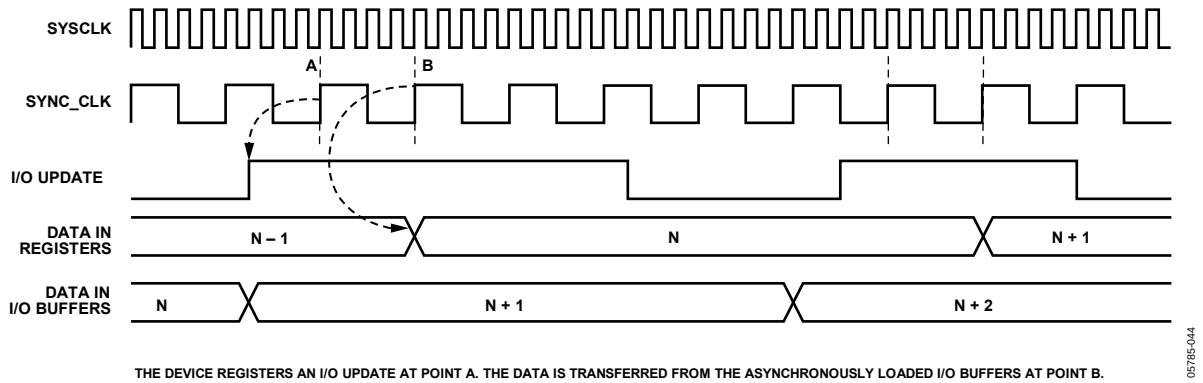


Figure 47. I/O_UPDATE Timing

I/O PORT

OVERVIEW

The AD9911 I/O port offers multiple configurations to provide significant flexibility. The I/O port includes an SPI-compatible mode of operation. Flexibility is provided by four data (SDIO_0:3) pins supporting four programmable modes of I/O operation.

Three of the four data pins (SDIO_1:3) can be used for functions other than I/O port operation. These pins may be set to initiate a ramp-up or ramp-down (RU/RD) of the 10-bit amplitude output scalar. One of these pins (SDIO_3) may be used to provide the SYNC_I/O function.

The maximum speed of the I/O port SCLK is 200 MHz. The maximum data throughput of 800 Mbps is achieved by using all SDIO_0:3 pins.

There are four sets of addresses (0x03 to 0x18) that channel enable bits can access to provide channel independence when using the auxiliary DDS cores for either test-tone generation or spur killing. See the Control Register Descriptions section for further discussion of programming channels that are common or independent from one another.

I/O operation of the AD9911 occurs at the register level, not the byte level; the controller expects that all byte(s) contained in the register address are accessed. The SYNC_I/O function can be used to abort an I/O operation, thereby not allowing all bytes to be accessed. This feature can be used to program only a part of the addressed register. Note that only completed bytes are stored.

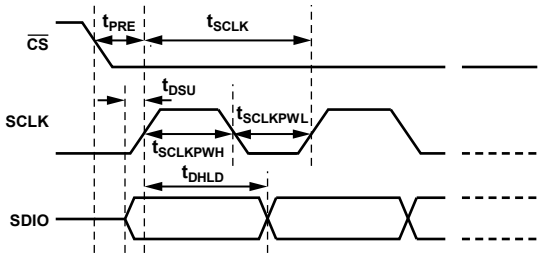
There are two phases to a communications cycle. The first is the instruction phase, which writes the instruction byte into the AD9911. Each bit of the instruction byte is registered on each corresponding rising edge of SCLK. The instruction byte defines whether the upcoming data transfer is a write or read operation and contains the serial address of the address register.

Phase 2 of the I/O cycle is of the data transfer (write/read) between the I/O port controller and the I/O port buffer. The number of bytes transferred during this phase of the communication cycle is a function of the register being accessed. The actual number of additional SCLK rising edges required for the data transfer and instruction byte depends on the number of byte(s) in the register and the I/O mode of operation.

For example, when accessing Function Register 1, (FR1), which is three bytes wide, Phase 2 of the I/O cycle requires that three bytes are transferred. After transferring all data bytes per the instruction byte, the communication cycle is complete.

Upon completion of a communication cycle, the AD9911 I/O port controller expects the next set of rising SCLK edges to be the instruction byte for the next communication cycle. Data writes occur on the rising edge of SCLK. Data reads occur on the falling edge of SCLK. See Figure 43 and Figure 44.

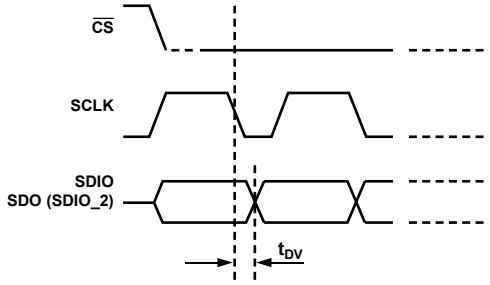
An I/O_UPDATE transfers data from the I/O port buffer to active registers. The I/O_UPDATE can either be sent for each communication cycle or when all I/O operations are complete. Data remains inactive until an I/O_UPDATE is sent, with the exception of the channel enable bits in the Channel Select Register (CSR). These bits require no I/O_UPDATE to be enabled.



SYMBOL	DEFINITION	MIN
t_{PRE}	$\overline{CS}$ SETUP TIME	1.0ns
t_{SCLK}	PERIOD OF SERIAL DATA CLOCK	5.0ns
t_{DSU}	SERIAL DATA SETUP TIME	2.2ns
$t_{SCLKPWH}$	SERIAL DATA CLOCK PULSE WIDTH HIGH	2.2ns
$t_{SCLKPWL}$	SERIAL DATA CLOCK PULSE WIDTH LOW	1.6ns
t_{DHLD}	SERIAL DATA HOLD TIME	0ns

05785-045

Figure 48. Set-Up and Hold Timing for the I/O Port



SYMBOL	DEFINITION	MIN
t_{DV}	DATA VALID TIME	12ns

05785-046

Figure 49. Timing Diagram for Data Read for I/O Port

INSTRUCTION BYTE DESCRIPTION

The instruction byte contains the information displayed in Table 22 where x = don't care.

Table 22.

MSB	D6	D5	D4	D3	D2	D1	LSB
R/Wb	x	x	A4	A3	A2	A1	A0

Bit 7 of the instruction byte (R/Wb) determines whether a read or write data transfer occurs after the instruction byte write. set indicates a read operation; Cleared indicates a write operation. Bit 4 to Bit 0 of the instruction byte determine which register is accessed during the data transfer portion of the communications cycle. The internal byte addresses are generated by the AD9911.

I/O PORT PIN DESCRIPTION

Data Clock (SCLK)
The clock pin is used to synchronize data to and from the internal state machines of the AD9911.

Chip Select ($\overline{CS}$)
The chip select pin allows more than one AD9911 device to be on the same communications lines. The chip select is an active low enable pin. Defined SDIO inputs go to a high impedance state when $\overline{CS}$ is high. If $\overline{CS}$ is driven high during any communications cycle, that cycle is suspended until $\overline{CS}$ is reactivated low.

Data I/O (SDIO_0:3)
Of the four SDIO pins, only the SDIO_0 pin is dedicated to this function. SDIO_1:3 can be used to control the ramping of the output amplitude. Bits <2:1> in the channel select register (CSR Register 0x00) control the configuration of these pins. See the I/O Modes of Operation section for more information.

I/O PORT FUNCTION DESCRIPTION

Serial Data Out (SDO)
The SDO function is available in single-bit (3-wire) mode only. In SDO mode, data is read from the SDIO_2 pin for protocols that use separate lines for reading and writing data (see Table 23 for pin configuration options). Bits <2:1> in the CSR register (Register 0x00) control the configuration of this pin. The SDO function is not available in 2-bit and 4-bit I/O modes.

SYNC_I/O
The SYNC_I/O function is available in 1-bit and 2-bit modes. SDIO_3 serves as the SYNC_I/O pin, as configured by Bits <2:1> in the CSR register (Register 0x00). Otherwise, the SYNC_I/O function is used to synchronize the I/O port state machines without affecting the addressable register contents. An active high input on the SYNC_I/O pin causes the current communication cycle to abort. After SDIO_3 returns low (Logic 0), another communication cycle can begin. The SYNC_I/O function is not available in 4-bit I/O mode.

MSB/LSB TRANSFER DESCRIPTION

The AD9911 I/O port supports either MSB or LSB first data formats. This functionality is controlled by CSR <0> in the channel select register (CSR). MSB-first is the default. When CSR <0> is set, the I/O port is LSB-first. The instruction byte must be written in the manner selected by CSR <0>.

Example

To write the Function Register 1 (FR1) in MSB-first format, apply an instruction byte of MSB > 00000001 < LSB, starting with the MSB. The internal controller recognizes a write transfer of three bytes starting with the MSB, Bit <23>, in the FR1 address (Register 0x01). Bytes are written on each consecutive rising SCLK edge until Bit<0> is transferred. This indicates the I/O communication cycle is complete and the next byte is considered an instruction byte.

To write the Function Register 1 (FR1) in LSB-first format, apply an instruction byte of MSB > 00000001 < LSB, starting with the LSB. The internal controller recognizes a write transfer of three bytes, starting with the LSB, Bit <0>, in the FR1 address (Register 0x01). Bytes are written on each consecutive rising SCLK edge until Bit <23> is transferred. Once the last data bit is written, the I/O communication cycle is complete and the next byte is considered an instruction byte.

I/O MODES OF OPERATION

There are four selectable modes of I/O port operation:

- Single-bit serial 2-wire mode (default mode).
- Single-bit, 3-wire mode.
- 2-bit mode.
- 4-bit mode (SYNC_I/O not available).

Table 23 displays the function of all six I/O interface pins, depending on the mode of I/O operation selected.

Table 23. I/O Port Pin Function vs. I/O Mode

Pin Name	Single Bit, 2-Wire Mode	Single Bit, 3-Wire Mode	2-Bit Mode	4-Bit Mode
SCLK	I/O Clock	I/O Clock	I/O Clock	I/O Clock
CSB	Chip Select	Chip Select	Chip Select	Chip Select
SDIO_0	Data I/O	Data In	Data I/O	Data I/O
SDIO_1	Not used for SDIO[1]	Not used for SDIO[1]	Data I/O	Data I/O
SDIO_2	Not used for SDIO[1]	Serial Data Out (SDO)	Not used for SDIO[1]	Serial Data I/O
SDIO_3	SYNC_I/O	SYNC_I/O	SYNC_I/O	Serial Data I/O

[1]In this mode, these pins can be used for RU/RD operation.

The two bits, CSR <2:1>, in the channel select register set the I/O mode of operation. These bits are defined as follows:

CSR <2:1> = 00. Single bit serial mode (2-wire mode)

CSR <2:1> = 01. Single bit serial mode (3-wire mode)

CSR <2:1> = 10. 2-bit mode

CSR <2:1> = 11. 4-bit mode

Single-Bit Serial (2- and 3-Wire) Modes

The single-bit serial mode interface allows read/write access to all registers that configure the AD9911. MSB-first or LSB-first transfer formats and the SYNC_I/O function are supported.

In 2-wire mode, the SDIO_0 pin is the single serial data I/O pin. In 3-wire mode, the SDIO_0 pin is the serial data input pin and the SDIO_2 pin is the output. For both modes, the SDIO_3 pin is configured as an input and operates as the SYNC_I/O pin. The SDIO_1 pin is unused.

2-Bit Mode

The SPI port operation in 2-bit mode is identical to the SPI port operation in single bit mode, except that two bits of data are registered on each rising edge of SCLK, cutting in half the number of cycles required to program the device. The SDIO_0 pin contains the even numbered data bits using the notation D <7:0> while the SDIO_1 pin contains the odd numbered data bits regardless of whether in MSB- or LSB-first format (see Figure 47).

4-Bit Mode

The SPI port in 4-bit mode is identical to the SPI port in single bit mode, except that four bits of data are registered on each rising edge of SCLK.

This reduces by 75% the number of cycles required to program the device. Note that when reprogramming the device for 4-bit mode, it is important to keep the SDIO_3 pin at Logic 0 until the device is programmed out of the single bit serial mode. Failure to do so can result in the I/O port controller being out of sequence.

Figure 50 through Figure 52 are write timing diagrams for the I/O modes available. Both MSB and LSB-first modes are shown. LSB-first bits are shown in parenthesis. The clock stall low/high feature shown is not required, but rather is used to show that data (SDIO) must have the proper setup time relative to the rising edge of SCLK.

Figure 53 through Figure 56 are read timing diagrams for each I/O mode available. Both MSB and LSB-first modes are shown. LSB-first bits are shown in parenthesis. The clock stall low/high feature shown is not required. It is used to show that data (SDIO) must have the proper set-up time relative to the rising edge of SCLK for the instruction byte and the read data that follows the falling edge of SCLK.

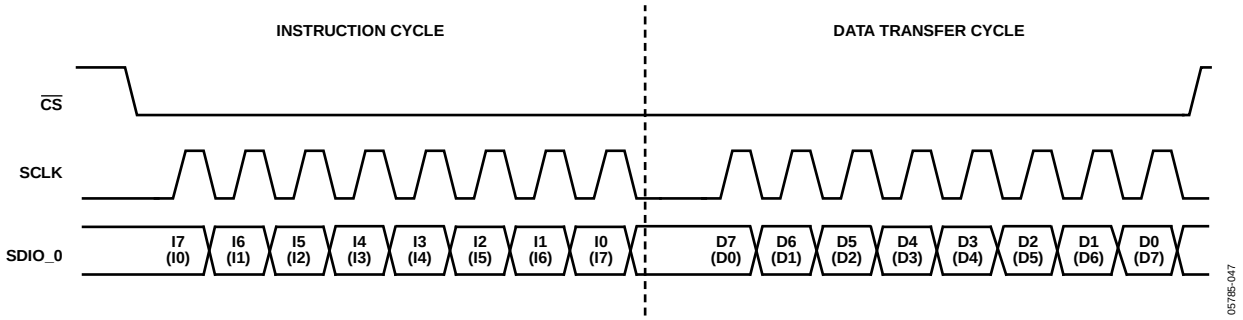


Figure 50. Single-Bit Serial Mode Write Timing—Clock Stall Low

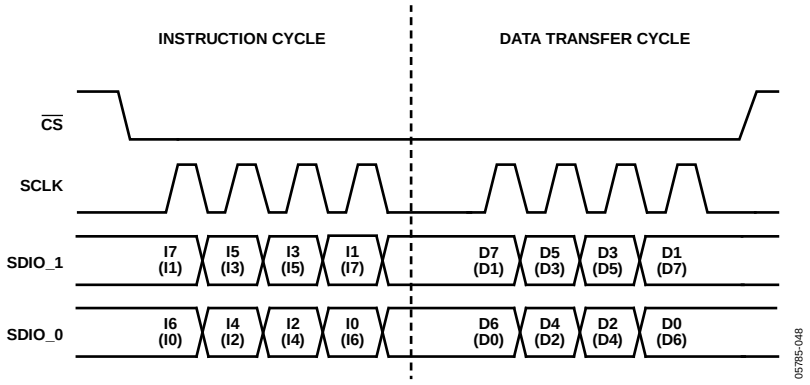


Figure 51. 2-Bit Mode Write Timing—Clock Stall Low

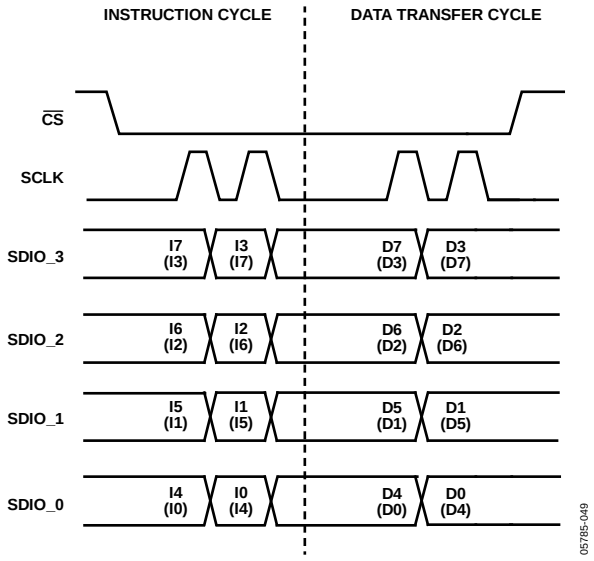


Figure 52. 4-Bit Mode Write Timing—Clock Stall Low

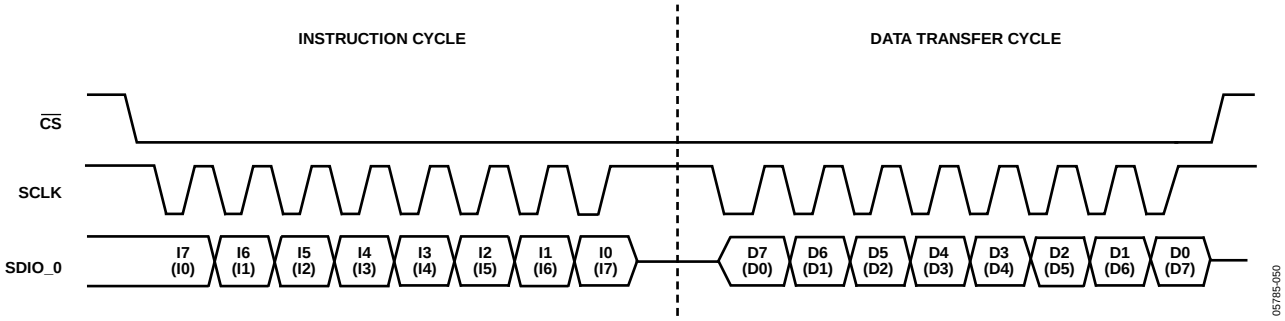


Figure 53. Single-Bit Serial Mode (2-Wire) Read Timing—Clock Stall High

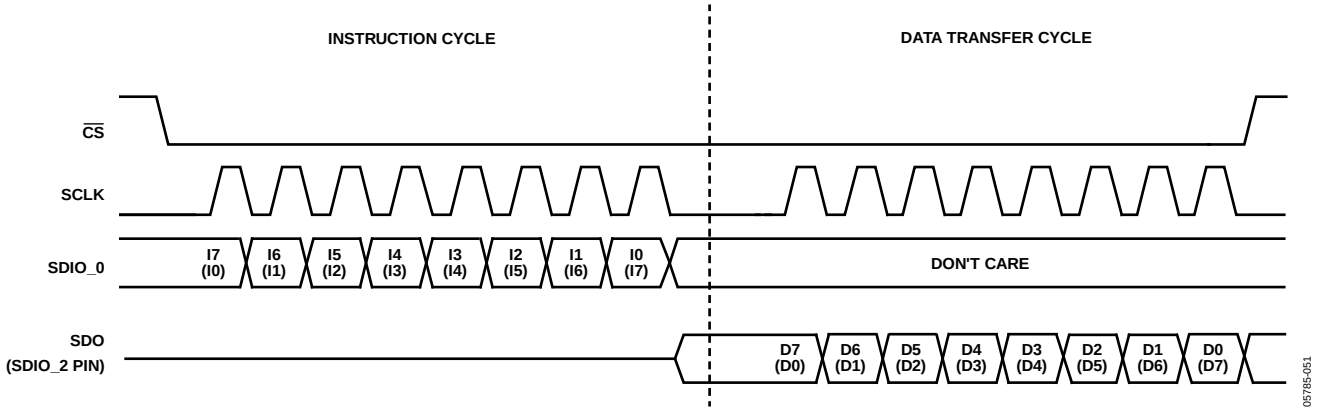


Figure 54. Single-Bit Serial Mode (3-Wire) Read Timing—Clock Stall Low

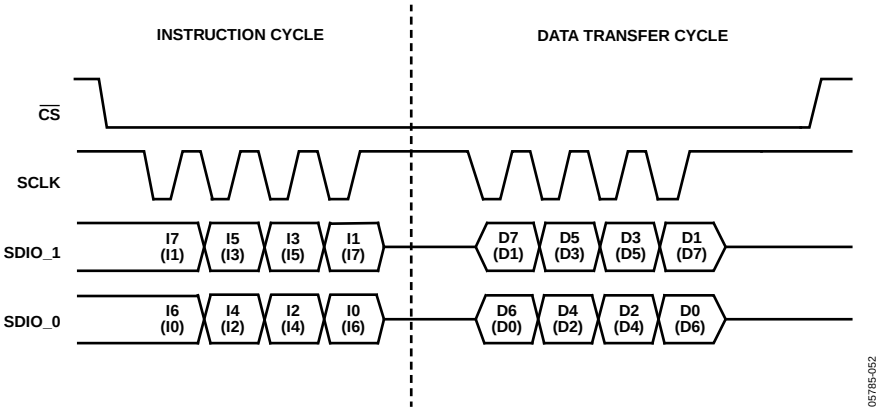


Figure 55. 2-Bit Mode Read Timing—Clock Stall High

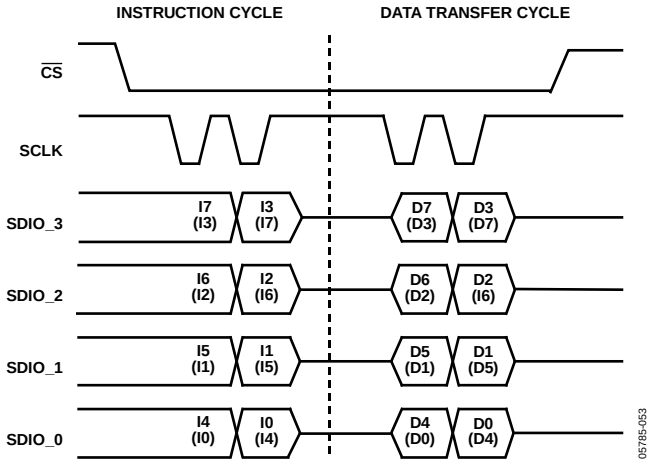


Figure 56. 4-Bit Mode Read Timing—Clock Stall High

REGISTER MAPS

CONTROL REGISTER MAP

Table 24.

Register Name (Address)	Bit Range	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value
Channel Select Register (CSR) (0x00)	<7:0>	Auxiliary Channel 3 (W/R enable[1])	Auxiliary Channel 2 (W/R enable[1])	Primary Channel 1 (W/R enable[1])	Auxiliary Channel 0 (W/R enable[1])	Must be 0	I/0 mode select <2:1>		LSB first	0xF0
Function Register 1 (FR1) (0x01)	<7:0>	Reference clock input power down	External power down mode	Sync clock disable	DAC reference power down	Open	Test-tone enable	Manual hardware synchronization	Manual software synchronization	0x00
	<15:8>	Open	Profile pin configuration <14:12>			Ramp up/ramp down <11:10>		Modulation Level <9:8>		0x00
	<23:16>	VCO gain control	PLL divider ratio <22:18>					Charge pump control <17:16>		0x00
Function Register 2 (FR2) (0x02)	<7:0>	Multidevice synchronization slave enable	Multidevice synchronization master enable	Multidevice synchronization status	Multidevice synchronization mask	Open <3:2>		System clock offset <1:0>		0x00
	<15:8>	All channels auto clear sweep accumulator	All channels clear sweep accumulator	All channels auto clear phase accumulator	All channels clear phase accumulator	Open <11:10>		Open <9:8>		0x00

[1] Channel enable bits do not require an I/O update to be activated. These bits are active immediately after the byte containing the bits is written. All other bits need an I/O update to become active. The channel enable bits determine if the channel registers and/or profile registers are written to or not.

CHANNEL REGISTER MAP

Table 25.

Register Name (Address)	Bit Range	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	(LSB) Bit 0	Default Value
Channel Function[1] (CFR) (0x03)	<7:0>	Digital power-down	DAC power down	Matched pipe delays active	Auto clear sweep accumulator	Clear sweep accumulator	Auto clear phase accumulator	Clear phase accumulator[2]	Sine wave output enable	0x02
	<15:8>	Linear sweep no-dwell	Linear sweep enable	Load SRR at I/O Update	Open	Open	Must be 0	DAC full-scale current control <9:8>		0x03
	<23:16>	Amplitude frequency phase select <23:22>		Open <21:19>			Data align bits for SpurKiller mode <18:16>			0x00
Channel Frequency Tuning Word 0[1] (CTW0) (0x04)	<7:0>	Frequency Tuning Word 0 <7:0>								0x00
	<15:8>	Frequency Tuning Word 0 <15:8>								
	<23:16>	Frequency Tuning Word 0 <23:16>								
	<31:24>	Frequency Tuning Word 0 <31:24>								
Channel Phase[1] Offset Word 0 (CPOW0) (0x05)	<7:0>	Phase Offset Word 0								0x00
	<15:8>	Open <15:14>		Phase Offset Word 0 <13:8>						0x00
Amplitude Control (ACR) (0x06)	<7:0>	Amplitude scale factor								0x00
	<15:8>	Increment/decrement step size <15:14>		Open	Amplitude multiplier enable	Ramp-up/ ramp-down enable	Load ARR at I/O update	Amplitude scale factor <9:8>		0x00
	<23:16>	Amplitude ramp rate <23:16>								–
Linear Sweep Ramp Rate[1] (LSR) (0x07)	<7:0>	Linear sweep rising ramp rate (RSRR) <7:0>								–
	<15:8>	Linear sweep falling ramp rate (FSRR) <15:8>								–
LSR Rising Delta[1] (RDW) (0x08)	<7:0>	Rising delta word <7:0>								–
	<15:8>	Rising delta word <15:8>								–
	<23:16>	Rising delta word <23:16>								–
	<31:24>	Rising delta word <31:24>								–
LSR Falling Delta[1] (FDW) (0x09)	<7:0>	Falling delta word <7:0>								–
	<15:8>	Falling delta word <15:8>								–
	<23:16>	Falling delta word <23:16>								–
	<31:24>	Falling delta word <31:24>								–

[1] There are four sets of channel registers and profile registers, one per channel. This is not shown in the channel or profile register maps because the addresses of all channel registers and profile registers are the same for each channel. Therefore, the channel enable bits determine if the channel registers and/or profile registers are written to or not.

[2] The clear accumulator bit is set after a master reset. It self clears when an I/O update is asserted.

PROFILE REGISTER MAP

Table 26.

Register Name (address)	Bit Range	MSB Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	LSB Bit 0	Default Value
Channel Word 1 (CTW1) (0x0A)	<31:0>	Frequency tuning word <31:0> or phase word <31:18> or amplitude word <31:22>								–
Channel Word 2 (CTW2) (0x0B)	<31:0>	Frequency tuning word <31:0> or phase word <31:18> or amplitude word <31:22>								–
Channel Word 3 (CTW3) (0x0C)	<31:0>	Frequency tuning word <31:0> or phase word <31:18> or amplitude word <31:22>								–
Channel Word 4 (CTW4) (0x0D)	<31:0>	Frequency tuning word <31:0> or phase word <31:18> or amplitude word <31:22>								–
Channel Word 5 (CTW5) (0x0E)	<31:0>	Frequency tuning word <31:0> or phase word <31:18> or amplitude word <31:22>								–
Channel Word 6 (CTW6) (0x0F)	<31:0>	Frequency tuning word <31:0> or phase word <31:18> or amplitude word <31:22>								–
Channel Word 7 (CTW7) (0x10)	<31:0>	Frequency tuning word <31:0> or phase word <31:18> or amplitude word <31:22>								–
Channel Word 8 (CTW8) (0x11)	<31:0>	Frequency tuning word <31:0> or phase word <31:18> or amplitude word <31:22>								–
Channel Word 9 (CTW9) (0x12)	<31:0>	Frequency tuning word <31:0> or phase word <31:18> or amplitude word <31:22>								–
Channel Word 10 (CTW10) (0x13)	<31:0>	Frequency tuning word <31:0> or phase word <31:18> or amplitude word <31:22>								–
Channel Word 11 (CTW11) (0x14)	<31:0>	Frequency tuning word <31:0> or phase word <31:18> or amplitude word <31:22>								–
Channel Word 12 (CTW12) (0x15)	<31:0>	Frequency tuning word <31:0> or phase word <31:18> or amplitude word <31:22>								–
Channel Word 13 (CTW13) (0x16)	<31:0>	Frequency tuning word <31:0> or phase word <31:18> or amplitude word <31:22>								–
Channel Word 14 (CTW14) (0x17)	<31:0>	Frequency tuning word <31:0> or phase word <31:18> or amplitude word <31:22>								–
Channel Word 15 (CTW15) (0x18)	<31:0>	Frequency tuning word <31:0> or phase word <31:18> or amplitude word <31:22>								–

CONTROL REGISTER DESCRIPTIONS

CHANNEL SELECT REGISTER (CSR)

The CSR register determines if channels are enabled or disabled by the status of the channel enable bits. Channels are enabled by default. The CSR register also determines which mode and format (MSB-first or LSB-first) of operation is active.

The CSR is comprised of one byte located in Register 0x00.

CSR <0> LSB-first

CSR <0> = 0 (default), the serial interface, accepts data in MSB-first format. CSR <0> = 1, the interface, accepts data in LSB-first format.

CSR <2:1> I/O mode select

CSR <2:1> 00 = single bit serial (2-wire mode).
01 = single bit serial (3-wire mode).
10 = 2-bit mode.
11 = 4-bit mode.

See the I/O Modes of Operation section for more details.

CSR <3> = must be cleared to 0.

CSR <7:4> channel enable bits.

CSR <7:4> bits are active immediately once written. They do not require an I/O update to take effect.

There are four sets of channel registers and profile registers, one per channel. This is not shown in the channel or profile register map. The addresses of all channel registers and profile registers are the same for each channel. Therefore, the channel enable bits distinguish the channel registers and profile registers values for each channel.

For example,

CSR <7:4> = 0010, only primary Channel 1 receives commands from the channel and profile registers.

CSR <7:4> = 0000, only auxiliary Channel 0 receives commands from the channel registers and profile registers.

CSR <7:4> = 0011, both Channel 0 and Channel 1 receive commands from the channel registers and profile registers.

Function Register 1 (FR1) Description

FR1 is comprised of three bytes located in Register 0x01. The FR1 is used to control the mode of operation of the chip. The functionality of each bit is detailed as follows:

FR1 <0> manual software synchronization bit.

FR1 <0> = 0 (default), the software manual synchronization feature is inactive. FR1 <0> = 1.The manual software synchronization feature is active. See Synchronizing Multiple AD9911 Devices section for details.

FR1 <1> Manual hardware synchronization bit.

FR1 <1> = 0 (default), the manual hardware synchronization feature is inactive. FR1 <1> = 1, the manual hardware synchronization feature is active. See the Synchronizing Multiple AD9911 Devices +section for details.

FR1 <2> Test-tone modulation enable.

FR1 <2> = 0 (default) disables and 1 enables.

FR1 <3> open.

FR1 <4> DAC reference power-down.

FR1 <4> = 0 (default). The DAC reference is enabled.
FR1 <4> = 1. DAC reference is disabled and powered down.

FR1 <5> SYNC_CLK disable.

FR1 <5> = 0 (default), the SYNC_CLK pin is active.

FR1 <5> = 1. The SYNC_CLK pin assumes a static Logic 0 state (disabled). The pin drive logic is shut down. The synchronization circuitry remains active internally (necessary for normal device operation.)

FR1 <6> external power-down mode.

FR1 <6> = 0 (default). The external power-down mode is in the fast recovery power-down mode. When the PWR_DWN_CTL input pin is high, the digital logic and the DAC digital logic are powered down. The DACs bias circuitry, PLL, oscillator, and clock input circuitry are not powered down.

FR1 <6> = 1. The external power down mode is in the full power-down mode. When the PWR_DWN_CTL input pin is high, all functions are powered down. This includes the DAC and PLL, which take a significant amount of time to power up.

FR1 <7> clock input power-down.

FR1 <7> = 0 (default). The clock input circuitry is enabled for operation. FR1 <7> = 1. The clock input circuitry is disabled and is in a low power dissipation state.

FR1 <9:8> modulation level bits.

The modulation (FSK, PSK, and ASK) level bits control the level (2/4/8/16) of modulation to be performed. See Table 7 for settings.

FR1 <11:10> RU/RD bits.

The RU/RD bits control how the profile pins and SDIO_1:3 pins are assigned. See Table 8 for settings

FR1 <12:14> profile pin configuration bits.

The profile pin configuration bits assign the profile and SDIO pins for the different tasks. See the Shift Keying Modulation section for examples.

FR1 <15> inactive.

FR1 <17:16> charge pump current control.

FR1 <17:16> = 00 (default), the charge pump current is 75 μA.
= 01 charge pump current is 100 μA.
= 10 charge pump current is 125 μA.
= 11 charge pump current is 150 μA.

FR1 <22:18> PLL divider values.

FR1 <22:18>, if the value is > 3 and < 21, the PLL is enabled and the value sets the multiplication factor. If the value is < 4 or >20 the PLL is disabled.

FR1 <23> PLL VCO gain.

FR1 <23> = 0 (default), the low range (system clock below 160 MHz). FR1 <23> = 1, the high range (system clock above 255 MHz).

Function Register 2 (FR2) Description

The FR2 is comprised of two bytes located in Address 0x02.

The FR2 is used to control the various functions, features, and modes of the AD9911. The functionality of each bit is as follows:

FR2<1:0> system clock offset. See the Synchronizing Multiple AD9911 Devices section for more details.

FR2 <3:2> inactive.

FR2 <4:7>. Multidevice synchronization bits. See the Synchronizing Multiple AD9911 Devices section for more details.

FR2 <11:8> inactive.

FR2 <12> Clear phase accumulator.

FR2 <12> = 0 (default), the phase accumulator functions as normal. FR2 <12> = 1, the phase accumulator memory elements are asynchronously cleared.

FR2 <13> Auto clear phase accumulator.

FR2 <13> = 0 (default). A new frequency tuning word is applied to the inputs of the phase accumulator, but not loaded into the accumulator.

FR2 <13> = 1. This bit automatically synchronously clears (loads zeros into) the phase accumulator for one cycle upon reception of the I/O update sequence indicator on both channels.

FR2 <14> Clear sweep accumulator.

FR2 <14> = 0 (default), the sweep accumulator functions as normal. FR2 <14> = 1, the sweep accumulator memory elements are asynchronously cleared.

FR2 <15> Auto clear sweep accumulator.

FR2 <15> = 0 (default). A new delta word is applied to the input, as in normal operation, but not loaded into the accumulator. FR2 <15> = 1. This bit automatically synchronously clears (loads 0s) the sweep accumulator for one cycle upon reception of the I/O_UPDATE sequence indicator on both channels.

CHANNEL FUNCTION REGISTER (CFR) DESCRIPTION

CFR <0> Enable sine function.

CFR <0> = 0 (default). The angle-to-amplitude conversion logic employs a cosine function. CFR <0> = 1. The angle-to-amplitude conversion logic employs a sine function.

CFR <1> Clear phase accumulator.

CFR <1> = 0 (default). The phase accumulator functions as normal. CFR <1> = 1. The phase accumulator memory elements are asynchronously cleared.

CFR <2> auto clear phase accumulator.

CFR <2> = 0 (default). A new frequency tuning word is applied to the inputs of the phase accumulator, but not loaded into the accumulator. CFR <2> = 1. This bit automatically synchronously clears (loads 0s) the phase accumulator for one cycle upon reception of the I/O_UPDATE sequence indicator.

CFR <3> clear sweep accumulator.

CFR <3> = 0 (default). The sweep accumulator functions as normal. CFR <3> = 1. The sweep accumulator memory elements are asynchronously cleared.

CFR <4> auto clear sweep accumulator.

CFR <4> = 0 (default). A new delta word is applied to the input, as in normal operation, but not loaded into the accumulator. CFR <4> = 1. This bit automatically synchronously clears (loads 0s) the sweep accumulator for one cycle upon reception of the I/O_UPDATE sequence indicator.

CFR <5> match pipe delays active.

CFR <5> = 0 (default), match pipe delay mode is inactive. CFR <5> = 1, match pipe delay mode is active. See the Single-Tone Mode—Matched Pipeline Delay section for details.

CFR <6> DAC power-down.

CFR <6> = 0 (default). The DAC is enabled for operation. CFR <6> = 1. The DAC is disabled and held in its lowest power dissipation state.

CFR <7> digital power-down.

CFR <7> = 0 (default). The digital core is enabled for operation.

CFR <7> = 1. The digital core is disabled and is in its lowest power dissipation state.

CFR <9:8>. DAC LSB control (see Table 5).

CFR <9:8> = 00 (default).

CFR <10> must be cleared to 0.

CFR <13> linear sweep ramp rate load at I/O_UPDATE.

CFR <13> = 0 (default). The linear sweep ramp rate timer is loaded only upon timeout (timer = 1); it is not loaded by the I/O_UPDATE input signal.

CFR <13> = 1. The linear sweep ramp rate timer is loaded upon timeout (timer = 1) or at the time of an I/O_UPDATE input signal.

CFR <14> linear sweep enable.

CFR <14> = 0 (default). The linear sweep capability of the AD9911 is inactive. CFR <14> = 1. The linear sweep capability of the AD9911 is active. The delta frequency tuning word is applied to the frequency accumulator at the programmed ramp rate.

CFR <15> linear sweep no-dwell.

CFR <15> = 0 (default). The linear sweep no-dwell function is inactive. CFR <15> = 1. The linear sweep no-dwell function is active. See the Linear Sweep (Shaped) Modulation Mode section for details. If CFR <14> is clear, this bit is ignored.

CFR <18:16> Data align bits for SpurKiller mode. See the SpurKiller/Multitone Mode section for details.

CFR <21:19> inactive.

CFR <23:22> amplitude/frequency/phase select controls, the type of modulation is to be performed for that channel. See the Shift Keying Mode section for examples.

Channel Frequency Tuning Word 0 (CFTW0) Description

CFTW0 <32:0> Frequency Tuning Word 0 for each channel.

Channel Phase Offset Word 0 (CPOW0) Description

CPOW0 <13:0> Phase Offset Word 0 for each channel.

CPOW0 <15:14> inactive.

Amplitude Control Register (ACR) Description

ACR <9:0> amplitude scale factor.

ACR <10> amplitude ramp rate load control bit.

ACR <10> = 0 (default). The amplitude ramp rate timer is loaded only upon timeout (timer = 1) and is not loaded by an I/O_UPDATE input signal (or change in the profile select bits).

ACR <10> = 1. The amplitude ramp rate timer is loaded upon timeout (timer =1) or at the time of an I/O_UPDATE input signal (or change in profile select bits).

ACR <11> auto RU/RD enable (only valid when ACR <12> is active high).

ACR <11> = 0 (default). When ACR <12> is active, Logic 0 on ACR <11> enables the manual RU/RD operation. See the Output Amplitude Control section of this document for details. ACR <11> = 1. If ACR <12> is active, a Logic 1 on ACR <11> enables the AUTO RU/RD operation. See the Output Amplitude Control section for details.

ACR <12> amplitude multiplier enable.

ACR <12> = 0 (default). Amplitude multiplier is disabled. The associated clocks are stopped for power saving; the data from the DDS core is routed around the multipliers.

ACR <12> = 1, amplitude multiplier is enabled.

ACR <13> inactive.

ACR <15:14> amplitude increment/decrement step size. See Table 20 for details.

ACR <23:16> amplitude ramp rate value.

Channel Linear Sweep Register (LSR) Description

LSR <15:0> linear sweep rising ramp rate.

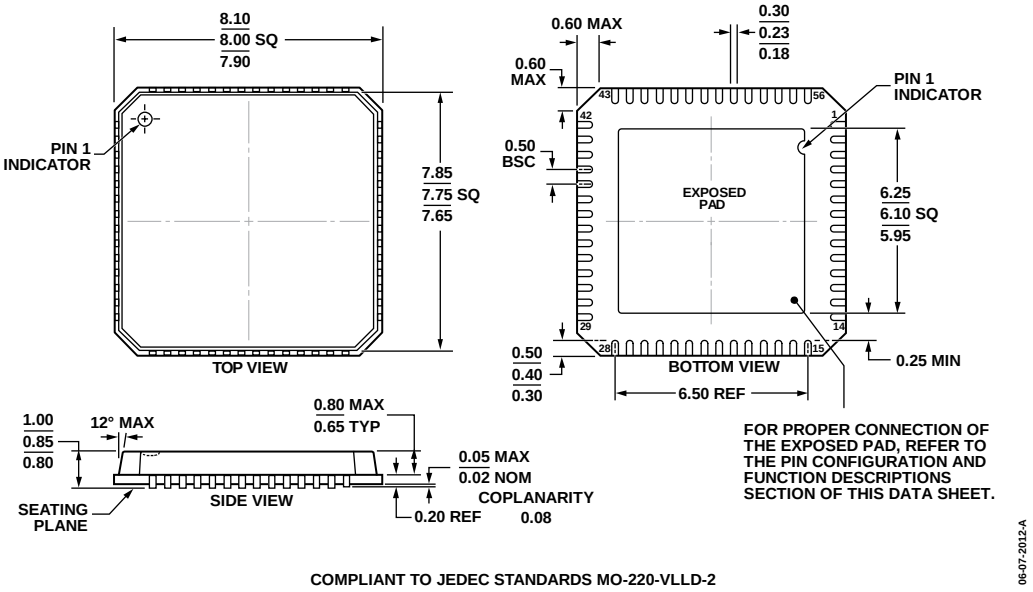
Channel Linear Sweep Rising Delta Word Register (RDW) Description

RDW <31:0> 32-bit rising delta tuning word.

Channel Linear Sweep Falling Delta Word Register (FDW) Description

FDW <31:0> 32-bit falling delta tuning word.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-VLLD-2

Figure 57. 56-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
8 mm × 8 mm Body, Very Thin Quad
(CP-56-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD9911BCPZ	–40°C to +85°C	56-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-56-1
AD9911BCPZ-REEL7	–40°C to +85°C	56-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-56-1
AD9911/PCB		Evaluation Board	

[1] Z = RoHS Compliant Part..

Mouser Electronics

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Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Analog Devices Inc.:

AD9911/PCBZ AD9911BCPZ AD9911BCPZ-REEL7