74HCT4538

Dual retriggerable precision monostable multivibrator

Rev. 6 — 11 February 2021 | Product data sheet

1. General description

The 74HCT4538 is a dual retriggerable-resettable monostable multivibrator. Each multivibrator has two trigger/retrigger inputs ($n\overline{A}$ and nB), a direct reset input ($n\overline{CD}$), two complementary outputs (nQ and $n\overline{Q}$), and two pins (nREXT/CEXT and nCEXT) for connecting the external timing components C_{EXT} and R_{EXT}. Typical pulse width variation over temperature range is ± 0.2 %. The device may be triggered by either the positive or the negative edges of the input pulse. The duration and accuracy of the output pulse are determined by the external timing components C_{EXT} and R_{EXT}. The output pulse width (T_W) is equal to 0.7 × R_{EXT} × C_{EXT}. The linear design techniques guarantee precise control of the output pulse width. A LOW level at $n\overline{CD}$ terminates the output pulse immediately. Schmitt-trigger action in the trigger inputs makes the circuit highly tolerant to slower rise and fall times. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}.

2. Features and benefits

- Tolerant of slow trigger rise and fall times
- High noise immunity
- Separate reset inputs
- Triggering from falling or rising edge
- Complies with JEDEC standard no. 7A
- Wide supply voltage range from 4.5 to 5.5 V
- CMOS low power dissipation
- TTL input levels
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level B
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HCT4538D	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HCT4538PW	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1

nexperia

4. Functional diagram

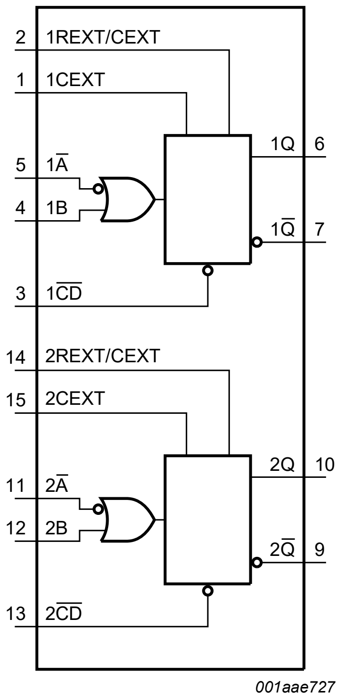


Fig. 1. Functional diagram

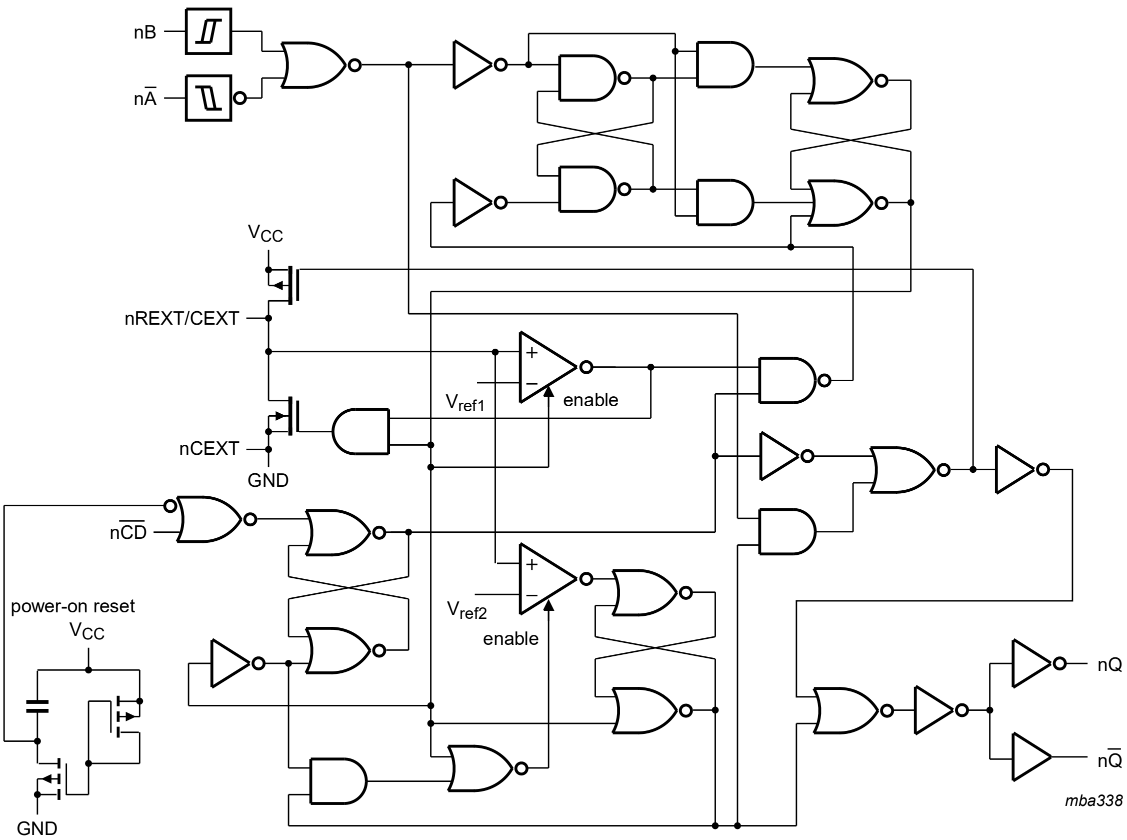


Fig. 2. Logic diagram (one multivibrator)

5. Pinning information

5.1. Pinning

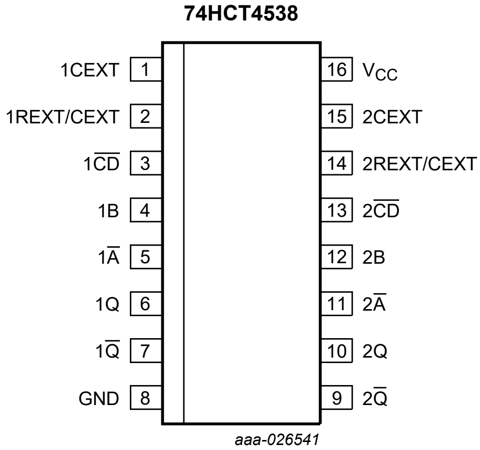


Fig. 3. Pin configuration SOT109-1 (SO16)

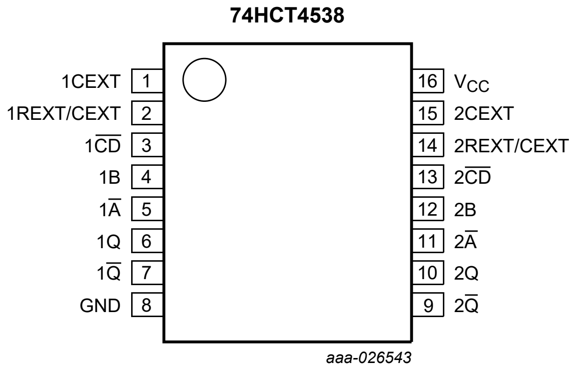


Fig. 4. Pin configuration SOT403-1 (TSSOP16)

5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1CEXT, 2CEXT	1, 15	external capacitor connection (always connected to ground)
1REXT/CEXT, 2REXT/CEXT	2, 14	external capacitor/resistor connection
1$\overline{CD}$, 2$\overline{CD}$	3, 13	direct reset input (active LOW)
1B, 2B	4, 12	input (LOW to HIGH triggered)
1$\overline{A}$, 2$\overline{A}$	5, 11	input (HIGH to LOW triggered)
1Q, 2Q	6, 10	output
1$\overline{Q}$, 2$\overline{Q}$	7, 9	complementary output (active LOW)
GND	8	ground (0 V)
V_{CC}	16	supply voltage

6. Functional description

Table 3. Function table

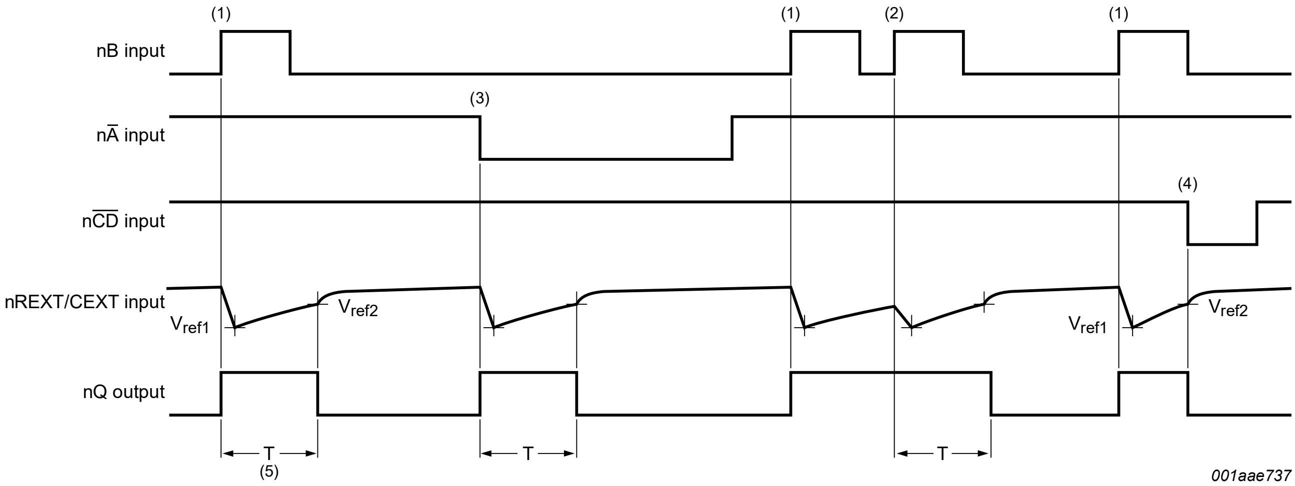
H = HIGH voltage level; L = LOW voltage level; X = don't care;

↑ = positive-going transition; ↓ = negative-going transition;

⊓ *= one HIGH level output pulse, with the pule width determined by C_{EXT} and R_{EXT};*

⊔ *= one LOW level output pulse, with the pulse width determined by C_{EXT} and R_{EXT}.*

Inputs			Outputs	
n$\overline{A}$	**nB**	**n$\overline{CD}$**	**nQ**	**n$\overline{Q}$**
↓	L	H	⊓	⊔
H	↑	H	⊓	⊔
X	X	L	L	H



(1) Positive edge triggering.
(2) Positive edge re-triggering (pulse lengthening).
(3) Negative edge triggering.
(4) Reset (pulse shortening).
(5) $T_W = 0.7 \times R_{EXT} \times C_{EXT}$ (see also Fig. 6).

Fig. 5. Timing diagram

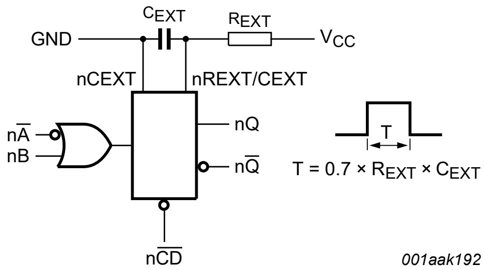


Fig. 6. Connection of the external timing components R_{EXT} and C_{EXT}

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7.0	V
I_{IK}	input clamping current	V_I < -0.5 V or V_I > V_{CC} + 0.5 V [1]	-	±20	mA
I_{OK}	output clamping current	V_O < -0.5 V or V_O > V_{CC} + 0.5 V [1]	-	±20	mA
I_O	output current	V_O = -0.5 V to V_{CC} + 0.5 V	-	±25	mA
I_{CC}	supply current		-	+50	mA
I_{GND}	ground current		-50	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	T_{amb} = -40 °C to +125 °C [2]	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SOT109-1 (SO16) package: P_{tot} derates linearly with 12.4 mW/K above 110 °C.
For SOT403-1 (TSSOP16) package: P_{tot} derates linearly with 8.5 mW/K above 91 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		4.5	5.0	5.5	V
V_I	input voltage		0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	V
T_{amb}	ambient temperature		-40	-	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V_{CC} = 4.5 V	-	1.67	139	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
V_{IH}	HIGH-level input voltage	V_{CC} = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	2.0	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	-	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}; V_{CC} = 4.5 V								
		I_O = -20 µA	4.4	4.5	-	4.4	-	4.4	-	V
		I_O = -4.0 mA	3.98	4.32	-	3.84	-	3.7	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}; V_{CC} = 4.5 V								
		I_O = 20 µA; V_{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 4.0 mA; V_{CC} = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
I_I	input leakage current	V_I = V_{CC} or GND; V_{CC} = 5.5 V	-	-	±0.1	-	±1	-	±1	µA
		pin nREXT/CEXT; V_I = 2.0 V or GND; other inputs at V_{CC} or GND; V_{CC} = 5.5 V [1]	-	-	±0.5	-	±5	-	±10	µA
I_{CC}	supply current	V_I = V_{CC} or GND; I_O = 0 A; V_{CC} = 5.5 V	-	-	8.0	-	80	-	160	µA
ΔI_{CC}	additional supply current	V_I = V_{CC} - 2.1 V; I_O = 0 A; other inputs at V_{CC} or GND; V_{CC} = 4.5 V to 5.5 V								
		pin n$\overline{A}$, nB	-	50	180	-	225	-	245	µA
		pin n$\overline{CD}$	-	65	234	-	293	-	319	µA
C_I	input capacitance		-	3.5	-	-	-	-	-	pF

[1] This measurement can only be carried out after a trigger pulse is applied.

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 9.

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t_{PLH}	LOW to HIGH propagation delay	n$\overline{A}$, nB to nQ; see Fig. 7								
		V_{CC} = 4.5 V	-	35	60	-	75	-	90	ns
		V_{CC} = 5.0 V; C_L = 15 pF	-	30	-	-	-	-	-	ns
		n$\overline{CD}$ to n$\overline{Q}$; see Fig. 7								
		V_{CC} = 4.5 V	-	35	60	-	75	-	90	ns
t_{PHL}	HIGH to LOW propagation delay	n$\overline{A}$, nB to n$\overline{Q}$; see Fig. 7								
		V_{CC} = 4.5 V	-	35	60	-	75	-	90	ns
		V_{CC} = 5.0 V; C_L = 15 pF	-	30	-	-	-	-	-	ns
		n$\overline{CD}$ to nQ; see Fig. 7								
		V_{CC} = 4.5 V	-	35	60	-	75	-	90	ns
t_t	transition time	nQ and n$\overline{Q}$; see Fig. 7 [1]								
		V_{CC} = 4.5 V	-	7	15	-	19	-	21	ns
t_W	pulse width	n$\overline{A}$ LOW; see Fig. 8								
		V_{CC} = 4.5 V	20	11	-	25	-	30	-	ns
		nB HIGH; see Fig. 8								
		V_{CC} = 4.5 V	16	5	-	20	-	24	-	ns
		n$\overline{CD}$ LOW; see Fig. 8								
		V_{CC} = 4.5 V	20	11	-	25	-	30	-	ns
		nQ and n$\overline{Q}$ HIGH or LOW; see Fig. 8								
		V_{CC} = 5.0 V; C_{EXT} = 0.1 μF; R_{EXT} = 10 kΩ	630	700	770	602	798	595	805	μs
t_{rec}	recovery time	n$\overline{CD}$ to n$\overline{A}$, nB; see Fig. 8								
		V_{CC} = 4.5 V	7	2	-	9	-	11	-	ns
t_{rtrig}	retrigger time	n$\overline{A}$, nB; see Fig. 8; X = C_{EXT} / (4.5 x V_{CC})								
		V_{CC} = 4.5 V	-	80+X	-	-	-	-	-	ns
R_{EXT}	external timing resistor	V_{CC} = 5.0 V	2	-	1000	-	-	-	-	kΩ
C_{EXT}	external timing capacitor	V_{CC} = 5.0 V	no limits							
C_{PD}	power dissipation capacitance	per multivibrator; V_I = GND to V_{CC} - 1.5 V [2]	-	138	-	-	-	-	-	pF

[1] t_t is the same as t_{THL} and t_{TLH}.

[2] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}{}^2 \times f_i + \Sigma(C_L \times V_{CC}{}^2 \times f_o) + 0.48 \times C_{EXT} \times V_{CC}{}^2 \times f_o + D \times 0.8 \times V_{CC}$ where:

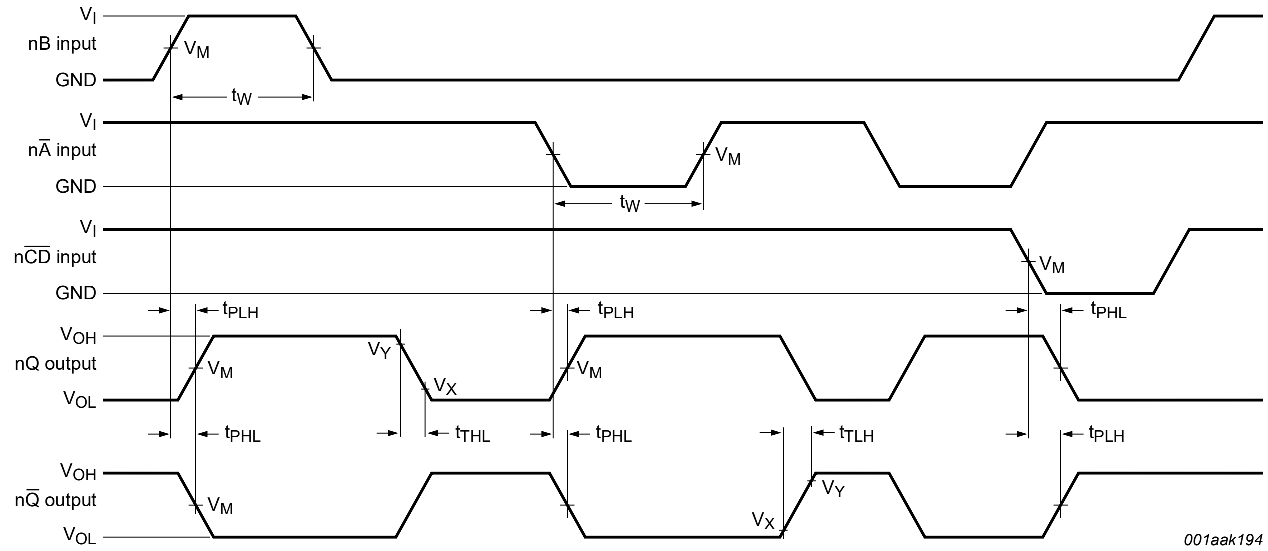
f_i = input frequency in MHz; f_o = output frequency in MHz;

$\Sigma(C_L \times V_{CC}{}^2 \times f_o)$ = sum of the outputs; C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

D = duty cycle factor in %; C_{EXT} = external timing capacitance in pF.

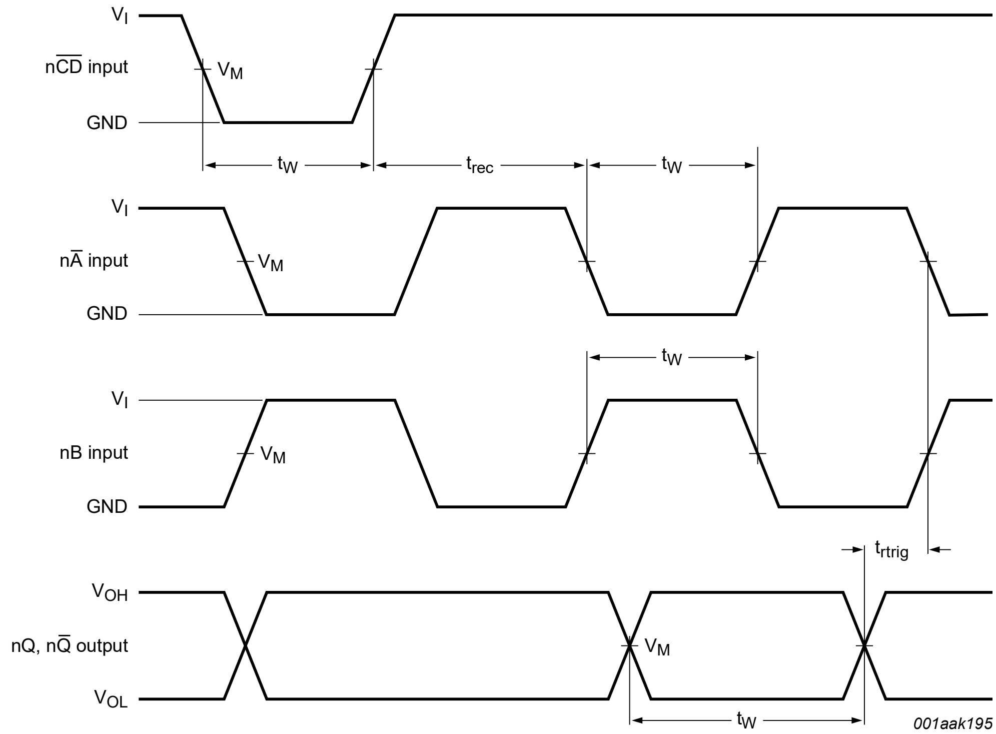
10.1. Waveforms and test circuit



Measurement points are given in Table 8.

Logic levels: V_{OL} and V_{OH} are typical output levels that occur with the output load.

Fig. 7. Waveforms showing propagation delays and transition times



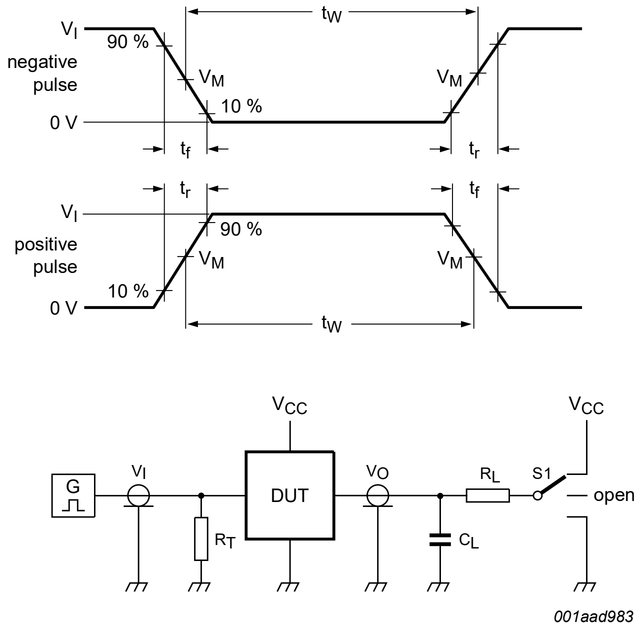
Measurement points are given in Table 8.

Logic levels: V_{OL} and V_{OH} are typical output levels that occur with the output load.

Fig. 8. Waveforms showing nA̅, nB, nQ, nQ̅ pulse widths, recovery and retrigger times

Table 8. Measurement points

Input	Output		
V_M	V_M	V_X	V_Y
1.3 V	1.3 V	$0.1V_{CC}$	$0.9V_{CC}$



Test data is given in Table 9 .

Definitions test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = Load capacitance including jig and probe capacitance.

R_L = Load resistance.

S1 = Test selection switch

Fig. 9. Test circuit for measuring switching times

Table 9. Test data

Input		Load		S1 position
V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}
3 V	6 ns	15 pF, 50 pF	1 kΩ	open

11. Application information

11.1. Power-down considerations

A large capacitor (C_{EXT}) may cause problems when powering-down the monostable due to energy stored in this capacitor. When a system containing this device is powered-down or rapid decrease of V_{CC} to zero occurs, the monostable may sustain damage, due to the capacitor discharging through the input protection diodes. To avoid this possibility, use a damping diode (D_{EXT}) preferably a germanium or Schottky type diode able to withstand large current surges and connect as shown in Fig. 10

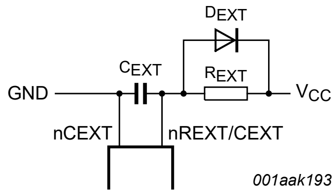
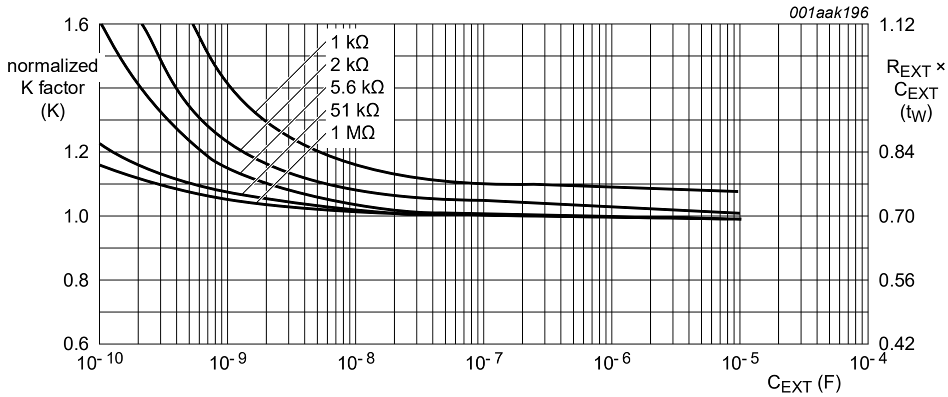


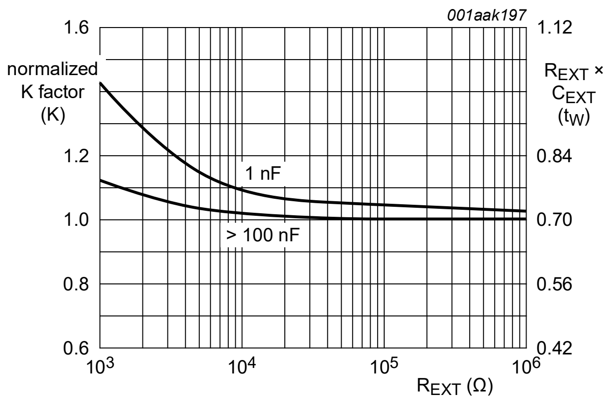
Fig. 10. Power-down protection circuit

11.2. Graphs



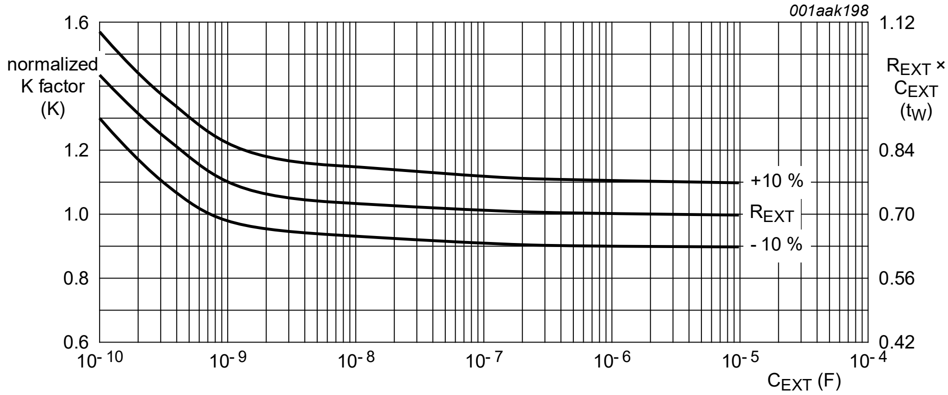
V_{CC} = 4.5 V; T_{amb} = 25 °C.

Fig. 11. Typical pulse width accuracy versus external capacitance



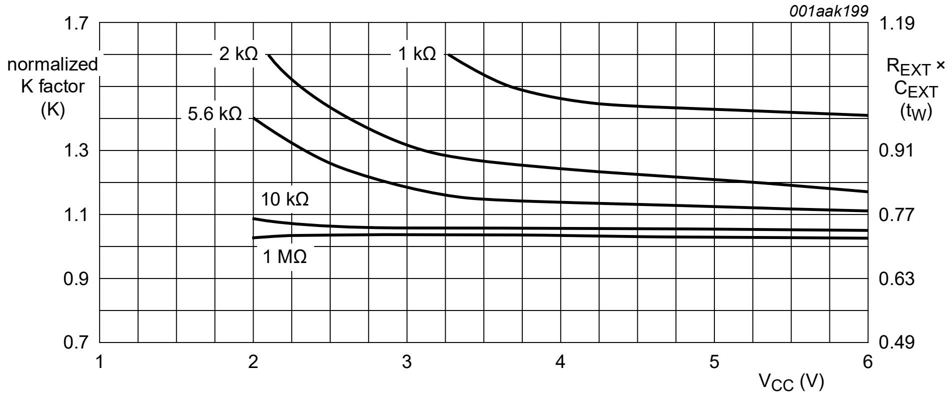
V_{CC} = 4.5 V; T_{amb} = 25 °C.

Fig. 12. Typical pulse width accuracy versus external resistance



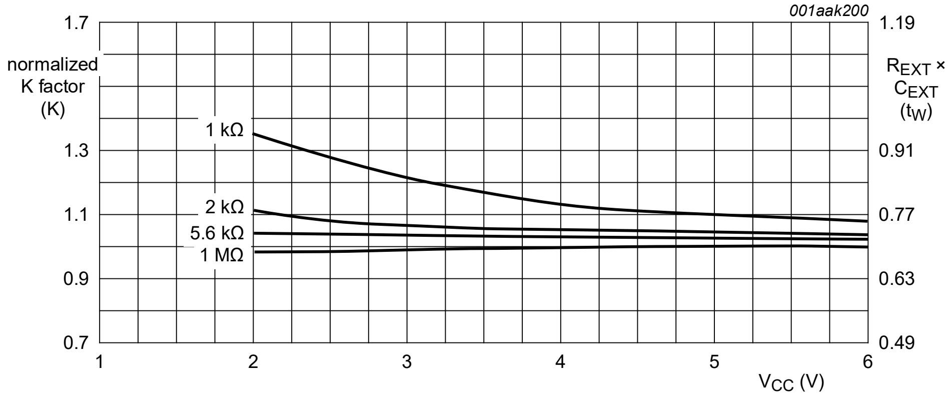
V_{CC} = 4.5 V; R_{EXT} = 10 kΩ; T_{amb} = 25 °C.

Fig. 13. Typical pulse width accuracy versus external capacitance



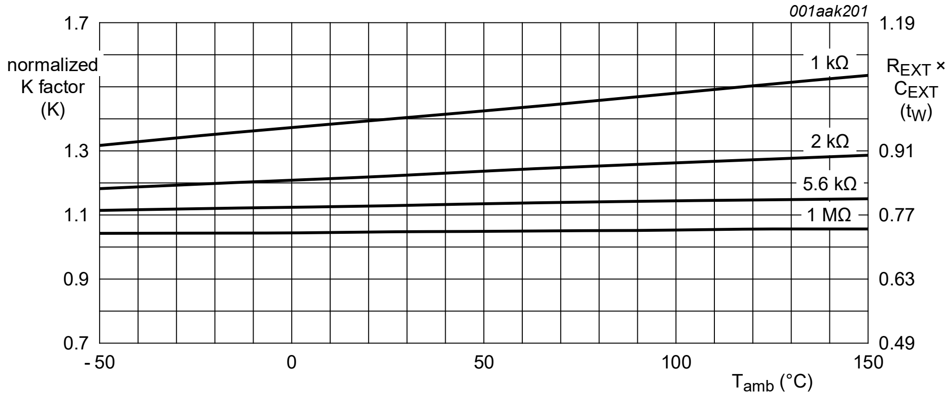
C_{EXT} = 1 nF; T_{amb} = 25 °C.

Fig. 14. Typical pulse width accuracy versus power supply



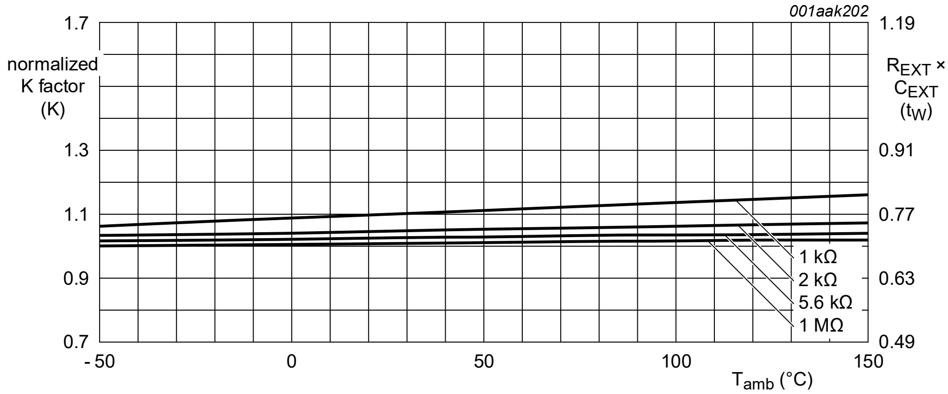
C_{EXT} = 100 nF; T_{amb} = 25 °C.

Fig. 15. Typical pulse width accuracy versus power supply



V_{CC} = 4.5 V; C_{EXT} = 1 nF; T_{amb} = 25 °C.

Fig. 16. Typical pulse width accuracy versus temperature

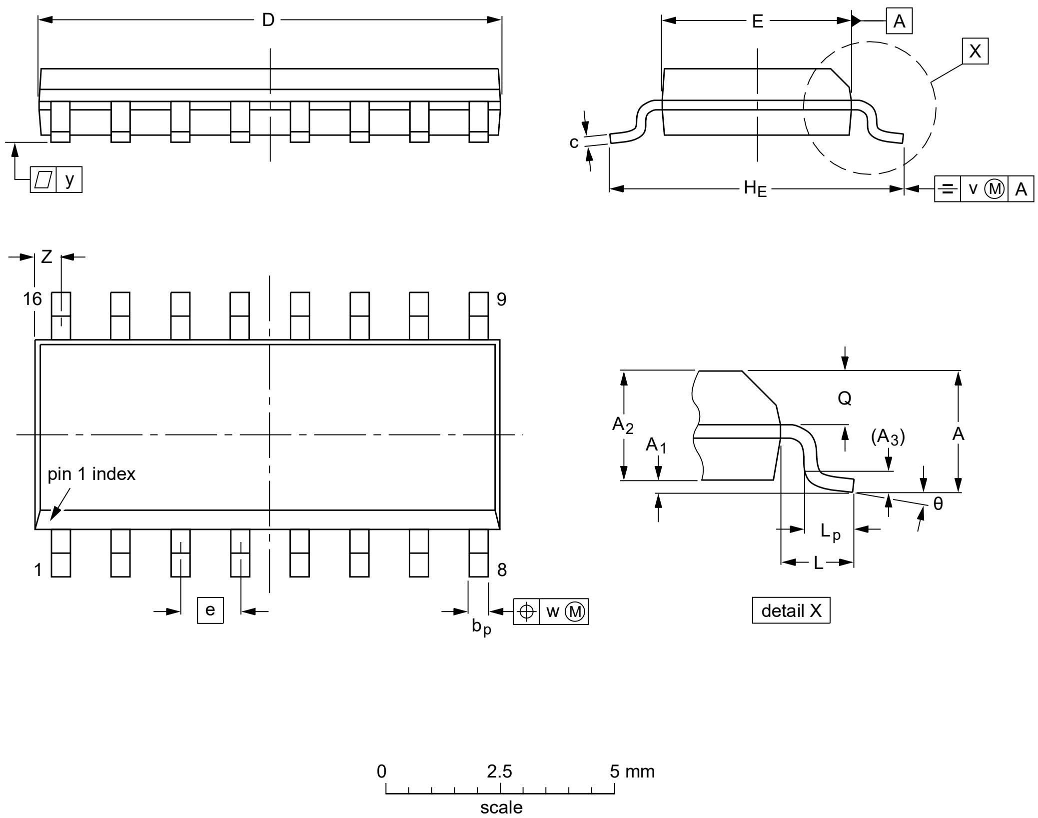


V_{CC} = 4.5 V; C_{EXT} = 1 μF; T_{amb} = 25 °C.

Fig. 17. Typical pulse width accuracy versus temperature

12. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	H_E	L	L_p	Q	v	w	y	Z(1)	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

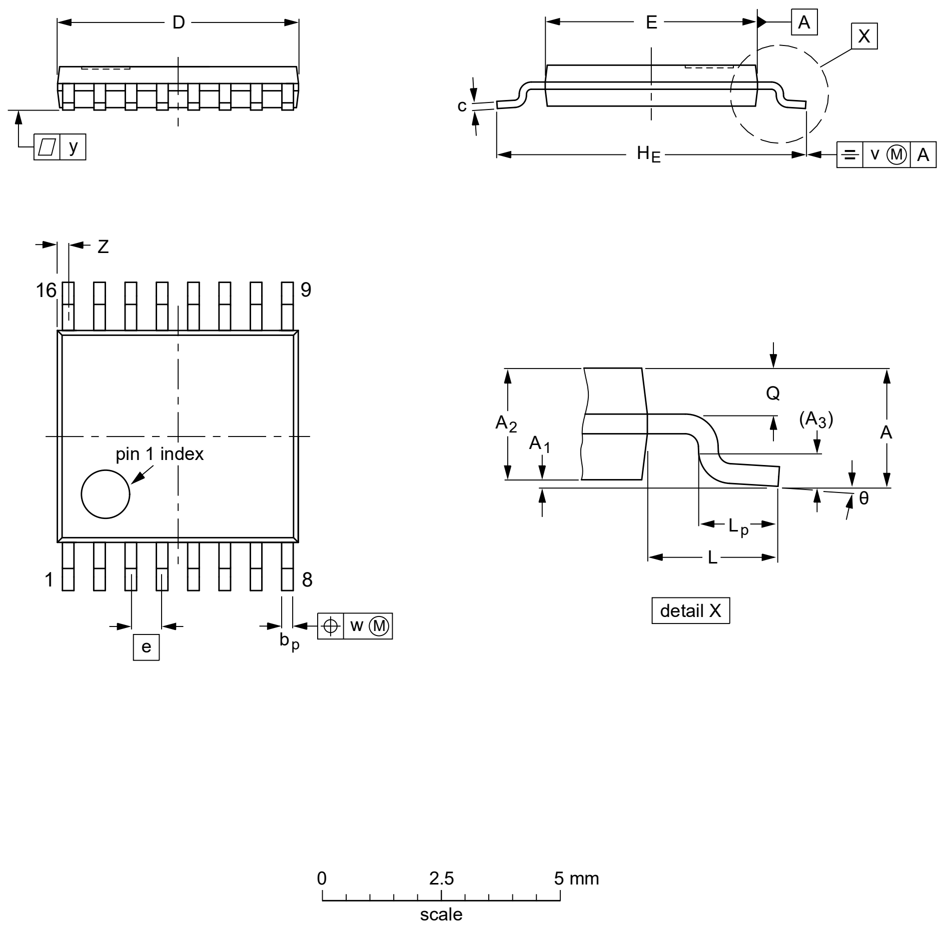
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT109-1	076E07	MS-012				~~99-12-27~~ 03-02-19

Fig. 18. Package outline SOT109-1 (SO16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT403-1		MO-153				~~99-12-27~~ 03-02-18

Fig. 19. Package outline SOT403-1 (TSSOP16)

13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HCT4538 v.6	20210211	Product data sheet	-	74HCT4538 v.5
Modifications:	• Type number 74HCT4538DB (SOT338-1 / SSOP16) removed. • Section 2 updated. • Section 7: Derating values for P_{tot} total power dissipation updated.			
74HCT4538 v.5	20170317	Product data sheet	-	74HC_HCT4538 v.4
Modifications:	• Type numbers 74HC4538D, 74HC4538DB and 74HC4538PW removed.			
74HC_HCT4538 v.4	20160224	Product data sheet	-	74HC_HCT4538 v.3
Modifications:	• Type numbers 74HC4538N and 74HCT4538N (SOT38-4) removed.			
74HC_HCT4538 v.3	20090608	Product data sheet	-	74HC_HCT4538_CNV v.2
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Pin names changed throughout. • Section Section 7, Section 8 and Section 9 added, taken from the 74HC/T HCMOS Family characteristics/specification (March 1988). • Test circuit added: Fig. 9. • Quick reference data incorporated in to Section 9 and Section 10. • Package information added for DIP16, SO16, SSOP16 and TSSOP16 packages.			
74HC_HCT4538_CNV v.2	19970902	Product specification	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. Nexperia does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

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