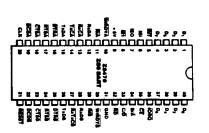


### Zilog

Z08470 Customer Procurement Spec (CPS)

GENERAL DESCRIPTION

In Z80 DART (Dual-Channel Asynchronous Hecever/
Transmitter) is a dual-channel multifunction peripheral
component that statisties a wide variety of asynchronous
serial data communications requirements in microcomputer
systems. The Z80 DART is used as a serial-to-parallel,
parallel-to-serial connectifunction in asynchronous
applications in addition, the device also provides moder
controls for both channels in applications where moder
controls are not needed, these lines can be used for
general-purpose VO.



40-Pin Dual-In-Line Package (DIP), Pin Assignments

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desion.

Zlog, Inc 1315 Dell Ave , Campbell, California 95008 Telephone (408)370-8000 TWX 910-338-7621

(MARCOM) DC2847

DOCUMENT CONTROL\_ MASTER

## DC CHARACTERISTICS

Ĭ	Parenty	•	ł	Ĩ	Test Condition
ř	Chock Inqual Low Vollage	•£0-	+0.45*	۷	
š	Clock Input High Vollage	AC-000	+5.54	<	
<b>خ</b>	Input Low Vollage	-0.34	•0.0	<	
Į.	ingual High Vollage	· 2.0*	.5.5	<	
đ	Output Low Vollege		.0.44	<	Q - 20mA
ğ	Output High Vallage	•24•		<	Q1 250 A
•	Input/3-State Output Lastings Current	700	5	3.	0.4 < V <sub>PM</sub> < 2.4V
5	Ri Pin Lesiage Current	ě	• • •	3	0.4 < V <sub>PM</sub> < 2.4V
ส	Power Supply Current		8	3	

in-orth PPC No. - - PV sPh a losted b Gueranteed by Design e Gueranteed by Cheracterization

# AC CHARACTERISTICS\*

8	<b>3</b>	<b>=</b>	7	16	15	ī	<b>5</b>	z	=	ಕ	•	•	7	•	5	•	•	₩	1	I
ToC(W/RWz)	TOC(W/RPI)	TOTOWIRWIN	TOC(INT)	TOREIGNEON	TOTEL(TEO)	TOM I (TEO)	TafEIRO)	Take (C)	Talopon	ToPID(DOz)	1000		T603(0)	T-MO(C)	Š	ಕ	ਰੋ	\$	8	*
Clock 4 to W/RDY Float Datey (Wast Mode)	Clock 1 to W/RDY 4 Datay (Ready Mode)	IORG I or CE I to WIRDY IDalay (Max Mode)	Clock 1 to INT 4 Datey	REI 4 to REO 4 Datay	IEI 1 to IEO 1 Dalay (after ED decode)	MT 4 to IEO 4 Daley (interrupt before M1)	IEI to IORO I Setup Time (INTRICK Cycle)	MT to Clack t Setup Time	IONG I to Date Out Date; (INTRCX Cycle)	RD to Data Out Roat Datey	Date in to Clock I Setup (Write or M1 Cycle)	Clock 1 to Date Out Datey	IORO, RD to Clock t Setup Time	CE, C/D, B/Ā to Clock † Satup Time	Clock Width (Low)	Clock Rise Time	Clock Fell Time	Chack Wilden (Flight)	Clock Cycle Time	Personaler
							140 0	8			80		115.	š	ã			98.	250	F 70
130°	120	210c	200	8	<b>100</b> °	190 c			1800	1100		220			2000	30.	8	\$000°	900	
							120°	75•			8		8	8	š			3	8	¥ 0.
110¢	800	175 e	350 <b>•</b>	70•	700	180°			100°	8		50			2000°	15 <b>e</b>	5.	2000	•000	1

'Union neroscords (re).

a Tested
b Gueranteed by Design
c Gueranteed by Cheracterization

• Ģ 0

# AC CHARACTERISTICS (Continued)

			180-4 DART		280-6 DAR	DART
Humber	Number Symbol	Parameter	ş		<b>\$</b>	ř
-	*	Pulse Width (High)	200°		2000	
N	\$	Pulse Width (Low)	200°		200°	
	Telec C	RC Cycle Time	2000		3000	
•	N BO	BC Width (Low)	1800	ļ	ğ	
•	N BC	TiC width (High)	<b>10</b> 00		<b>8</b> 00	•
•	Totac(tho)	InC + to 1stD Delay		8		220
7	Tobic(W/RRI)	SiC 4 to W/RDY 4 Datay (Ready Mode)	9.0	•	50	•
•	Tellicont)	EC to NT t Datey	9.0	•	80	•
•	Toffuic	RicC Cycle Time	200°	8	300	8
ಕ	<b>1</b>	Rick Width (Low)	180°	•	8	
=	<b>1</b>	Ruc was (ragh)	ğ		8	8,
12	TeRNO(ReC)	RuD to RxC 1 Setup Time (x1 Mode)	9		ő	
ü	THANDANC)	RbD Hald Time (x1 Mode)	140c		ğ	
z	Toffic(W/RRI)	RxC 1 to W/RDY I Datey (Ready Mode)	10°	130	ō	130
ಕ	TURNC(INT)	RIC 110 RVT + Daley	100	136	ő	130

\* In plint of the System Cock rate must be at least the arrest the answer must be achieve minimum of one complete dock cycle. I these could be System Cock Pariods.

I these could be System Cock Pariods.

I the could be supported that the system of the System Cock Pariods of the System Cock

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