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February 2016

# HCPL3700M AC/DC to Logic Interface Optocoupler

## Features

- AC or DC Input
- Programmable Sense Voltage
- Logic Level Compatibility
- Threshold Guaranteed Over Temperature (0°C to 70°C)
- Safety and Regulatory Approvals
  - UL1577, 5,000 VAC<sub>RMS</sub> for 1 Minute
  - DIN EN/IEC60747-5-5

## Applications

- Low Voltage Detection
- 5 V to 240 V AC/DC Voltage Sensing
- Relay Contact Monitor
- Current Sensing
- Microprocessor Interface
- Industrial Controls

## Description

The HCPL3700M voltage/current threshold detection optocoupler consists of an AlGaAs LED connected to a threshold sensing input buffer IC which are optically coupled to a high gain darlington output. The input buffer chip is capable of controlling threshold levels over a wide range of input voltages with a single resistor. The output is TTL and CMOS compatible.

## Schematics

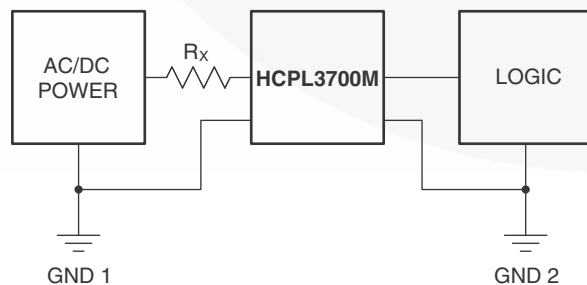
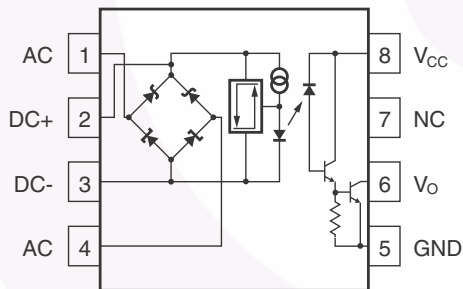


Figure 1. Schematic

## Package Outlines

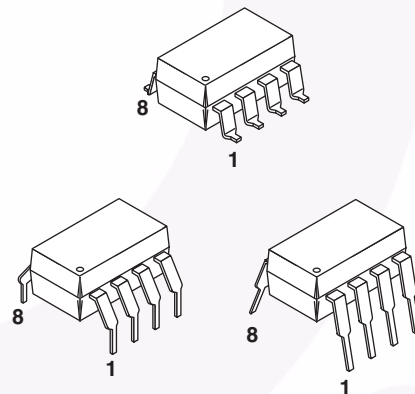


Figure 2. Package Outlines

TRUTH TABLE  
(Positive Logic)

Input	Output
H	L
L	H

A 0.1µF bypass capacitor must be connected between pins 8 and 5.

## Safety and Insulation Ratings

As per DIN EN/IEC 60747-5-5, this optocoupler is suitable for “safe electrical insulation” only within the safety limit data. Compliance with the safety ratings shall be ensured by means of protective circuits.

Parameter	Characteristics	
Installation Classifications per DIN VDE 0110/1.89 Table 1, For Rated Mains Voltage	< 150 V <sub>RMS</sub>	I–IV
	< 300 V <sub>RMS</sub>	I–IV
	< 450 V <sub>RMS</sub>	I–III
	< 600 V <sub>RMS</sub>	I–III
	< 1000 V <sub>RMS</sub> (Option TV)	I–III
Climatic Classification	40/85/21	
Pollution Degree (DIN VDE 0110/1.89)	2	
Comparative Tracking Index	175	

Symbol	Parameter	Value	Unit
V <sub>PR</sub>	Input-to-Output Test Voltage, Method A, V <sub>IORM</sub> × 1.6 = V <sub>PR</sub> , Type and Sample Test with t <sub>m</sub> = 10 s, Partial Discharge < 5 pC	2,262	V <sub>peak</sub>
	Input-to-Output Test Voltage, Method B, V <sub>IORM</sub> × 1.875 = V <sub>PR</sub> , 100% Production Test with t <sub>m</sub> = 1 s, Partial Discharge < 5 pC	2,651	V <sub>peak</sub>
V <sub>IORM</sub>	Maximum Working Insulation Voltage	1,414	V <sub>peak</sub>
V <sub>IOTM</sub>	Highest Allowable Over-Voltage	6,000	V <sub>peak</sub>
	External Creepage	≥ 8	mm
	External Clearance	≥ 7.4	mm
	External Clearance (for Option TV, 0.4" Lead Spacing)	≥ 10.16	mm
DTI	Distance Through Insulation (Insulation Thickness)	≥ 0.5	mm
T <sub>S</sub>	Case Temperature <sup>(1)</sup>	150	°C
I <sub>S,INPUT</sub>	Input Current <sup>(1)</sup>	25	mA
P <sub>S,OUTPUT</sub>	Output Power (Duty Factor ≤ 2.7%) <sup>(1)</sup>	250	mW
R <sub>IO</sub>	Insulation Resistance at T <sub>S</sub> , V <sub>IO</sub> = 500 V <sup>(1)</sup>	> 10 <sup>9</sup>	Ω

**Note:**

1. Safety limit value - maximum values allowed in the event of a failure.

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.  $T_A = 25^\circ\text{C}$  unless otherwise specified.

Symbol	Parameter	Value	Unit
$T_{STG}$	Storage Temperature	-40 to +125	$^\circ\text{C}$
$T_{OPR}$	Operating Temperature	-40 to +85	$^\circ\text{C}$
$T_J$	Junction Temperature	-40 to +125	$^\circ\text{C}$
$T_{SOL}$	Lead Solder Temperature	260 for 10 sec	$^\circ\text{C}$
$P_T$	Total Package Power Dissipation <sup>(2)</sup>	305	mW
<b>EMITTER</b>			
$I_{IN}$	Input Current	Average	50
		Surge, 3 ms, 120 Hz Pulse Rate	140
		Transient, 10 $\mu\text{s}$ , 120 Hz Pulse Rate	500
$V_{IN}$	Input Voltage (Pins 2-3)	-0.5	V
$P_{IN}$	Input Power Dissipation <sup>(3)</sup>	230	mW
<b>DETECTOR</b>			
$I_O$	Output Current (Average) <sup>(4)</sup>	30	mA
$V_{CC}$	Supply Voltage (Pins 8-5)	-0.5 to 20	V
$V_O$	Output Voltage (Pins 6-5)	-0.5 to 20	V
$P_O$	Output Power Dissipation <sup>(5)</sup>	210	mW

### Notes:

2. Derate linearly above  $70^\circ\text{C}$  free-air temperature at a rate of  $2.5 \text{ mW}/^\circ\text{C}$ .
3. Derate linearly above  $70^\circ\text{C}$  free-air temperature at a rate of  $1.8 \text{ mW}/^\circ\text{C}$ .
4. Derate linearly above  $70^\circ\text{C}$  free-air temperature at a rate of  $0.6 \text{ mA}/^\circ\text{C}$ .
5. Derate linearly above  $70^\circ\text{C}$  free-air temperature at a rate of  $1.9 \text{ mW}/^\circ\text{C}$ .

## Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Min.	Max.	Unit
$V_{CC}$	Supply Voltage	2	18	V
$T_A$	Ambient Operating Temperature	0	70	$^\circ\text{C}$
f	Operating Frequency	0	4	kHz

**Electrical Characteristics** ( $T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$  Unless otherwise specified)

Symbol	Parameter		Test Conditions	Min.	Typ.	Max.	Unit
$I_{TH+}$	Input Threshold Current		$V_{IN} = V_{TH+}$ , $V_{CC} = 4.5\text{ V}$	1.96	2.40	3.11	mA
$I_{TH-}$			$V_O = 0.4\text{ V}$ , $I_O \geq 4.2\text{ mA}^{(6)}$	1.00	1.20	1.62	
$V_{TH+}$	Input Threshold Voltage	DC (Pins 2, 3)	$V_{IN} = V_2 - V_3$ (Pins 1 & 4 Open) $V_{CC} = 4.5\text{ V}$ , $V_O = 0.4\text{ V}^{(6)}$ $I_O \geq 4.2\text{ mA}$	3.35	3.80	4.05	V
$V_{TH-}$			$V_{IN} = V_2 - V_3$ (Pins 1 & 4 Open) $V_{CC} = 4.5\text{ V}$ , $V_O = 2.4\text{ V}^{(6)}$ $I_O \geq 100\text{ }\mu\text{A}$	2.01	2.50	2.86	V
$V_{TH+}$		AC (Pins 1, 4)	$ V_{IN} = V_1 - V_4 $ (Pins 2 & 3 Open) $V_{CC} = 4.5\text{ V}$ , $V_O = 0.4\text{ V}^{(6)}$ $I_O \geq 4.2\text{ mA}$	4.23	5.00	5.50	V
$V_{TH-}$			$ V_{IN} = IV_1 - V_4 $ (Pins 2 & 3 Open) $V_{CC} = 4.5\text{ V}$ , $V_O = 2.4\text{ V}^{(6)}$ $I_O \leq 100\text{ }\mu\text{A}$	2.87	3.70	4.20	V
$I_{HYS}$	Hysteresis		$I_{HYS} = I_{TH+} - I_{TH-}$		1.2		mA
$V_{HYS}$			$V_{HYS} = V_{TH+} - V_{TH-}$		1.3		V
$V_{IHC1}$	Input Clamp Voltage		$V_{IHC1} = V_2 - V_3$ , $V_3 = \text{GND}$ , $I_{IN} = 10\text{ mA}$ , Pins 1 & 4 connected to Pin 3	5.4	6.3	6.6	V
$V_{IHC2}$			$V_{IHC2} =  V_1 - V_4 $ , $ I_{IN}  = 10\text{ mA}$ (Pins 2 & 3 Open)	6.1	7.0	7.3	V
$V_{IHC3}$			$V_{IHC3} = V_2 - V_3$ , $V_3 = \text{GND}$ , $I_{IN} = 15\text{ mA}$ (Pins 1 & 4 Open)		12.5	13.4	V
$V_{ILC}$			$V_{ILC} = V_2 - V_3$ , $V_3 = \text{GND}$ , $I_{IN} = -10\text{ mA}$		-0.75		V
$I_{IN}$	Input Current		$V_{IN} = V_2 - V_3 = 5.0\text{ V}$ (Pins 1 & 4 Open)	3.0	3.7	4.4	mA
$V_{D1,2}$	Bridge Diode		$I_{IN} = 3\text{ mA}$		0.65		V
$V_{D3,4}$	Forward Voltage		$I_{IN} = 3\text{ mA}$		0.65		V
$V_{OL}$	Logic LOW Output Voltage		$V_{CC} = 4.5\text{ V}$ , $I_{OL} = 4.2\text{ mA}^{(6)}$		0.04	0.40	V
$I_{OH}$	Logic HIGH Output Current		$V_{OH} = V_{CC} = 18\text{ V}^{(6)}$			100	$\mu\text{A}$
$I_{CCL}$	Logic LOW Supply Current		$V_2 - V_3 = 5.0\text{ V}$ , $V_O = \text{Open}$ , $V_{CC} = 5\text{ V}$		1.0	4	mA
$I_{CCH}$	Logic HIGH Supply Current		$V_{CC} = 18\text{ V}$ , $V_O = \text{Open}$		0.01	4	$\mu\text{A}$
$C_{IN}$	Input Capacitance		$f = 1\text{ MHz}$ , $V_{IN} = 0\text{ V}$ (Pins 2 & 3, Pins 1 & 4 Open)		50		pF

**Note:**

6. Logic LOW output level at pin 6 occurs when  $V_{IN} \geq V_{TH+}$  and when  $V_{IN} > V_{TH-}$  once  $V_{IN}$  exceeds  $V_{TH+}$ .  
Logic HIGH output level at pin 6 occurs when  $V_{IN} \leq V_{TH-}$  and when  $V_{IN} < V_{TH+}$  once decreases below  $V_{TH-}$ .

**Switching Characteristics** ( $T_A = 25^\circ\text{C}$ ,  $V_{CC} = 5\text{ V}$  unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{PHL}$	Propagation Delay Time (to Output Low Level)	$R_L = 4.7\text{ k}\Omega$ , $C_L = 30\text{ pF}^{(7)}$		6.0	15	$\mu\text{s}$
$t_{PLH}$	Propagation Delay Time (to Output High Level)	$R_L = 4.7\text{ k}\Omega$ , $C_L = 30\text{ pF}^{(7)}$		25.0	40	$\mu\text{s}$
$t_R$	Output Rise Time (10–90%)	$R_L = 4.7\text{ k}\Omega$ , $C_L = 30\text{ pF}$		45		$\mu\text{s}$
$t_F$	Output Fall Time (90–10%)	$R_L = 4.7\text{ k}\Omega$ , $C_L = 30\text{ pF}$		0.5		$\mu\text{s}$
$ CM_H $	Common Mode Transient Immunity (at Output High Level)	$I_{IN} = 0\text{ mA}$ , $R_L = 4.7\text{ k}\Omega$ , $V_{O\text{ min}} = 2.0\text{ V}$ , $V_{CM} = 1400\text{ V}^{(8)(9)}$		4000		$\text{V}/\mu\text{s}$
$ CM_L $	Common Mode Transient Immunity (at Output Low Level)	$I_{IN} = 3.11\text{ mA}$ , $R_L = 4.7\text{ k}\Omega$ , $V_{O\text{ max}} = 0.8\text{ V}$ , $V_{CM} = 1400\text{ V}^{(8)(9)}$		600		$\text{V}/\mu\text{s}$

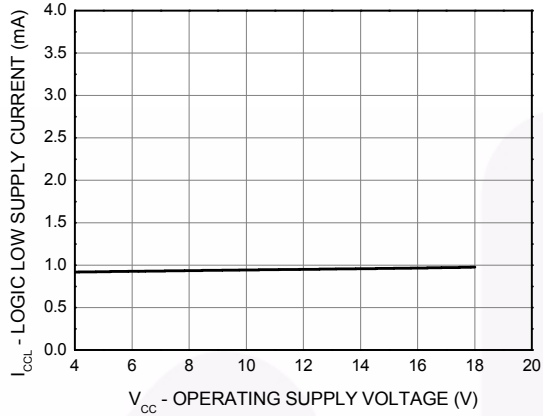
**Isolation Characteristics** ( $T_A = 25^\circ\text{C}$  unless otherwise specified.)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{ISO}$	Withstand Isolation Voltage	$RH \leq 50\%$ , $I_{I-O} \leq 10\text{ }\mu\text{A}$ $t = 1\text{ minute}$ , $f = 50\text{ Hz}^{(10)(11)}$	5000			$\text{VAC}_{\text{RMS}}$
$R_{I-O}$	Resistance (Input to Output)	$V_{IO} = 500\text{ V}_{\text{DC}}^{(10)}$		$10^{12}$		$\Omega$
$C_{I-O}$	Capacitance (Input to Output)	$f = 1\text{ MHz}$ , $V_{IO} = 0\text{ V}_{\text{DC}}$		0.6		$\text{pF}$

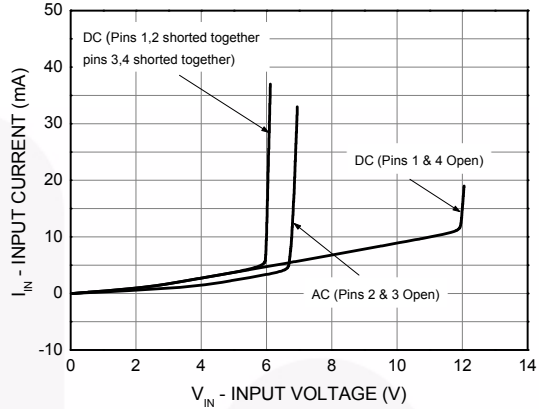
**Notes:**

- $T_{PHL}$  propagation delay is measured from the 2.5 V level of the leading edge of a 5.0 V input pulse (1  $\mu\text{s}$  rise time) to the 1.5 V level on the leading edge of the output pulse.  $T_{PLH}$  propagation delay is measured on the trailing edges of the input and output pulse. (Refer to Fig. 11)
- Common mode transient immunity in logic high level is the maximum tolerable (positive)  $dV_{cm}/dt$  on the leading edge of the common mode pulse signal  $V_{CM}$ , to assure that the output will remain in a logic high state (i.e.,  $V_O > 2.0\text{ V}$ ). Common mode transient immunity in logic low level is the maximum tolerable (negative)  $dV_{cm}/dt$  on the trailing edge of the common mode pulse signal,  $V_{CM}$ , to assure that the output will remain in a logic low state (i.e.,  $V_O < 0.8\text{ V}$ ). Refer to Fig. 12.
- In applications where  $dV_{cm}/dt$  may exceed 50,000  $\text{V}/\mu\text{s}$  (Such as static discharge), a series resistor,  $R_{CC}$ , should be included to protect the detector chip from destructive surge currents. The recommended value for  $R_{CC}$  is 240  $\Omega$  per volt of allowable drop in  $V_{CC}$  (between pin 8 and  $V_{CC}$ ) with a minimum value of 240  $\Omega$ .
- Device is considered a two terminal device: Pins 1, 2, 3 and 4 are shorted together and Pins 5, 6, 7 and 8 are shorted together.
- The 5000  $\text{VAC}_{\text{RMS}}/1\text{ min.}$  capability is validated by a 6000  $\text{VAC}_{\text{RMS}}/1\text{ sec.}$  dielectric voltage withstand test.

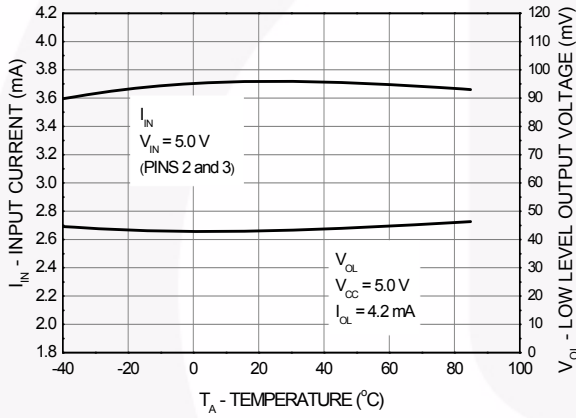
## Typical Performance Curves



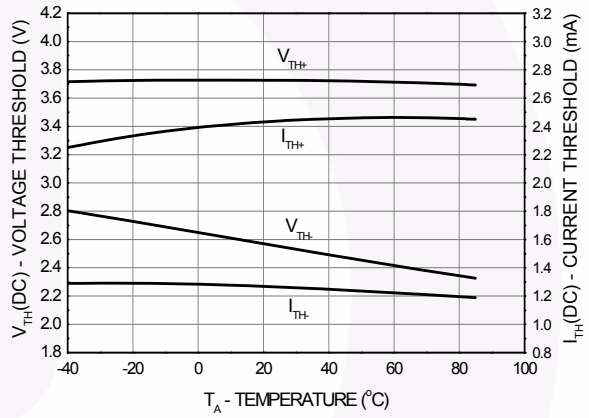
**Figure 3. Logic Low Supply Current vs. Operating Supply Voltage**



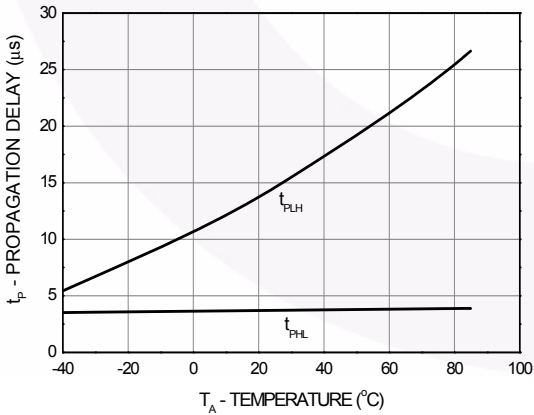
**Figure 4. Input Current vs. Input Voltage**



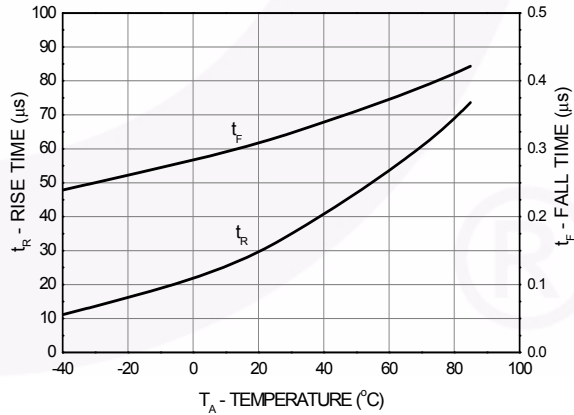
**Figure 5. Input Current/Low Level Output Voltage vs. Temperature**



**Figure 6. Current Threshold/Voltage Threshold vs. Temperature**



**Figure 7. Propagation Delay vs. Temperature**



**Figure 8. Rise and Fall Time vs. Temperature**

Typical Performance Curves (Continued)

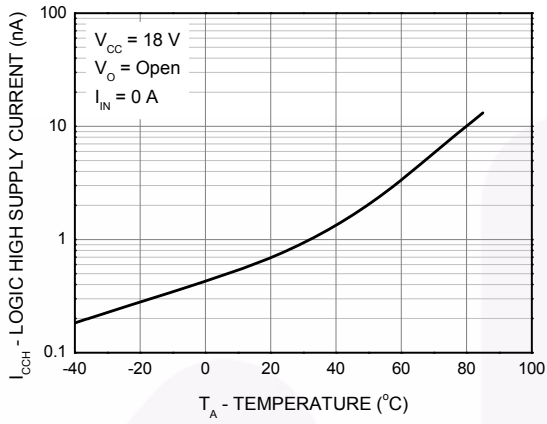


Figure 9. Logic High Supply Current vs. Temperature

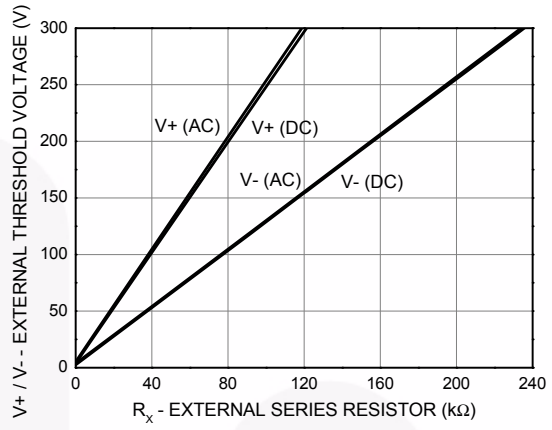
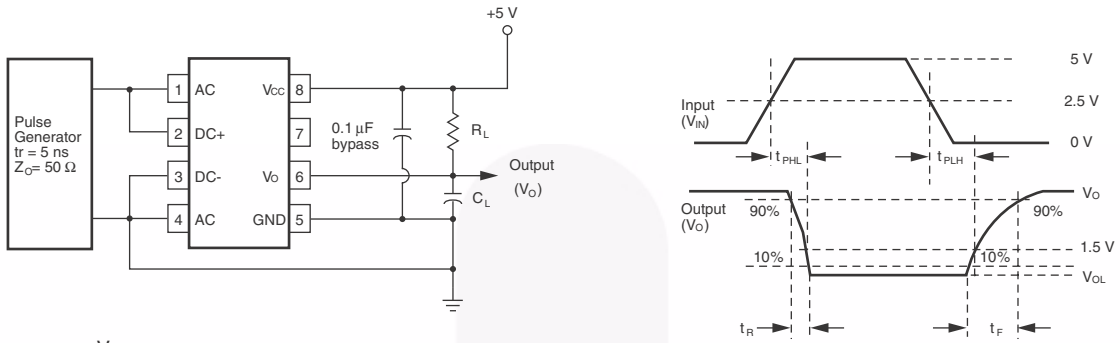


Figure 10. External Threshold Characteristics  $V_+/V_-$  vs.  $R_x$

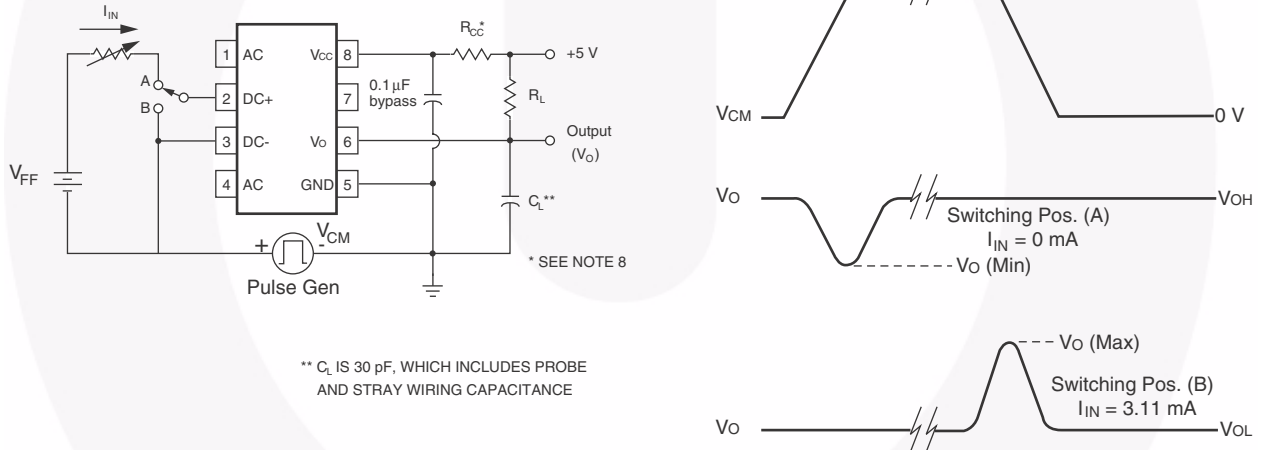


Test Circuits



$V_{IN}$   
 Pulse Amplitude = 50 V  
 Pulse Width = 1 ms  
 f = 100 Hz  
 $T_r = T_f = 1.0 \mu s$  (10%–90%)

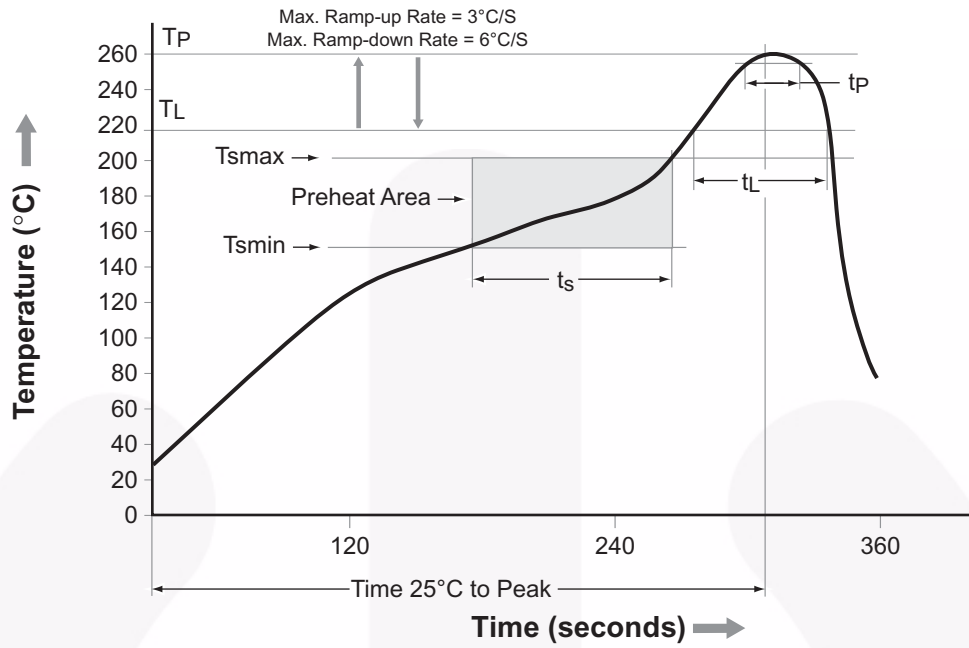
Fig. 11. Switching Test Circuit



\*\*  $C_L$  IS 30 pF, WHICH INCLUDES PROBE AND STRAY WIRING CAPACITANCE

Fig. 12. Test Circuit for Common Mode Transient Immunity and Typical Waveforms

### Reflow Profile



Profile Feature	Pb-Free Assembly Profile
Temperature Min. (Tsmín)	150°C
Temperature Max. (Tsmáx)	200°C
Time (ts) from (Tsmín to Tsmáx)	60–120 seconds
Ramp-up Rate (tL to tp)	3°C/second max.
Liquidous Temperature (TL)	217°C
Time (tL) Maintained Above (TL)	60–150 seconds
Peak Body Package Temperature	260°C +0°C / -5°C
Time (tp) within 5°C of 260°C	30 seconds
Ramp-down Rate (TP to TL)	6°C/second max.
Time 25°C to Peak Temperature	8 minutes max.

Figure 13. Reflow Profile

## Ordering Information

Part Number	Package	Packing Method
HCPL3700M	DIP 8-Pin	Tube (50 units)
HCPL3700SM	SMT 8-Pin (Lead Bend)	Tube (50 units)
HCPL3700SDM	SMT 8-Pin (Lead Bend)	Tape and Reel (1,000 units)
HCPL3700VM	DIP 8-Pin, DIN EN/IEC60747-5-5 option	Tube (50 units)
HCPL3700SVM	SMT 8-Pin (Lead Bend), DIN EN/IEC 60747-5-5 option	Tube (50 units)
HCPL3700SDVM	SMT 8-Pin (Lead Bend), DIN EN/IEC 60747-5-5 option	Tape and Reel (1,000 units)
HCPL3700TVM	DIP 8-Pin, 0.4" Lead Spacing, DIN EN/IEC 60747-5-5 option	Tube (50 units)

## Marking Information

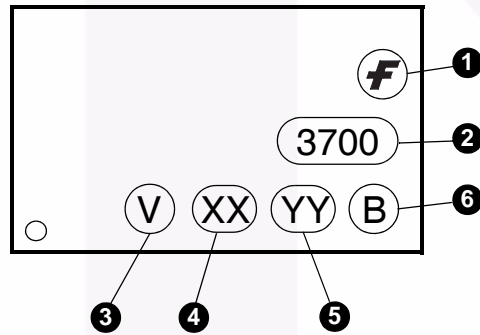


Figure 14. Top Mark

### Definitions

1	Fairchild Logo
2	Device Number
3	DIN EN/IEC60747-5-5 Option (only appears on component ordered with this option)
4	Two Digit Year Code, e.g., '15'
5	Two Digit Work Week Ranging from '01' to '53'
6	Assembly Package Code



- NOTES:  
 A) NO STANDARD APPLIES TO THIS PACKAGE  
 B) ALL DIMENSIONS ARE IN MILLIMETERS.  
 C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSION  
 D) DRAWING FILENAME AND REVISION: MKT-N08GREV7



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