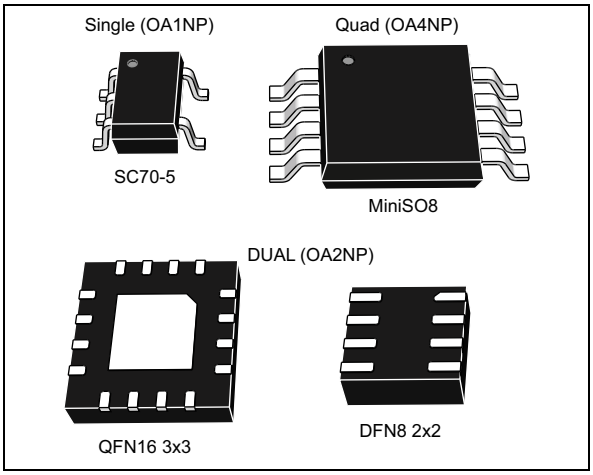
# OA1NP, OA2NP, OA4NP

## Low power, rail-to-rail input and output, CMOS op amp

**Datasheet - production data**




## Features

- Low power: 580 nA typ. per channel at 25 °C at $V_{CC}$ = 1.8 V
- Low supply voltage: 1.5 V - 5.5 V
- Unity gain stable
- Rail-to-rail input and output
- Gain bandwidth product: 8 kHz typ.
- Low input bias current: 5 pA max at 25 °C
- High tolerance to ESD: 2 kV HBM
- Industrial temperature range: -40 °C to +85 °C

### Benefits

- 42 years of typical equivalent lifetime (OA1NP) if supplied by a 220 mAh coin type Lithium battery
- Tolerance to power supply transient drops
- Accurate signal conditioning of high impedance sensors
- Fast desaturation

## Applications

- Wearable
- Fitness and healthcare
- Medical instrumentation

## Description

The OA1NP, OA2NP, OA4NP series of CMOS operational amplifiers offer a low power consumption of 580 nA typical and 750 nA maximum per channel when supplied by 1.8 V. Combined with a supply voltage range of 1.5 V to 5.5 V, these features allow the OA1NP, OA2NP, OA4NP op amp series to be efficiently supplied by a coin type Lithium battery or a regulated voltage in low power applications.

The OA1NP, OA2NP, OA4NP are respectively the single, dual and quad operational amplifier versions.

The 8 kHz gain bandwidth of these devices make them ideal for wearable, fitness and healthcare and sensors signal conditioning applications.

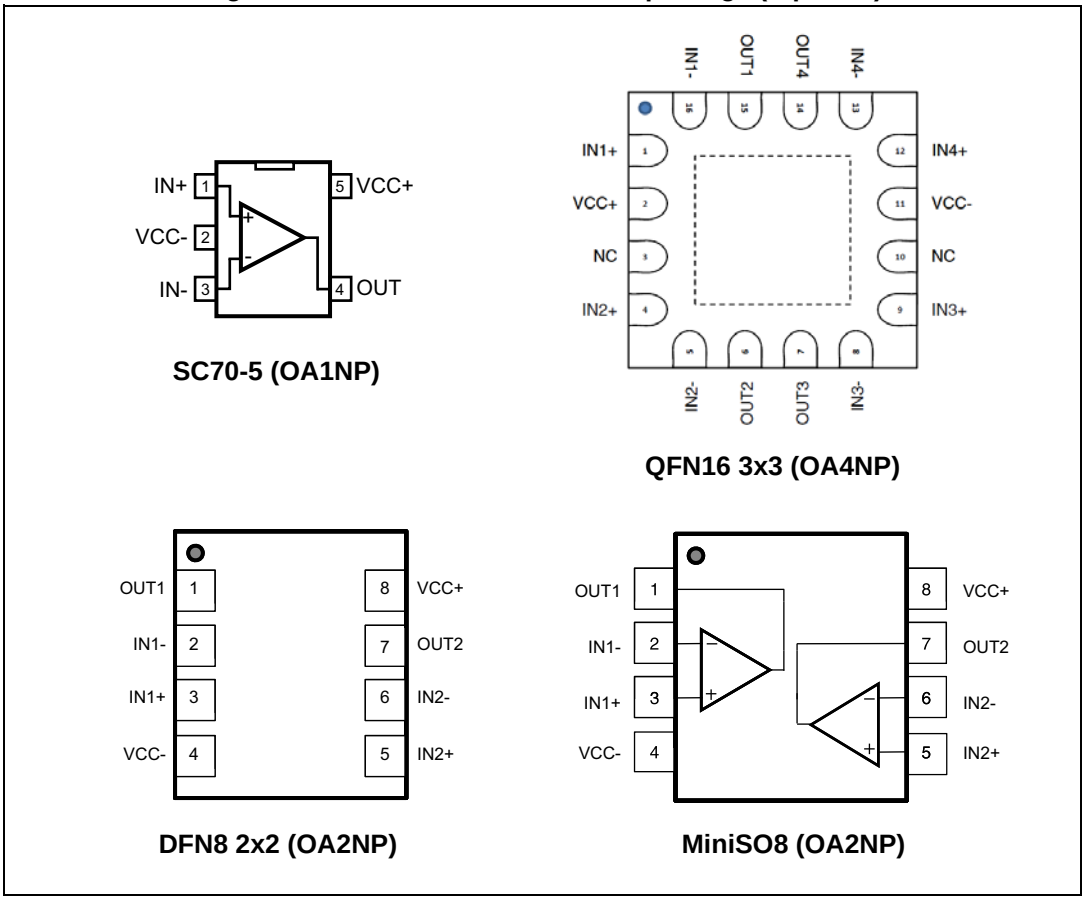
**Table 1. Device summary**

| Order codes | Temperature range | Packages | Packing | Marking |
|---|---|---|---|---|
| OA1NP22C | -40 ° C to +85 ° C | SC70-5 | Tape and reel | K22 |
| OA2NP22Q | | DFN8 2x2 | | K24 |
| OA2NP34S | | MiniSO8 | | K160 |
| OA4NP33Q | | QFN16 3x3 | | K160 |

# Contents

# 1 Package pin connections

**Figure 1. Pin connections for each package (top view)**



# 2 Absolute maximum ratings and operating conditions

**Table 2. Absolute maximum ratings (AMR)**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{cc}$ | Supply voltage(1) | 6 | V |
| $V_{id}$ | Differential input voltage(2) | $\pm V_{cc}$ | |
| $V_{in}$ | Input voltage(3) | $V_{cc-}$ - 0.2 to $V_{cc+}$ + 0.2 | |
| $I_{in}$ | Input current(4) | 10 | mA |
| $T_{stg}$ | Storage temperature | -65 to +150 | °C |
| $R_{thja}$ | Thermal resistance junction to ambient(5)(6)<br>SC70-5<br>DFN8 2x2<br>MiniSO8<br>QFN16 3x3 | <br>205<br>117<br>190<br>45 | °C/W |
| $T_j$ | Maximum junction temperature | 150 | °C |
| ESD | HBM: human body model(7) | 2000 | V |
| | MM: machine model(8) | 200 | |
| | CDM: charged device model(9)<br>All other packages except SC70-5<br>SC70-5 | <br>1000<br>900 | |
| | Latch-up immunity(10) | 200 | mA |

1. All voltage values, except the differential voltage are with respect to the network ground terminal.
2. The differential voltage is the non-inverting input terminal with respect to the inverting input terminal.
3. ($V_{cc+}$ - $V_{in}$) must not exceed 6 V, ($V_{in}$ - $V_{cc-}$) must not exceed 6 V.
4. The input current must be limited by a resistor in series with the inputs.
5. Short-circuits can cause excessive heating and destructive dissipation.
6. $R_{th}$ are typical values.
7. Related to ESDA/JEDEC JS-001 Apr. 2010
8. Related to JEDEC JESD22-A115C Nov.2010
9. Related to JEDEC JESD22-C101-E Dec. 2009
10. Related to JEDEC JESD78C Sept. 2010

**Table 3. Operating conditions**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{cc}$ | Supply voltage | 1.5 to 5.5 | V |
| $V_{icm}$ | Common mode input voltage range | $V_{cc-}$ - 0.1 to $V_{cc+}$ + 0.1 | |
| $T_{oper}$ | Operating free air temperature range | -40 to +85 | °C |

# 3 Electrical characteristics

$V_{CC}$+ = 1.8 V with $V_{CC}$- = 0 V, $V_{icm}$ = $V_{CC}$/2, $T_{amb}$ = 25 ° C, and $R_L$ = 1 MΩ connected to $V_{CC}$/2 (unless otherwise specified)

**Table 4. Electrical characteristics**

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **DC performance** | | | | | | |
| $V_{io}$ | Input offset voltage | | -3 | 0.1 | 3 | mV |
| | | -40 °C < T< 85 °C | -3.4 | | 3.4 | |
| $\Delta V_{io}/\Delta T$ | Input offset voltage drift | -40 °C < T< 85 °C | | | 5 | µV/°C |
| $\Delta V_{io}$ | Long-term input offset voltage drift | T = 25 °C(1) | | 0.18 | | $\frac{\mu V}{\sqrt{month}}$ |
| $I_{io}$ | Input offset current (2) | | | 1 | 5 | pA |
| | | -40 °C < T< 85 °C | | | 30 | |
| $I_{ib}$ | Input bias current (2) | | | 1 | 5 | |
| | | -40 °C < T< 85 °C | | | 30 | |
| CMR | Common mode rejection ratio 20 log ($\Delta V_{icm}/\Delta V_{io}$) | $V_{icm}$ = 0 to 0.6 V, $V_{out}$ = $V_{CC}$/2 | 65 | 85 | | dB |
| | | -40 °C < T< 85 °C | 65 | | | |
| | | $V_{icm}$ = 0 to 1.8 V, $V_{out}$ = $V_{CC}$/2 | 55 | 74 | | |
| | | -40°C < T< 85 °C | 55 | | | |
| $A_{vd}$ | Large signal voltage gain | $V_{out}$ = 0.3 V to ($V_{CC+}$ - 0.3 V) $R_L$ = 100 kΩ | 95 | 115 | | |
| | | -40 °C < T< 85 °C | 95 | | | |
| $V_{OH}$ | High level output voltage (drop from $V_{CC}$+) | $R_L$ = 100 kΩ | | | 40 | mV |
| | | -40 °C < T< 85 °C | | | 40 | |
| $V_{OL}$ | Low level output voltage | $R_L$ = 100 kΩ | | | 40 | |
| | | -40 °C < T< 85 °C | | | 40 | |
| $I_{out}$ | Output sink current | $V_{out}$ = $V_{CC}$, $V_{ID}$ = -200 mV | 4 | 5 | | mA |
| | | -40 °C < T< 85 °C | 4 | | | |
| | Output source current | $V_{out}$ = 0 V, $V_{ID}$ = + 200 mV | 4 | 5 | | |
| | | -40 °C < T< 85 °C | 4 | | | |
| $I_{CC}$ | Supply current (per channel) | No load, $V_{out}$ = $V_{CC}$/2 | | 580 | 750 | nA |
| | | -40 °C < T< 85 °C | | | 800 | |
| **AC performance** | | | | | | |
| GBP | Gain bandwidth product | $R_L$ = 1 MΩ, $C_L$ = 60 pF | | 8 | | kHz |
| $F_u$ | Unity gain frequency | | | 8 | | |
| $\Phi_m$ | Phase margin | | | 60 | | degrees |
| $G_m$ | Gain margin | | | 10 | | dB |

**Table 4. Electrical characteristics (continued)**

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| SR | Slew rate (10 % to 90 %) | $R_L$ = 1 MΩ, $C_L$ = 60 pF<br>$V_{out}$ = 0.3 V to ($V_{CC+}$ - 0.3 V) | | 3 | | V/ms |
| $e_n$ | Equivalent input noise voltage | f = 100 Hz | | 265 | | $\frac{nV}{\sqrt{Hz}}$ |
| | | f = 1 kHz | | 265 | | |
| $\int e_n$ | Low-frequency peak-to-peak input noise | Bandwidth: f = 0.1 to 10 Hz | | 9 | | $\mu V_{pp}$ |
| $i_n$ | Equivalent input noise current | f = 100 Hz | | 0.64 | | $\frac{fA}{\sqrt{Hz}}$ |
| | | f = 1 kHz | | 4.4 | | |
| $t_{rec}$ | Overload recovery time | 100 mV from rail in comparator<br>$R_L$ = 100 kΩ, $V_{ID}$ = ±$V_{CC}$<br>-40 °C < T< 85 °C | | 30 | | µs |

1. Typical value is based on the $V_{io}$ drift observed after 1000h at 125 °C extrapolated to 25 °C using the Arrhenius law and assuming an activation energy of 0.7 eV. The operational amplifier is aged in follower mode configuration.
2. Guaranteed by design.

$V_{CC}$+ = 3.3 V with $V_{CC}$- = 0 V, $V_{icm}$ = $V_{CC}$/2, $T_{amb}$ = 25 ° C, and $R_L$ = 1 MΩ connected to $V_{CC}$/2 (unless otherwise specified)

**Table 5. Electrical characteristics**

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **DC performance** | | | | | | |
| $V_{io}$ | Input offset voltage | | -3 | 0.1 | 3 | mV |
| | | -40 °C < T< 85 °C | -3.4 | | 3.4 | |
| $\Delta V_{io}/\Delta T$ | Input offset voltage drift | -40 °C < T< 85 °C | | | 5 | µV/°C |
| $\Delta V_{io}$ | Long-term input offset voltage drift | T = 25 °C(1) | | 0.36 | | $\frac{\mu V}{\sqrt{month}}$ |
| $I_{io}$ | Input offset current(2) | | | 1 | 5 | pA |
| | | -40 °C < T< 85 °C | | | 30 | |
| $I_{ib}$ | Input bias current(2) | | | 1 | 5 | |
| | | -40 °C < T< 85 °C | | | 30 | |
| CMR | Common mode rejection ratio 20 log ($\Delta V_{icm}/\Delta V_{io}$) | $V_{icm}$ = 0 to 2.1 V, $V_{out}$ = $V_{CC}$/2 | 70 | 92 | | dB |
| | | -40 °C < T< 85 °C | 70 | | | |
| | | $V_{icm}$ = 0 to 3.3 V, $V_{out}$ = $V_{CC}$/2 | 60 | 77 | | |
| | | -40 °C < T< 85 °C | 60 | | | |
| $A_{vd}$ | Large signal voltage gain | $V_{out}$ = 0.3 V to ($V_{CC+}$ - 0.3 V) $R_L$= 100 kΩ | 105 | 120 | | |
| | | -40 °C < T< 85 °C | 105 | | | |
| $V_{OH}$ | High level output voltage (drop from $V_{CC}$+) | $R_L$ = 100 kΩ | | | 40 | mV |
| | | -40 °C < T< 85 °C | | | 40 | |
| $V_{OL}$ | Low level output voltage | $R_L$ = 100 kΩ | | | 40 | |
| | | -40 °C < T< 85 °C | | | 40 | |
| $I_{out}$ | Output sink current | $V_{out}$ = $V_{CC}$, $V_{ID}$= -200 mV | 6 | 9 | | mA |
| | | -40 °C < T< 85 °C | 6 | | | |
| | Output source current | $V_{out}$ = 0 V, $V_{ID}$ = + 200 mV | 8 | 11 | | |
| | | -40 °C < T< 85 °C | 8 | | | |
| $I_{CC}$ | Supply current (per channel) | No load, $V_{out}$ = $V_{CC}$/2 | | 600 | 800 | nA |
| | | -40 °C < T< 85 °C | | | 850 | |
| **AC performance** | | | | | | |
| GBP | Gain bandwidth product | $R_L$ = 1 MΩ, $C_L$ = 60 pF | | 8 | | kHz |
| $F_u$ | Unity gain frequency | | | 8 | | |
| $\Phi_m$ | Phase margin | | | 60 | | degrees |
| $G_m$ | Gain margin | | | 11 | | dB |

**Table 5. Electrical characteristics (continued)**

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| SR | Slew rate (10 % to 90 %) | $R_L$ = 1 MΩ, $C_L$ = 60 pF, $V_{out}$ = 0.3 V to ($V_{CC+}$ - 0.3 V) | | 3 | | V/ms |
| $e_n$ | Equivalent input noise voltage | f = 100 Hz | | 260 | | $\frac{nV}{\sqrt{Hz}}$ |
| | | f = 1 kHz | | 255 | | |
| $\int e_n$ | Low-frequency peak-to-peak input noise | Bandwidth: f = 0.1 to 10 Hz | | 8.6 | | $\mu V_{pp}$ |
| $i_n$ | Equivalent input noise current | f = 100 Hz | | 0.55 | | $\frac{fA}{\sqrt{Hz}}$ |
| | | f = 1 kHz | | 3.8 | | |
| $t_{rec}$ | Overload recovery time | 100 mV from rail in comparator $R_L$ = 100 kΩ, $V_{ID}$= ±$V_{CC}$ -40 °C < T< 85 °C | | 30 | | µs |

1. Typical value is based on the $V_{io}$ drift observed after 1000h at 125 °C extrapolated to 25 °C using the Arrhenius law and assuming an activation energy of 0.7 eV. The operational amplifier is aged in follower mode configuration.
2. Guaranteed by design.

$V_{CC}$+ = 5 V with $V_{CC}$- = 0 V, $V_{icm}$ = $V_{CC}$/2, $T_{amb}$ = 25 ° C, and $R_L$ = 1 MΩ connected to $V_{CC}$/2 (unless otherwise specified)

**Table 6. Electrical characteristics**

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **DC performance** | | | | | | |
| $V_{io}$ | Input offset voltage | | -3 | 0.1 | 3 | mV |
| | | -40 °C < T< 85 °C | -3.4 | | 3.4 | |
| $\Delta V_{io}/\Delta T$ | Input offset voltage drift | -40 °C < T< 85 °C | | | 5 | µV/°C |
| $\Delta V_{io}$ | Long-term input offset voltage drift | T = 25 °C(1) | | 1.1 | | $\frac{\mu V}{\sqrt{month}}$ |
| $I_{io}$ | Input offset current(2) | | | 1 | 5 | pA |
| | | -40 °C < T< 85 °C | | | 30 | |
| $I_{ib}$ | Input bias current (2) | | | 1 | 5 | |
| | | -40 °C < T< 85 °C | | | 30 | |
| CMR | Common mode rejection ratio 20 log ($\Delta V_{icm}/\Delta V_{io}$) | $V_{icm}$ = 0 to 3.8 V, $V_{out}$ = $V_{CC}$/2 | 70 | 90 | | dB |
| | | -40 °C < T< 85 °C | 70 | | | |
| | | $V_{icm}$ = 0 to 5 V, $V_{out}$ = $V_{CC}$/2 | 65 | 82 | | |
| | | -40 °C < T< 85 °C | 65 | | | |
| SVR | Supply voltage rejection ratio | $V_{CC}$ = 1.5 to 5.5 V, $V_{icm}$ = 0 V | 70 | 90 | | |
| | | -40 °C < T< 85 °C | 70 | | | |
| $A_{vd}$ | Large signal voltage gain | $V_{out}$ = 0.3 V to ($V_{cc+}$ - 0.3 V) $R_L$= 100 kΩ | 110 | 130 | | |
| | | -40°C < T< 85 °C | 110 | | | |
| $V_{OH}$ | High level output voltage (drop from $V_{CC}$+) | $R_L$ = 100 kΩ | | | 40 | mV |
| | | -40 °C < T< 85 °C | | | 40 | |
| $V_{OL}$ | Low level output voltage | $R_L$ = 100 kΩ | | | 40 | |
| | | -40 °C < T< 85 °C | | | 40 | |
| $I_{out}$ | Output sink current | $V_{out}$ = $V_{CC}$, $V_{ID}$ = -200 mV | 6 | 9 | | mA |
| | | -40 °C < T< 85 °C | 6 | | | |
| | Output source current | $V_{out}$ = 0 V, $V_{ID}$ = + 200 mV | 8 | 11 | | |
| | | -40 °C < T< 85 °C | 8 | | | |
| $I_{CC}$ | Supply current (per channel) | No load, $V_{out}$ = $V_{CC}$/2 | | 650 | 850 | nA |
| | | -40 °C < T< 85 °C | | | 950 | |

**Table 6. Electrical characteristics (continued)**

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **AC performance** | | | | | | |
| GBP | Gain bandwidth product | $R_L$ = 1 MΩ, $C_L$ = 60 pF | | 9 | | kHz |
| $F_u$ | Unity gain frequency | | | 8.6 | | |
| $\Phi_m$ | Phase margin | | | 60 | | degrees |
| $G_m$ | Gain margin | | | 12 | | dB |
| SR | Slew rate (10 % to 90 %) | $R_L$ = 1 MΩ, $C_L$ = 60 pF, $V_{out}$ = 0.3 V to ($V_{CC+}$ - 0.3 V) | | 3 | | V/ms |
| $e_n$ | Equivalent input noise voltage | f = 100 Hz | | 240 | | $\frac{nV}{\sqrt{Hz}}$ |
| | | f = 1 kHz | | 225 | | |
| $\int e_n$ | Low-frequency peak-to-peak input noise | Bandwidth: f = 0.1 to 10 Hz | | 8.1 | | $\mu V_{pp}$ |
| $i_n$ | Equivalent input noise current | f = 100 Hz | | 0.18 | | $\frac{fA}{\sqrt{Hz}}$ |
| | | f = 1 kHz | | 3.5 | | |
| $t_{rec}$ | Overload recovery time | 100 mV from rail in comparator $R_L$ = 100 kΩ, $V_{ID}$= ±$V_{CC}$ -40 °C < T< 85 °C | | 30 | | µs |
| EMIRR | Electromagnetic interference rejection ratio(3) | $V_{in}$ = -10 dBm, f = 400 MHz | | 73 | | dB |
| | | $V_{in}$ = -10 dBm, f = 900 MHz | | 88 | | |
| | | $V_{in}$ = -10 dBm, f = 1.8 GHz | | 80 | | |
| | | $V_{in}$ = -10 dBm, f = 2.4 GHz | | 80 | | |

1. Typical value is based on the $V_{io}$ drift observed after 1000h at 125 °C extrapolated to 25 °C using the Arrhenius law and assuming an activation energy of 0.7 eV. The operational amplifier is aged in follower mode configuration.
2. Guaranteed by design.
3. Based on evaluations performed only in conductive mode.

**Figure 2. Supply current vs. supply voltage**

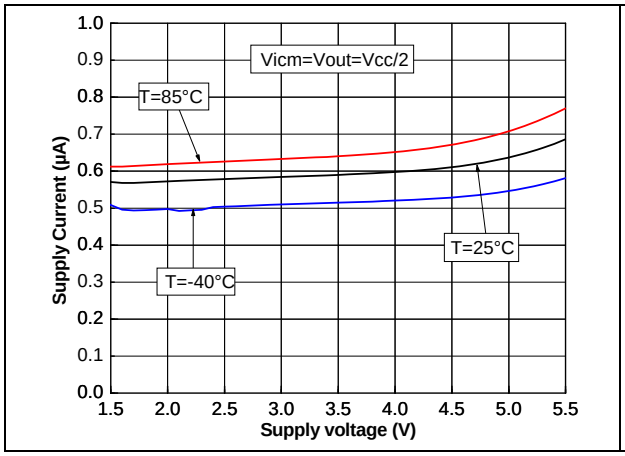



**Figure 3. Supply current vs. input common mode voltage**

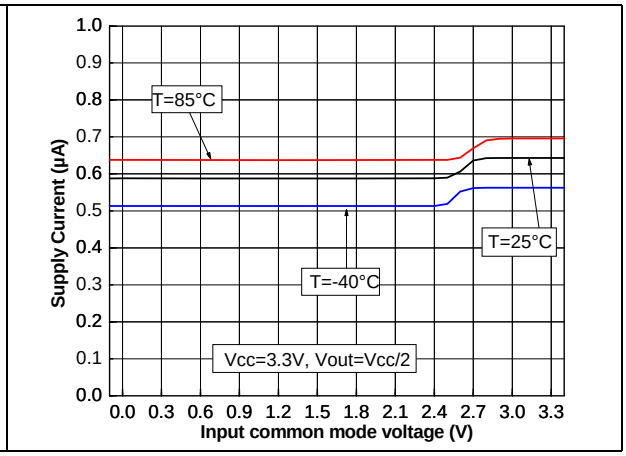



**Figure 4. Supply current in saturation mode**

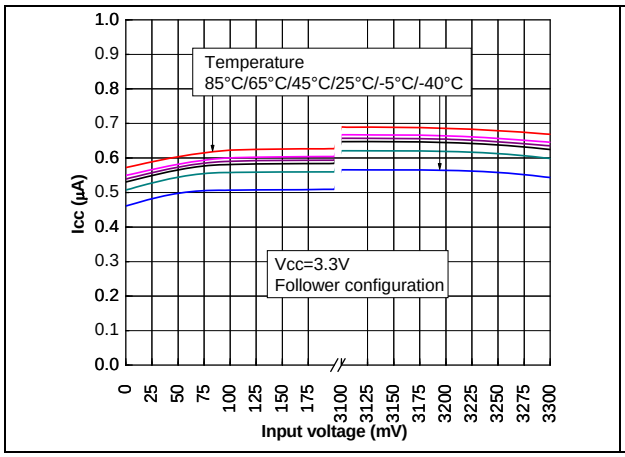



**Figure 5. Input offset voltage distribution**

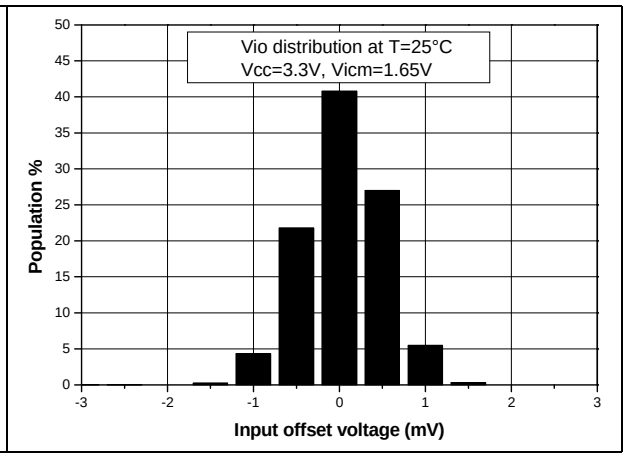



**Figure 6. Input offset voltage vs. common mode voltage**

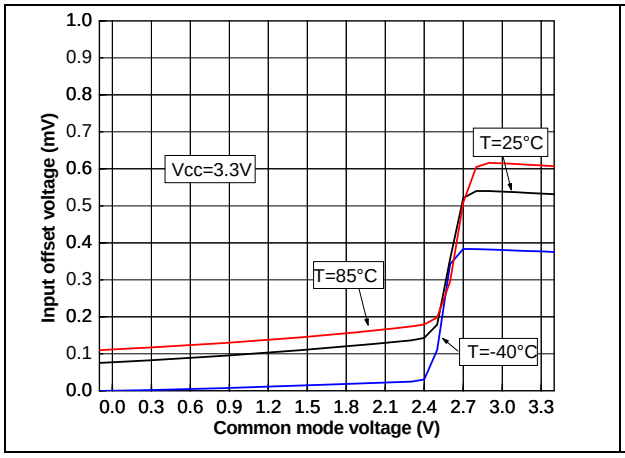



**Figure 7. Input offset voltage vs. temperature at 3.3 V supply voltage**

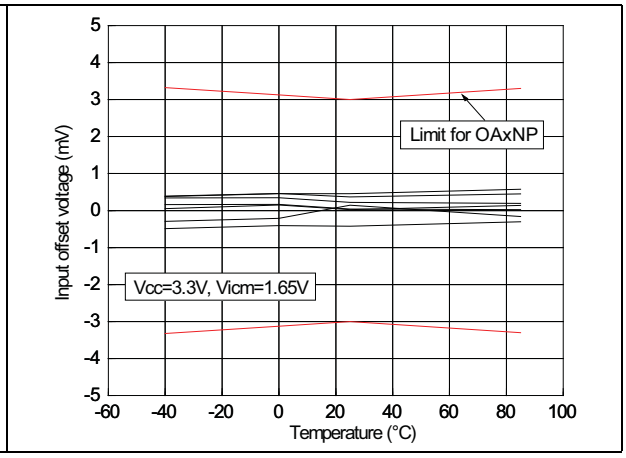


**Figure 8. Input offset voltage temperature coefficient distribution**

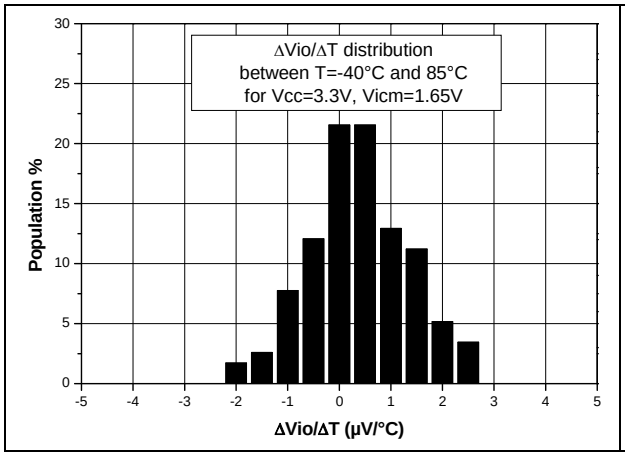



**Figure 9. Input bias current vs. temperature at mid $V_{ICM}$**

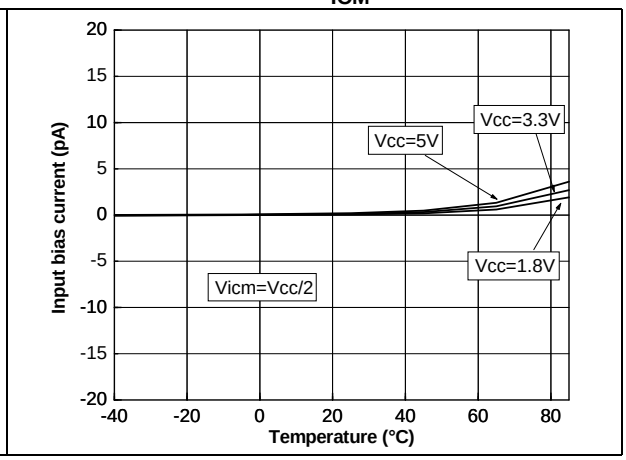



**Figure 10. Input bias current vs. temperature at low $V_{ICM}$**

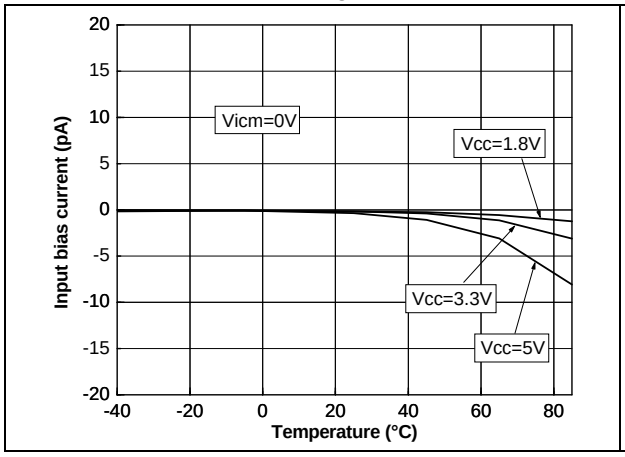



**Figure 11. Input bias current vs. temperature at high $V_{ICM}$**

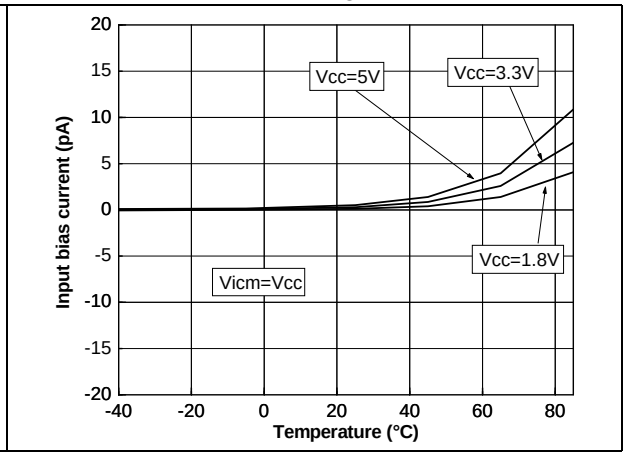



**Figure 12. Output characteristics at 1.8 V supply voltage**

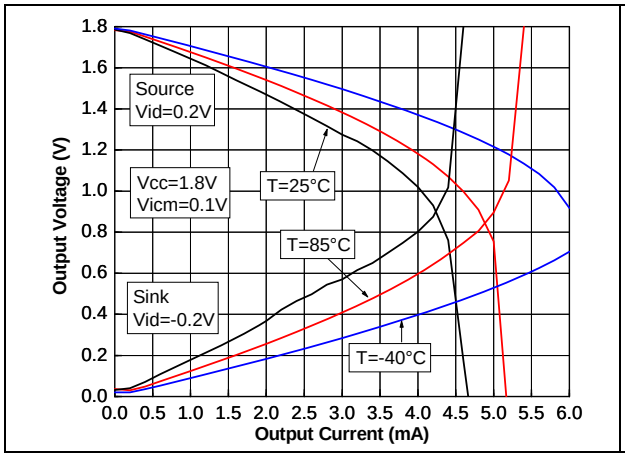



**Figure 13. Output characteristics at 3.3 V supply voltage**

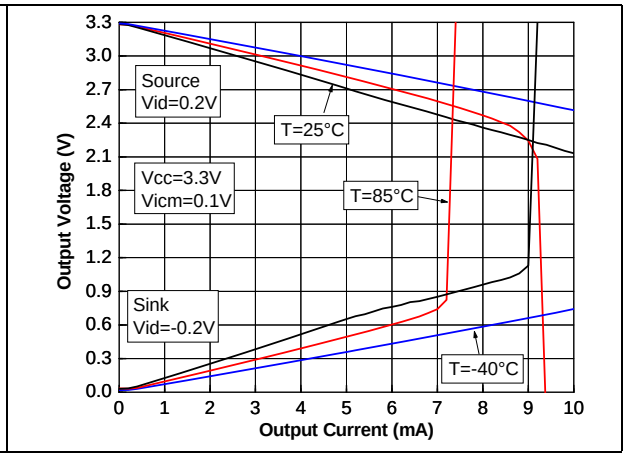


**Figure 14. Output characteristics at 5 V supply voltage**

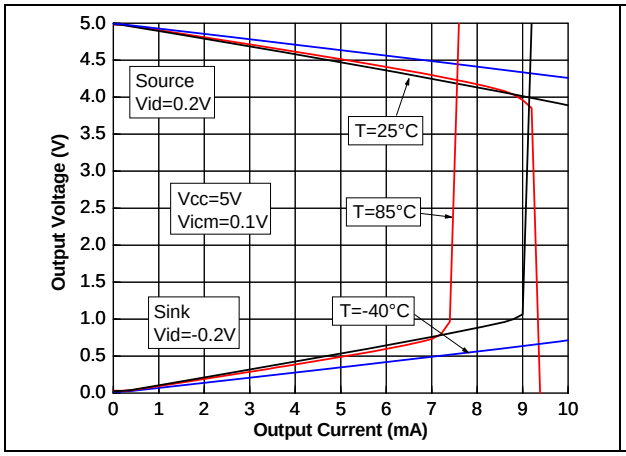



**Figure 15. Output voltage vs. input voltage close to the rails**

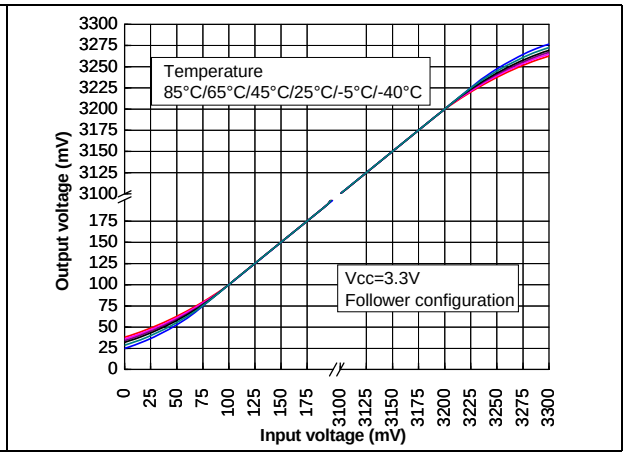



**Figure 16. Output saturation with a sine wave on input**

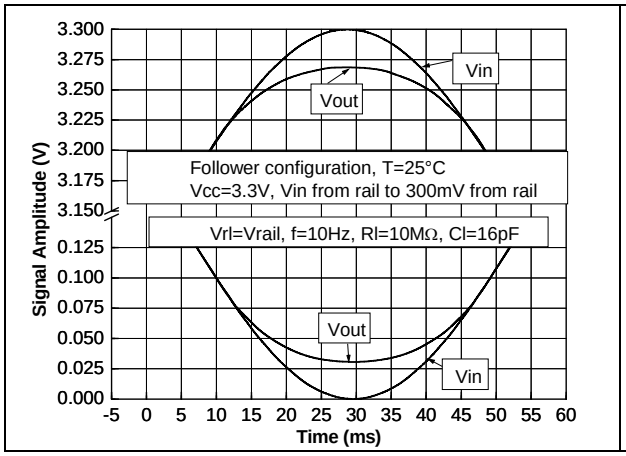



**Figure 17. Desaturation time**

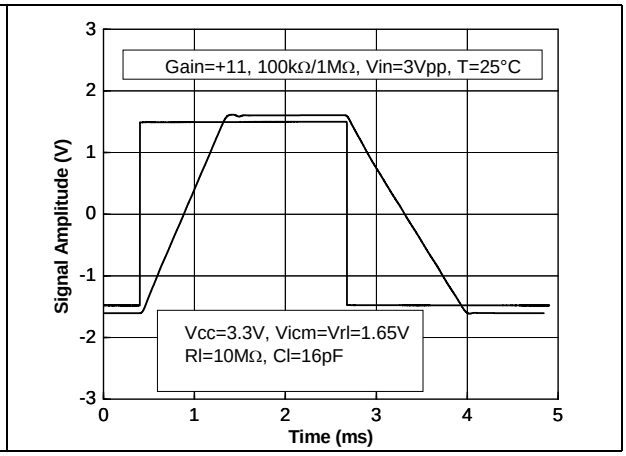



**Figure 18. Phase reversal free**

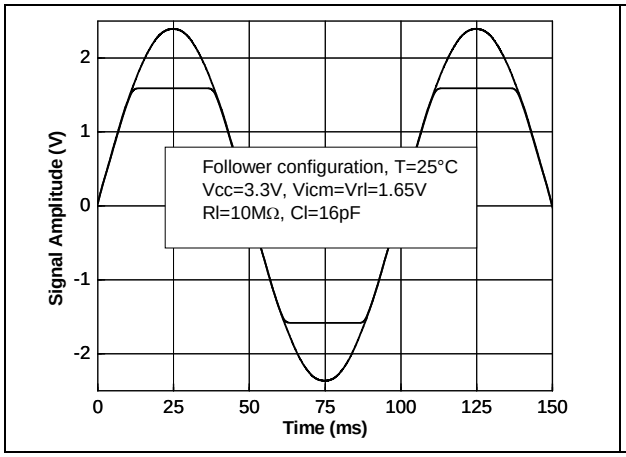



**Figure 19. Slew rate vs. supply voltage**

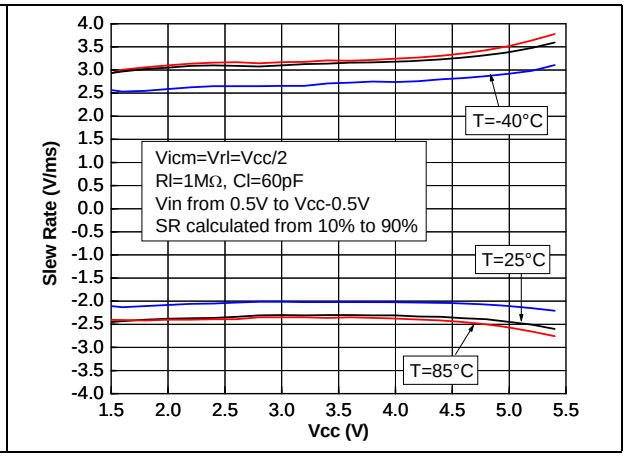


**Figure 20. Output swing vs. input signal frequency**

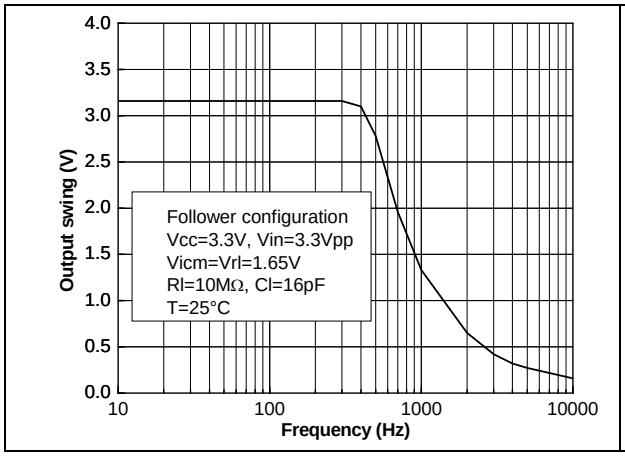



**Figure 21. Triangulation of a sine wave**

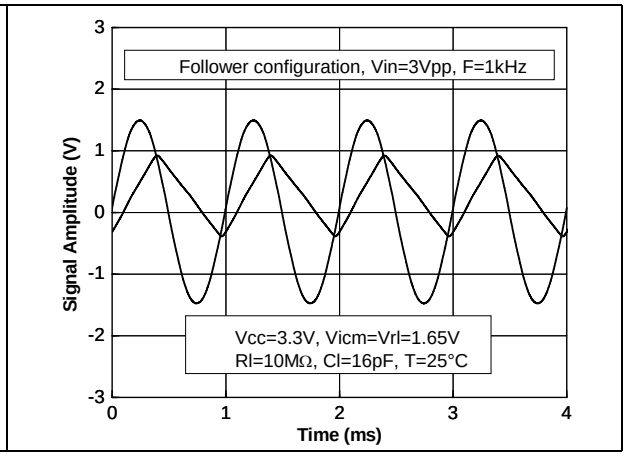



**Figure 22. Large signal response at 3.3 V supply voltage**

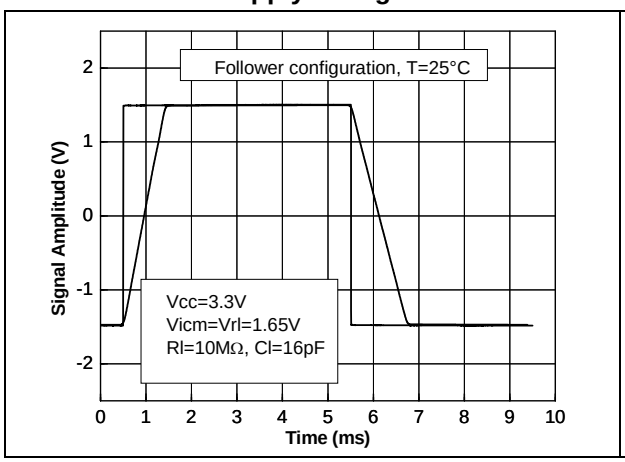



**Figure 23. Small signal response at 3.3 V supply voltage**

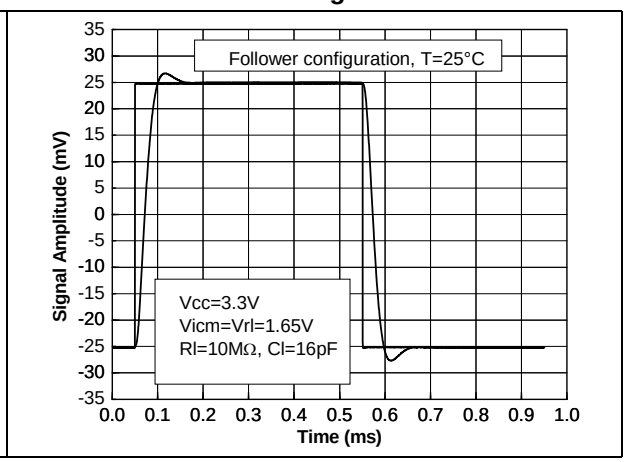



**Figure 24. Overshoot vs. capacitive load at 3.3 V supply voltage**

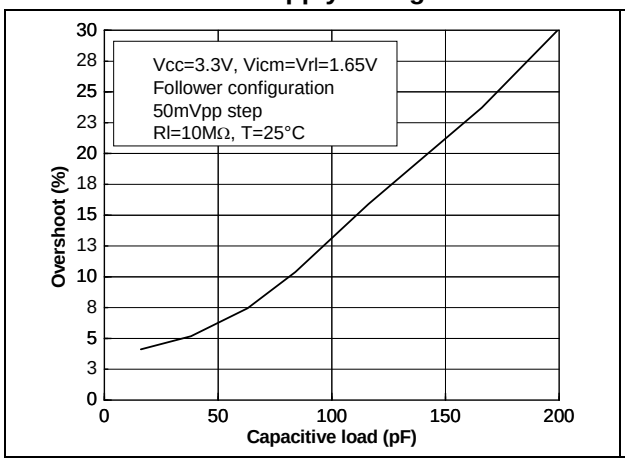



**Figure 25. Phase margin vs. capacitive load at 3.3 V supply voltage**

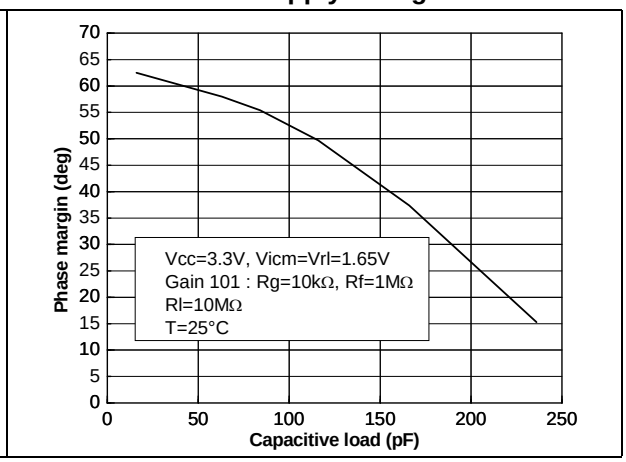


**Figure 26. Bode diagram for different feedback values**

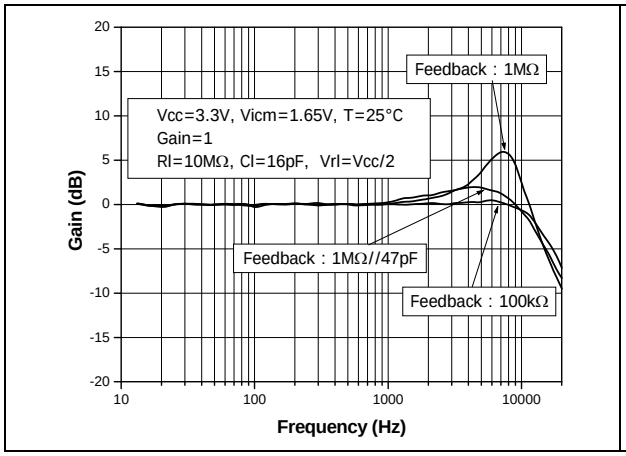



**Figure 27. Bode diagram at 1.8 V supply voltage**

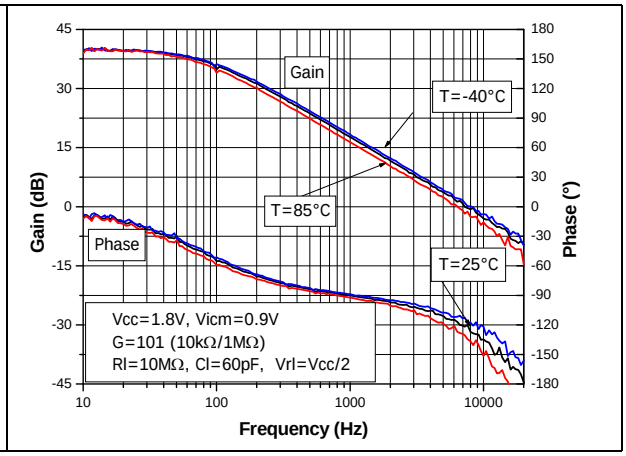



**Figure 28. Bode diagram at 3.3 V supply voltage**

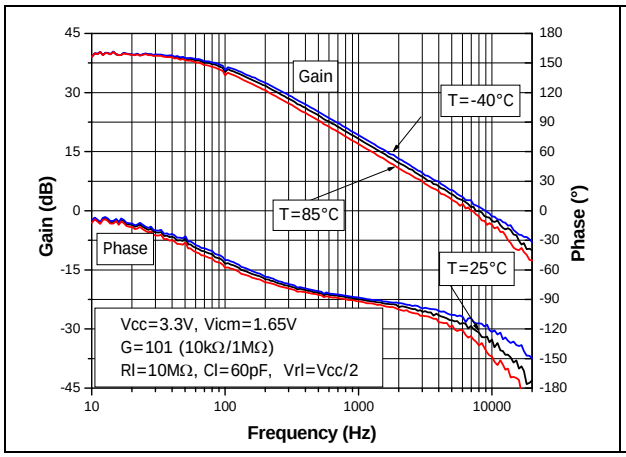



**Figure 29. Bode diagram at 5 V supply voltage**

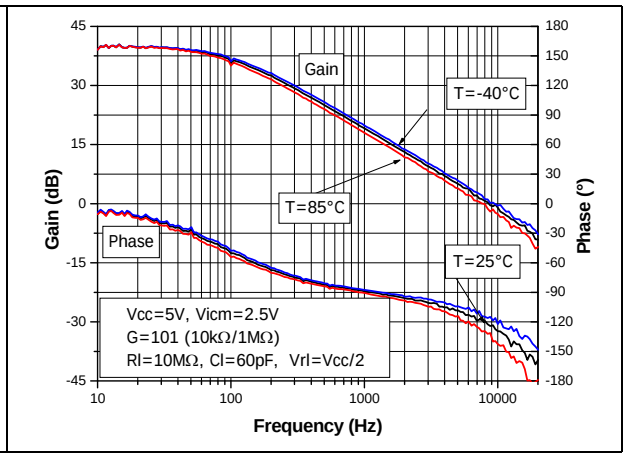



**Figure 30. Gain bandwidth product vs. input common mode voltage**

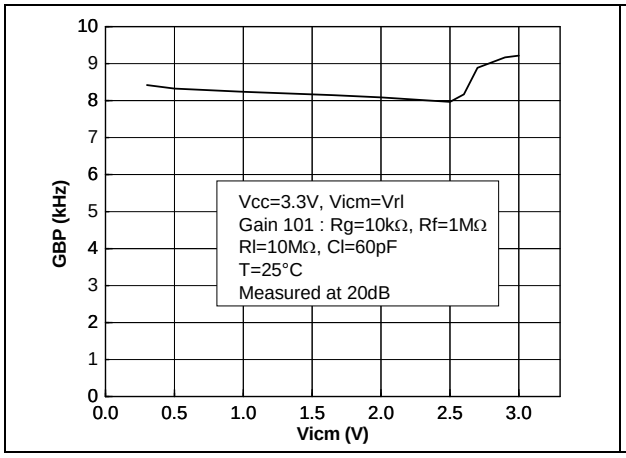



**Figure 31. Gain vs. input common mode voltage**

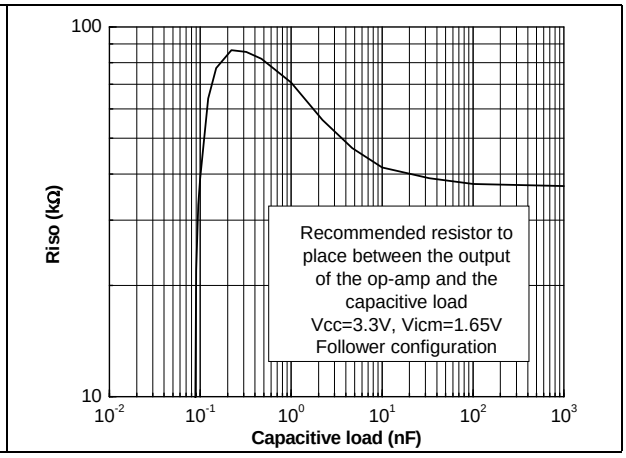


**Figure 32. Noise at 1.8 V supply voltage in follower configuration**

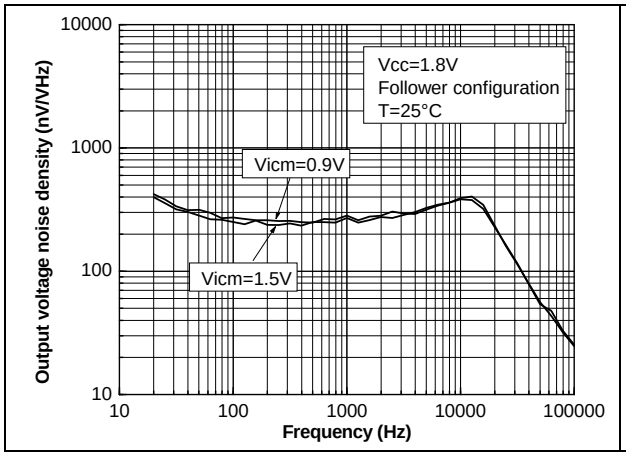



**Figure 33. Noise at 3.3 V supply voltage in follower configuration**

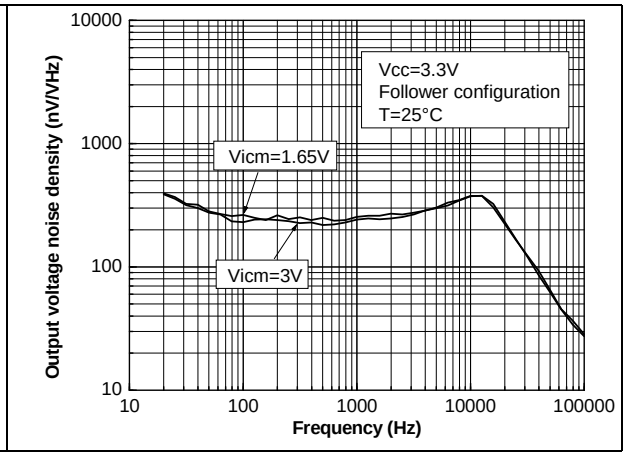



**Figure 34. Noise at 5 V supply voltage in follower configuration**

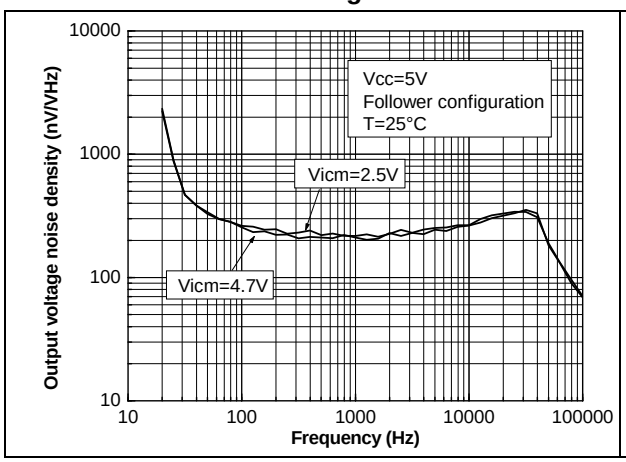



**Figure 35. Noise amplitude on 0.1 to 10 Hz frequency range**

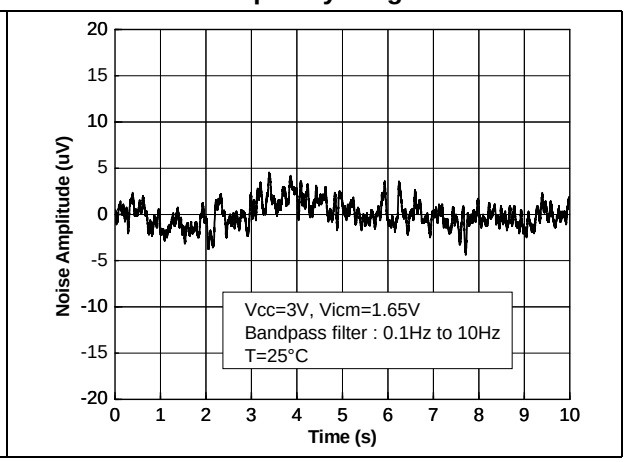



**Figure 36. Channel separation on OA2NP**

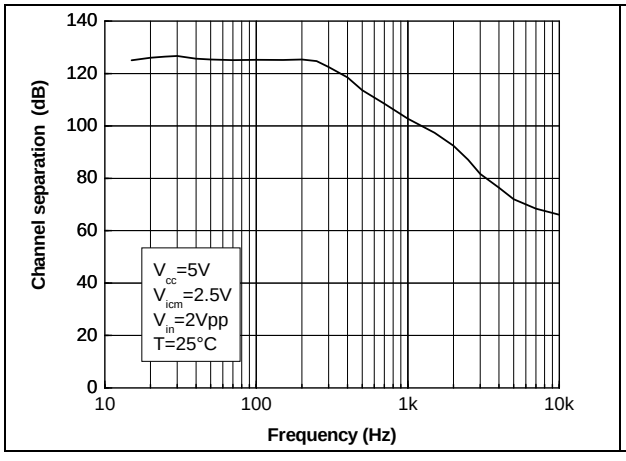
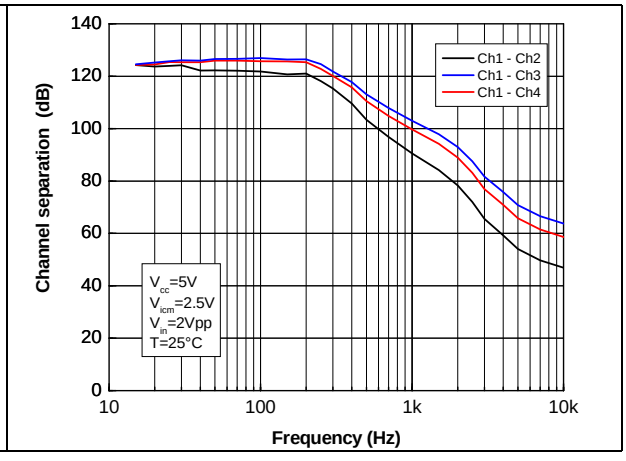



**Figure 37. Channel separation on OA4NP**



# 4 Application information

## 4.1 Operating voltages

The OA1NP, OA2NP and OA4NP series of low power op amp can operate from 1.5 V to 5.5 V. Their parameters are fully specified at 1.8 V, 3.3 V, and 5 V supply voltages and are very stable in the full $V_{CC}$ range. Additionally, main specifications are guaranteed on the industrial temperature range from -40 to +85 ° C.

## 4.2 Rail-to-rail input

The OA1NP, OA2NP and OA4NP series is built with two complementary PMOS and NMOS input differential pairs. Thus, these devices have a rail-to-rail input, and the input common mode range is extended from $V_{CC-}$ - 0.1 V to $V_{CC+}$ + 0.1 V.

The devices have been designed to prevent phase reversal behavior.

## 4.3 Input offset voltage drift over temperature

The maximum input voltage drift over the temperature variation is defined as the offset variation related to the offset value measured at 25 °C. The operational amplifier is one of the main circuits of the signal conditioning chain, and the amplifier input offset is a major contributor to the chain accuracy. The signal chain accuracy at 25 °C can be compensated during production at application level. The maximum input voltage drift over temperature enables the system designer to anticipate the effects of temperature variations.

The maximum input voltage drift over temperature is computed in *Equation 1*.

**Equation 1**

$$\frac{\Delta V_{io}}{\Delta T} = \max\left|\frac{V_{io}(T) - V_{io}(25°C)}{T - 25°C}\right|$$

with T = -40 °C and 85 °C.

The datasheet maximum value is guaranteed by measurements on a representative sample size ensuring a $C_{pk}$ (process capability index) greater than 2.

## 4.4 Long term input offset voltage drift

To evaluate product reliability, two types of stress acceleration are used:

- Voltage acceleration, by changing the applied voltage
- Temperature acceleration, by changing the die temperature (below the maximum junction temperature allowed by the technology) with the ambient temperature.

The voltage acceleration has been defined based on JEDEC results, and is defined using *Equation 2*.

**Equation 2**

$$A_{FV} = e^{\beta \cdot (V_S - V_U)}$$

Where:

$A_{FV}$ is the voltage acceleration factor

$\beta$ is the voltage acceleration constant in 1/V, constant technology parameter ($\beta = 1$)

$V_S$ is the stress voltage used for the accelerated test

$V_U$ is the voltage used for the application

The temperature acceleration is driven by the Arrhenius model, and is defined in *Equation 3*.

**Equation 3**

$$A_{FT} = e^{\frac{E_a}{k} \cdot \left(\frac{1}{T_U} - \frac{1}{T_S}\right)}$$

Where:

$A_{FT}$ is the temperature acceleration factor

$E_a$ is the activation energy of the technology based on the failure rate

k is the Boltzmann constant ($8.6173 \times 10^{-5}$ $eVk^{-1}$)

$T_U$ is the temperature of the die when $V_U$ is used (°K)

$T_S$ is the temperature of the die under temperature stress (°K)

The final acceleration factor, $A_F$, is the multiplication of the voltage acceleration factor and the temperature acceleration factor (*Equation 4*).

**Equation 4**

$$A_F = A_{FT} \times A_{FV}$$

$A_F$ is calculated using the temperature and voltage defined in the mission profile of the product. The $A_F$ value can then be used in *Equation 5* to calculate the number of months of use equivalent to 1000 hours of reliable stress duration.

**Equation 5**

$$Months = A_F \times 1000\ h \times 12\ months / (24\ h \times 365.25\ days)$$

To evaluate the op amp reliability, a follower stress condition is used where $V_{CC}$ is defined as a function of the maximum operating voltage and the absolute maximum rating (as recommended by JEDEC rules).

The $V_{io}$ drift (in µV) of the product after 1000 h of stress is tracked with parameters at different measurement conditions (see *Equation 6*).

**Equation 6**

$$V_{CC} = \max V_{op} \text{ with } V_{icm} = V_{CC}/2$$

The long term drift parameter ($\Delta V_{io}$), estimating the reliability performance of the product, is obtained using the ratio of the $V_{io}$ (input offset voltage value) drift over the square root of the calculated number of months (*Equation 7*).

**Equation 7**

$$\Delta V_{io} = \frac{V_{io}drift}{\sqrt{(months)}}$$

where $V_{io}$ drift is the measured drift value in the specified test conditions after 1000 h stress duration.

## 4.5 Schematic optimization aiming for low power

To benefit from the full performance of the The OA1NP, OA2NP and OA4NP series, the impedances must be maximized so that current consumption is not lost where it is not required.

For example, an aluminum electrolytic capacitance can have significantly high leakage. This leakage may be greater than the current consumption of the op amp. For this reason, ceramic type capacitors are preferred.

For the same reason, big resistor values should be used in the feedback loop. However, there are three main limitations to be considered when choosing a resistor.

1. When the The OA1NP, OA2NP and OA4NP series is used with a sensor: the resistance connected between the sensor and the input must remain much higher than the impedance of the sensor itself.
2. Noise generated: a100 kΩ resistor generates 40 $\frac{nV}{\sqrt{Hz}}$, a bigger resistor value generates even more noise.
3. Leakage on the PCB: leakage can be generated by moisture. This can be improved by using a specific coating process on the PCB.

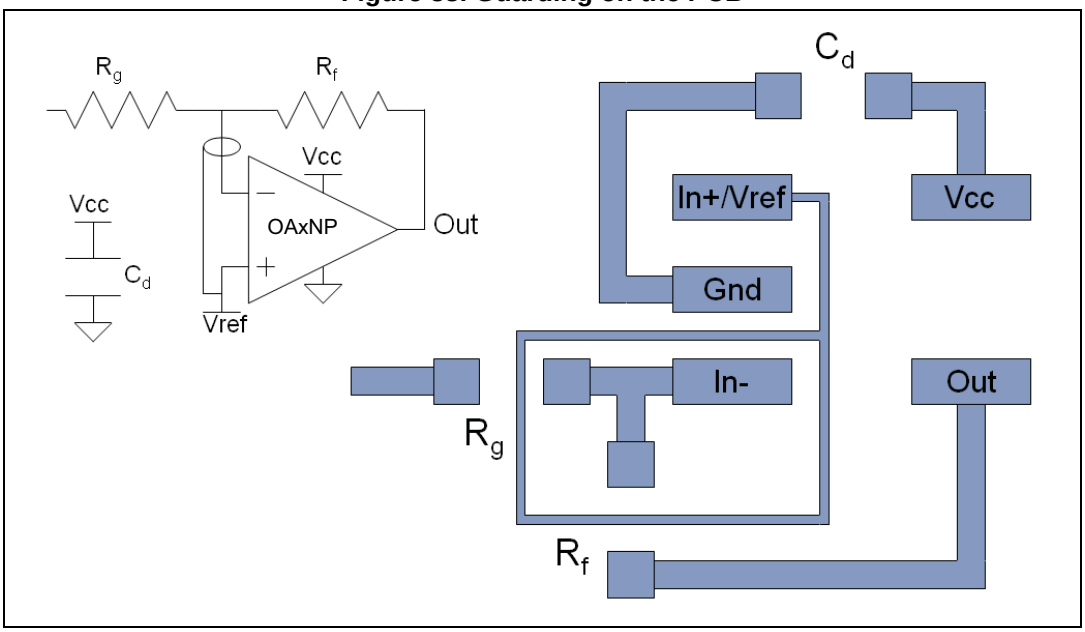
## 4.6 PCB layout considerations

For correct operation, it is advised to add 10 nF decoupling capacitors as close as possible to the power supply pins.

Minimizing the leakage from sensitive high impedance nodes on the inputs of the OA1NP, OA2NP, OA4NP series can be performed with a guarding technique. The technique consists of surrounding high impedance tracks by a low impedance track (the ring). The ring is at the same electrical potential as the high impedance node.

Therefore, even if some parasitic impedance exists between the tracks, no leakage current can flow through them as they are at the same potential (see *Figure 38*).

**Figure 38. Guarding on the PCB**



## 4.7 Using the OA1NP, OA2NP, OA4NP series with sensors

The OA1NP, OA2NP, OA4NP series has MOS inputs, thus input bias currents can be guaranteed down to 5 pA maximum at ambient temperature. This is an important parameter when the operational amplifier is used in combination with high impedance sensors.

The OA1NP, OA2NP, and OA4NP series is perfectly suited for trans-impedance configuration as shown in *Figure 39*. This configuration allows a current to be converted into a voltage value with a gain set by the user. It is an ideal choice for portable electrochemical gas sensing or photo/UV sensing applications. The OA1NP, OA2NP, OA4NP series, using trans-impedance configuration, is able to provide a voltage value based on the physical parameter sensed by the sensor.

### Electrochemical gas sensors

The output current of electrochemical gas sensors is generally in the range of tens of nA to hundreds of µA. As the input bias current of the OA1NP, OA2NP, and OA4NP is very low (see *Figure 9*, *Figure 10*, and *Figure 11*) compared to these current values, the OA1NP, OA2NP, OA4NP series is well adapted for use with the electrochemical sensors of two or three electrodes. *Figure 40* shows a potentiostat (electronic hardware required to control a three electrode cell) schematic using the OA1NP, OA2NP, and OA4NP. In such a configuration, the devices minimize leakage in the reference electrode compared to the current being measured on the working electrode.

**Figure 39. Trans-impedance amplifier schematic**

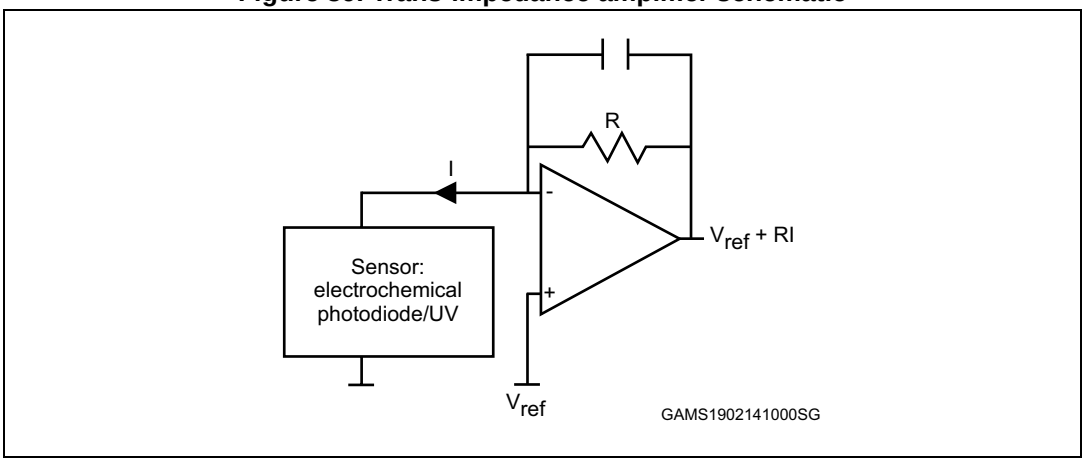
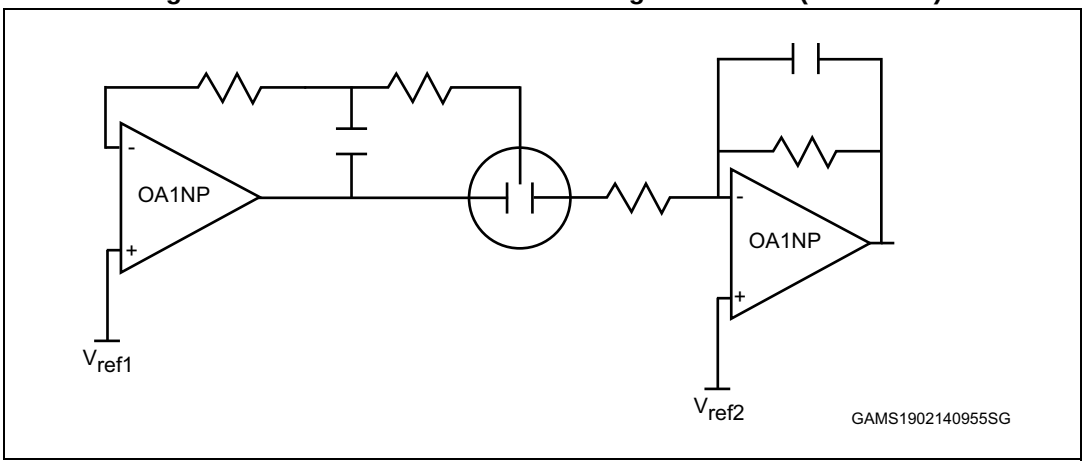


**Figure 40. Potentiostat schematic using the OA1NP (or OA2NP)**




## 4.8 Fast desaturation

When the OA1NP, OA2NP, and OA4NP, operational amplifiers go into saturation mode, they take a short period of time to recover, typically thirty microseconds. When recovering after saturation, the OA1NP, OA2NP, and OA4NP series does not exhibit any voltage peaks that could generate issues (such as false alarms) in the application (see *Figure 17*). This is because the internal gain of the amplifier decreases smoothly when the output signal gets close to the $V_{CC+}$ or $V_{CC-}$ supply rails (see *Figure 15* and *Figure 16*).

Thus, to maintain signal integrity, the user should take care that the output signal stays at 100 mV from the supply rails.

With a trans-impedance schematic, a voltage reference can be used to keep the signal away from the supply rails.

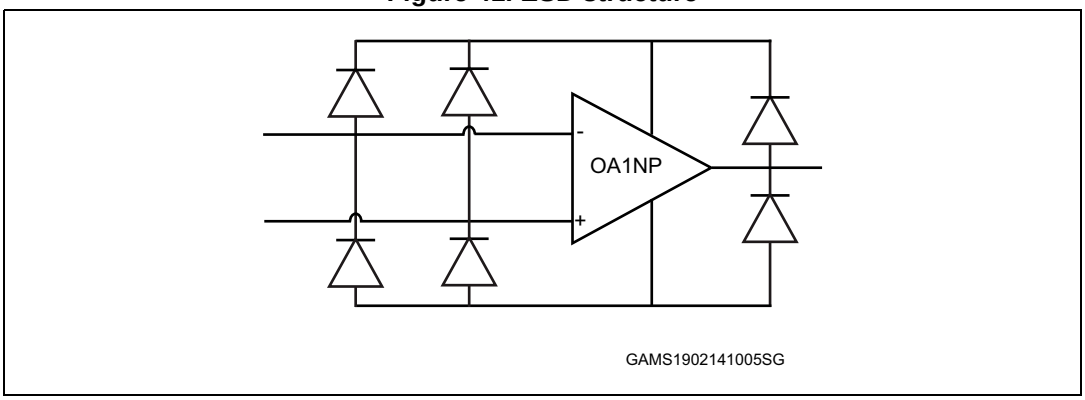
## 4.9 Using the OA1NP, OA2NP, OA4NP series in comparator mode

The OA1NP, OA2NP, and OA4NP series can be used as a comparator. In this case, the output stage of the device always operates in saturation mode. In addition, *Figure 4* shows the current consumption is not bigger and even decreases smoothly close to the rails. The OA1NP, OA2NP, and OA4NP are obviously operational amplifiers and are therefore optimized to be used in linear mode. We recommend to use the TS88 series of nanopower comparators if the primary function is to perform a signal comparison only.

## 4.10 ESD structure of OA1NP, OA2NP, OA4NP series

The OA1NP, OA2NP and OA4NP are protected against electrostatic discharge (ESD) with dedicated diodes (see *Figure 41*). These diodes must be considered at application level especially when signals applied on the input pins go beyond the power supply rails ($V_{CC+}$ or $V_{CC-}$).

**Figure 41. ESD structure**




Current through the diodes must be limited to a maximum of 10 mA as stated in *Table 2*. A serial resistor or a Schottky diode can be used on the inputs to improve protection but the 10 mA limit of input current must be strictly observed.

# 5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

## 5.1 SC70-5 package mechanical data

**Figure 42. SC70-5 package mechanical drawing**

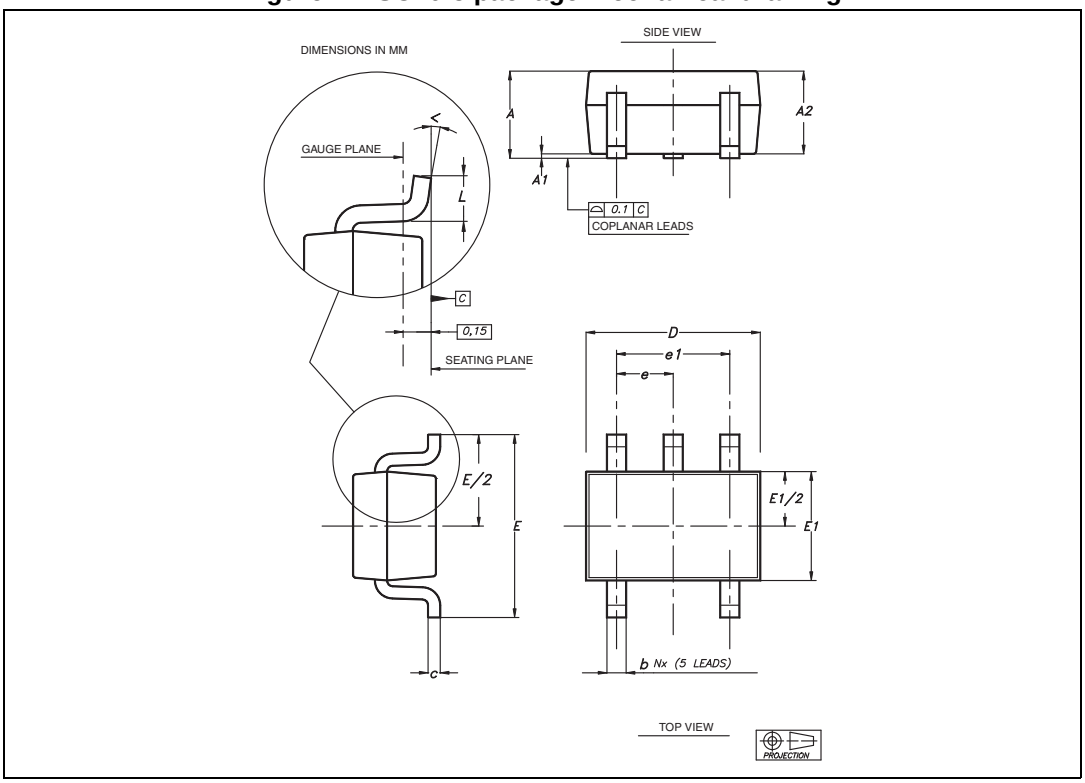



**Table 7. SC70-5 package mechanical data**

| Ref | Dimensions | | | | | |
|---|---|---|---|---|---|---|
| | Millimeters | | | Inches | | |
| | Min | Typ | Max | Min | Typ | Max |
| A | 0.80 | | 1.10 | 0.315 | | 0.043 |
| A1 | | | 0.10 | | | 0.004 |
| A2 | 0.80 | 0.90 | 1.00 | 0.315 | 0.035 | 0.039 |
| b | 0.15 | | 0.30 | 0.006 | | 0.012 |
| c | 0.10 | | 0.22 | 0.004 | | 0.009 |
| D | 1.80 | 2.00 | 2.20 | 0.071 | 0.079 | 0.087 |
| E | 1.80 | 2.10 | 2.40 | 0.071 | 0.083 | 0.094 |
| E1 | 1.15 | 1.25 | 1.35 | 0.045 | 0.049 | 0.053 |
| e | | 0.65 | | | 0.025 | |
| e1 | | 1.30 | | | 0.051 | |
| L | 0.26 | 0.36 | 0.46 | 0.010 | 0.014 | 0.018 |
| < | 0 ° | | 8 ° | 0 ° | | 8 ° |

## 5.2 DFN8 2x2 package information

**Figure 43. DFN8 2x2 package mechanical drawing**

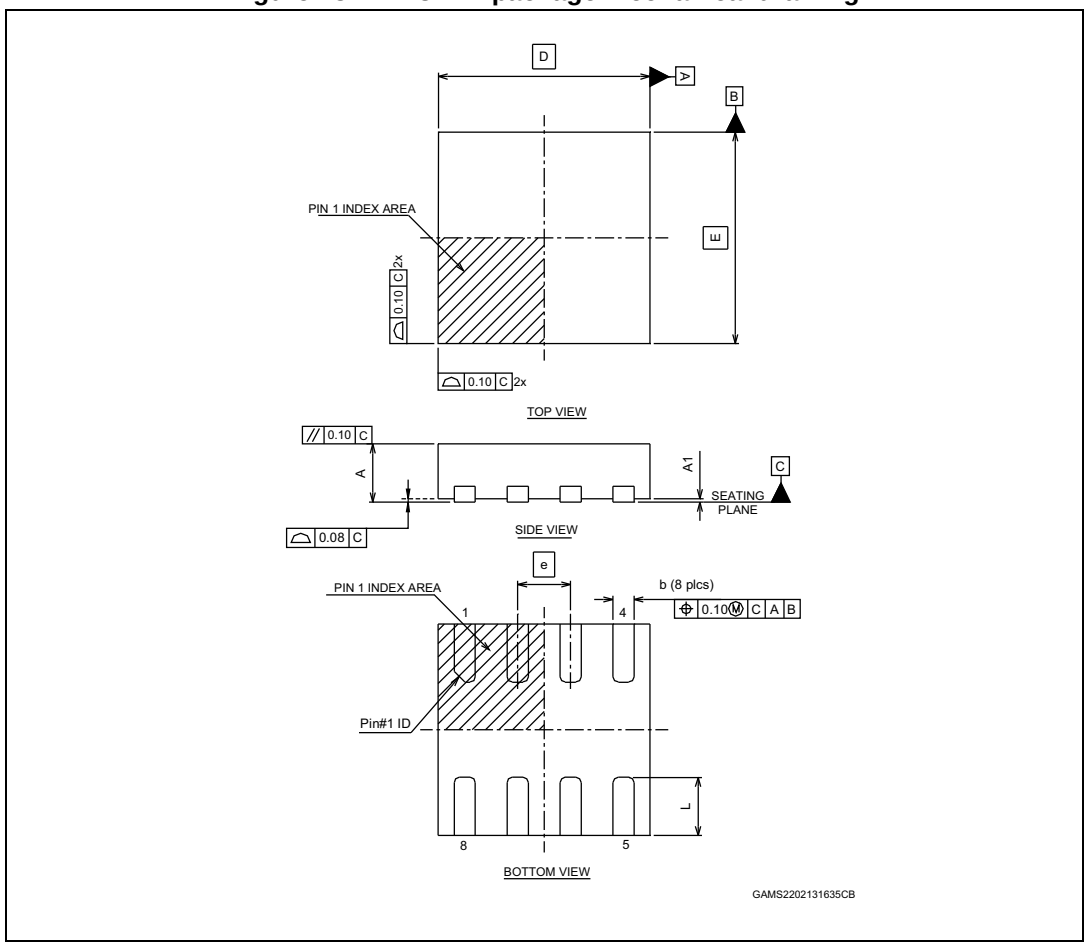



**Table 8. DFN8 2x2 package mechanical data**

| Ref. | Dimensions | | | | | |
|---|---|---|---|---|---|---|
| | Millimeters | | | Inches | | |
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| A | 0.70 | 0.75 | 0.80 | 0.028 | 0.030 | 0.031 |
| A1 | 0.00 | 0.02 | 0.05 | 0.000 | 0.001 | 0.002 |
| b | 0.15 | 0.20 | 0.25 | 0.006 | 0.008 | 0.010 |
| D | | 2.00 | | | 0.079 | |
| E | | 2.00 | | | 0.079 | |
| e | | 0.50 | | | 0.020 | |
| L | 0.045 | 0.55 | 0.65 | 0.018 | 0.022 | 0.026 |
| N | 8 | | | | | |

## 5.3 MiniSO8 package information

**Figure 44. MiniSO8 package mechanical drawing**

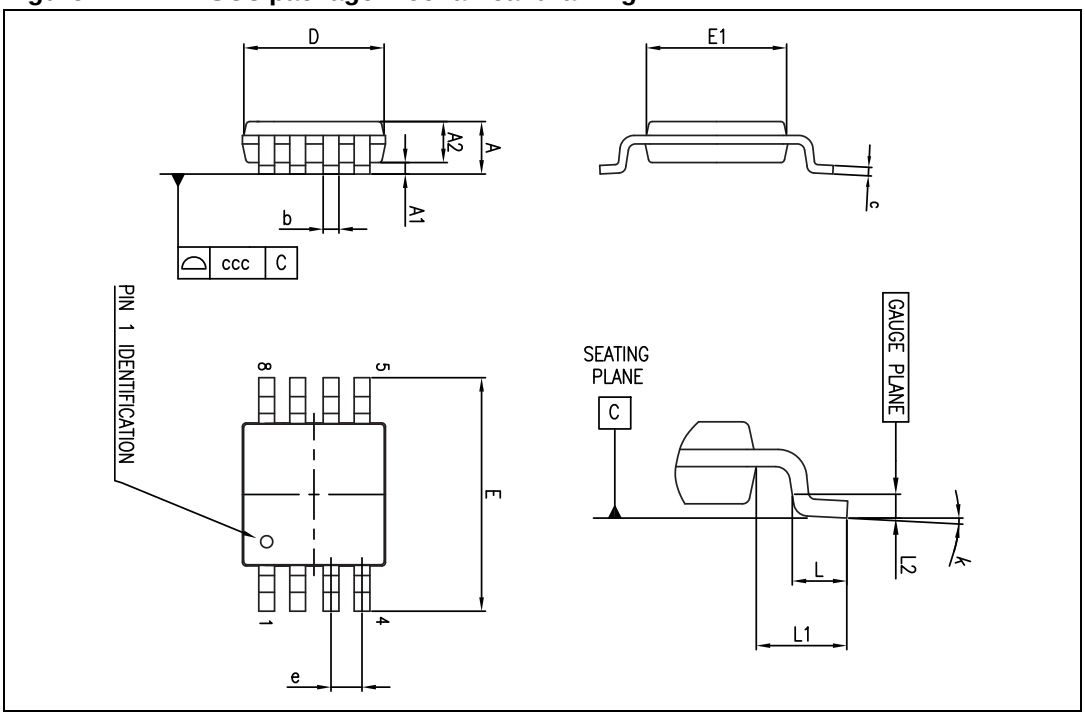



**Table 9. MiniSO8 package mechanical data**

| Ref. | Dimensions | | | | | |
|---|---|---|---|---|---|---|
| | Millimeters | | | Inches | | |
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| A | | | 1.1 | | | 0.043 |
| A1 | 0 | | 0.15 | 0 | | 0.006 |
| A2 | 0.75 | 0.85 | 0.95 | 0.030 | 0.033 | 0.037 |
| b | 0.22 | | 0.40 | 0.009 | | 0.016 |
| c | 0.08 | | 0.23 | 0.003 | | 0.009 |
| D | 2.80 | 3.00 | 3.20 | 0.11 | 0.118 | 0.126 |
| E | 4.65 | 4.90 | 5.15 | 0.183 | 0.193 | 0.203 |
| E1 | 2.80 | 3.00 | 3.10 | 0.11 | 0.118 | 0.122 |
| e | | 0.65 | | | 0.026 | |
| L | 0.40 | 0.60 | 0.80 | 0.016 | 0.024 | 0.031 |
| L1 | | 0.95 | | | 0.037 | |
| L2 | | 0.25 | | | 0.010 | |
| k | 0 ° | | 8 ° | 0 ° | | 8 ° |
| ccc | | | 0.10 | | | 0.004 |

## 5.4 QFN16 package information

**Figure 45. QFN16 package mechanical drawing**

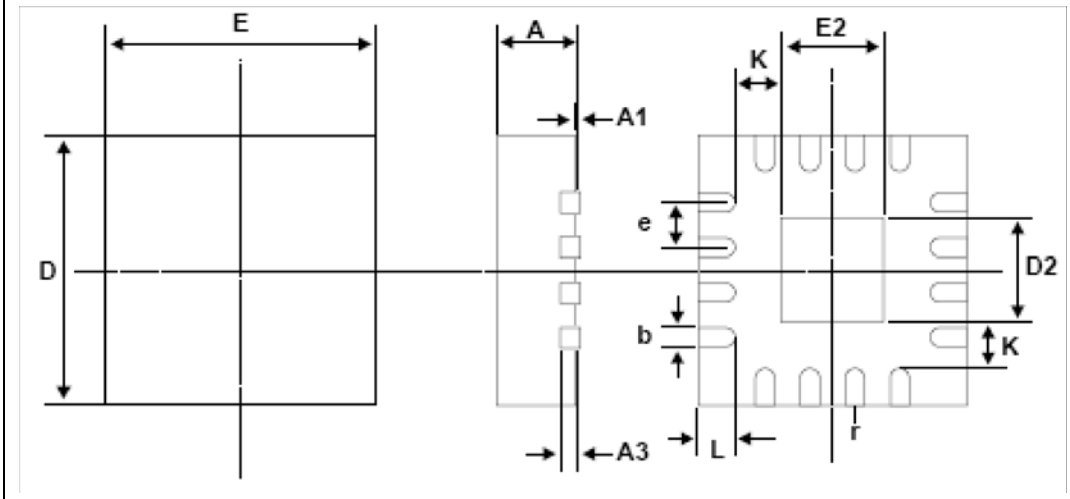



**Table 10. QFN16 package mechanical data**

| Ref. | Dimensions | | | | | |
|---|---|---|---|---|---|---|
| | Millimeters | | | Inches | | |
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| A | 0.80 | 0.90 | 1.00 | 0.032 | 0.035 | 0.039 |
| A1 | | 0.02 | 0.05 | | 0.001 | 0.002 |
| A3 | | 0.2 | | | 0.008 | |
| b | 0.18 | 0.23 | 0.30 | 0.007 | 0.009 | 0.012 |
| D | | 3.00 | | | 0.118 | |
| D2 | 1.00 | 1.15 | 1.25 | 0.039 | 0.045 | 0.049 |
| E | | 3.00 | | | 0.118 | |
| E2 | 1.00 | 1.15 | 1.25 | 0.039 | 0.045 | 0.049 |
| e | | 0.5 | | | 0.02 | |
| K | | 0.2 | | | 0.008 | |
| L | 0.30 | 0.40 | 0.50 | 0.012 | 0.016 | 0.020 |
| r | 0.09 | | | 0.006 | | |

**Figure 46. QFN16 3x3 footprint recommendation**

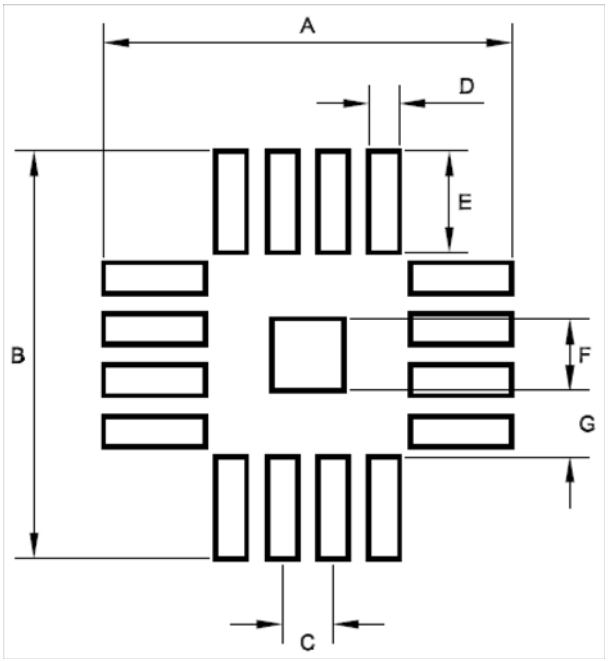



**Table 11. Footprint data**

| Footprint data | | |
|---|---|---|
| **Ref** | **Millimeters** | **Inches** |
| A | 4.00 | 0.158 |
| B | | |
| C | 0.50 | 0.020 |
| D | 0.30 | 0.012 |
| E | 1.00 | 0.039 |
| F | 0.70 | 0.028 |
| G | 0.66 | 0.026 |

# 6 Revision history

Table 12. Document revision history

| Date | Revision | Changes |
|---|---|---|
| 28-Feb-2014 | 1 | Initial release |
| 06-Mar-2014 | 2 | Update *Section 4.8 on page 22* |