



# BUK6Y10-30P

30 V, P-channel Trench MOSFET

17 April 2020

Product data sheet

## 1. General description

P-channel enhancement mode MOSFET in an LFPAK56 (Power SO8) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

This product has been designed and qualified to AEC-Q101 standard for use in high-performance automotive applications such as reverse battery protection.

## 2. Features and benefits

- High thermal power dissipation capability
- Suitable for thermally demanding environments due to 175 °C rating
- Trench MOSFET technology
- AEC-Q101 qualified

## 3. Applications

- Reverse battery protection
- Power management
- High-side load switch
- Motor drive

## 4. Quick reference data

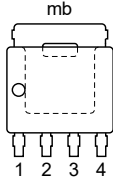
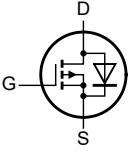
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$T_j = 25\text{ °C}$	-	-	-30	V
$V_{GS}$	gate-source voltage	[1]	-20	-	20	V
$I_D$	drain current	$V_{GS} = -10\text{ V}; T_{mb} = 25\text{ °C}$	-	-	-80	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$	-	-	110	W
<b>Static characteristics</b>						
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = -10\text{ V}; I_D = -13.5\text{ A}; T_j = 25\text{ °C}$	-	8	10	mΩ

[1]  $V_{GS} = -20\text{ V}/+5\text{ V}$  according AEC-Q101 at  $T_j = 175\text{ °C}$ ;  $V_{GS} = -20\text{ V}/+20\text{ V}$  according AEC-Q101 at  $T_j = 150\text{ °C}$

## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 <p><b>LFPAK56; Power-SO8 (SOT669)</b></p>	 <p>017aaa094</p>
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

## 6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK6Y10-30P	LFPAK56; Power-SO8	plastic, single-ended surface-mounted package; 4 terminals	SOT669

## 7. Marking

Table 4. Marking codes

Type number	Marking code
BUK6Y10-30P	6Y1030P

## 8. Limiting values

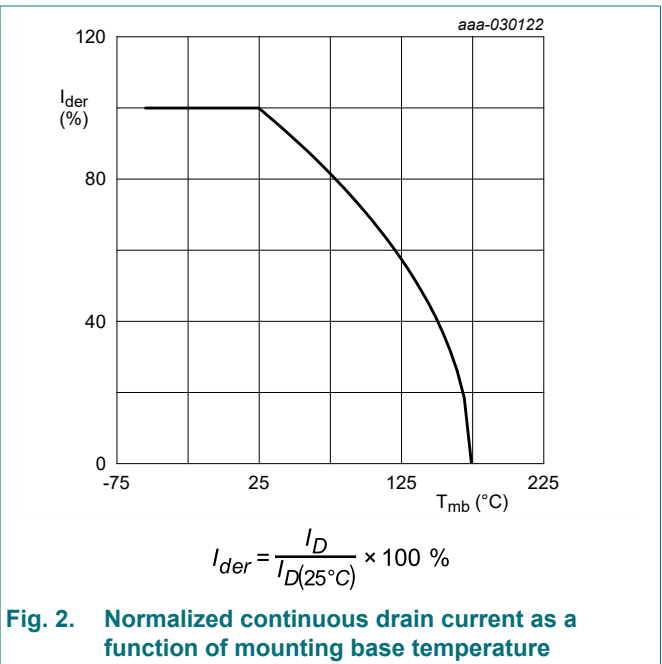
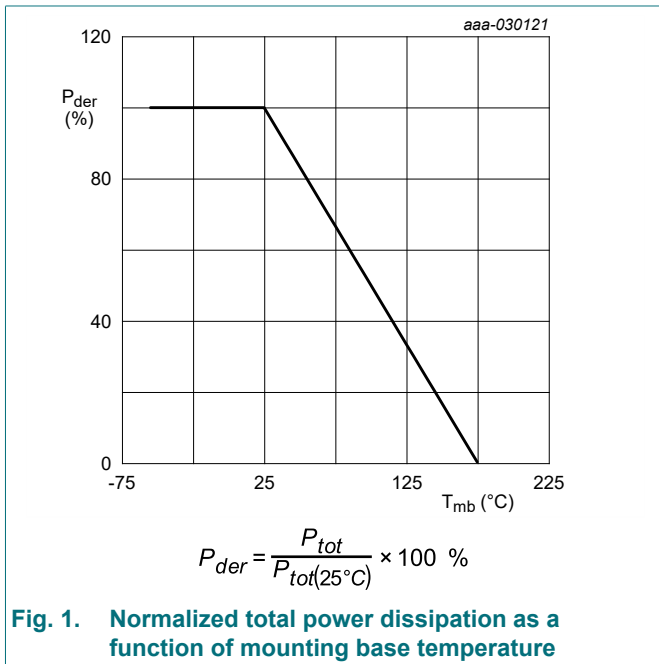
**Table 5. Limiting values**

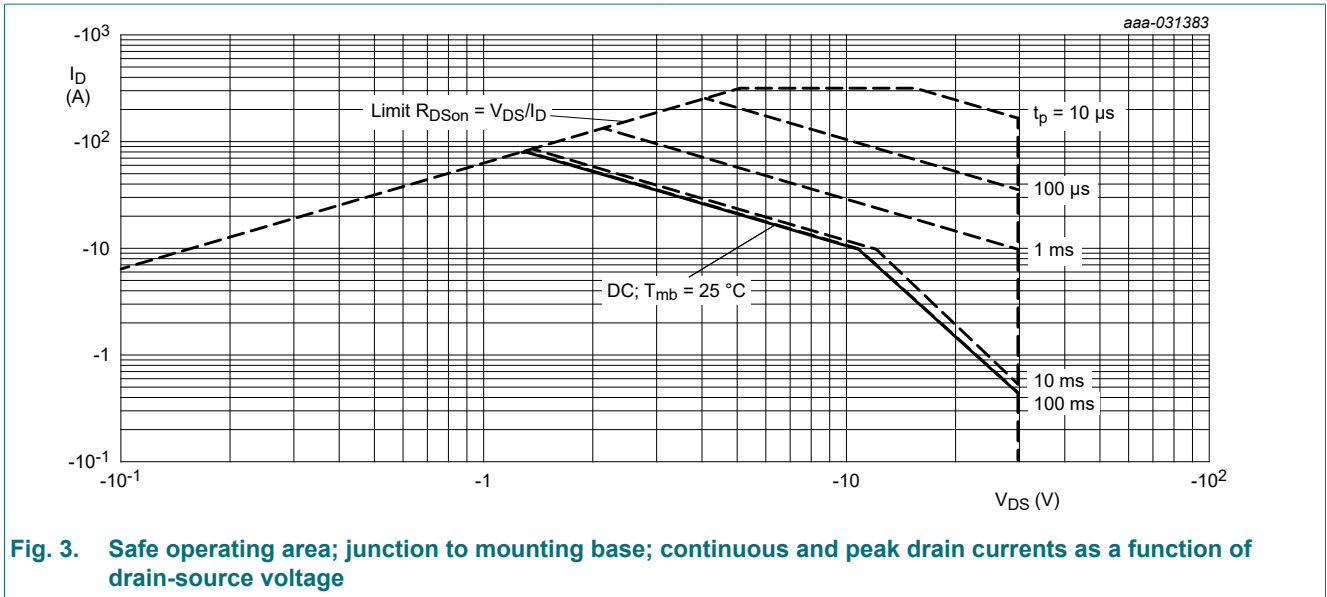
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>DS</sub>	drain-source voltage	T <sub>j</sub> = 25 °C	-	-30	V
V <sub>GS</sub>	gate-source voltage	[1]	-20	20	V
I <sub>D</sub>	drain current	V <sub>GS</sub> = -10 V; T <sub>mb</sub> = 25 °C	-	-80	A
		V <sub>GS</sub> = -10 V; T <sub>mb</sub> = 100 °C	-	-57	A
I <sub>DM</sub>	peak drain current	single pulse; t <sub>p</sub> ≤ 10 μs; T <sub>mb</sub> = 25 °C	-	-320	A
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C	-	110	W
T <sub>j</sub>	junction temperature		-55	175	°C
T <sub>amb</sub>	ambient temperature		-55	175	°C
T <sub>stg</sub>	storage temperature		-65	175	°C
<b>Source-drain diode</b>					
I <sub>S</sub>	source current	T <sub>mb</sub> = 25 °C	-	-80	A
I <sub>SM</sub>	peak source current	single pulse; t <sub>p</sub> ≤ 10 μs; T <sub>mb</sub> = 25 °C	-	-320	A
<b>ESD maximum rating</b>					
V <sub>ESD</sub>	electrostatic discharge voltage	HBM	[2]	800	V
<b>Avalanche ruggedness</b>					
E <sub>DS(AL)S</sub>	non-repetitive drain-source avalanche energy	T <sub>j(initial)</sub> = 25 °C; I <sub>D</sub> = -5.3 A; DUT in avalanche (unclamped)	-	80	mJ

[1] V<sub>GS</sub> = -20 V/+5 V according AEC-Q101 at T<sub>j</sub> = 175 °C; V<sub>GS</sub> = -20 V/+20 V according AEC-Q101 at T<sub>j</sub> = 150 °C

[2] Measured between all pins.





## 9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base		-	1.1	1.4	K/W

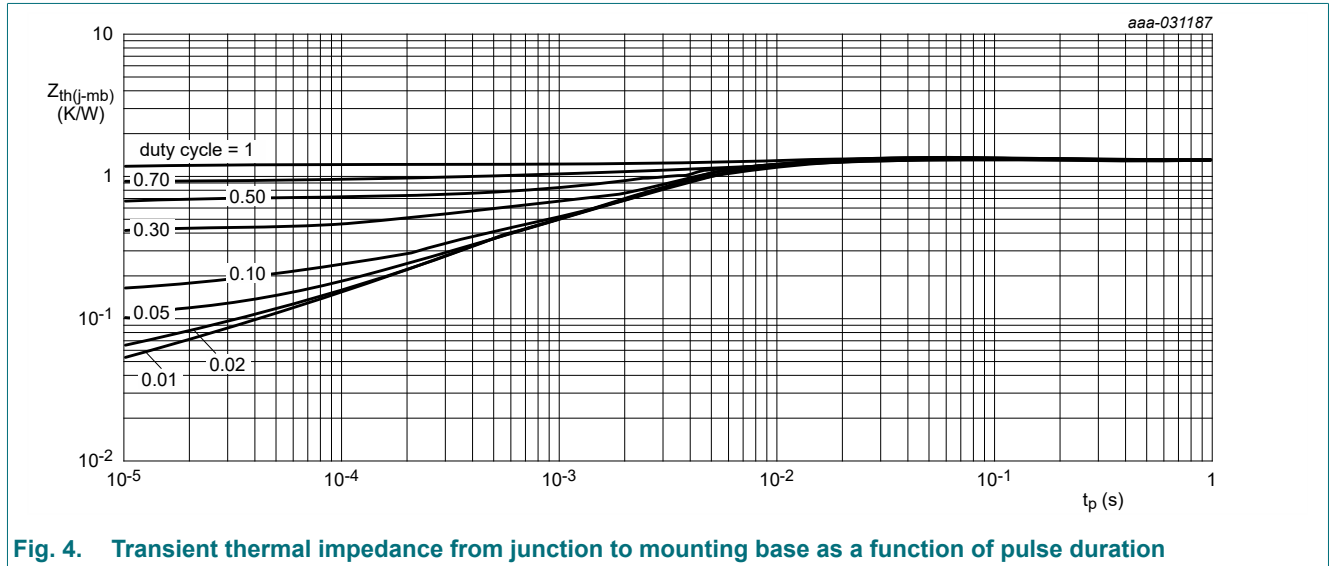


Fig. 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

## 10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = -250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	-30	-	-	V
$V_{GSth}$	gate-source threshold voltage	$I_D = -250 \mu A; V_{DS}=V_{GS}; T_j = 25 \text{ }^\circ C$	-1.5	-2	-3	V
$I_{DSS}$	drain leakage current	$V_{DS} = -30 V; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	-1	$\mu A$
		$V_{DS} = -30 V; V_{GS} = 0 V; T_j = 125 \text{ }^\circ C$	-	-	-10	$\mu A$
$I_{GSS}$	gate leakage current	$V_{GS} = -20 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	-100	nA
		$V_{GS} = 20 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	100	nA
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = -10 V; I_D = -13.5 A; T_j = 25 \text{ }^\circ C$	-	8	10	m $\Omega$
		$V_{GS} = -10 V; I_D = -13.5 A; T_j = 175 \text{ }^\circ C$	-	13	16	m $\Omega$
		$V_{GS} = -4.5 V; I_D = -8.5 A; T_j = 25 \text{ }^\circ C$	-	19	25	m $\Omega$
$g_{fs}$	forward transconductance	$V_{DS} = -5 V; I_D = -13.5 A; T_j = 25 \text{ }^\circ C$	-	31	-	S
$R_G$	gate resistance	$f = 1 \text{ MHz}$	-	8.8	-	$\Omega$
<b>Dynamic characteristics</b>						
$Q_{G(tot)}$	total gate charge	$V_{DS} = -15 V; I_D = -12 A; V_{GS} = -10 V; T_j = 25 \text{ }^\circ C$	-	42.5	64	nC
$Q_{GS}$	gate-source charge		-	8.4	-	nC
$Q_{GD}$	gate-drain charge		-	9.3	-	nC
$C_{iss}$	input capacitance	$V_{DS} = -15 V; f = 1 \text{ MHz}; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	-	2360	-	pF
$C_{oss}$	output capacitance		-	470	-	pF
$C_{rss}$	reverse transfer capacitance		-	270	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = -15 V; I_D = -13.5 A; V_{GS} = -10 V; R_{G(ext)} = 6 \text{ } \Omega; T_j = 25 \text{ }^\circ C$	-	10	-	ns
$t_r$	rise time		-	38	-	ns
$t_{d(off)}$	turn-off delay time		-	80	-	ns
$t_f$	fall time		-	580	-	ns
<b>Source-drain diode</b>						
$V_{SD}$	source-drain voltage	$I_S = -80 A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-0.7	-1.2	V
$t_{rr}$	reverse recovery time	$I_S = -80 A; di_S/dt = 100 A/\mu s; V_{GS} = -10 V; V_{DS} = -15 V; T_j = 25 \text{ }^\circ C$	-	24	-	ns
$Q_r$	recovered charge		-	17	-	nC

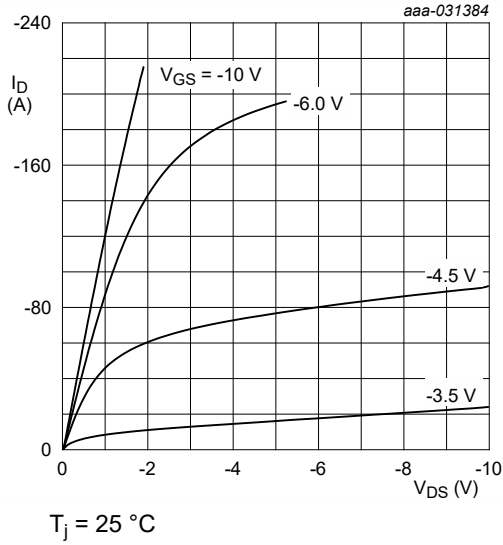


Fig. 5. Output characteristics: drain current as a function of drain-source voltage; typical values

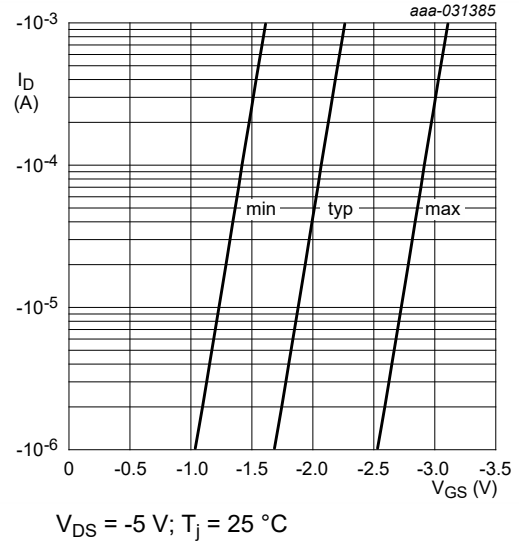


Fig. 6. Sub-threshold drain current as a function of gate-source voltage

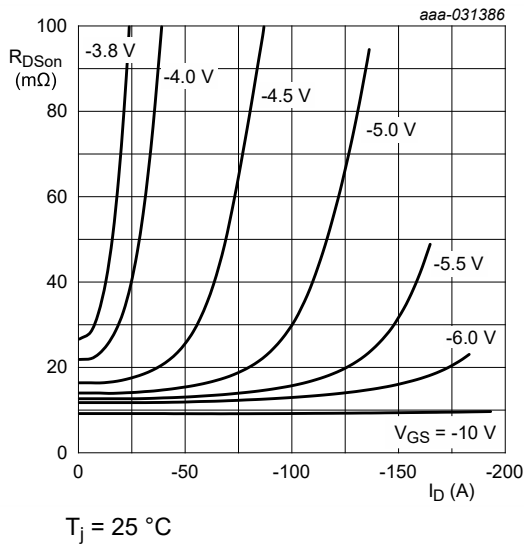


Fig. 7. Drain-source on-state resistance as a function of drain current; typical values

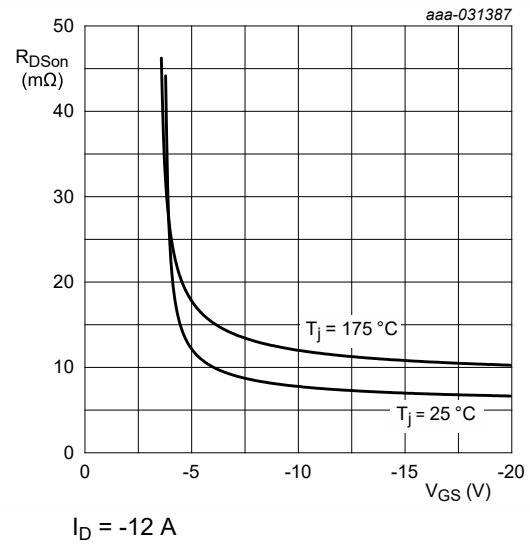


Fig. 8. Drain-source on-state resistance as a function of gate-source voltage; typical values

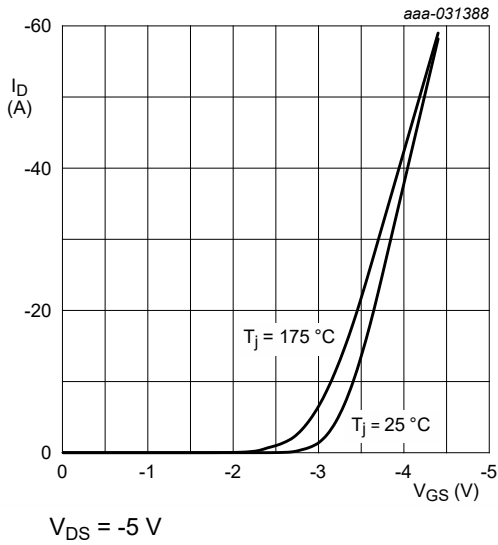


Fig. 9. Transfer characteristics: drain current as a function of gate-source voltage; typical values

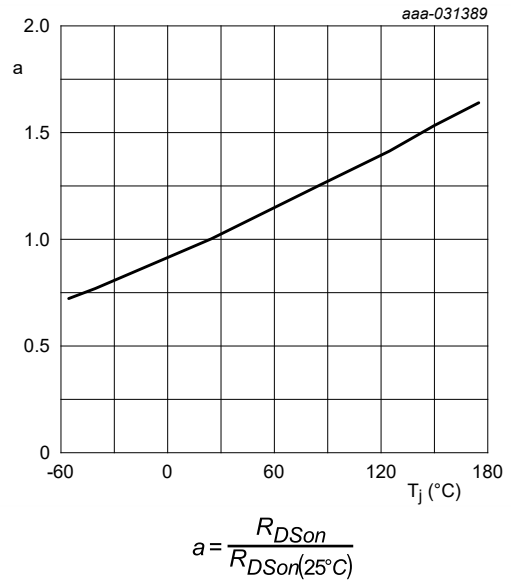


Fig. 10. Normalized drain-source on-state resistance as a function of junction temperature; typical values

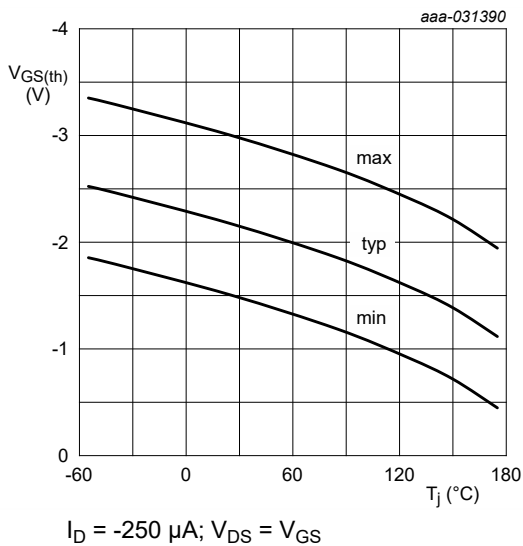


Fig. 11. Gate-source threshold voltage as a function of junction temperature

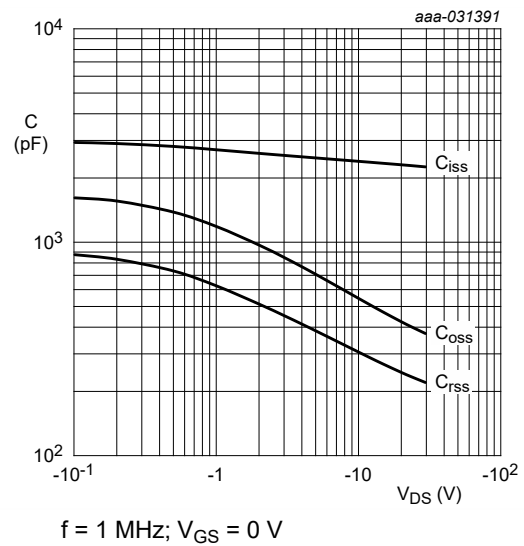
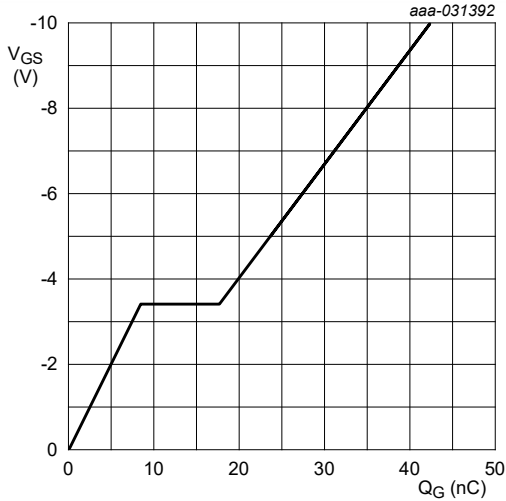


Fig. 12. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values





$V_{DS} = -15\text{ V}; I_D = -12\text{ A}; T_j = 25\text{ }^\circ\text{C}$

Fig. 13. Gate-source voltage as a function of gate charge; typical values

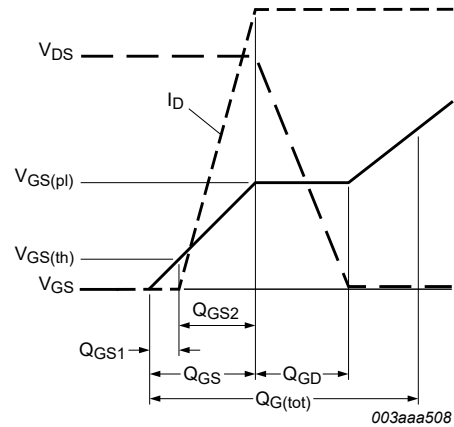
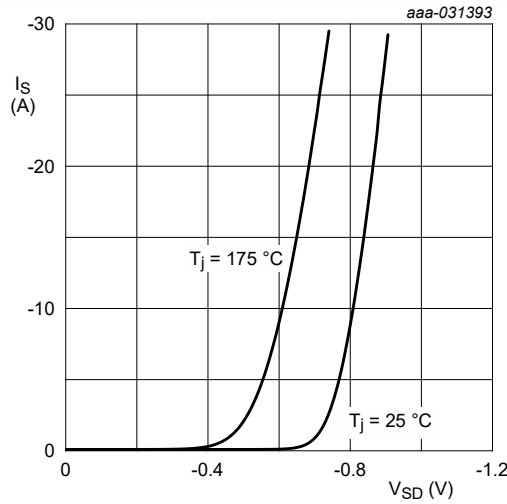


Fig. 14. Gate charge waveform definitions



$V_{GS} = 0\text{ V}$

Fig. 15. Source current as a function of source-drain voltage; typical values

## 11. Test information



Fig. 16. Duty cycle definition

### Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - *Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

12. Package outline

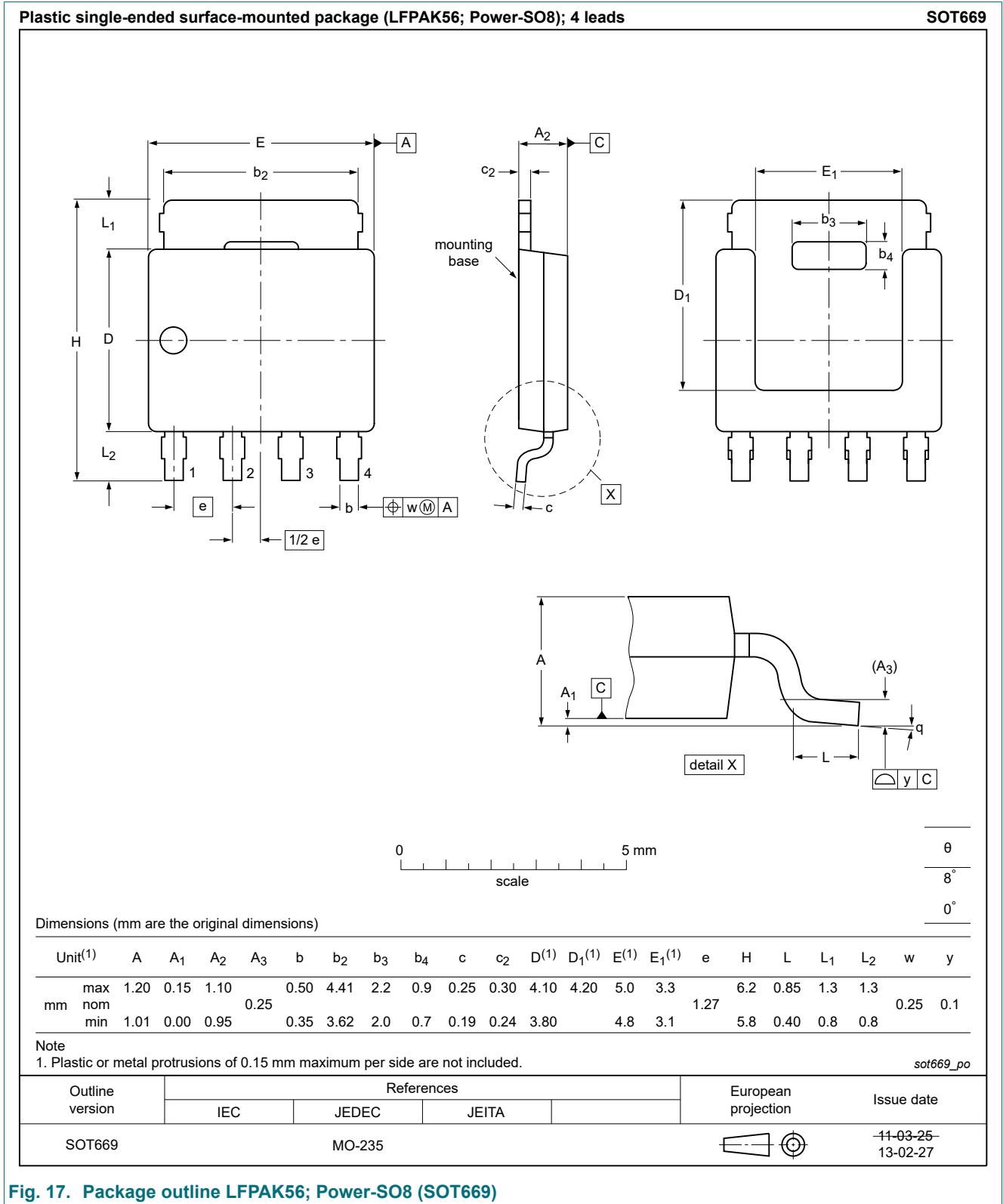


Fig. 17. Package outline LFAK56; Power-SO8 (SOT669)

## 13. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
BUK6Y10-30P v.1	20200417	Product data sheet	-	-

## 14. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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