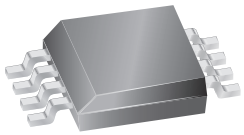
Wide Input Voltage 3.0 A Step-Down Regulator

FEATURES AND BENEFITS

- 8 to 50 V input range
- Integrated DMOS switch
- Adjustable fixed off-time
- Highly efficient
- Adjustable 0.8 to 24 V output

PACKAGE: 8-Lead SOIC with Exposed Thermal Pad (suffix LJ)



Approximate Footprint

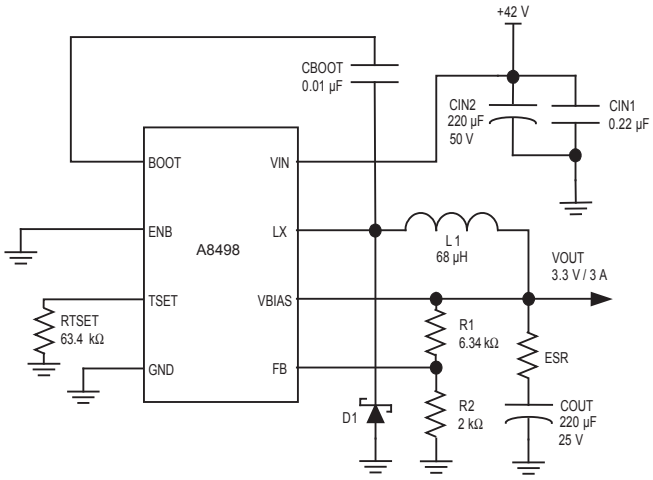
DESCRIPTION

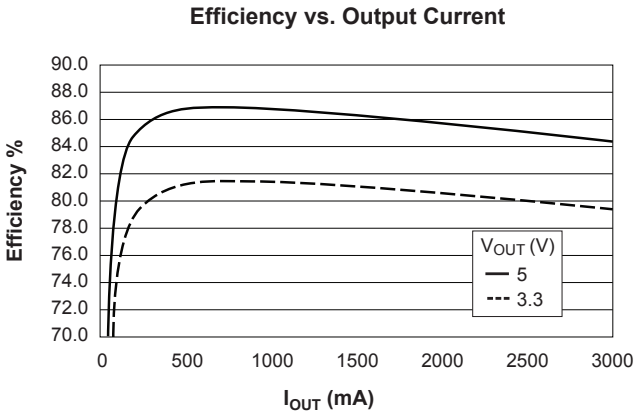
The A8498 is a step-down regulator that will handle a wide input operating voltage range.

The A8498 is supplied in a low-profile 8-lead SOIC with exposed pad (package LJ).

Applications include:

- Applications with 8 to 50 V input voltage range needing buck regulator for 3.0 A output current
- Consumer equipment power
- Uninterruptible power supplies (lead acid battery charger)
- Automotive telematics: 9 to 16 V input, with higher voltage protection
- 12 V lighter-powered applications (portable DVD, etc.)
- Point of Sale (POS) applications
- Industrial applications with 24 or 36 V bus





Typical Application

Circuit for 42 V step down to 3.3 V at 3 A. Efficiency data from circuit shown in left panel. Data is for reference only.

SPECIFICATIONS

SELECTION GUIDE

Part Number [1]	Packing [b]	Description
A8498SLJTR-T	13 in. reel, 3000 pieces/reel	LJ package, SOIC surface mount with exposed thermal pad

[a] Leadframe plating 100% matte tin.
[b] Contact Allegro for additional packing options.

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Conditions	Min.	Typ.	Max.	Units
Load Supply Voltage, VIN pin	V_{IN}		–	–	50	V
Input Voltage, VBIAS pin	V_{BIAS}		–0.3	–	7	V
Switching Voltage	V_S		–1	–	–	V
Input Voltage Range, ENB pin	V_{ENB}		–0.3	–	7	V
Operating Ambient Temperature Range	T_A		–20	–	85	°C
Junction Temperature	T_J(max)		–	–	150	°C
Storage Temperature	T_S		–55	–	150	°C

*Output current rating may be limited by duty cycle, ambient temperature, and heat sinking. Under any set of conditions, do not exceed the specified current ratings, or a junction temperature, T_J, of 150°C.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Test Conditions*	Value	Unit
Package Thermal Resistance	$R_{\theta JA}$	LJ package, 4-layer PCB	35	°C/W

*Additional thermal information available on the Allegro website.

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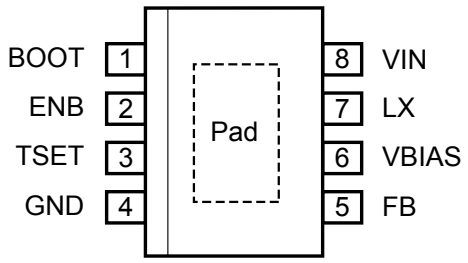
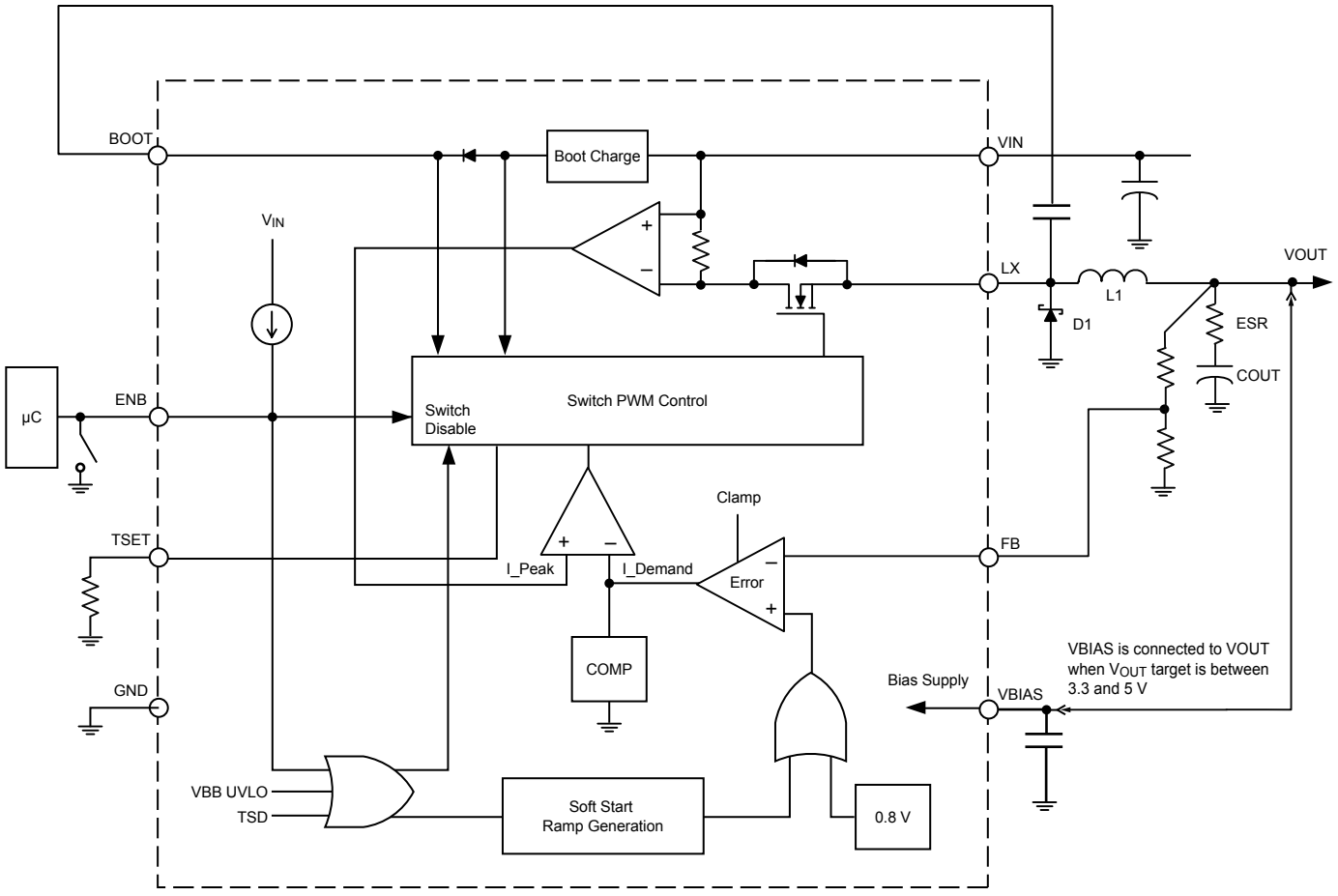


Package LJ, 8-Pin SOIC Pinout Diagram

Terminal List Table

Number	Name	Description
1	BOOT	Gate drive boost node
2	ENB	On/off control; logic input
3	TSET	Off-time setting
4	GND	Ground
5	FB	Feedback for adjustable regulator
6	VBIAS	Bias supply input
7	LX	Buck switching node
8	VIN	Supply input



Functional Block Diagram

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ELECTRICAL CHARACTERISTICS [1][2]: Valid at T_A = 25°C, V_{IN} = 8 to 50 V (unless noted otherwise)

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
VIN Quiescent Current	$I_{VIN(Q)}$	V_{ENB} = LOW, V_{IN} = 42 V, V_{BIAS} = 3.2 V, V_{FB} = 1.5 V (not switching)	–	0.90	1.35	mA
		V_{ENB} = LOW, V_{IN} = 42 V, V_{BIAS} < 3 V, V_{FB} = 1.5 V	–	4.4	6.35	mA
		V_{ENB} = HIGH	–	–	100	µA
VBIAS Input Current	I_{BIAS}	V_{BIAS} = V_{OUT}	–	3.5	5	mA
Buck Switch On Resistance	$R_{DS(on)}$	T_A = 25°C, I_{OUT} = 3 A	–	450	–	mΩ
		T_A = 125°C, I_{OUT} = 3 A	–	650	–	mΩ
Fixed Off-Time Proportion		Based on calculated value	–15	–	15	%
Feedback Voltage	V_{FB}		0.784	0.8	0.816	V
Output Voltage Regulation	V_{OUT}	I_{OUT} = 0 mA to 3 A	–3	–	3	%
Feedback Input Bias Current	I_{FB}		–400	–100	100	nA
Soft Start Time	t_{ss}		5	10	15	ms
Buck Switch Current Limit	I_{CL}	V_{FB} > 0.4 V	3.5	–	5	A
		V_{FB} < 0.4 V	0.5	–	1.5	A
ENB Open Circuit Voltage	V_{OC}	Output disabled	2.0	–	7	V
ENB Input Voltage Threshold	$V_{ENB(0)}$	LOW level input (Logic 0), output enabled	–	–	1.0	V
ENB Input Current	$I_{ENB(0)}$	V_{ENB} = 0 V	–10	–	–1	µA
VIN Undervoltage Threshold	V_{UVLO}	V_{IN} rising	6.6	6.9	7.2	V
VIN Undervoltage Hysteresis	$V_{UVLO(hys)}$	V_{IN} falling	0.7	–	1.1	V
Thermal Shutdown Temperature	T_{JTSD}	Temperature increasing	–	165	–	°C
Thermal Shutdown Hysteresis	$T_{JTSD(hys)}$	Recovery = T_{JTSD} – $T_{JTSD(hys)}$	–	15	–	°C

[1] Negative current is defined as coming out of (sourcing) the specified device pin.
[2] Specifications over the junction temperature range of 0ºC to 125ºC are assured by design and characterization.

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FUNCTIONAL DESCRIPTION

The A8498 is a fixed off-time, current-mode–controlled buck switching regulator. The regulator requires an external clamping diode, inductor, and filter capacitor, and operates in both continuous and discontinuous modes. An internal blanking circuit is used to filter out transients resulting from the reverse recovery of the external clamp diode. Typical blanking time is 200 ns.

The value of a resistor between the TSET pin and ground determines the fixed off-time (see graph in the t_{OFF} section).

V_{OUT}. The output voltage is adjustable from 0.8 to 24 V, based on the combination of the value of the external resistor divider and the internal 0.8 V ±2% reference. The voltage can be calculated with the following formula:

$$V_{OUT} = V_{FB} \times (1 + R1/R2) \qquad (1)$$

Light Load Regulation

To maintain voltage regulation during light load conditions, the switching regulator enters a cycle-skipping mode. As the output current decreases, there remains some energy that is stored during the power switch minimum on-time. In order to prevent the output voltage from rising, the regulator skips cycles once it reaches the minimum on-time, effectively making the off-time larger.

Soft Start

An internal ramp generator and counter allow the output to slowly ramp up. This limits the maximum demand on the external power supply by controlling the inrush current required to charge the external capacitor and any dc load at startup. Internally, the ramp is set to 10 ms nominal rise time. During soft start, current limit is 3.5 A minimum.

The following conditions are required to trigger a soft start:

- $V_{IN} > 6$ V
- ENB pin input falling edge
- Reset of a TSD (thermal shut down) event

V_{BIAS}

To improve overall system efficiency, the regulator output, V_{OUT}, is connected to the VBIAS input to supply the operating bias current during normal operating conditions. During startup the circuitry is run off the VIN supply. VBIAS should be connected to VOUT when the V_{OUT} target level is between 3.3 and 5 V. If the output voltage is less than 3.3 V, then the A8498 can operate with an internal supply and pay a penalty in efficiency, as the bias current will come from the high voltage supply, VIN. VBIAS can also be supplied with an external voltage source. No power-up sequencing is required for normal operation.

ON/OFF Control

The ENB pin is externally pulled to ground to enable the device and begin the soft start sequence. When the ENB is open circuited, the switcher is disabled and the output decays to 0 V.

Protection

The buck switch will be disabled under one or more of the following fault conditions:

- $V_{IN} < 6$ V
- ENB pin = open circuit
- TSD fault

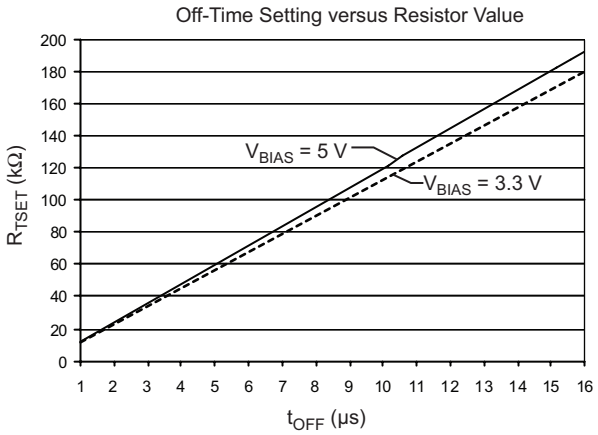
When the device comes out of a TSD fault, it will go into a soft start to limit inrush current.

t_{OFF}

The value of a resistor between the TSET pin and ground determines the fixed off-time. The formula to calculate t_{OFF} (µs) is:

$$t_{OFF} = R_{TSET}\left(\frac{1-0.03\ V_{BIAS}}{10.2 \times 10^{9}}\right), \qquad (2)$$

where R_{TSET} (kΩ) is the value of the resistor. Results are shown in the following graph:



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t_{ON}

From the volt-second balance of the inductor, the turn-on time, t_{on}, can be calculated approximately by the equation:

$$t_{ON} = \frac{(V_{OUT} + V_f + I_{OUT} \times R_L) \times t_{OFF}}{V_{IN} - I_{OUT} \times R_{DS(on)} - I_{OUT} \times R_L - V_{OUT}} \quad (3)$$

where

V_f is the voltage drop across the external Schottky diode,
R_L is the winding resistance of the inductor, and
$R_{DS(on)}$ is the on-resistance of the switching MOSFET.

The switching frequency is calculated as follows:

$$f_{SW} = \frac{1}{t_{ON} + t_{OFF}} \quad (4)$$

Shorted Load

If the voltage on the FB pin falls below 0.4 V, the regulator will invoke a 1.5 A typical overcurrent limit to handle the shorted load condition at the regulator output. For low output voltages at power up and in the case of a shorted output, the off-time is extended to prevent loss of control of the current limit due to the minimum on-time of the switcher.

The extension of the off-time is based on the value of the TSET multiplier and the FB voltage, as shown in the following table:

V_{FB} (V)	TSET Multiplier
< 0.16	$8 \times t_{OFF}$
< 0.32	$4 \times t_{OFF}$
< 0.5	$2 \times t_{OFF}$
> 0.5	t_{OFF}

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COMPONENT SELECTION

L1

The inductor must be rated to handle the total load current. The value should be chosen to keep the ripple current to a reasonable value. The ripple current, I_{RIPPLE}, can be calculated by:

$$I_{RIPPLE} = V_{L(OFF)} \times t_{OFF} / L \quad (5)$$

$$V_{L(OFF)} = V_{OUT} + V_f + I_{L(AV)} \times R_L \quad (6)$$

Example:

Given V_{OUT} = 5 V, V_f = 0.55 V, V_{IN} = 42 V, I_{LOAD} = 0.5 A, power inductor with L = 180 µH and R_L = 0.5 Ω Rdc at 55°C, t_{OFF} = 7 µs, and $R_{DS(on)}$ = 0.5 Ω.

Substituting into equation 6:

$$V_{L(OFF)} = 5\ V + 0.55\ V + 0.5\ A \times 0.5\ \Omega = 5.8\ V$$

Substituting into equation 5:

$$I_{RIPPLE} = 5.8\ V \times 7\ \mu s / 180\ \mu H = 225\ mA$$

The switching frequency, f_{SW}, can then be estimated by:

$$f_{SW} = 1 / (t_{ON} + t_{OFF}) \quad (7)$$

$$t_{ON} = I_{RIPPLE} \times L / V_{L(ON)} \quad (8)$$

$$V_{L(ON)} = V_{IN} - I_{L(AV)} \times R_{DS(on)} - I_{L(AV)} \times R_L - V_{OUT} \quad (9)$$

Substituting into equation 9:

$$V_{L(ON)} = 42\ V - 0.5\ A \times 0.5\ \Omega - 0.5\ A \times 0.5\ \Omega - 5\ V = 36.5\ V$$

Substituting into equation 8:

$$t_{ON} = 225\ mA \times 180\ \mu H / 36.5\ V = 1.11\ \mu s$$

Substituting into equation 7:

$$f_{SW} = 1 / (7\ \mu s + 1.11\ \mu s) = 123\ kHz$$

Higher inductor values can be chosen to lower the ripple current. This may be an option if it is required to increase the total maximum current available above that drawn from the switching regulator. The maximum total current available, $I_{LOAD(MAX)}$, is:

$$I_{LOAD(MAX)} = I_{CL}(min) - I_{RIPPLE} / 2 \quad (10)$$

where I_{CL}(min) is 3.5 A, from the Electrical Characteristics table.

D1

The Schottky catch diode should be rated to handle 1.2 times the maximum load current. The voltage rating should be higher than the maximum input voltage expected during all operating conditions. The duty cycle for high input voltages can be very close to 100%.

COUT

The main consideration in selecting an output capacitor is voltage ripple on the output. For electrolytic output capacitors, a low-ESR type is recommended.

The peak-to-peak output voltage ripple is simply I_{RIPPLE} × ESR. Note that increasing the inductor value can decrease the ripple current. The ESR should be in the range from 50 to 500 mΩ.

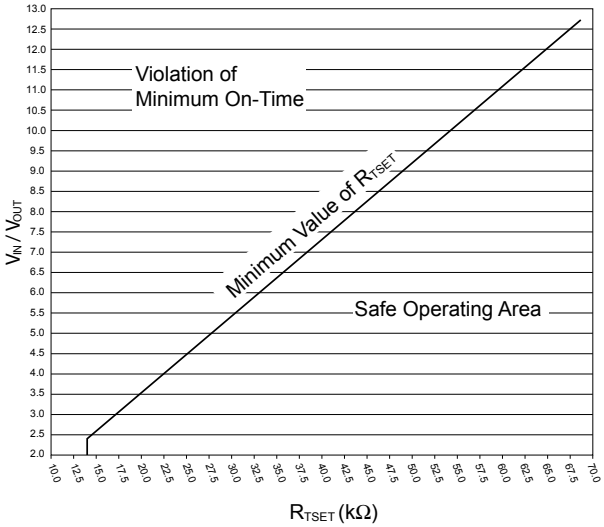
RTSET Selection

Correct selection of RTSET values will ensure that minimum on time of the switcher is not violated and prevent the switcher from cycle skipping. For a given V_{IN} to V_{OUT} ratio, the RTSET value must be greater than or equal to the value defined by the curve in the plot below.

Note. The curve represents the minimum RTSET value. When calculating R_{TSET}, be sure to use V_{IN}(max) / V_{OUT}(min). Resistor tolerance should also be considered, so that under no operating conditions the resistance on the TSET pin is allowed to go below the minimum value.

FB Resistor Selection

The impedance of the FB network should be kept low to improve noise immunity. Large value resistors can pick up noise generated by the inductor, which can affect voltage regulation of the switcher.



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Recommended Components

Component	V_{IN} = 42 V (Through Hole)		V_{IN} = 24 V (SMD)		V_{IN} = 12 V (SMD)	
	Description	Part Number	Description	Part Number	Description	Part Number
Inductor	Sumida, 68 µH	RCH1216BNP-680K	47 µH, 53 mΩ, 3.9 A, ±20%	CDRH127/LDNP-470MC	33 µH, 53 mΩ, 3.9 A, ±20%	CDRH127/LDNP-330MC
Diode	NIEC Schottky Barrier, 60 V, TO-252AA	NSQ03A06	Schottky, 30V, 3A, SMA	B330	Schottky, 20 V, 3 A, SMA	B320
CBOOT	Ceramic X7A, 0.01 µF, 100 V	Generic	Ceramic, X7R, ±10%, 0.01 µF / 50 V	C0603C103K5RACTU (Kemet)	Ceramic, X7R, ±10%, 0.01 µF / 50 V	C0603C103K5RACTU (Kemet)
CIN1	Ceramic X7A, 0.22 µF, 50 V	Generic	Ceramic, X7R, ±10%, 0.1 µF / 50 V	GRM188R71H104KA93D (Murata)	Ceramic, X7R, ±10%, 0.1 µF / 50 V	GRM188R71H104KA93D (Murata)
CIN2	Rubycon ZL, 220 µF, 50 V	50-ZL-220-M-10 X 16	Aluminum electrolytic, 35 V / 82 µF, 930 mA ripple current	35V-ZAV-820-8 X 12 (two)	Aluminum electrolytic, 35 V / 82 µF, 930 mA ripple current	35V-ZAV-820-8 X 12 (two)
COUT	Rubycon ZL, 220 µF, 25 V	25-ZL-220-M-8 X 11.5	Aluminum electrolytic, 6.3 V / 330 µF, 450 mA ripple current	EEVFC0J331P (Panasonic)	Aluminum electrolytic, 6.3 V / 330 µF, 450 mA ripple current	EEVFC0J331P (Panasonic)
R1	2.55 kΩ at VOUT = 1.8 V 6.34 kΩ at VOUT = 3.3 V 10.5 kΩ at VOUT = 5.0 V		2.55 kΩ at VOUT = 1.8 V 6.34 kΩ at VOUT = 3.3 V 10.5 kΩ at VOUT = 5.0 V		2.55 kΩ at VOUT = 1.8 V 6.34 kΩ at VOUT = 3.3 V 10.5 kΩ at VOUT = 5.0 V	
R2	2 kΩ		2 kΩ		2 kΩ	
R_{TSET}	63.4 kΩ		47.5 kΩ		35.2 kΩ	

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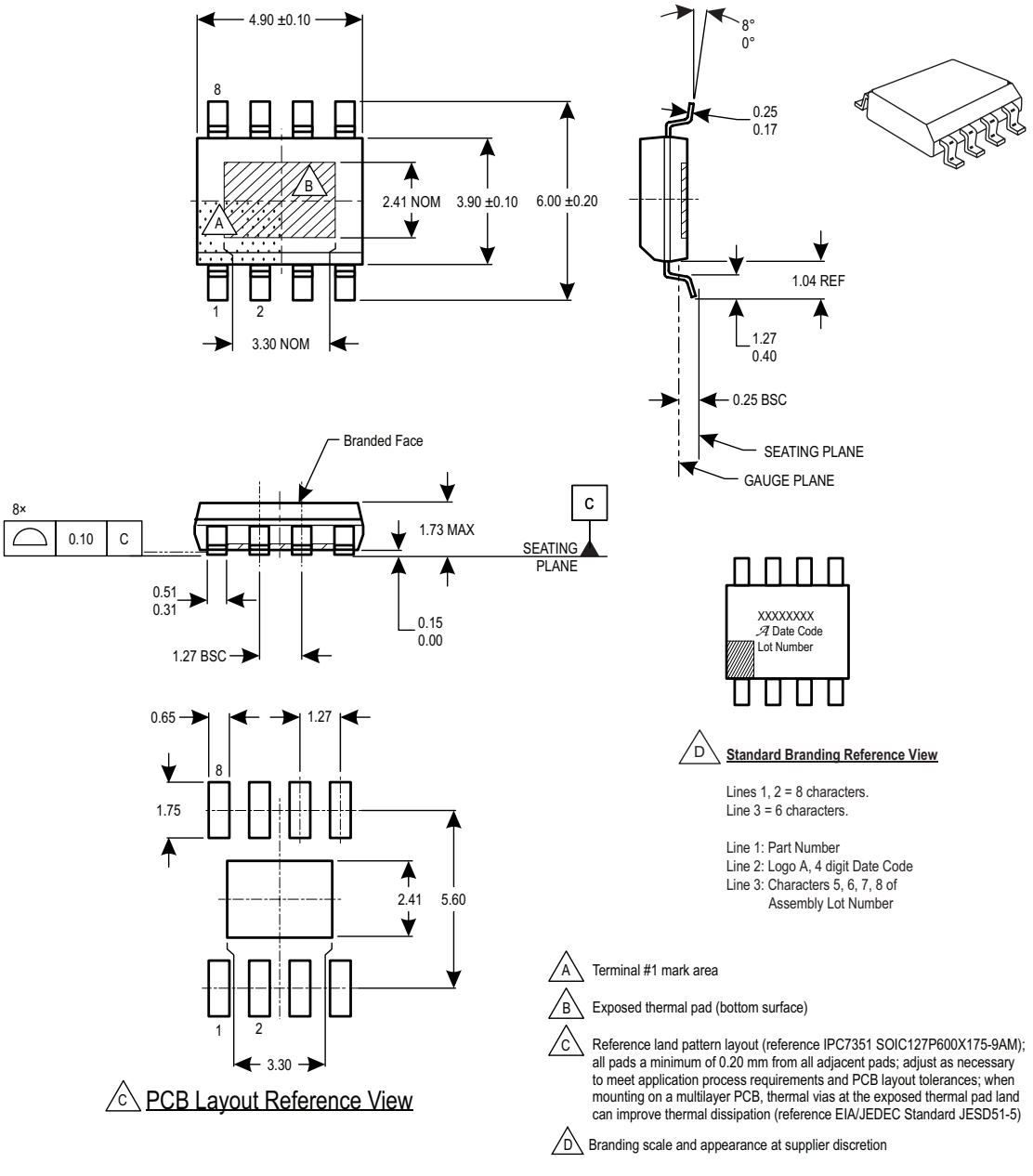
PACKAGE OUTLINE DRAWING

For Reference Only – Not for Tooling Use

(Reference Allegro DWG-0000380, Rev. 2 and JEDEC MS-012BA)
Dimensions in millimeters – NOT TO SCALE
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown



C PCB Layout Reference View

D Standard Branding Reference View

Lines 1, 2 = 8 characters.
Line 3 = 6 characters.

Line 1: Part Number
Line 2: Logo A, 4 digit Date Code
Line 3: Characters 5, 6, 7, 8 of
Assembly Lot Number

A Terminal #1 mark area

B Exposed thermal pad (bottom surface)

C Reference land pattern layout (reference IPC7351 SOIC127P600X175-9AM); all pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

D Branding scale and appearance at supplier discretion

Package LJ 8-Pin SOIC with Exposed Thermal Pad

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Revision History

Number	Date	Description
6	September 10, 2014	Revised I_{CL} Max. spec.
7	July 7, 2016	Revised V_{ENB} Max. spec.
8	May 14, 2020	Minor editorial updates
9	May 16, 2022	Updated package drawing and minor editorial updates

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