



# STB9NK60Z, STP9NK60Z, STP9NK60ZFP

N-channel 600 V, 0.85  $\Omega$  typ., 7 A Zener-protected SuperMESH™ Power MOSFET in D<sup>2</sup>PAK, TO-220 and TO-220FP packages

Datasheet – production data

## Features

Order codes	V <sub>DS</sub>	R <sub>DS(on) max</sub>	I <sub>D</sub>	P <sub>TOT</sub>
STB9NK60ZT4	600 V	0.95 $\Omega$	7 A	125 W
STP9NK60Z				30 W
STP9NK60ZFP				30 W

- Extremely high dv/dt capability
- Improved ESD capability
- 100% avalanche tested
- Gate charge minimized
- Very low intrinsic capacitances

## Applications

- Switching applications

## Description

These devices are N-channel Zener-protected Power MOSFETs developed using STMicroelectronics' SuperMESH™ technology, achieved through optimization of ST's well established strip-based PowerMESH™ layout. In addition to a significant reduction in on-resistance, this device is designed to ensure a high level of dv/dt capability for the most demanding applications.

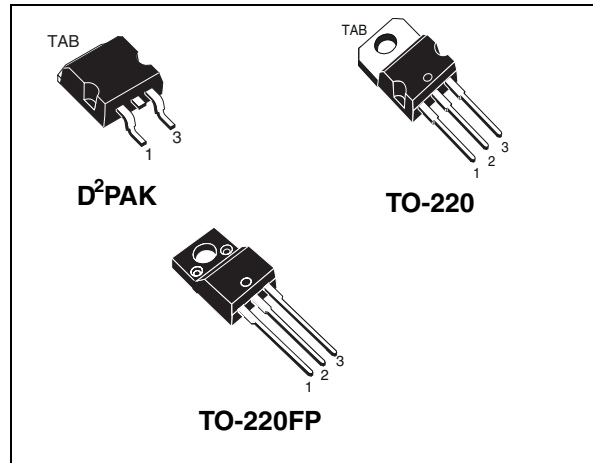


Figure 1. Internal schematic diagram

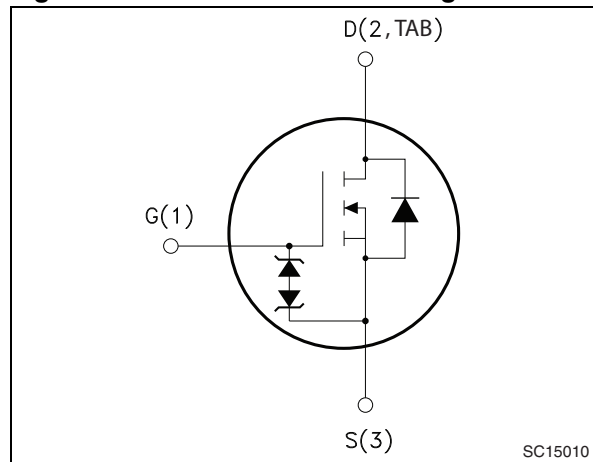


Table 1. Device summary

Order codes	Marking	Package	Packaging
STB9NK60ZT4	B9NK60Z	D <sup>2</sup> PAK	Tube
STP9NK60Z	P9NK60Z	TO-220	
STP9NK60ZFP	P9NK60ZFP	TO-220FP	

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value		Unit
		D <sup>2</sup> PAK, TO-220	TO-220FP	
V <sub>DS</sub>	Drain-source voltage	600		V
V <sub>GS</sub>	Gate-source voltage	± 30		V
I <sub>D</sub>	Drain current (continuous) at T <sub>C</sub> = 25°C	7	7 <sup>(1)</sup>	A
I <sub>D</sub>	Drain current (continuous) at T <sub>C</sub> =100°C	4.4	4.4 <sup>(1)</sup>	A
I <sub>DM</sub> <sup>(2)</sup>	Drain current (pulsed)	28	28 <sup>(1)</sup>	A
P <sub>TOT</sub>	Total dissipation at T <sub>C</sub> = 25°C	125	30	W
	Derating Factor	1	0.24	W/°C
ESD	Gate-source human body model (R=1,5 kΩ, C=100 pF)	4		kV
dv/dt <sup>(3)</sup>	Peak diode recovery voltage slope	4.5		V/ns
V <sub>ISO</sub>	Insulation withstand voltage (RMS) from all three leads to external heat sink (t = 1 s, T <sub>C</sub> = 25 °C)	--	2500	V
T <sub>J</sub> T <sub>stg</sub>	Operating junction temperature Storage temperature	-55 to 150		°C

- Limited by maximum junction temperature
- Pulse width limited by safe operating area
- I<sub>SD</sub> ≤ 7A, di/dt ≤ 200A/μs, V<sub>DD</sub> ≤ V<sub>(BR)DSS</sub>, T<sub>J</sub> ≤ T<sub>JMAX</sub>

**Table 3. Thermal data**

Symbol	Parameter	Value			Unit
		D <sup>2</sup> PAK	TO-220	TO-220FP	
R <sub>thj-case</sub>	Thermal resistance junction-case max	1		4.2	°C/W
R <sub>thj-amb</sub>	Thermal resistance junction-ambient max		62.5		°C/W
R <sub>thj-pcb</sub>	Thermal resistance junction-pcb max <sup>(1)</sup>	30			°C/W

- When mounted on minimum footprint

**Table 4. Avalanche characteristics**

Symbol	Parameter	Value	Unit
$I_{AR}$	Avalanche current, repetitive or not-repetitive <sup>(1)</sup>	7	A
$E_{AS}$	Single pulse avalanche energy <sup>(2)</sup>	235	mJ

1. Pulse width limited by  $T_{j,Max}$

2. Starting  $T_j=25\text{ °C}$ ,  $I_D=I_{AR}$ ,  $V_{DD}=50\text{ V}$

## 2 Electrical characteristics

( $T_{CASE}=25^{\circ}\text{C}$  unless otherwise specified)

**Table 5. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage $V_{GS}=0$	$I_D = 1 \text{ mA}$	600			V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = 600 \text{ V}$ , $V_{DS} = 600 \text{ V}$ , $T_C = 125^{\circ}\text{C}$			1 50	$\mu\text{A}$ $\mu\text{A}$
$I_{GSS}$	Gate body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 20 \text{ V}$			$\pm 10$	$\mu\text{A}$
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 100 \mu\text{A}$	3	3.75	4.5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10 \text{ V}$ , $I_D = 3.5 \text{ A}$		0.85	0.95	$\Omega$

**Table 6. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} = 15 \text{ V}$ , $I_D = 3.5 \text{ A}$	-	5.3		S
$C_{iss}$	Input capacitance	$V_{DS} = 25 \text{ V}$ , $f = 1 \text{ MHz}$ , $V_{GS} = 0$	-	1110		pF
$C_{oss}$	Output capacitance			135		pF
$C_{rss}$	Reverse transfer capacitance			30		pF
$C_{oss eq}^{(2)}$	Equivalent output capacitance	$V_{GS} = 0$ , $V_{DS} = 0 \text{ V to } 480 \text{ V}$	-	72		pF
$Q_g$	Total gate charge	$V_{DD} = 480 \text{ V}$ , $I_D = 7 \text{ A}$		38	53	nC
$Q_{gs}$	Gate-source charge	$V_{GS} = 10 \text{ V}$	-	7		nC
$Q_{gd}$	Gate-drain charge	(see <a href="#">Figure 18</a> )		21		nC

1. Pulsed: pulse duration=300 $\mu\text{s}$ , duty cycle 1.5%

2.  $C_{oss eq}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$

**Table 7. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ $t_r$	Turn-on delay time Rise time	$V_{DD}=300\text{ V}$ , $I_D=3.5\text{ A}$ , $R_G=4.7\ \Omega$ , $V_{GS}=10\text{ V}$ (see <a href="#">Figure 19</a> )	-	19 17	-	ns ns
$t_{d(off)}$ $t_f$	Turn-off delay time Fall time	$V_{DD}=300\text{ V}$ , $I_D=3.5\text{ A}$ , $R_G=4.7\ \Omega$ , $V_{GS}=10\text{ V}$ (see <a href="#">Figure 19</a> )	-	43 15	-	ns ns

**Table 8. Gate-source zener diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	$I_{GS} = \pm 1\text{ mA}$ , $I_D=0$	30	-	-	V

The built-in back-to-back Zener diodes have been specifically designed to enhance not only the device's ESD capability, but also to make them capable of safely absorbing any voltage transients that may occasionally be applied from gate to source. In this respect, the Zener voltage is appropriate to achieve efficient and cost-effective protection of device integrity. The integrated Zener diodes thus eliminate the need for external components.

**Table 9. Source drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		7	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		28	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD}=7\text{ A}$ , $V_{GS}=0$	-		1.6	V
$t_{rr}$ $Q_{rr}$ $I_{RRM}$	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD}=7\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD}=30\text{ V}$ , $T_j=150\text{ }^\circ\text{C}$	-	480 3.5 14.5		ns $\mu\text{C}$ A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300  $\mu\text{s}$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for D<sup>2</sup>PAK and TO-220

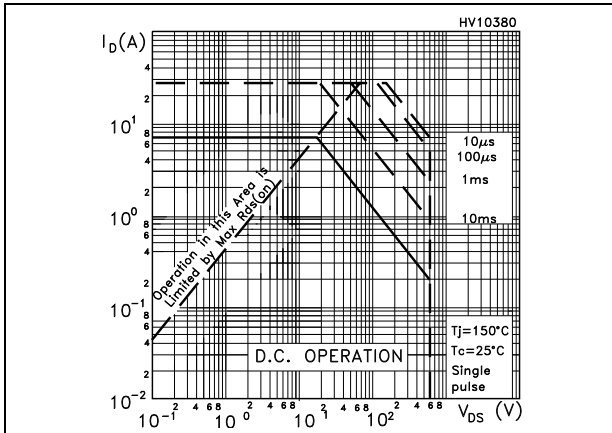


Figure 3. Thermal impedance for D<sup>2</sup>PAK and TO-220

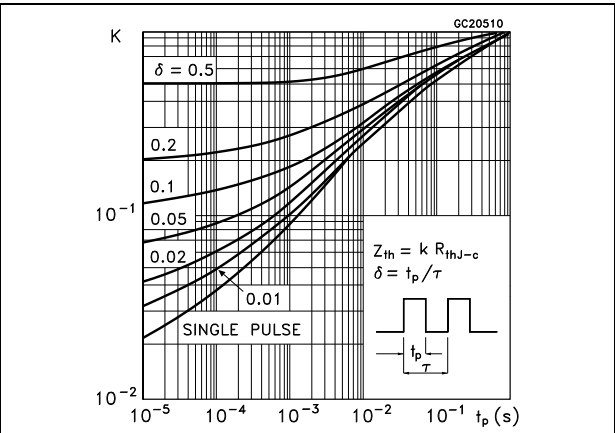


Figure 4. Safe operating area for TO-220FP

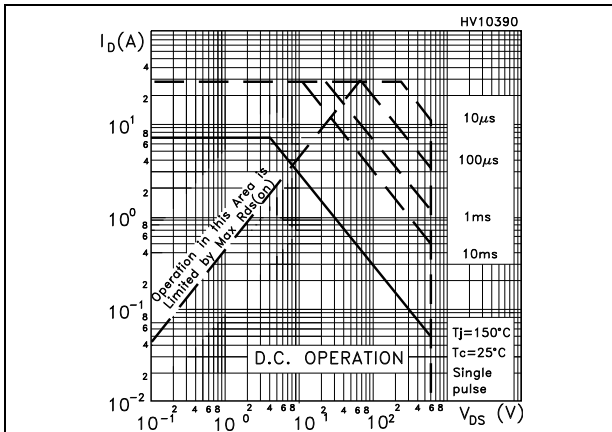


Figure 5. Thermal impedance for TO-220FP

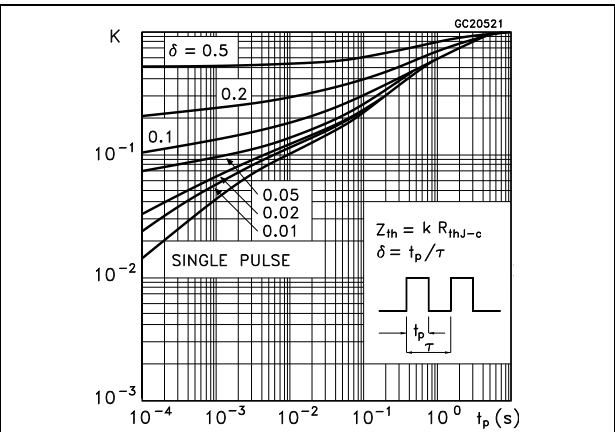


Figure 6. Output characteristics

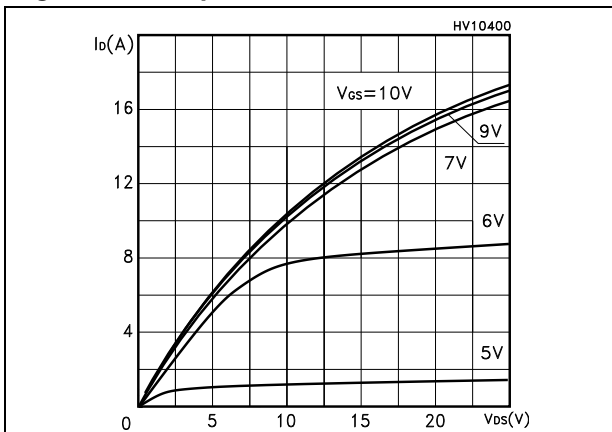


Figure 7. Transfer characteristics

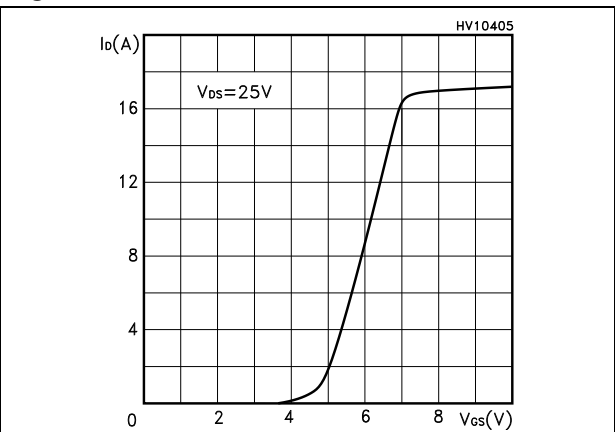


Figure 8. Transconductance

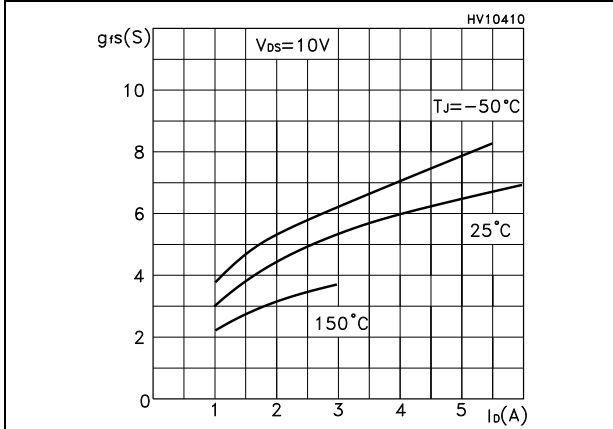


Figure 9. Static drain-source on-resistance

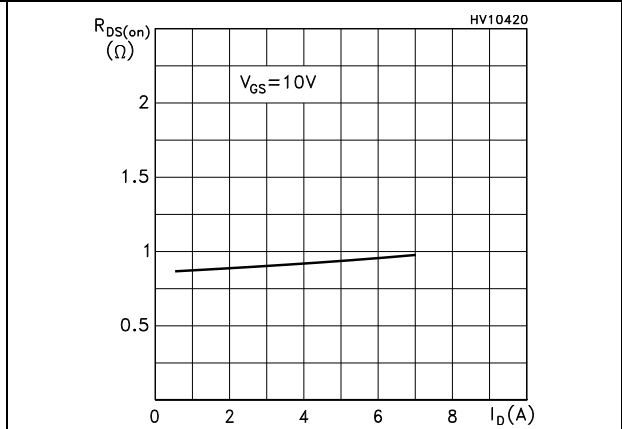


Figure 10. Gate charge vs gate-source voltage

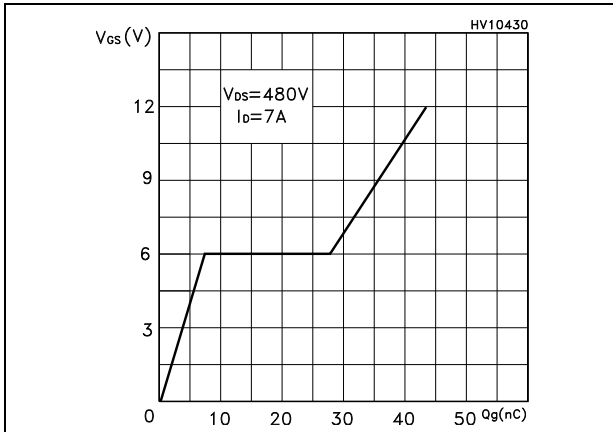


Figure 11. Capacitance variations

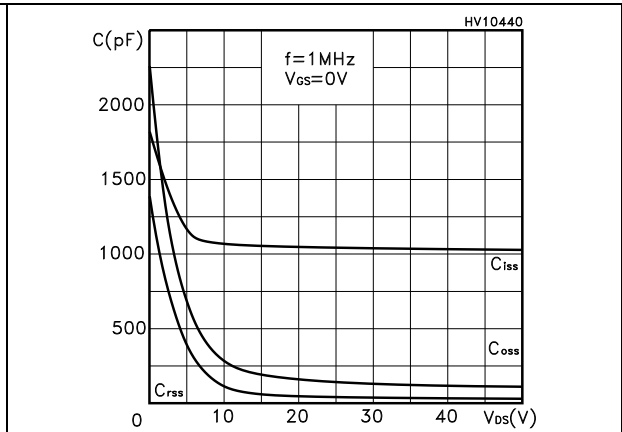


Figure 12. Normalized gate threshold voltage vs temperature

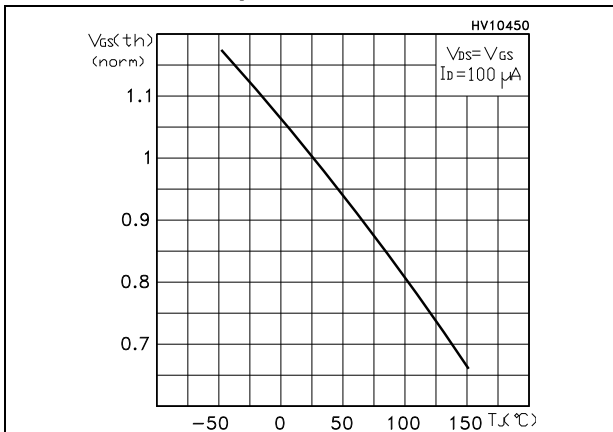


Figure 13. Normalized on-resistance vs temperature

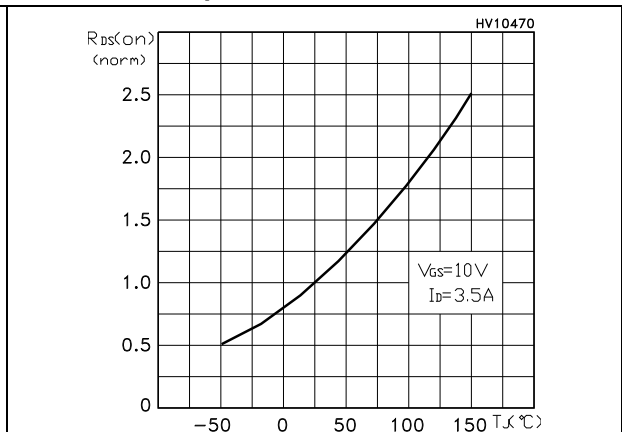




Figure 14. Source-drain diode forward characteristics

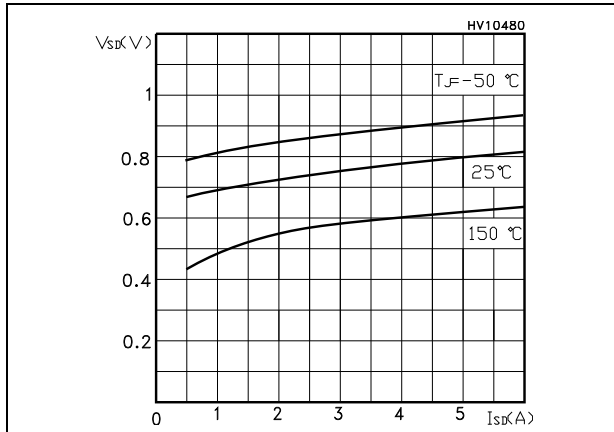


Figure 15. Normalized  $B_{VDSS}$  vs temperature

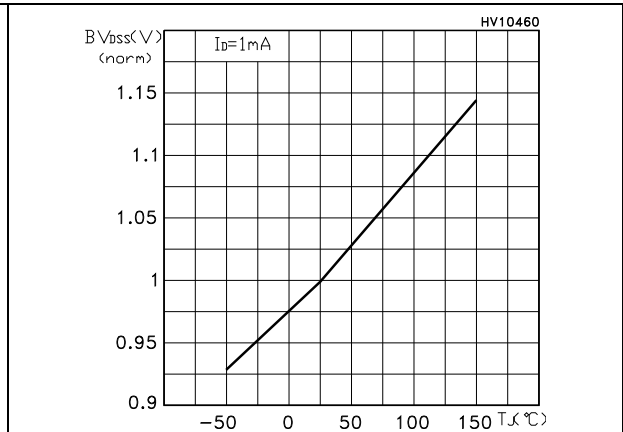
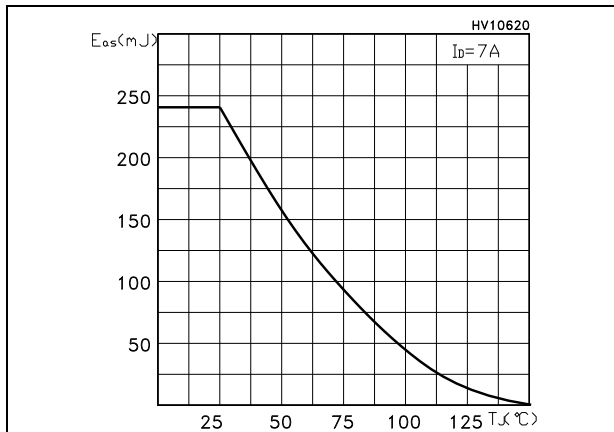
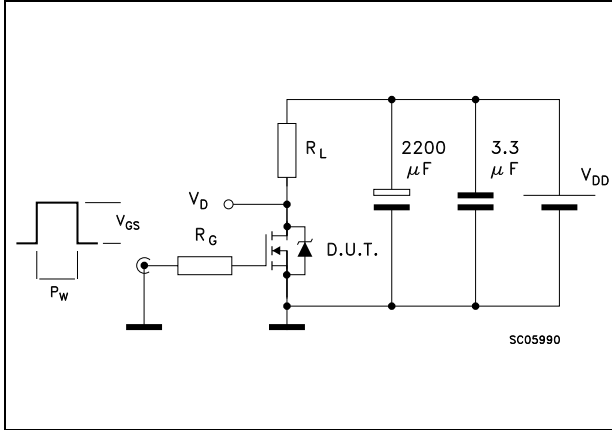


Figure 16. Maximum avalanche energy vs temperature

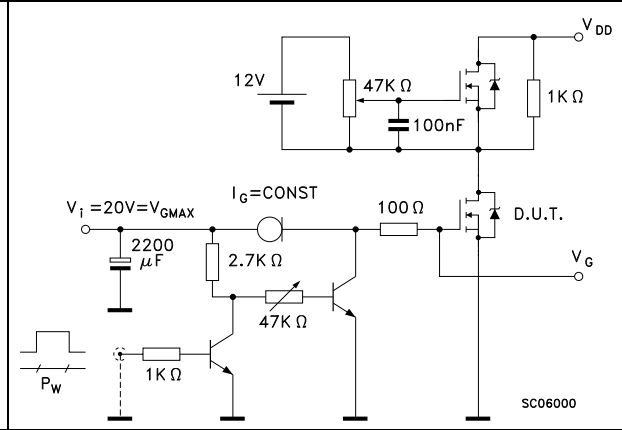


### 3 Test circuits

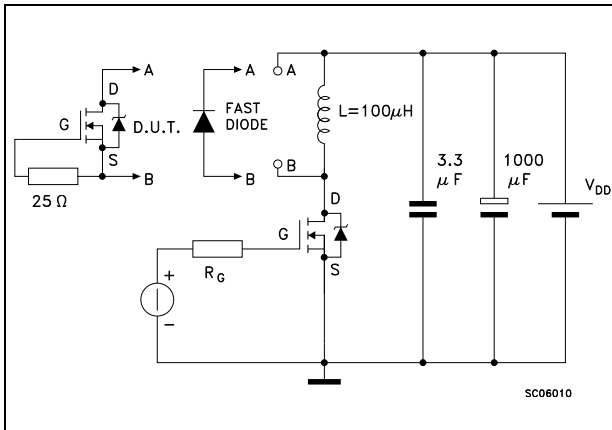
**Figure 17. Switching times test circuit for resistive load**



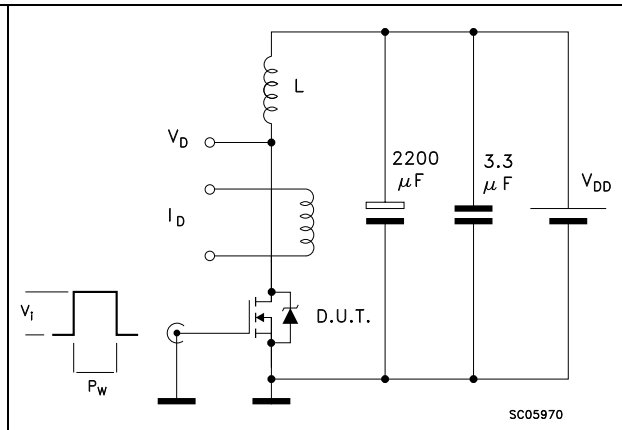
**Figure 18. Gate charge test circuit**



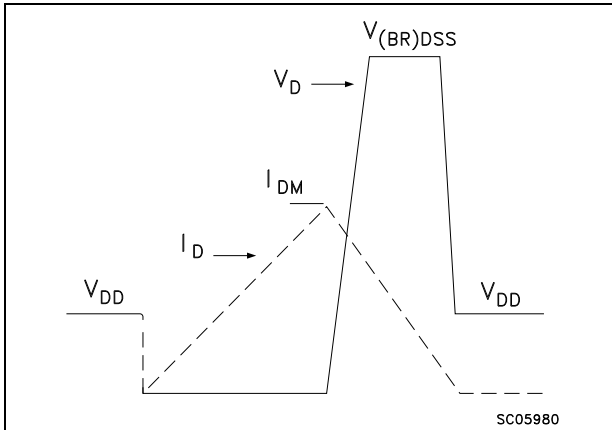
**Figure 19. Test circuit for inductive load switching and diode recovery times**



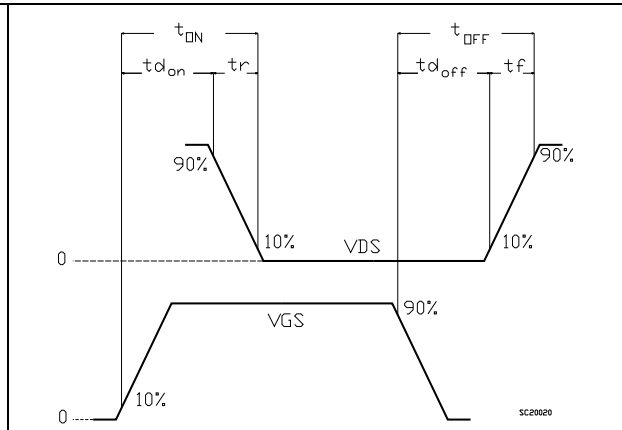
**Figure 20. Unclamped Inductive load test circuit**



**Figure 21. Unclamped inductive waveform**



**Figure 22. Switching time waveform**



## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK<sup>®</sup> is an ST trademark.

Table 10. D<sup>2</sup>PAK (TO-263) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50		
E	10		10.40
E1	8.50		
e		2.54	
e1	4.88		5.28
H	15		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.4	
V2	0°		8°

Figure 23. D<sup>2</sup>PAK (TO-263) drawing

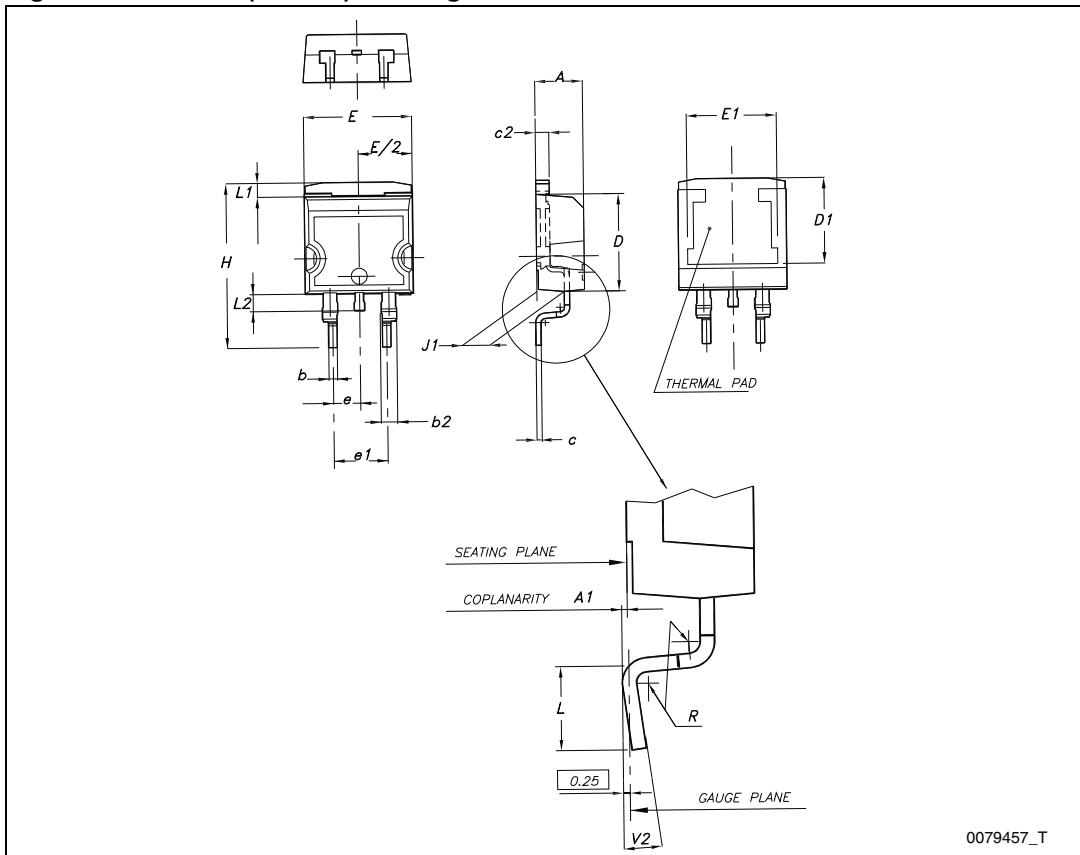
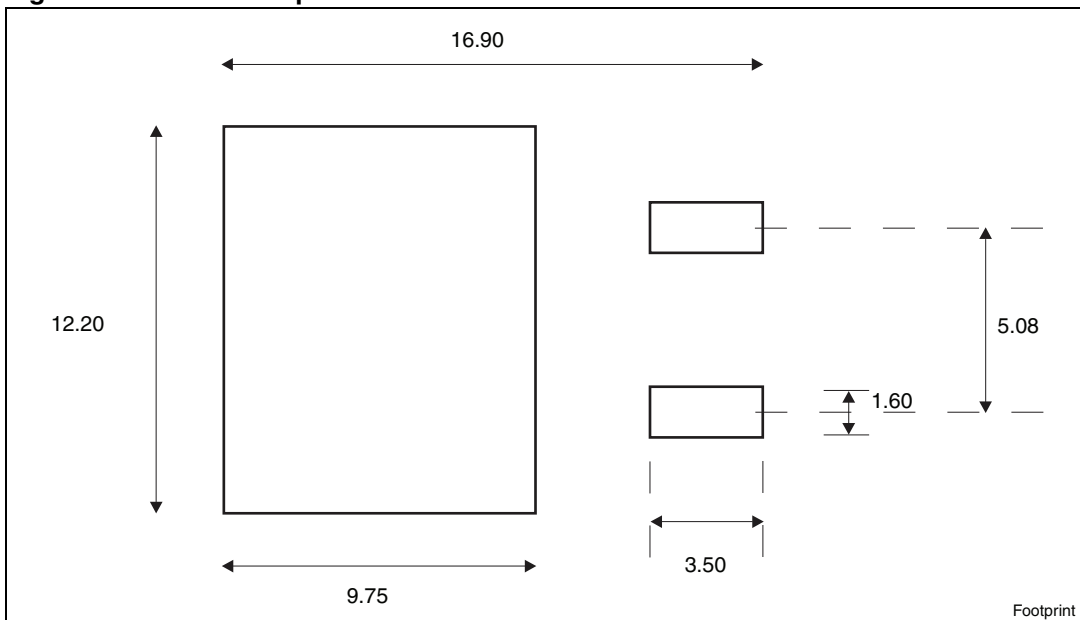


Figure 24. D<sup>2</sup>PAK footprint<sup>(a)</sup>



a. All dimension are in millimeters

Table 11. TO-220 type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
ØP	3.75		3.85
Q	2.65		2.95

Figure 25. TO-220 type A drawing

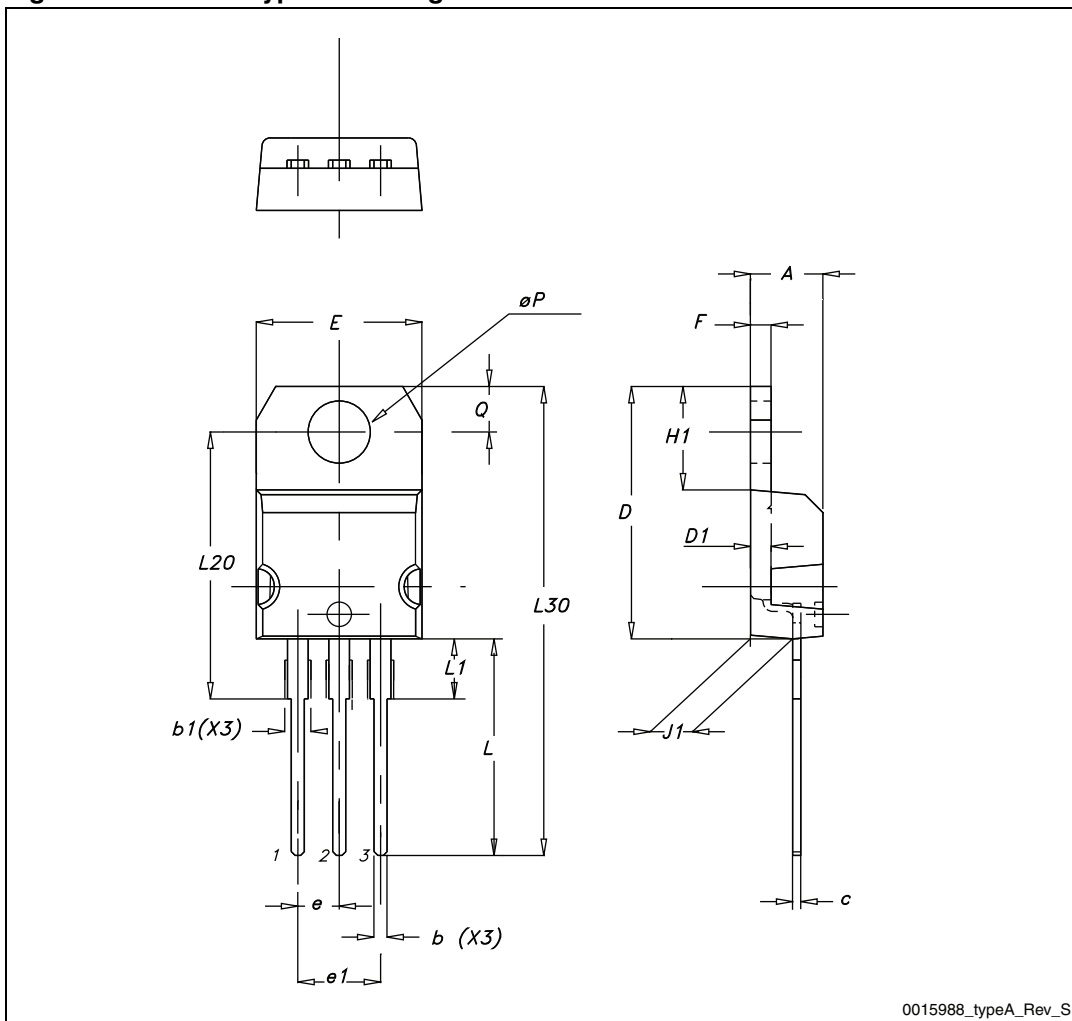
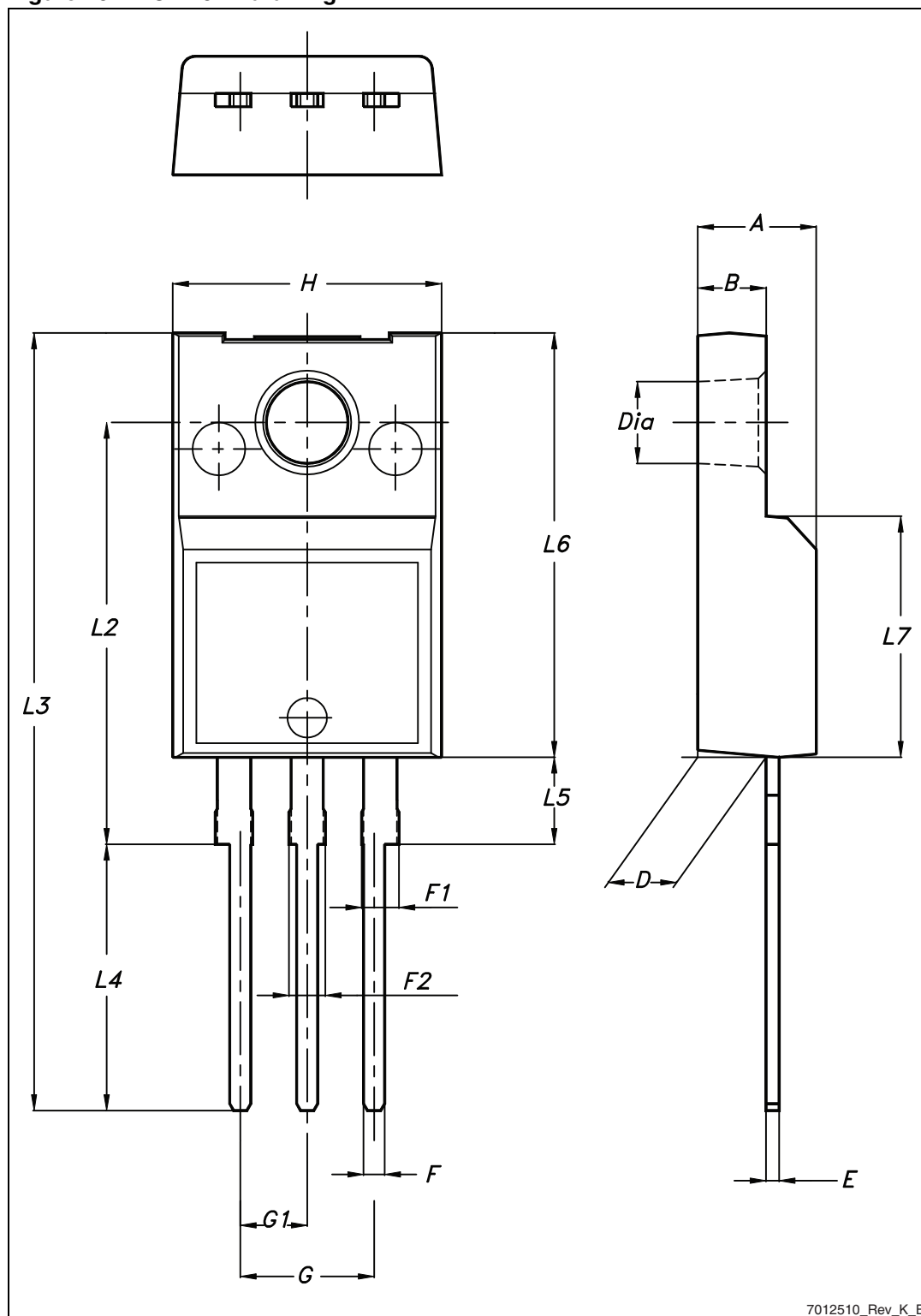


Table 12. TO-220FP mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2



Figure 26. TO-220FP drawing



7012510\_Rev\_K\_B

## 5 Revision history

Table 13. Document revision history

Date	Revision	Changes
31-Jan-2013	3	<ul style="list-style-type: none"><li>– Minor text changes</li><li>– The part number STB9NK60Z-1 has been moved to a separate datasheet</li><li>– Updated: <a href="#">Section 4: Package mechanical data</a>.</li></ul>

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