User's Manual

ISL78424EVAL3Z, ISL78434EVAL1Z

User's Manual: Evaluation Board

Automotive

Rev.01.00 Oct 2018

1. Overview

The ISL78424EVAL3Z and ISL78434EVAL1Z evaluation boards are designed to provide a quick and comprehensive method for evaluating the ISL78424 and ISL78434 100V 3A source, 4A sink half-bridge drivers for driving the gates of two NMOS FETs in a half-bridge configuration. Two N-channel MOSFETs are included on the evaluation board to allow for the evaluation of a half-bridge driven load such as a DC motor or a synchronous switching regulator.

The ISL784x4 family of FET drivers are offered in a 14 Ld HTSSOP package enhanced with a thermal EPAD. They operate from a supply voltage of 8V to 18V DC with the capability of driving a high-side N-channel FET in a 70V half-bridge configuration. A unique tri-level PWM input (ISL78424 only) allows control of both the high-side and low-side gate drivers with a single input. If the PWM pin is left floating, internal pull-up and pull-down resistors bias the PWM pin to the mid-level state. The mid-level state has both high-side and low-side sink drivers active to disable both MOSFETs. This is beneficial for multiphase DC/DC converters that require phase dropping or to implement asynchronous operation in a synchronous DC/DC converter. The ISL78434 has independent HI and LI driving pins that control their respective FET output driver signal.The ISL78434 features an input lockout protection to prevent both driver outputs going active high at the same time. The driver locks out any input logic from propagating to that driver output if the other input is already logic high.

The ISL78424 and ISL78434 feature separate pins for the sourcing and sinking driver outputs. The HO_H and HO_L are the high-side sourcing and sinking drivers, respectively. The LO_H and LO_L are the low-side sourcing and sinking drivers, respectively. Separate source and sink output pins allow optimizing the FET turn on/off times using gate drive limiting resistors

1.1 Key Features

- 3A source and 4A sink NMOS gate drivers
- Internal level shifter and bootstrap switch for gate driver on high-side FET
- Up to 70V high-side gate drive reference
- 8V to 18V bias supply operation
- Single PWM input for high-side and low-side gate driver with tri-level for turning off both drivers, (ISL78424 only)
- Independent HI and LI inputs for high-side and low-side gate driver, (ISL78434 only)
- Single resistor adjustable dead time from 35ns to 400ns, (ISL78424 only)

1.2 Specifications

These boards are optimized for the following operating conditions:

- V_{DD} supply = 8V to 18V
- V_{BRIDGE} supply input = 12V to 70V
- PWM switching frequency 10kHz to 1MHz
- Preset half-bridge dead time: 165ns with RDT = 10kΩ, (Adaptive dead time + programmable dead time)
- Peak gate drive current: 3A source and 4A sink

1.3 Ordering Information

Part Number	Description
ISL78424EVAL3Z	ISL78424AVEZ evaluation board
ISL78434EVAL1Z	ISL78434AVEZ evaluation board

1.4 Related Literature

For a full list of related documents, visit our website:

- ISL78424, ISL78434, ISL78444, ISL78224, ISL78226 product pages

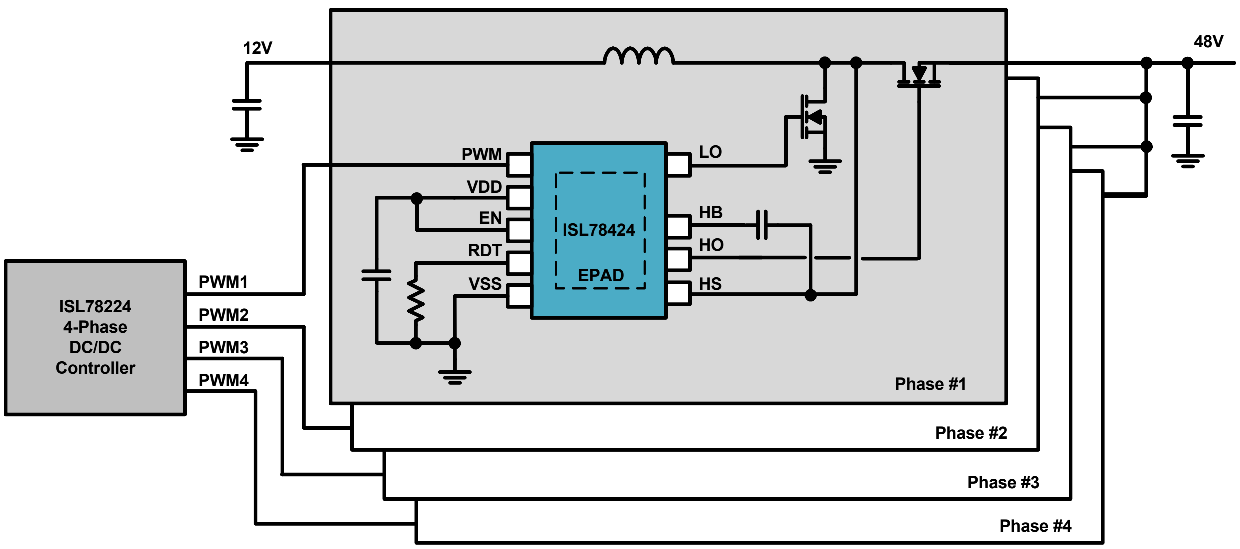

Figure 1. ISL78424EVAL3Z Block Diagram

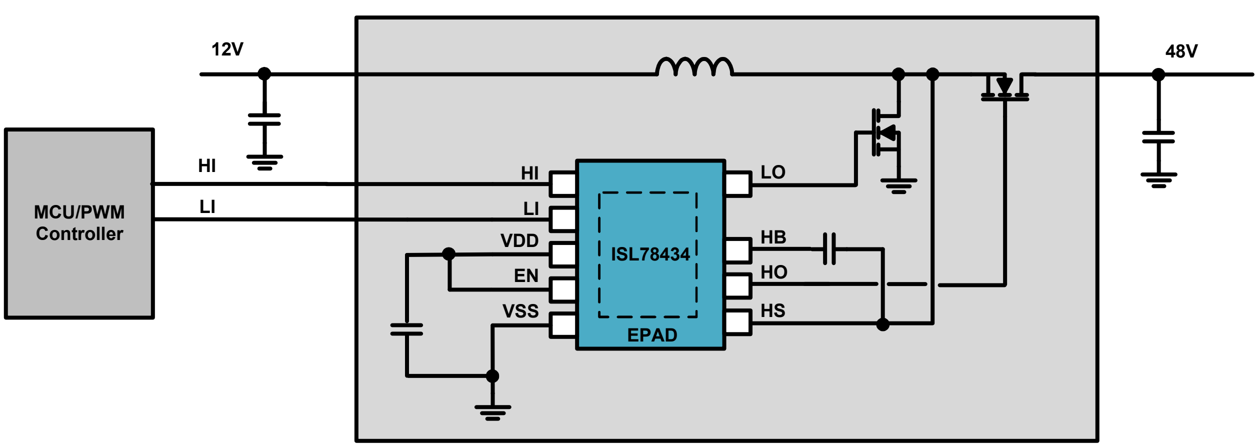

Figure 2. ISL78434EVAL1Z Block Diagram

2. Functional Description

The ISL78424EVAL3Z and ISL78434EVAL1Z are designed to provide a comprehensive and versatile platform for a user to evaluate the functionality and prototype an application of the ISL784x4 FET drivers. These evaluation boards provide an open loop type of application for either synchronous buck or boost applications where the output voltage is controlled using the duty cycle of the PWM pin for the ISL78424EVAL3Z, and by the ratio of the HI and LI signals for the ISL78434EVAL1Z (Note the ISL78434 has protections that prevent the HO and LO from both being in "High" logic state if both of these signals are asserted high).

2.1 Operating Range

The ISL784x4 FET drivers offer voltage ratings that are ideal for 48V automotive systems. The switching node (HS) can operate at voltages up to 70V, and can tolerate infrequent transient voltages up to 86V. The bootstrap (HB) node, supply to the high-side driver, can operate at a voltage of up to 86V, and can handle infrequent transients up to 100V. The logic pins of the ISL784x4 driver family are tolerant up to maximum V_{DD} of 18V. The gate drive of the high and low-side drivers is provided by V_{DD}.

2.2 Recommended Equipment

- 8V to 18V power supply with at least 2A source current capability
- 0V to 70V power supply to bias the half bridge
- 100kHz to 1MHz square wave generator with 0V to 5V logic levels output
- Minimum 4-channel oscilloscope to verify PWM, HO, LO, and HS signals
- Load such as DC motor, or electronic load (optional)

2.3 Quick Start Guide

(1) The dead time of the HO and LO signal is set to 110ns with a 10kΩ resistor from the RDT pin to GND. To change the dead time, replace the resistor at R10 with the value corresponding to the desired dead time.

(2) Ensure that the enable switch (SW_1) is set to the off position.

(3) Connect the power supply capable of 48V and 10A to VBAT_48V terminals {J_{19}(+) and J_{20}(-)}. Turn on supply to 48V.

(4) Connect 8V to 18V supply to the VDD terminals on board {J_2(+) and J_3(-). Turn on supply to 12V.

(5) For ISL78424: Connect a 0V to 5V (PWM pin capable of voltage up to V_{DD}) <500kHz square wave signal to PWM BNC connector J_{13}, shunt jumper J_{10} not needed.
For ISL78434: Apply the HI signal to the BNC connector J_9, the LI signal at the J_{13} BNC connector, and connect the shunt jumper to J_{10} (HI/LI pins capable of voltage up to V_{DD}).

(6) Toggle enable switch (SW_1) to the on position.

(7) Verify HO and LO outputs are switching. LO switches between GND and VDD (12V for this example) phase inverted from PWM. HO switches between GND and V_{HB} + V_{BRIDGE} (48V in this example) in phase with PWM.

2.4 Dead Time Measurement

(1) Ensure that there is no bandwidth limitation on any of the channels of the oscilloscope and they are set up to 5V/div.

(2) Connect a probe to the LO signal on J_1 (2 pin header, GND(-) towards top of board, LO(+) signal towards bottom of board.

(3) Connect a probe to the HO signal on J_6 (2 pin header, GND(-) towards top of board, HO(+) signal towards bottom of board.

(4) Connect a probe to the HS signal on J_5 (2 pin header, GND(-) towards left of board, HS(+) signal towards right of board.

(5) Add a math measurement to the scope and subtract the HO-HS signals.

(6) Dead time measurement t_{DTHL} = time from 50% level of (HO-HS) signal falling to 50% level of LO signal rising. With R_{DT} = 10kΩ, default configuration of board, the t_{DTHL} = 180ns (adaptive dead time (t_{ADTC}) + resistor programmed dead time (t_{DTHL})).

(7) Dead time measurement t_{DTLH} = time from 50% level of LO signal falling to 50% level of (HO-HS) signal rising. With R_{DT} = 10kΩ, default configuration of board, the t_{DTLH} = 180ns (adaptive dead time (t_{ADTC}) + resistor programmed dead time (t_{DTHL})).

3. PCB Layout Guidelines

(1) For best thermal performance, connect the driver EPAD to a low thermal impedance ground plane. Use as many vias as possible to connect the top layer Printed Circuit Board (PCB) thermal land to ground planes on other PCB layers. For best electrical performance, connect the VSS and AGND pins together through the EPAD to maintain a low impedance connection between the two pins.

(2) When adjustable dead time is used (ISL78424 only), connect the resistor to the RDT pin and GND plane close to the IC to minimize ground noise from disrupting the timing performance.

(3) Place the VDD decoupling capacitors and bootstrap capacitors close to the VDD-VSS and HB-HS pins, respectively. Use decoupling capacitors to reduce the influence of parasitic inductors. To be effective, these capacitors must also have the shortest possible lead lengths. If vias are used, connect several paralleled vias to reduce the inductance.

(4) Keep power loops as short as possible by paralleling the source and return traces.

(5) Adding resistance might be necessary to dampen resonating parasitic circuits. In PCB designs with long leads on the LO and HO outputs, add series gate resistors on the bridge FETs to dampen the oscillations.

(6) Large power components (power FETs, electrolytic capacitors, power resistors, etc.) have internal parasitic inductance that cannot be eliminated. This must be accounted for in the PCB layout and circuit design.

(7) If you simulate your circuits, consider including parasitic components.

3.1 ISL78424EVAL3Z Evaluation Board

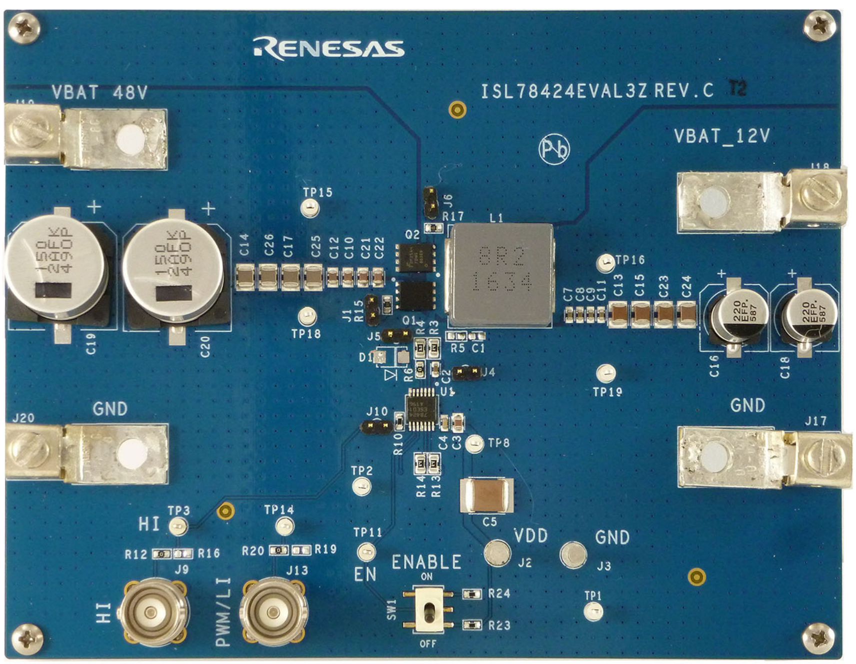

Figure 3. ISL78424EVAL3Z Evaluation Board

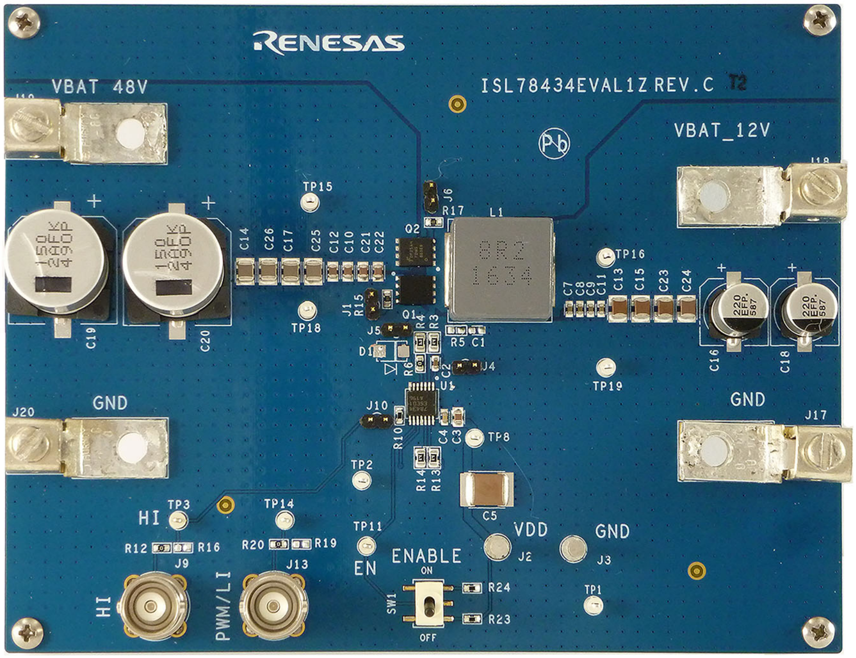

Figure 4. ISL78434EVAL1Z Evaluation Board

3.2 ISL78424EVAL3Z Circuit Schematic

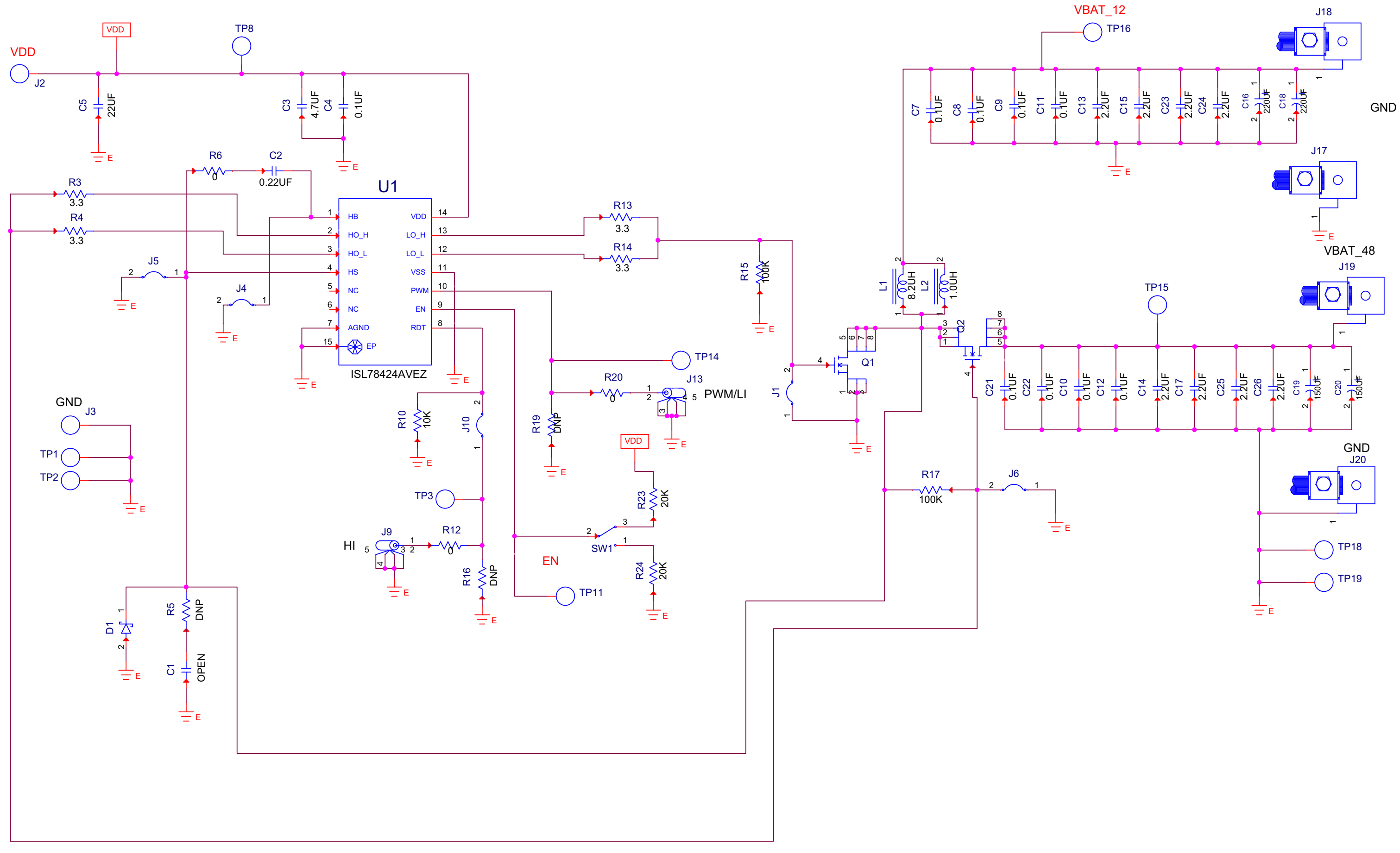

Figure 5. ISL78424EVAL3Z Schematic

3.3 ISL78434EVAL1Z Circuit Schematic

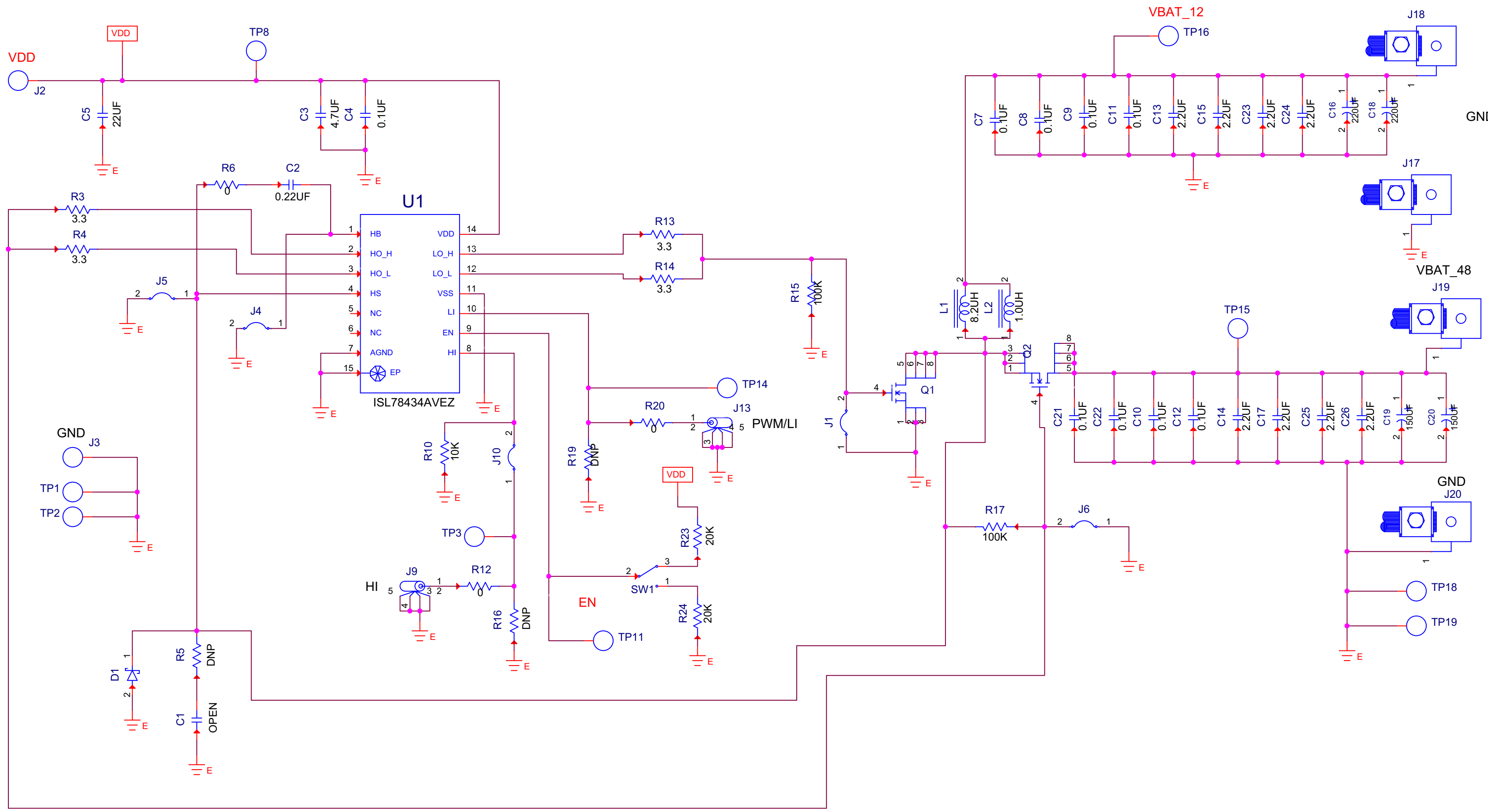

Figure 6. ISL78434EVAL1Z Schematic

3.4 Bill of Materials: ISL78424EVAL3Z and ISL78434EVAL1Z

Qty	Reference Designator	Description	Manufacturer	Manufacturer Part Number
1	U1	IC-4A, 86V, HALF-BRIDGE DRIVER, 14P, HTSSOP, ROHS	Renesas	ISL78424AVEZ for ISL78424EVAL3Z ISL78434AVEZ for ISL78434EVAL1Z
1	C5	CAPACITOR, SMD, 2220, 22µF, 25V, 20%, X7R, ROHS	TDK	C5750X7R1E226M
1	C3	CAP-AEC-Q200, SMD, 0805, 4.7µF, 35V, 10%, X7R, ROHS	TDK	CGA4J1X7R1V475K125AE
4	C10, C12, C21, C22	CAP-AEC-Q200, SMD, 0805, 0.1µF, 100V, 10%, X7R, ROHS	TDK	CGA4J2X7R2A104K125AA
2	C19, C20	CAP, SMD, 17X17, 150µF, 100V, 20%, ALUM.ELEC., ROHS	Panasonic	EEV-FK2A151M
4	C7-C9, C11	CAP, SMD, 0603, 0.1µF, 25V, 10%, X7R, ROHS	Yageo	CC0603KRX7R8BB104
1	C4	CAP, SMD, 0603, 0.1µF, 25V, +80 -20%, Y5V, ROHS	Murata	GRM39Y5V104Z025
1	C2	CAP, SMD, 0603, 0.22µF, 50V, 10%, X7R, ROHS	Murata	GCM188R71H224KA64D
4	C14, C17, C25, C26	CAP, SMD, 1210, 2.2µF, 100V, 10%, X7R, ROHS	Murata	GRM32ER72A225KA35L
4	C13, C15, C23, C24	CAP, SMD, 1210, 2.2µF, 50V, 10%, X7R, ROHS	TDK	C3225X7R1H225K
2	C16, C18	CAP, SMD, 8x10.2mm, 220µF, 20%, 25V, 80mΩ, ALUM.ELEC., ROHS	Panasonic	EEE-FP1E221AP
4	L1	COIL-INDUCTOR, AEC-Q200, SMD, 16.9x16.9, 8.2µH, 20%, 18A, ROHS	Bourns	SRP1770TA-8R2M
2	Q1, Q2	TRANSISTOR-MOS, N-CHANNEL, 8P, PWR56, 80V, 80A, ROHS	Fairchild	FDMS86368_F085
3	R6, R12, R20	RES, SMD, 0603, 0Ω, 1/10W, TF, ROHS	Venkel	CR0603-10W-000T
1	R10	RES, SMD, 0603, 10k, 1/10W, 1%, TF, ROHS	Venkel	CR0603-10W-1002FT
2	R15, R17	RES, SMD, 0603, 100k, 1/10W, 1%, TF, ROHS	Venkel	CR0603-10W-1003FT
2	R23, R24	RES, SMD, 0603, 20k, 1/10W, 1%, TF, ROHS	Venkel	CR0603-10W-2002FT
4	R3, R4, R13, R14	RES, SMD, 0805, 3.3Ω, 1/8W, 1%, TF, ROHS	Panasonic	ERJ-6RQF3R3V
1	SW1	SWITCH-TOGGLE, SMD, 6PIN, SPDT, 3POS, ON-OFF-ON, ROHS	ITT Industries/ C&K Division	GT13MSCBE
2	J2, J3	CONN-TURRET, TERMINAL POST, TH, ROHS	Keystone	1514-2
2	J9, J13	CONN-BNC, RECEPTACLE, TH, 4 POST, 50Ω, SILVERCONTACT, ROHS	Amphenol	31-5329-51RFX
10	TP1-3, TP8, TP11, TP14-TP16, TP18, TP19	CONN-MINI TEST POINT, VERTICAL, WHITE, ROHS	Keystone	5002
5	J1, J4-J6, J10	CONN-HEADER, 1x2, BRKAWY 1x36, 2.54mm, ROHS	Berg/FCI	68000-236HLF
	D1, R5, R16, R19, C1	DNP		

3.5 Board Layout

3.5.1 ISL78424EVAL3Z Layout

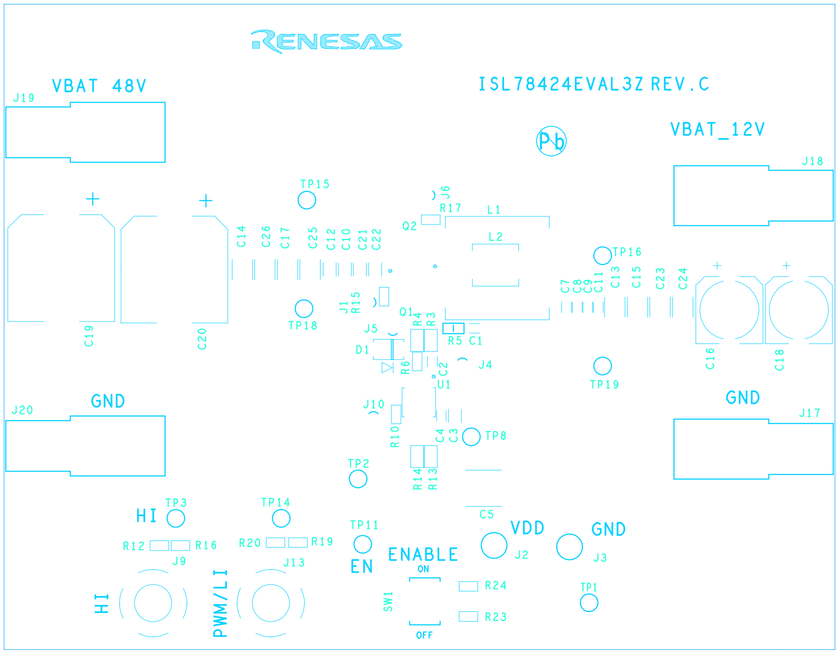

Figure 7. Silkscreen Top Layer

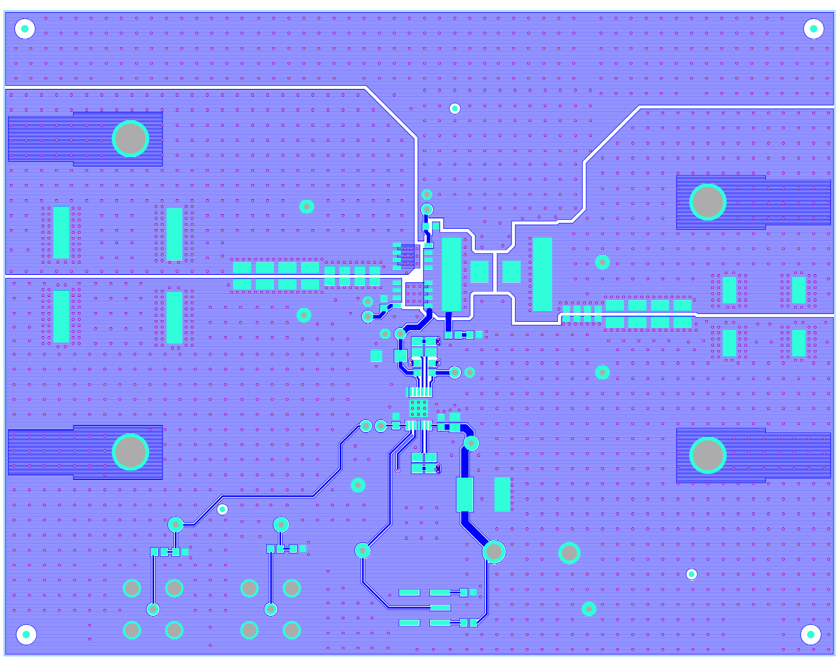

Figure 8. Layer 1

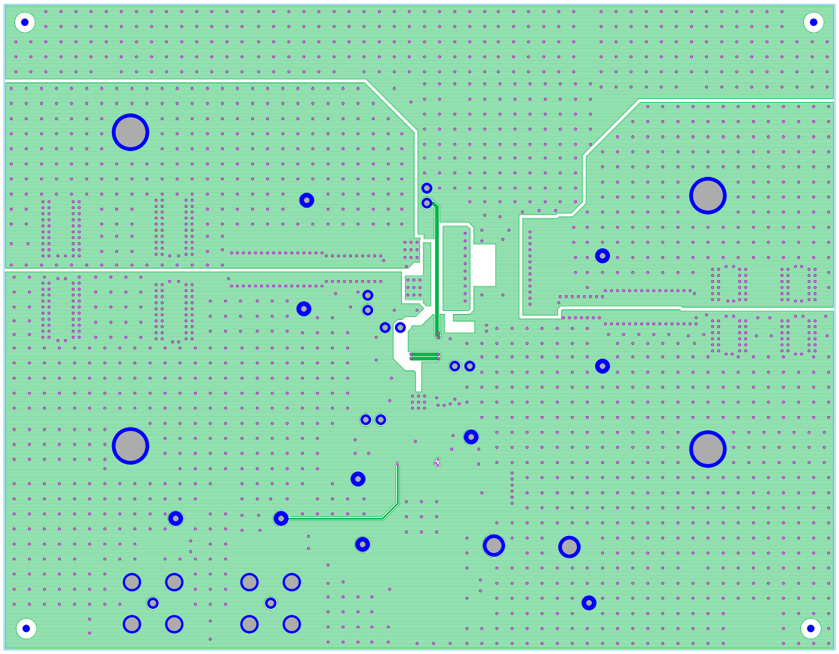

Figure 9. Layer 2

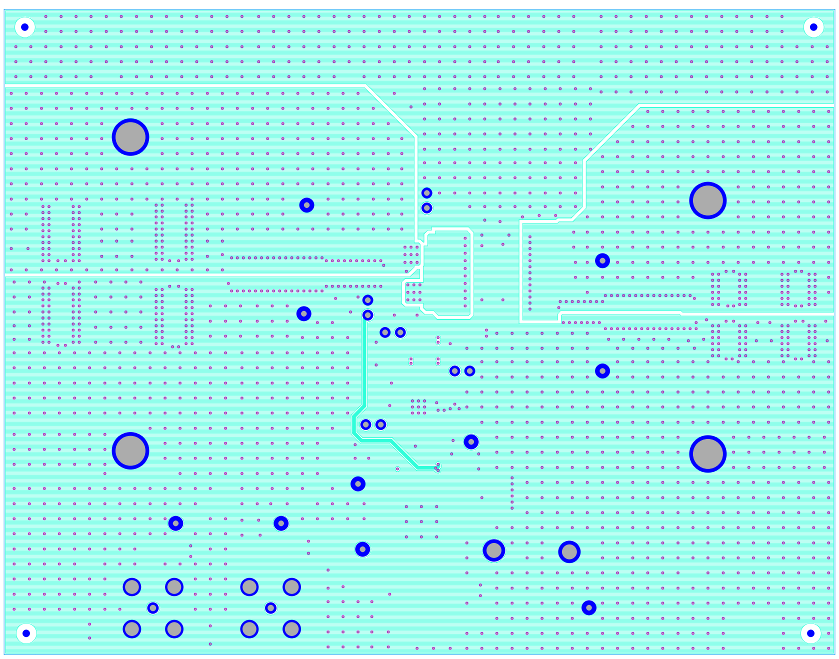

Figure 10. Layer 3

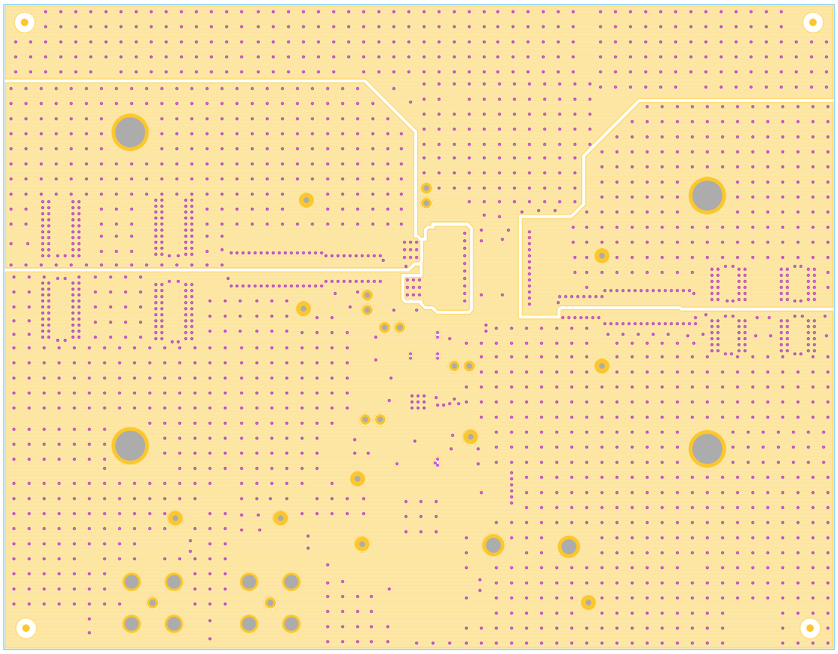

Figure 11. Layer 4

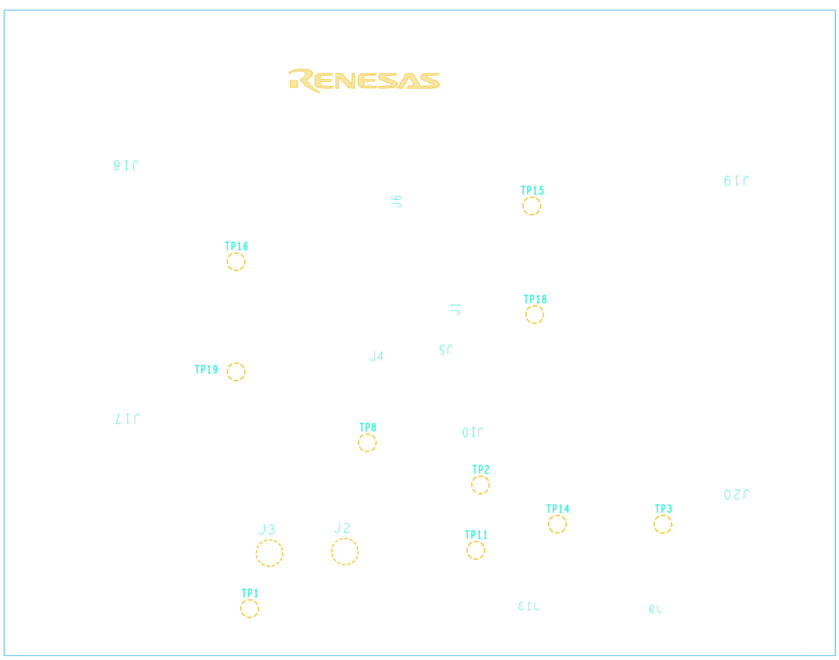

Figure 12. Silkscreen Bottom Layer

3.5.2 ISL78434EVAL1Z Layout

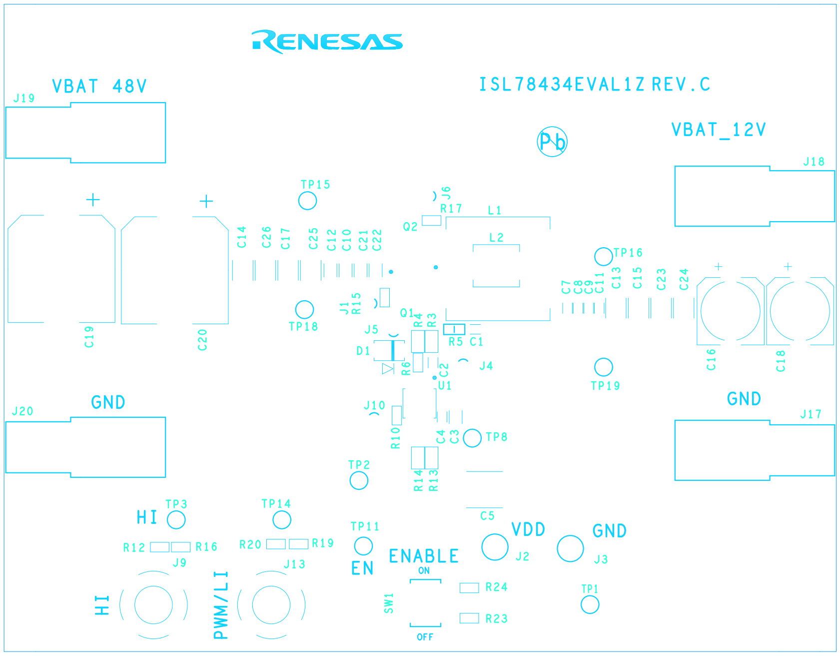

Figure 13. Silkscreen Top Layer

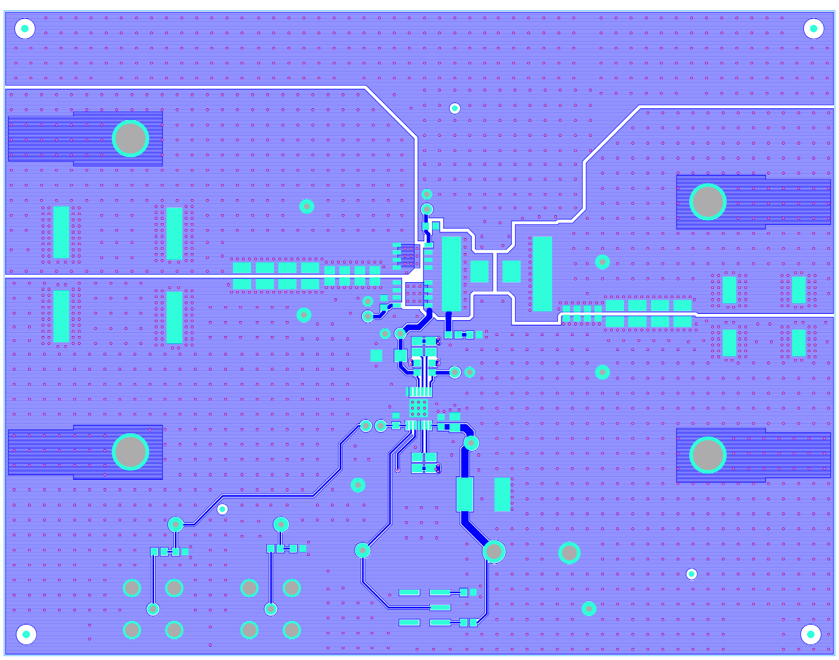

Figure 14. Layer 1

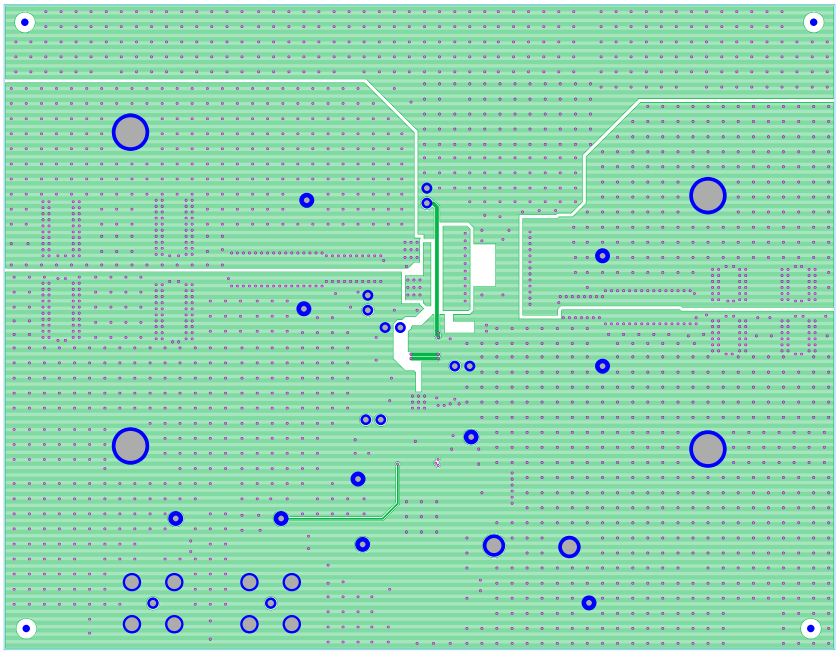

Figure 15. Layer 2

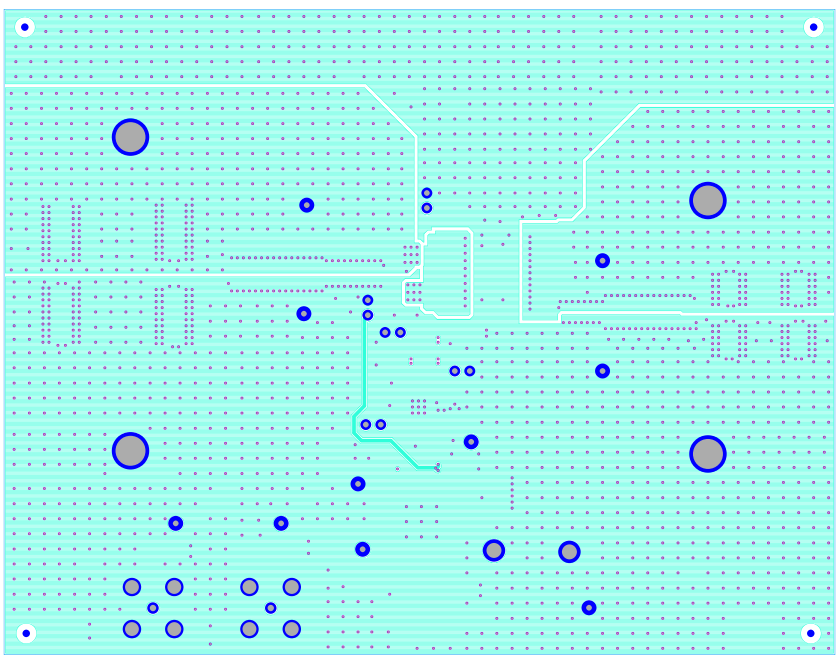

Figure 16. Layer 3

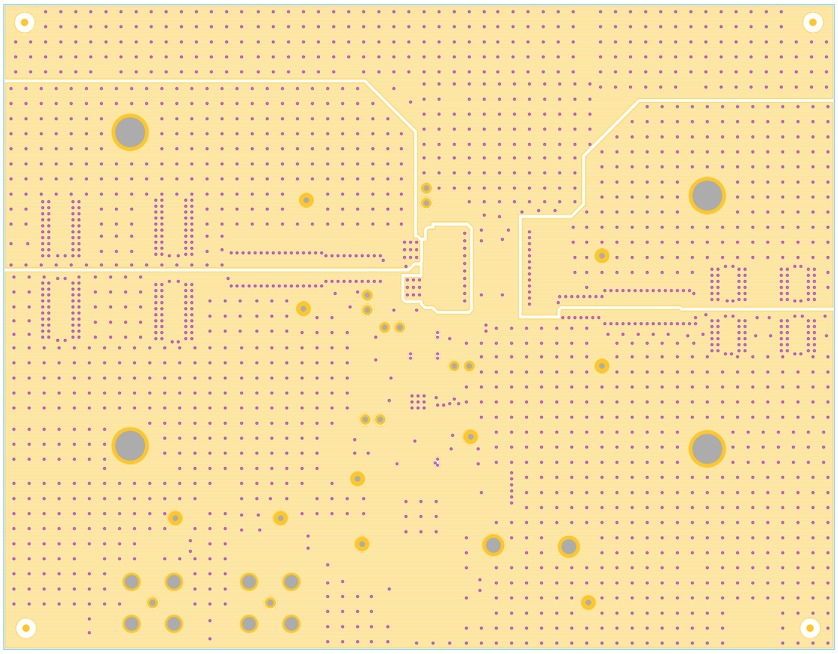

Figure 17. Layer 4

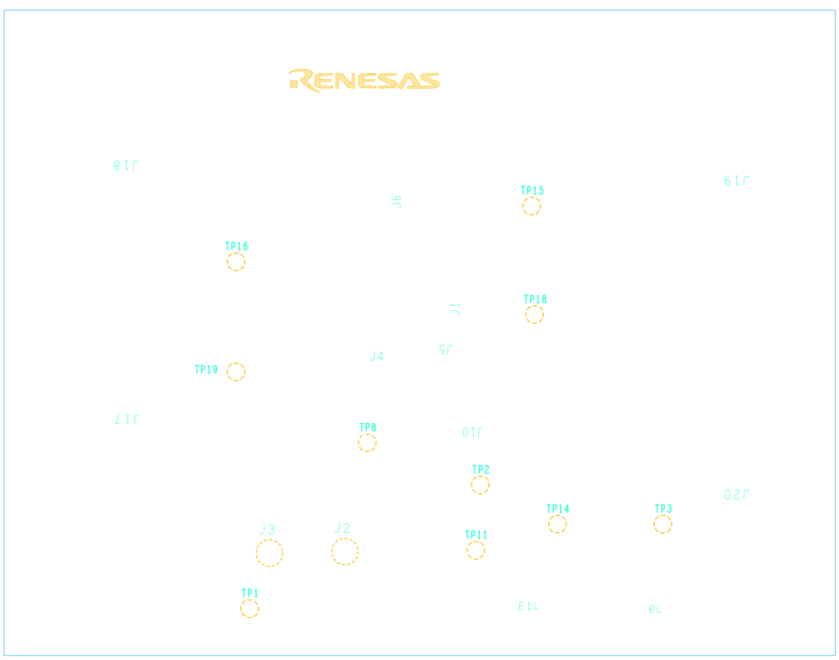

Figure 18. Silkscreen Bottom Layer

4. Typical Performance Curves

Unless noted: V_{DD} = 12V, V_{BRIDGE} = 48V, PWM = 100kHz square wave, 0V to 5V, 25% duty cycle, T_A = +25°C

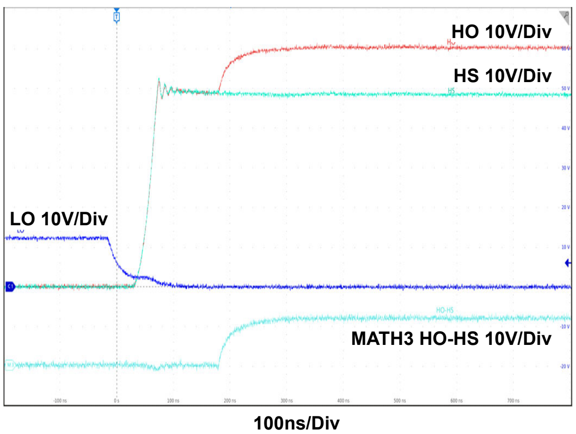

Figure 19. ISL78424EVAL3Z Dead Time LO Falling to HO Rising

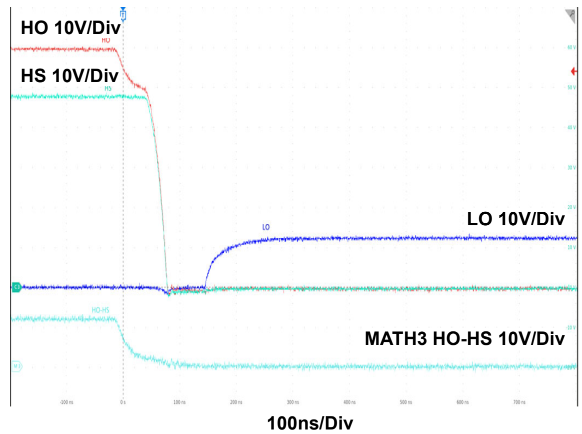

Figure 20. ISL78424EVAL3Z Dead Time HO Falling to LO Rising

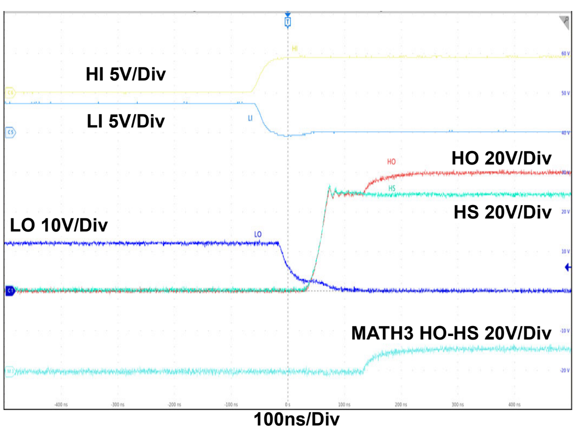

Figure 21. ISL78434EVAL1Z Dead Time LO Falling to HO Rising

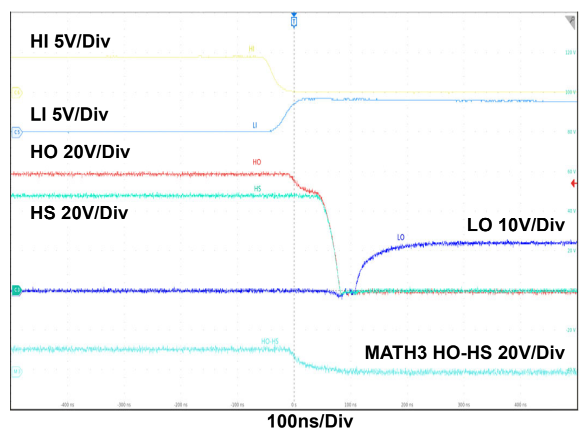

Figure 22. ISL78434EVAL1Z Dead Time HO Falling to LO Rising

5. Revision History

Rev.	Date	Description
01.00	Oct 23, 2018	Initial release

SALES OFFICES Renesas Electronics Corporation http://www.renesas.com

Refer to "http://www.renesas.com/" for the latest and detailed information.

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Colophon 7.2

ISL78424EVAL3Z,
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