DESCRIPTION

PT6311B is a Vacuum Fluorescent Display (VFD) Controller driven on a 1/8 to 1/16 duty factor housed in 52-pin plastic LQFP Package. Twelve segment output lines, 8 grid output lines, 8 segment/grid output drive lines, one display memory, control circuit, key scan circuit are all incorporated into a single chip to build a highly reliable peripheral device for a single chip micro computer. Serial data is fed to PT6311B via a three-line serial interface.
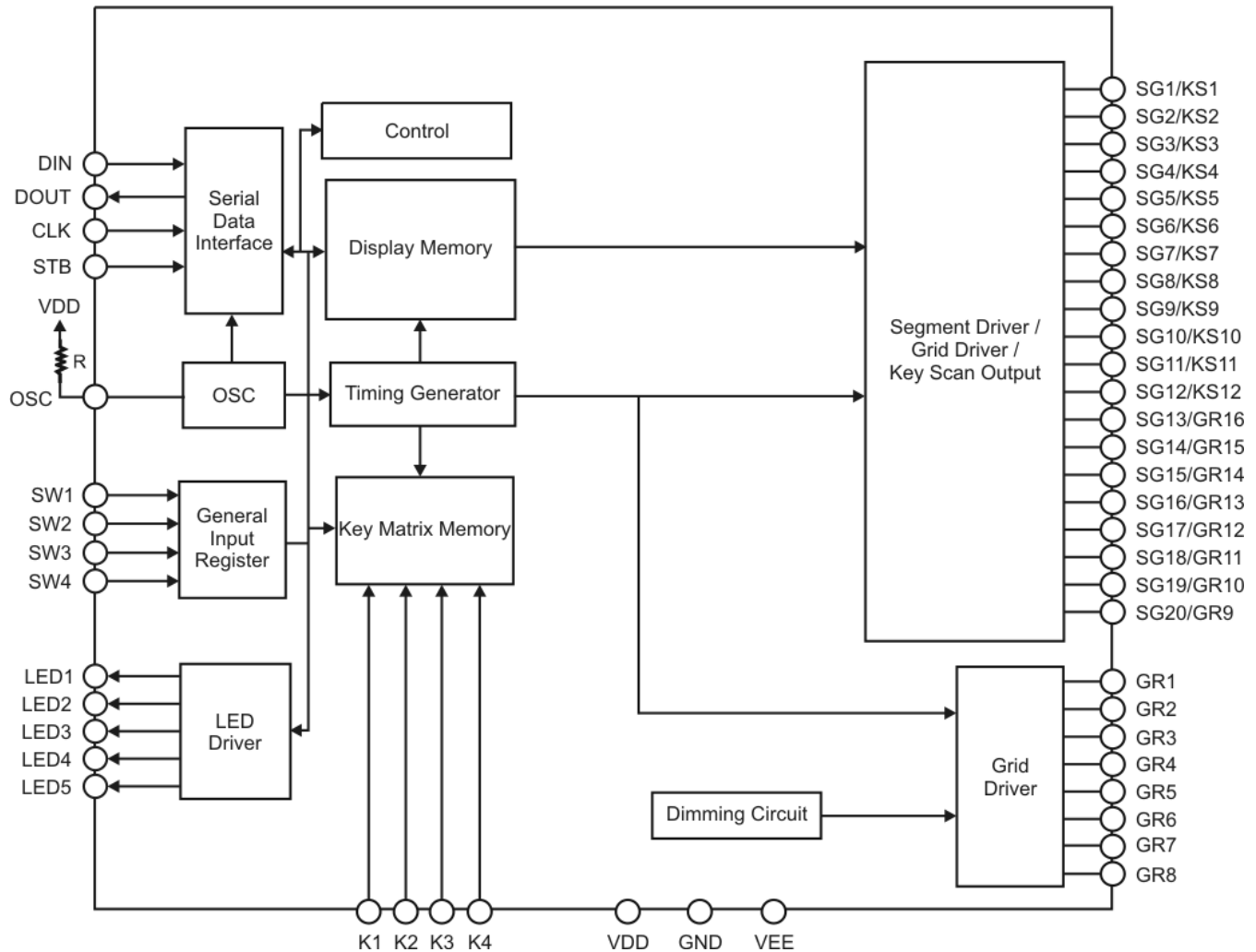
APPLICATION

- Microcomputer Peripheral Devices

FEATURES

- CMOS Technology
- Low Power Consumption
- Key Scanning (12 x 4 matrix)
- Multiple Display Modes: (12 segments, 16 digits to 20 segments, 8 digits)
- 8-Step Dimming Circuitry
- LED Ports Provide (5 channels, 20mA max.)
- 4- Bits General Purpose Input Ports Provided
- Serial Interface for Clock, Data Input, Data Output, Strobe Pins
- No External Resistors Needed for Driver Outputs
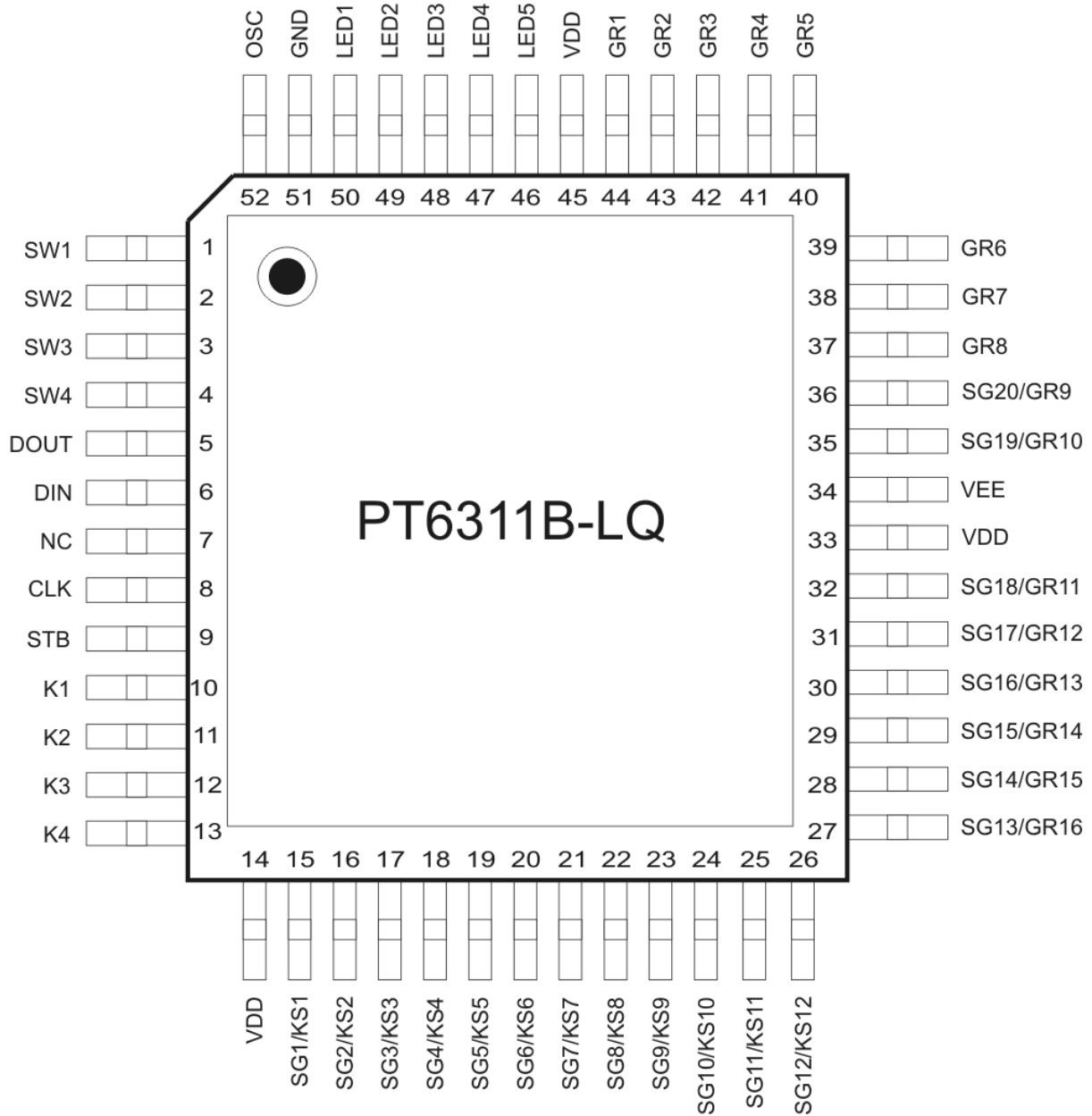- Available in 52 pins LQFP

BLOCK DIAGRAM

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12-GRID X 16-SEGMENT VFD APPLICATION CIRCUIT
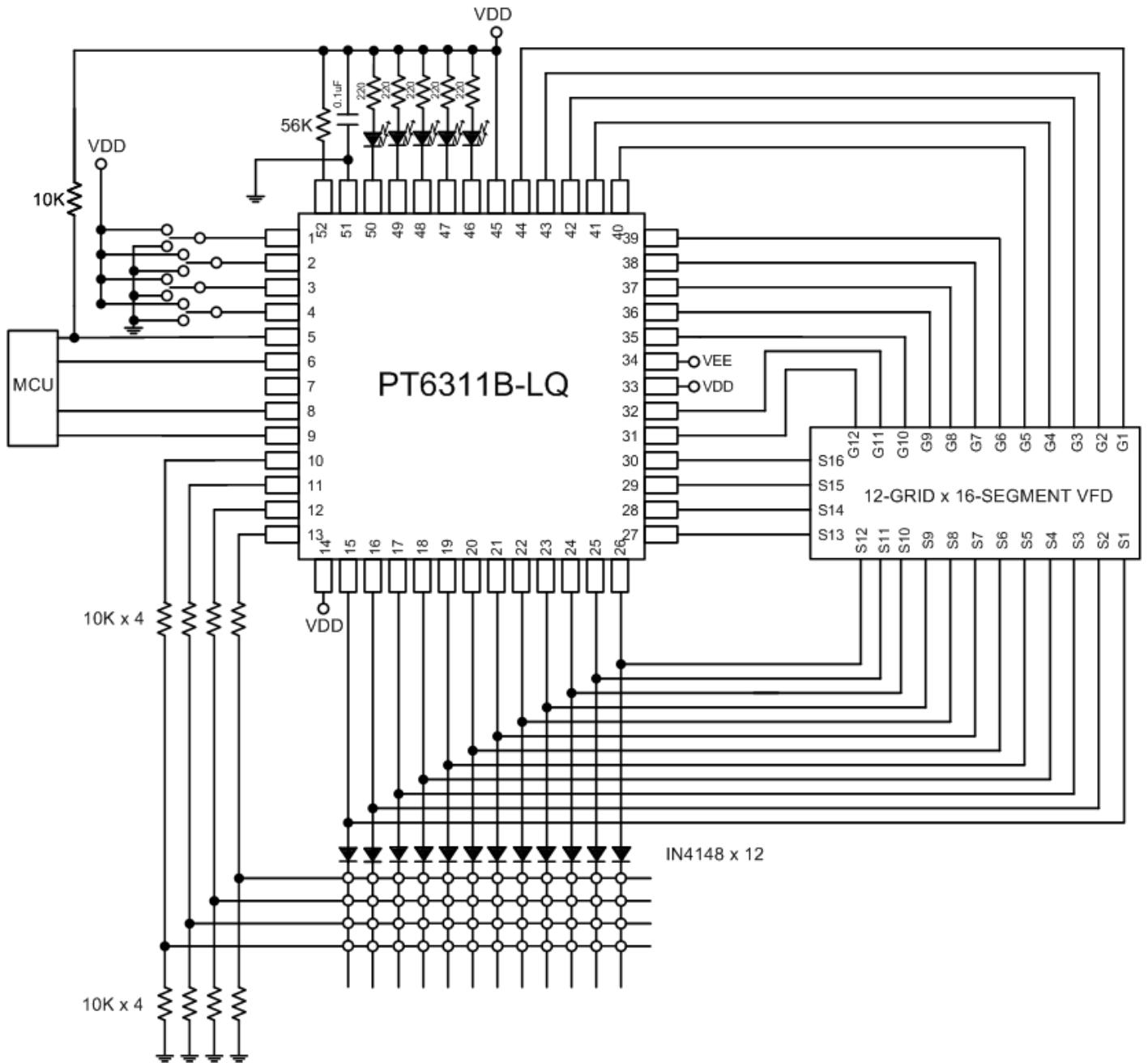
ORDER INFORMATION

Valid Part Number	Package Type	Top Code
PT6311B-LQ	52 Pins, LQFP	PT6311B-LQ

PIN CONFIGURATION

Top pins (left to right, 52–40): OSC, GND, LED1, LED2, LED3, LED4, LED5, VDD, GR1, GR2, GR3, GR4, GR5

Left pins (top to bottom, 1–13): SW1, SW2, SW3, SW4, DOUT, DIN, NC, CLK, STB, K1, K2, K3, K4

Right pins (top to bottom, 39–27): GR6, GR7, GR8, SG20/GR9, SG19/GR10, VEE, VDD, SG18/GR11, SG17/GR12, SG16/GR13, SG15/GR14, SG14/GR15, SG13/GR16

Bottom pins (left to right, 14–26): VDD, SG1/KS1, SG2/KS2, SG3/KS3, SG4/KS4, SG5/KS5, SG6/KS6, SG7/KS7, SG8/KS8, SG9/KS9, SG10/KS10, SG11/KS11, SG12/KS12

Center: PT6311B-LQ

PIN DESCRIPTION

Pin Name	I/O	Description	Pin No.
SW1 to SW4	I	General Purpose Input Pins	1 to 4
DOUT	O	Data Output Pin (N-Channel, Open-Drain) This pin outputs serial data at the falling edge of the shift clock (starting from the lower bit).	5
DIN	I	Data Input Pin This pin inputs serial data at the rising edge of the shift clock (starting from the lower bit).	6
NC	-	No Connection	7
CLK	I	Clock Input Pin This pin reads serial data at the rising edge and outputs data at the falling edge.	8
STB	I	Serial Interface Strobe Pin The data input after the STB has fallen is processed as a command. When this in is "HIGH", CLK is ignored.	9
K1 to K4	I	Key Data Input Pins The data inputted to these pins is latched at the end of the display cycle.	10 to 13
VDD	-	Logic Power Supply	14, 33, 45
SG1/KS1 to SG12/KS12	O	High-Voltage Segment Output Pins Also acts as the Key Source.	15 to 26
SG20/GR9 to SG19/GR10 SG18/GR11 to SG13/GR16	O	High-Voltage Segment/Grid Output Pins	36 to 35 32 to 27
VEE	-	Pull-Down Level	34
GR1 to GR8	O	High-Voltage Grid Output Pins	44 to 37
LED1 to LED5	O	LED Output Pin	50 to 46
GND	-	Ground Pin	51
OSC	I	Oscillator Input Pin A resistor is connected to this pin to determine the oscillation frequency.	52

INPUT/OUTPUT CONFIGURATIONS

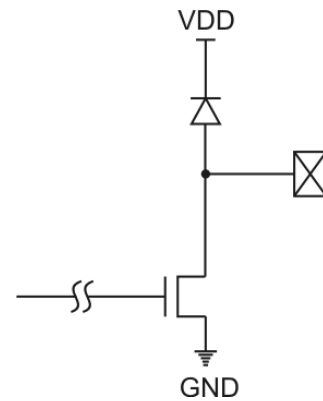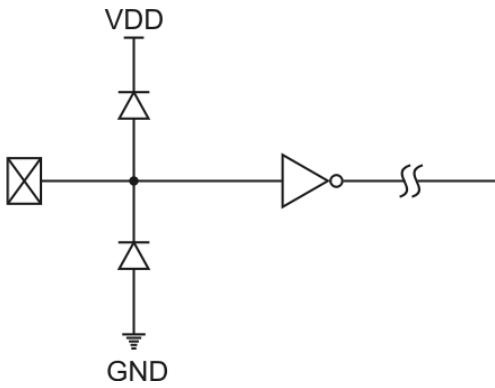The schematic diagrams of the input and output circuits of the logic section are shown below:

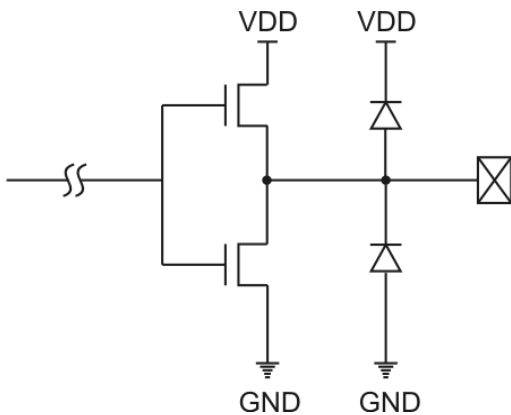*OUTPUT PINS: SGn/GRn*

INPUT PINS: DIN, CLK, STB
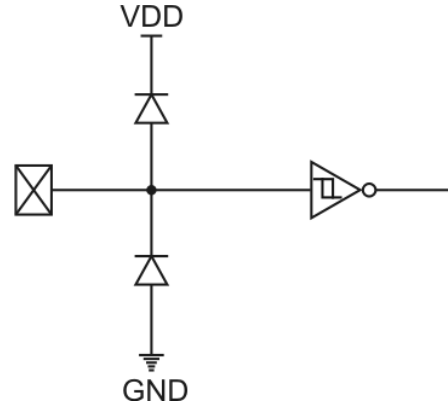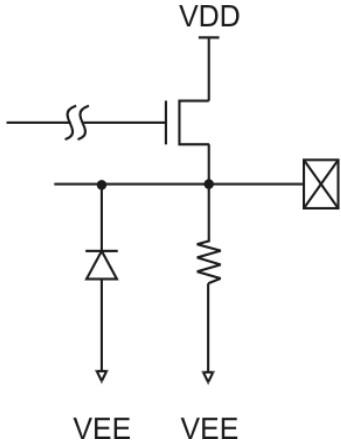
INPUT PINS: SW1 TO SW4, K1 TO K4

OUTPUT PIN: DOUT

OUTPUT PINS: LED1 TO LED5
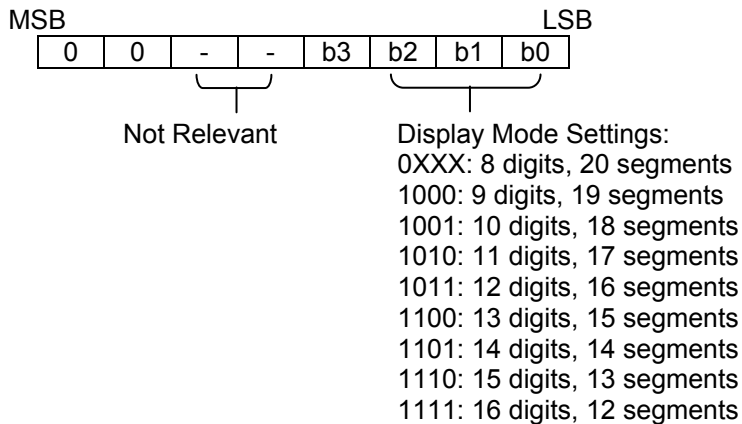
FUNCTION DESCRIPTION

COMMANDS

Commands determine the display mode and status of PT6311B. A command is the first byte (b0 to b7) inputted to PT6311B via the DIN Pin after STB Pin has changed from "HIGH" to "LOW" State. If for some reason the STB Pin is set to "HIGH" while data or commands are being transmitted, the serial communication is initialized, and the data/commands being transmitted are considered invalid.

COMMAND 1: DISPLAY MODE SETTING COMMANDS

PT6311B provides 9 display mode settings as shown in the diagram below: As stated earlier a command is the first one byte (b0 to b7) transmitted to PT6311B via the DIN Pin when STB is "LOW". However, for these commands, the bits 5 to 6 (b4 to b5) are ignored, bits 7 & 8 (b6 to b7) are given a value of "0".

The Display Mode Setting Commands determine the number of segments and grids to be used (1/8 to 1/16 duty, 20 to 12 segments). When these commands are executed, the display is forcibly turned off, the key scanning stops. A display command "ON" must be executed in order to resume display. If the same mode setting is selected, no command execution is take place, therefore, nothing happens.

When Power is turned "ON", the 16-digit, 12-segment modes is selected.

MSB   LSB

| 0 | 0 | - | - | b3 | b2 | b1 | b0 |

Not Relevant

Display Mode Settings:
0XXX: 8 digits, 20 segments
1000: 9 digits, 19 segments
1001: 10 digits, 18 segments
1010: 11 digits, 17 segments
1011: 12 digits, 16 segments
1100: 13 digits, 15 segments
1101: 14 digits, 14 segments
1110: 15 digits, 13 segments
1111: 16 digits, 12 segments

DISPLAY MODE AND RAM ADDRESS

Data transmitted from an external device to PT6311B via the serial interface are stored in the Display RAM and are assigned addresses. The RAM Addresses of PT6311B are given below in 8 bits unit.
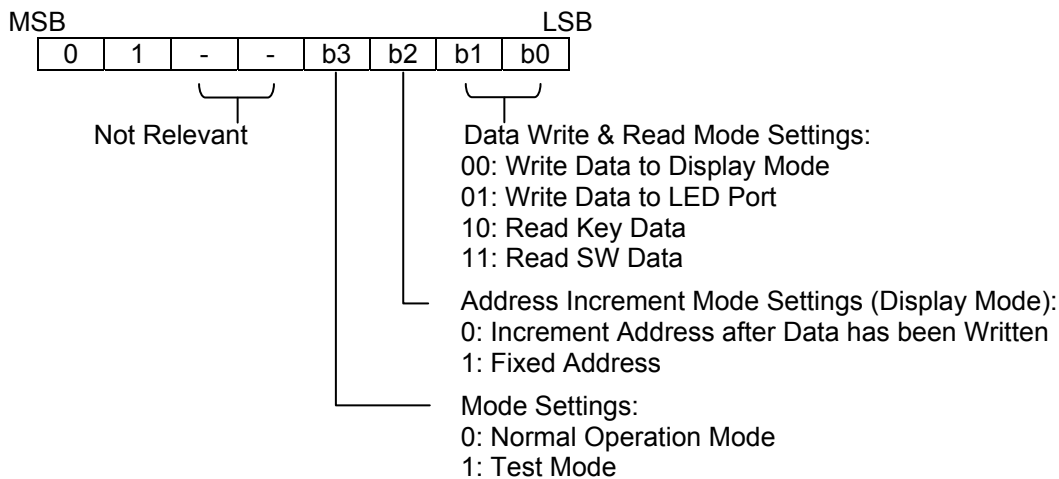
SG1 SG4	SG5 SG8	SG9 SG12	SG13 SG16	SG17 SG20	
00HL	00HU	01HL	01HU	02HL	DIG1
03HL	03HU	04HL	04HU	05HL	DIG2
06HL	06HU	07HL	07HU	08HL	DIG3
09HL	09HU	0AHL	0AHU	0BHL	DIG4
0CHL	0CHU	0DHL	0DHU	0EHL	DIG5
0FHL	0FHU	10HL	10HU	11HL	DIG6
12HL	12HU	13HL	13HU	14HL	DIG7
15HL	15HU	16HL	16HU	17HL	DIG8
18HL	18HU	19HL	19HU	1AHL	DIG9
1BHL	1BHU	1CHL	1CHU	1DHL	DIG10
1EHL	1EHU	1FHL	1FHU	20HL	DIG11
21HL	21HU	22HL	22HU	23HL	DIG12
24HL	24HU	25HL	25HU	26HL	DIG13
27HL	27HU	28HL	28HU	29HL	DIG14
2AHL	2AHU	2BHL	2BHU	2CHL	DIG15
2DHL	2DHU	2EHL	2EHU	2FHL	DIG16

b0 b3	b4 b7
xxHL	xxHU
Lower 4 bits	Higher 4 bits
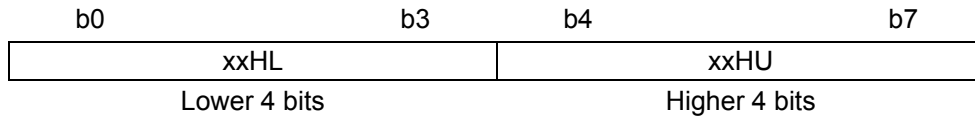
COMMAND 2: DATA SETTING COMMANDS

The Data Setting Commands executes the Data Write or Data Read Modes for PT6311B. The data Setting Command, the bits 5 and 6 (b4, b5) are ignored, bit 7 (b6) is given the value of "1" while bit 8 (b7) is given the value of "0". Please refer to the diagram below.

When power is turned ON, bit 4 to bit 1 (b3 to b0) are given the value of "0".

MSB							LSB
0	1	-	-	b3	b2	b1	b0

Not Relevant

Data Write & Read Mode Settings:
00: Write Data to Display Mode
01: Write Data to LED Port
10: Read Key Data
11: Read SW Data

Address Increment Mode Settings (Display Mode):
0: Increment Address after Data has been Written
1: Fixed Address

Mode Settings:
0: Normal Operation Mode
1: Test Mode

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PT6311B KEY MATRIX & KEY INPUT DATA STORAGE RAM

PT6311B Key Matrix consists of 12 x 4 array as shown below:
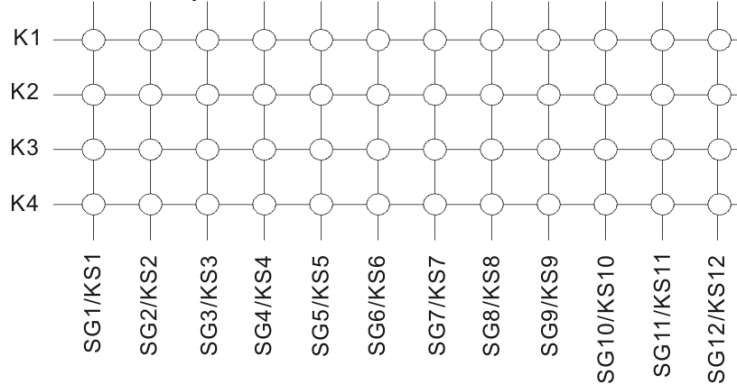
Each data inputted by each key are stored as follows. They are read by a READ Command, starting from the last significant bit. When the most significant bit of the data (SG12, b7) has been read, the least significant bit of the next data (SG1, b0) is read.
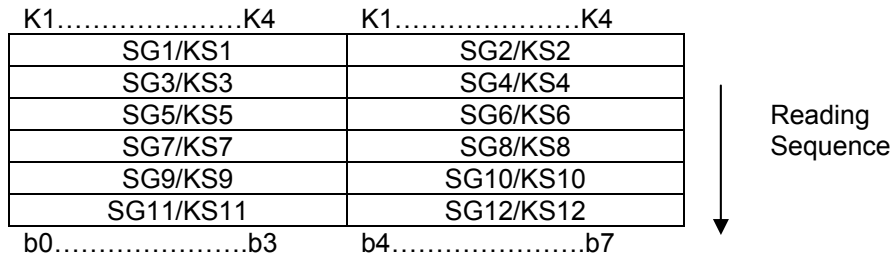
K1...................K4	K1...................K4
SG1/KS1	SG2/KS2
SG3/KS3	SG4/KS4
SG5/KS5	SG6/KS6
SG7/KS7	SG8/KS8
SG9/KS9	SG10/KS10
SG11/KS11	SG12/KS12
b0...................b3	b4...................b7

Reading Sequence

LED DISPLAY

PT6311B provides 5 LED Display Terminals, namely LED1 to LED5. Data is written to the LED Port starting from the least significant bit (b0) of the port using a WRITE Command. Each bit starting from the least significant (b0) activates a specific LED Display Terminal -- b0 corresponds LED1 Display, b1 activates LED2 and so forth. Since there are only 5 LED display terminals, bits 6 to 8 (b5 ~ b7) are not used and therefore ignored. This means that b5 to b7 does NOT in anyway activate any LED Display, they are totally ignored.

 When a bit (b0 ~ b4) in the LED Port is "0", the corresponding LED is ON. Conversely, when the bit is "1", the LED Display is turned OFF. For example, Bit 1 (as designated by b0) has the value of "0", then this means that LED1 is ON. It must be noted that when power is turned ON, bit 5 to bit 1 (b4 to b0) are given the value of "1". Please refer to the diagrams below:
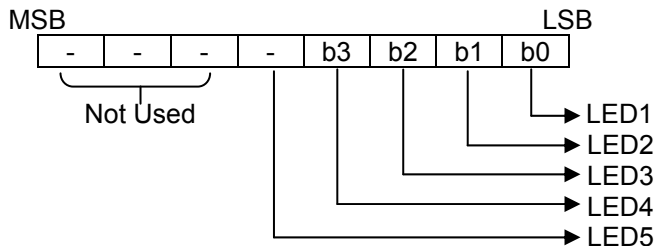
SWITCH DATA

PT6311B provides 4 Switch Inputs, namely: SW1 to SW4. SW Data is read starting from the least significant bit (b0) using a READ Command. Each bit starting from the least significant (b0) corresponds to a specific Switch Input -- b0 corresponds SW1, b1 to SW2 and so forth. Since there are only 4 Switch Inputs, Bits 5 to 8 (b4 to 7) are given the value of "0". Please refer to the diagram below.
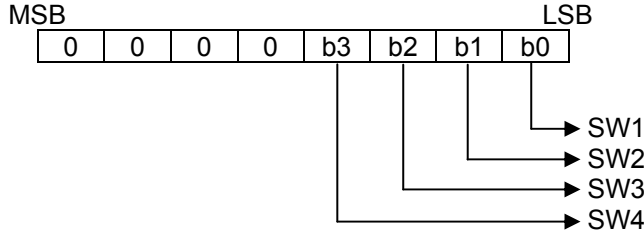
COMMAND 3: ADDRESS SETTING COMMANDS

Address Setting Commands are used to set the address of the display memory. The address is considered valid if it has a value of "00H" to "2FH". If the address is set to 30H or higher, the data is ignored until a valid address is set. When power is turned ON, the address is set at "00H".

Please refer to the diagram below.
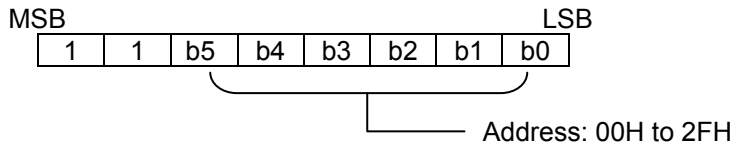
COMMAND 4: DISPLAY CONTROL COMMANDS

The Display Control Commands are used to turn ON or OFF a display. It also used to set the pulse width. Please refer to the diagram below. When the power is turned ON, a 1/16 pulse width is selected and the displayed is turned OFF (the key scanning is stopped).
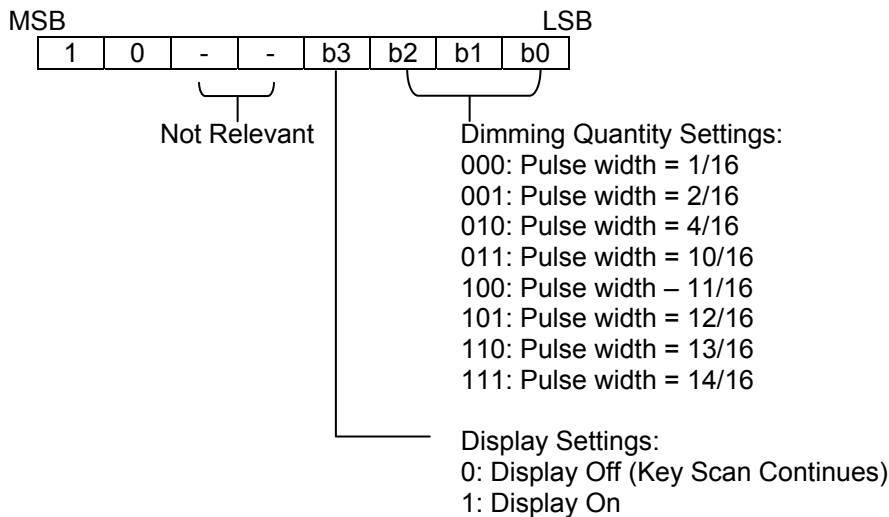
SCANNING AND DISPLAY TIMING

The key scanning and display timing diagram is given below. One cycle of key scanning consists of 2 frames. The data of the 12 x 4 matrix is stored in the RAM.

$T_{DISPLAY} \cong 500\mu s$

Key Scan Data

SG Output   DIG1   DIG2   DIG3   ············   DIGn   ····   DIG1

G1

G2

G3

Gn

1 Frame = $T_{DISPLAY}$ X (n +1)
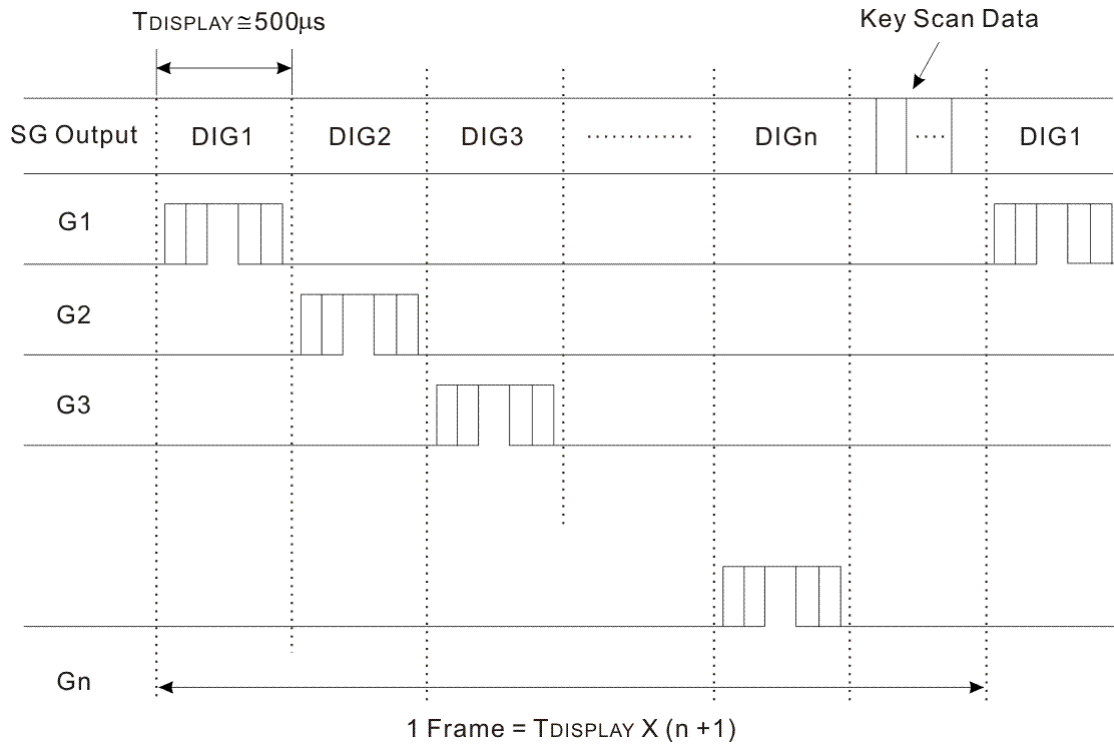
SERIAL COMMUNICATION FORMAT

The following diagram shows the PT6311B serial communication format. The DOUT Pin is an N-channel, open-drain output pin, therefore, it is highly recommended that an external pull-up resistor (1 KΩ to 10 KΩ) must be connected to DOUT.

RECEPTION (DATA/COMMAND WRITE)
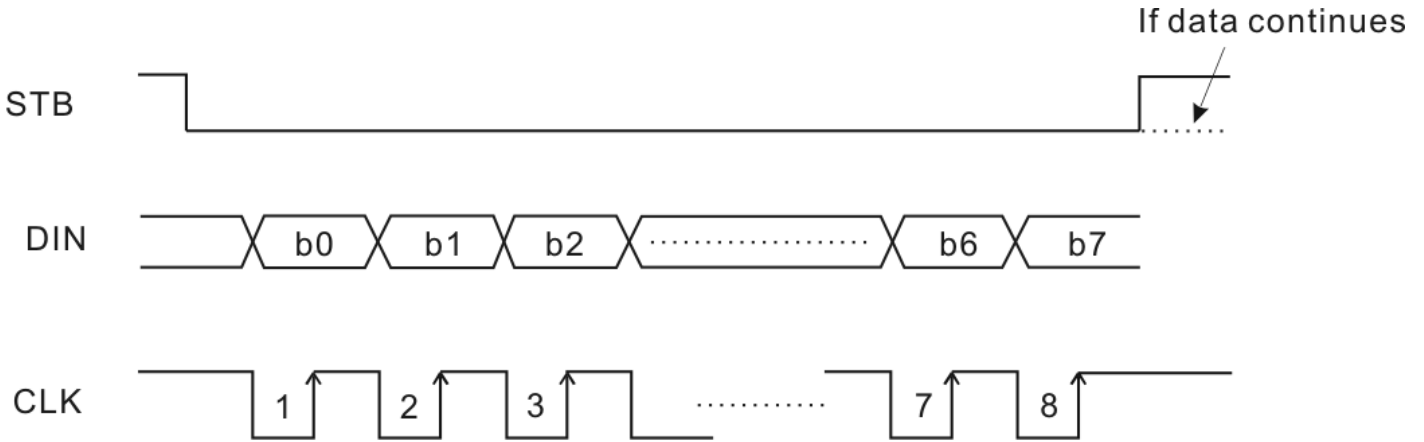
TRANSMISSION (DATA READ)
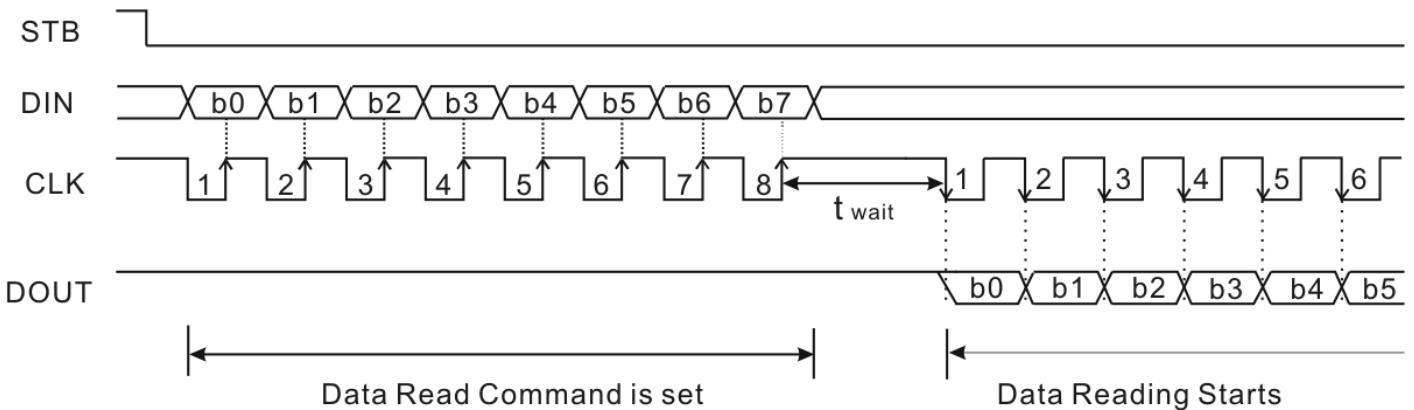
where: twait (waiting time) > 1μs

It must be noted that when the data is read, the waiting time (twait) between the rising of the eighth clock that has set the command and the falling of the first clock that has read the data is greater or equal to 1μs.

SWITCHING CHARACTERISTIC WAVEFORM

The PT6311B Switching Characteristics Waveform is given below.
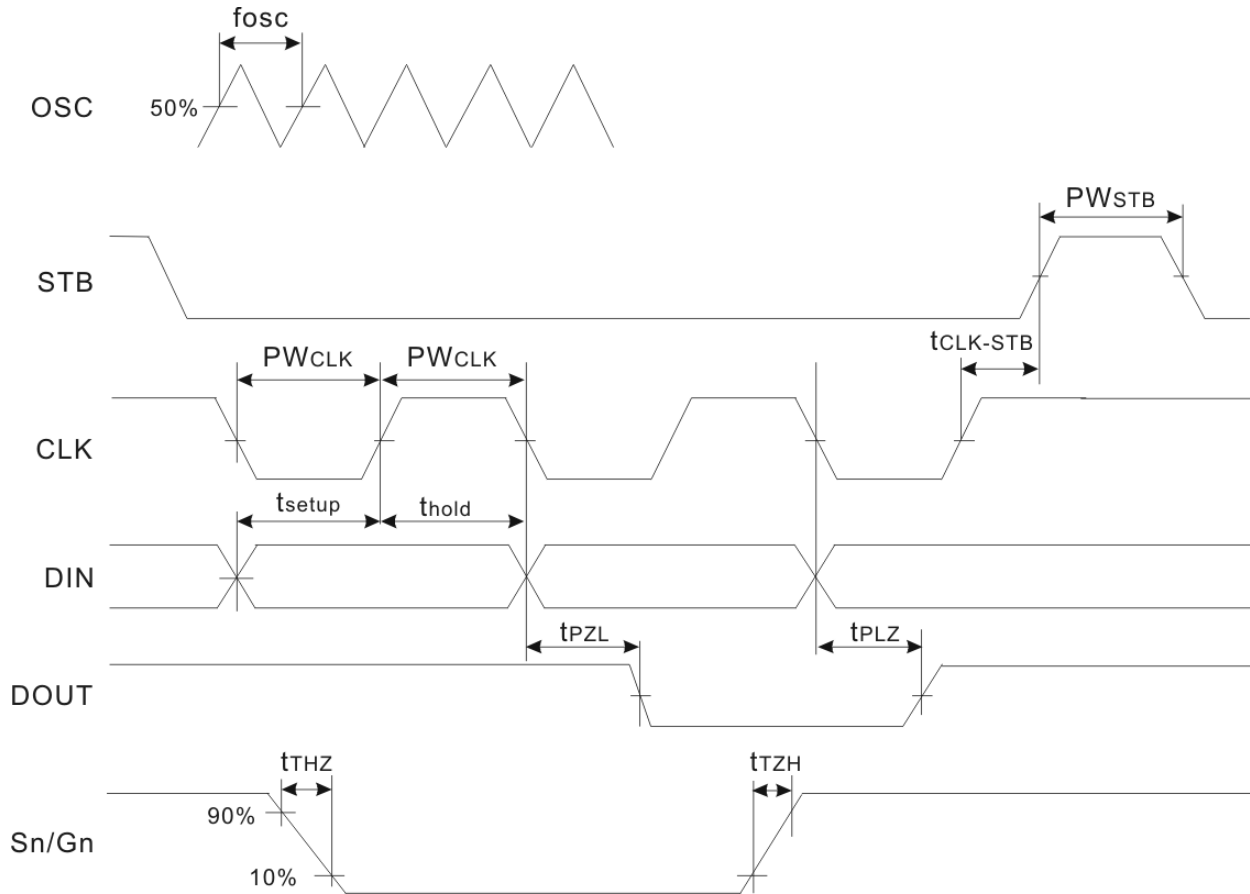
where:

fosc = Oscillation Frequency

PWSTB (Strobe Pulse Width) $\geq$ 1 μs

tsetup (Data Setup Time) $\geq$ 100 ns

tTZH1 (Segment Rise Time) $\leq$ 2.0 μs (VDD = 5 V)

tTZH2 (Grid Rise Time) $\leq$ 0.5 μs (VDD = 5 V)

tTHZ (Segment & Grid Fall Time) $\leq$ 150 μs

tPLZ (Propagation Delay Time) $\leq$ 400 ns (VDD = 5 V)

PWCLK (Clock Pulse Width) $\geq$ 400 ns

tCLK-STB (Clock - Strobe Time) $\geq$ 1 μs

thold (Data Hold Time) $\geq$ 100 ns

tTZH1 (Segment Rise Time) $\leq$ 4.0 μs (VDD = 3.3 V)

tTZH2 (Grid Rise Time) $\leq$ 1.2 μs (VDD = 3.3 V)

tPZL (Propagation Delay Time) $\leq$ 100 ns

tPLZ (Propagation Delay Time) $\leq$ 600 ns (VDD = 3.3 V)

APPLICATIONS

Display memories are updated by incrementing address. Please refer to the following diagram.

STB								
CLK								
DIN	Command 2	Command 3	Data 1	············	Data n	Command 1	Command 4
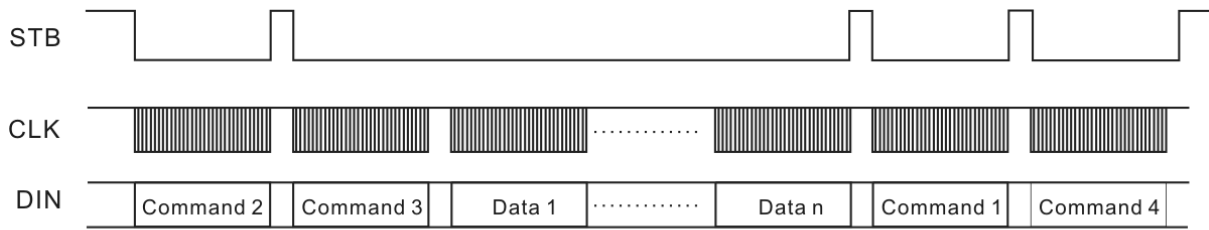
where: Command 1: Display Mode Setting Command
Command 2: Data Setting Command
Command 3: Address Setting Command
Data 1 to n : Transfer Display Data (48 Bytes max.)
Command 4: Display Control Command

The following diagram shows the waveforms when updating specific addresses.

STB					
CLK					
DIN	Command 2	Command 3	Data	Command 3	Data
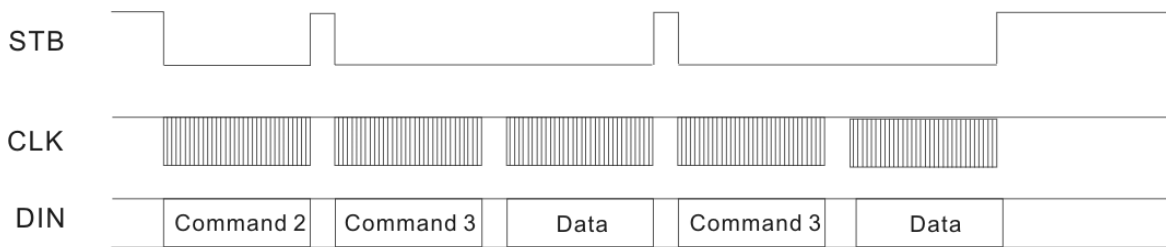
where: Command 2: Data Setting Command
Command 3: Address Setting Command
Data: Display Data

RECOMMENDED SOFTWARE FLOWCHART

```
                        ┌─────────────┐
                        │    START    │
                        └──────┬──────┘
                               │
                        ┌──────┴──────┐
                        │ Delay 200 ms│
                        └──────┬──────┘
                               │
                        ┌──────┴──────┐
                        │     SET     │──────────┐
                        │  COMMAND 2  │          │
                        │ (Write Data)│          │
                        └──────┬──────┘          │
                               │                 │
                        ┌──────┴──────┐          │
                        │     SET     │          │       INITIAL
                        │  COMMAND 3  │          │       SETTING
                        │Clear Display│          │
                        │    RAM      │          │
                        │ (See Note 5)│          │
                        └──────┬──────┘          │
                               │                 │
                        ┌──────┴──────┐          │
                        │     SET     │          │
                        │  COMMAND 1  │          │
                        └──────┬──────┘          │
                               │                 │
                        ┌──────┴──────┐          │
                        │     SET     │──────────┘
                        │  COMMAND 4  │
                        │(88H~8FH:    │
                        │ Display ON) │
                        └──────┬──────┘
                               │
                        ┌──────┴──────┐◄─────────┐
                        │    MAIN     │          │
                        │   PROGRAM   │          │
                        └──────┬──────┘          │
                               │                 │
                        ┌──────┴──────┐          │
                        │     SET     │          │
                        │  COMMAND 2  │          │
                        │(Read Key &  │          │       MAIN
                        │ Write Data  │          │       LOOP
                        │  Includeed) │          │
                        └──────┬──────┘          │
                               │                 │
                        ┌──────┴──────┐          │
                        │     SET     │          │
                        │  COMMAND 3  │          │
                        └──────┬──────┘          │
                               │                 │
                        ┌──────┴──────┐          │
                        │     SET     │          │
                        │  COMMAND 1  │          │
                        └──────┬──────┘          │
                               │                 │
                        ┌──────┴──────┐──────────┘
                        │     SET     │
                        │  COMMAND 4  │
                        └──────┬──────┘
                               │
                        ┌──────┴──────┐
                        │     END     │
                        └─────────────┘
```
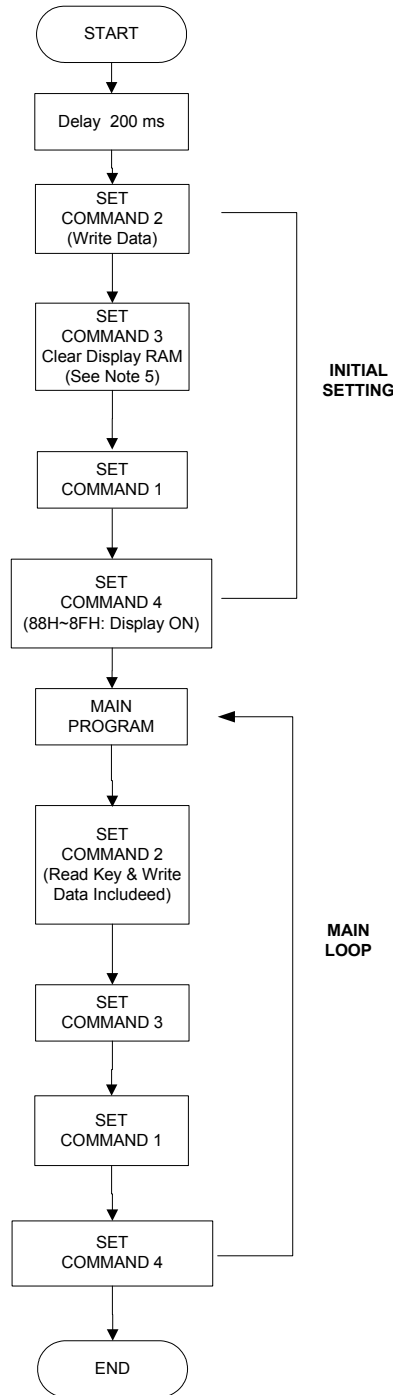
Notes:
1. Command 1: Display Mode Commands
2. Command 2: Data Setting Commands
3. Command 3: Address Setting Commands
4. Command 4: Display Control Commands
5. When IC power is applied for the first time, the contents of the Display RAM are not defined; thus, it is strongly suggested that the contents of the Display RAM must be cleared during the initial setting.

ABSOLUTE MAXIMUM RATINGS

(Unless otherwise stated, Ta=25℃, GND=0V)

Parameter	Symbol	Ratings	Unit
Logic supply voltage	VDD	-0.3 to +7	V
Driver supply voltage	VEE	VDD +0.3 to VDD -40	V
Logic input voltage	VI	-0.3 to VDD +0.3	V
VFD driver output voltage	VO	VEE -0.3 to VDD +0.3	V
LED driver output current	IOLED	+25	mA
Oscillation frequency	fosc	3M(Max.)	Hz
Operating temperature	Topr	-40 to +85	℃
Storage temperature	Tstg	-65 to +150	℃
VFD driver output current	IOVFD	-40 (Grid) -15 (Segment)	mA

RECOMMENDED OPERATING RANGE

(Unless otherwise stated, Ta=25℃, GND=0V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Logic supply voltage	VDD	3	5	5.5	V
High-Level input voltage	VIH	0.7VDD	-	VDD	V
Low-Level input voltage	VIL	0	-	0.3VDD	V
Driver supply voltage	VEE	VDD -35	-	0	V

POWER SUPPLY SEQUENCE
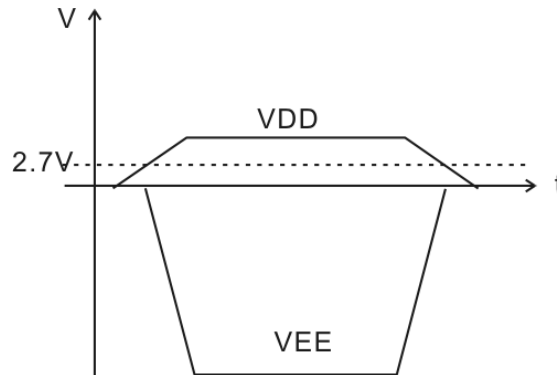
Note: The power on/off sequence suggestion:
Applications must observe the following sequence when turning the power on or off.
- At power on: First turn on the logic system power (VDD), and then turn on the driver power (VEE).
- At power off: First turn off the driver power (VEE), and then turn off the logic system power (VDD).

ELECTRICAL CHARACTERISTICS

(Unless otherwise stated, VDD=5V, GND=0V, VEE=VDD-35 V, Ta=25℃)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
High-Level output voltage	VOHLED	IOHLED=-1mA LED1 to LED5	0.9VDD	-	-	V
Low-Level output voltage	VOLLED	IOLLED=+20mA LED1 to LED5	-	-	1	V
Low-Level output voltage	VOLDOUT	DOUT, IOLDOUT=4mA	-	-	0.4	V
High-Level output current	IOHSG	VO=VDD -2V SG1 to SG12	-3	-	-	mA
High-Level output current	IOHGR	VO=VDD -2V, GR1 to GR8, SG13/GR16 to SG20/GR9	-15	-	-	mA
High-Level input voltage	VIH	-	0.7VDD	-	-	V
Low-Level input voltage	VIL	-	-	-	0.3VDD	V
Oscillation frequency	fosc	R=56KΩ	350	500	650	KHz
Input current	II	VI=VDD or GND	-	-	±1	µA
Dynamic current consumption	IDDdyn	Under no load Display OFF	-	-	5	mA

(Unless otherwise stated, VDD=3.3V, GND=0V, VEE=VDD-35 V, Ta=25℃)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
High-Level output voltage	VOHLED	IOHLED = -1mA LED1 to LED5	0.9VDD	-	-	V
Low-Level output voltage	VOLLED	IOLLED = +20mA LED1 to LED5	-	-	1	V
Low-Level output voltage	VOLDOUT	DOUT, IOLDOUT = 4mA	-	-	0.4	V
High-Level output current	IOHSG	VO = VDD -2V SG1 to SG12	-1.5	-	-	mA
High-Level output current	IOHGR	VO = VDD -2V GR1 to GR8, SG13/GR16 to SG20/GR9	-6	-	-	mA
High-Level input voltage	VIH	-	0.7VDD	-	-	V
Low-Level input voltage	VIL	-	-	-	0.2VDD	V
Oscillation frequency	fosc	R = 56 KΩ	350	500	650	KHz
Input current	II	VI = VDD or GND	-	-	±1	µA
Dynamic current consumption	IDDdyn	Under no load Display OFF	-	-	3	mA

PACKAGE INFORMATION

52 PINS, LQFP
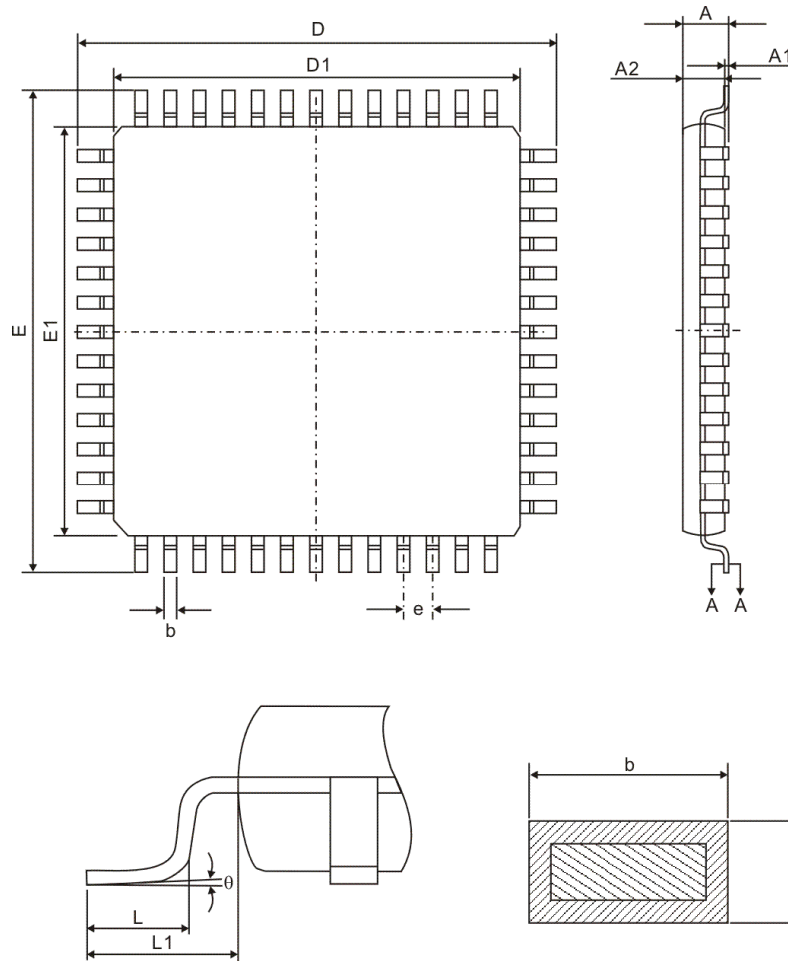
Symbol	Dimensions (MM)		
	Min.	Nom.	Max.
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
b	0.35	-	0.50
c	0.09	-	0.20
D	16.60 BSC		
D1	14.00 BSC		
E	16.60 BSC		
E1	14.00 BSC		
e	1.00 BSC		
θ	0°	3.5°	7°
L	0.70	0.85	1.00
L1	1.30 REF		

Note: Refer to JEDEC MS-026

IMPORTANT NOTICE

Princeton Technology Corporation (PTC) reserves the right to make corrections, modifications, enhancements, improvements, and other changes to its products and to discontinue any product without notice at any time.

PTC cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a PTC product. No circuit patent licenses are implied.

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