



## TS4621E

### High-performance class-G stereo headphone amplifier with I<sup>2</sup>C volume control

#### Features

- Power supply range: 2.3 V to 4.8 V
- 0.6 mA/channel quiescent current
- 2.1 mA current consumption with 100  $\mu$ W/channel (10 dB crest factor)
- 0.006% typical THD+N at 1 kHz
- 100 dB typical PSRR at 217 Hz
- 100 dB of SNR A-weighted at G = 0 dB
- Zero pop and click
- I<sup>2</sup>C interface for volume control
- Digital volume control range from -60 dB to +4 dB
- Independent right and left channel shutdown control
- Integrated high-efficiency buck converter
- Low software standby current: 5  $\mu$ A max
- Output-coupling capacitors removed
- Thermal shutdown and short-circuit protection
- Flip-chip package: 1.65 mm x 1.65 mm, 400  $\mu$ m pitch, 16 bumps

#### Applications

- Cellular phones, smart phones
- Mobile internet devices
- PMP/MP3 players

#### Description

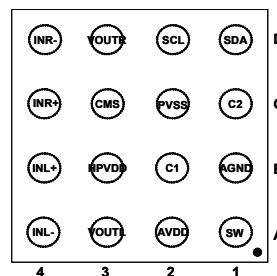
The TS4621E is a class-G stereo headphone driver dedicated to high audio performance, high power efficiency and space-constrained applications.

It is based on the core technology of a low power dissipation amplifier combined with a high-efficiency buck converter for supplying this amplifier.

TS4621EIJT - flip-chip



Pinout (top view)



Balls are underneath

When powered by a battery, the buck converter generates the appropriate voltage to the amplifier depending on the amplitude of the audio signal to supply the headsets. It achieves a total 2.1 mA current consumption at 100  $\mu$ W output power (10 dB crest factor).

THD+N is 0.02% maximum at 1 kHz and PSRR is 100 dB at 217 Hz, which ensures a high audio quality of the device in a wide range of environments.

The traditionally bulky output coupling capacitors can be removed.

A dedicated common-mode sense pin removes parasitic ground noise.

The TS4621E is designed to be used with an output serial resistor. It ensures unconditional stability over a wide range of capacitive loads.

The TS4621E is packaged in a tiny 16-bump flip-chip package with a pitch of 400  $\mu$ m.

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# 1 Absolute maximum ratings and operating conditions

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{CC}$	Supply voltage <sup>(1)</sup> during 1ms.	5.5	V
$V_{in+}, V_{in-}$	Input voltage referred to ground	+/- 1.2	V
$T_{stg}$	Storage temperature	-65 to +150	°C
$T_j$	Maximum junction temperature <sup>(2)</sup>	150	°C
$R_{thja}$	Thermal resistance junction to ambient <sup>(3)</sup>	200	°C/W
$P_d$	Power dissipation	Internally limited <sup>(4)</sup>	
ESD	Human body model (HBM) <sup>(5)</sup> All pins VOUTR, VOUTL vs. AGND	2 4	kV
	Machine model (MM), min. value <sup>(6)</sup>	100	V
	Charge device model (CDM) All pins VOUTR, VOUTL	500 750	V
	IEC61000-4-2 level 4, contact <sup>(7)</sup> IEC61000-4-2 level 4, air discharge <sup>(7)</sup>	+/- 8 +/- 15	kV
Latch-up	Latch-up immunity	200	mA
	Lead temperature (soldering, 10 sec)	260	°C

- All voltage values are measured with respect to the ground pin.
- Thermal shutdown is activated when maximum junction temperature is reached.
- The device is protected from over-temperature by a thermal shutdown mechanism, active at 150° C.
- Exceeding the power derating curves for long periods may provoke abnormal operation.
- Human body model: a 100 pF capacitor is charged to the specified voltage, then discharged through a 1.5 kΩ resistor between two pins of the device. This is done for all couples of connected pin combinations while the other pins are floating.
- Machine model: a 200 pF capacitor is charged to the specified voltage, then discharged directly between two pins of the device with no external series resistor (internal resistor < 5 Ω). This is done for all couples of connected pin combinations while the other pins are floating.
- The measurement is performed on an evaluation board, with ESD protection EMIF02-AV01F3.

**Table 2. Operating conditions**

Symbol	Parameter	Value	Unit
$V_{CC}$	Supply voltage	2.3 to 4.8	V
HPVDD	Buck DC output voltages High rail voltage Low rail voltage	1.9 1.2	V
SDA, SCL	Input voltage range	GND to $V_{CC}$	V
$R_L$	Load resistor	$\geq 16$	$\Omega$
$C_L$	Load capacitor Serial resistor of 12 $\Omega$ minimum, $R_L \geq 16 \Omega$	0.8 to 100	nF
$T_{oper}$	Operating free air temperature range	-40 to +85	$^{\circ}\text{C}$
$R_{thja}$	Flip-chip thermal resistance junction to ambient	90	$^{\circ}\text{C}/\text{W}$

## 2 Typical application schematics

Figure 1. Typical application schematics for the TS4621E

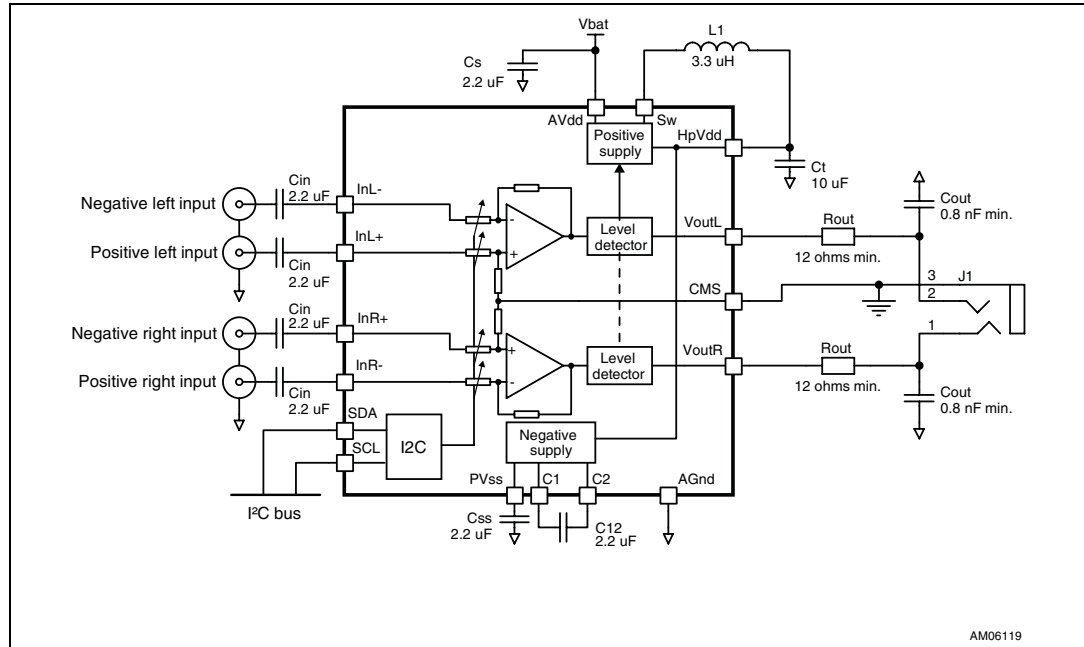


Table 3. TS4621E pin description

Pin number	Pin name	Pin definition
A1	SW	Switching node of the buck converter
A2	AVDD	Analog supply voltage, connect to battery
A3	VOU TL	Output signal for left audio channel
A4	INL-	Negative input signal for left audio channel
B1	AGND	Device ground
B2	C1	Flying capacitor terminal for internal negative supply generator
B3	HPVDD	Buck converter output, power supply for amplifier
B4	INL+	Positive input signal for left audio channel
C1	C2	Flying capacitor terminal for internal negative supply generator
C2	PVSS	Negative supply generator output
C3	CMS	Common mode sense, to be connected as close as possible to the ground of headphone/line out plug
C4	INR+	Positive input signal for right audio channel
D1	SDA	I <sup>2</sup> C data signal, up to V <sub>CC</sub> tolerant input
D2	SCL	I <sup>2</sup> C clock signal, up to V <sub>CC</sub> tolerant input
D3	VOU TR	Output signal for right audio channel
D4	INR-	Negative input signal for right audio channel

**Table 4. TS4621E component description**

Component	Value	Description
C <sub>s</sub>	2.2 μF	Decoupling capacitors for V <sub>CC</sub> . A 2.2 μF capacitor is sufficient for proper decoupling of the TS4621E. An X5R dielectric and 10 V rating voltage is recommended to minimize ΔC/ΔV when V <sub>CC</sub> = 4.8 V. Must be placed as close as possible to the TS4621E to minimize parasitic inductance and resistance.
C <sub>12</sub>	2.2 μF	Capacitor for internal negative power supply operation. An X5R dielectric and 6.3 V rating voltage is recommended to minimize ΔC/ΔV when HPVDD = 1.9 V. Must be placed as close as possible to the TS4621E to minimize parasitic inductance and resistance.
C <sub>SS</sub>	2.2 μF	Filtering capacitor for internal negative power supply. An X5R dielectric and 6.3 V rating voltage is recommended to minimize ΔC/ΔV when HPVDD = 1.9 V.
C <sub>in</sub>	$C_{in} = \frac{1}{2\pi Z_{in} F_c}$	Input coupling capacitor that forms with Z <sub>in</sub> /2 a first-order high-pass filter with a -3 dB cutoff frequency F <sub>c</sub> . For example, at maximum gain G = 4 dB, Z <sub>in</sub> = 12.5 kΩ, C <sub>in</sub> = 2.2 μF, therefore F <sub>c</sub> = 6 Hz.
C <sub>out</sub>	0.8 to 100 nF	Output capacitor of 0.8 nF minimum to 100 nF maximum. This capacitor is mandatory for operation of the TS4621E.
R <sub>out</sub>	12 Ω min.	Output resistor in-series with the TS4621E output. This 12 Ω minimum resistor is mandatory for operation of the TS4621E.
L <sub>1</sub>	3.3 μH	Inductor for the buck convertor. References of inductors: FDK: MIPSZ2012D3R3 (DC resistance = 0.19 Ω, rated current = 0.8 A) Murata: LQM2MPN3R3G0 (DC resistance = 0.12 Ω, rated current = 1.2 A)
C <sub>t</sub>	10 μF	Tank capacitor for internal buck convertor. An X5R dielectric and 6.3 V rating voltage is recommended to minimize ΔC/ΔV when HPVDD = 1.9 V. ESR of the C <sub>t</sub> capacitor must be as low as possible to obtain the best buck efficiency.

### 3 Electrical characteristics

**Table 5. Electrical characteristics of the I<sup>2</sup>C interface**  
for  $V_{CC} = +3.6\text{ V}$ ,  $AGND = 0\text{ V}$ ,  $T_{amb} = 25^\circ\text{C}$  (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
$V_{IL}$	Low level input voltage on SDA, SCL pins			0.6	V
$V_{IH}$	High level input voltage on SDA, SCL pins	1.2			V
$V_{OL}$	Low level output voltage, SDA pin, $I_{sink} = 3\text{mA}$			0.4	V
$I_{in}$	Input current on SDA, SCL		$\frac{V_{SDA, SCL}}{600\text{k}\Omega}$	10	$\mu\text{A}$

**Table 6. Electrical characteristics of the amplifier**  
for  $V_{CC} = +3.6\text{ V}$ ,  $AGND = 0\text{ V}$ ,  $R_L = 32\ \Omega + 15\ \Omega$ ,  $T_{amb} = 25^\circ\text{C}$   
(unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
$I_{CC}$	Quiescent supply current, no input signal, both channels enabled		1.2	1.5	mA
$I_s$	Supply current, with input modulation, both channels enabled, $HPVDD = 1.2\text{ V}$ , output power per channel, $F=1\text{kHz}$ $P_{out} = 100\ \mu\text{W}$ at 3 dB crest factor $P_{out} = 500\ \mu\text{W}$ at 3 dB crest factor $P_{out} = 1\text{ mW}$ at 3 dB crest factor $P_{out} = 100\ \mu\text{W}$ at 10 dB crest factor $P_{out} = 500\ \mu\text{W}$ at 10 dB crest factor $P_{out} = 1\text{ mW}$ at 10 dB crest factor		2.3 3.7 4.7 2.1 3.1 3.9	3.5 5 6.5	mA
$I_{STBY}$	Standby current, no input signal, I <sup>2</sup> C CR1 = 01h $V_{SDA} = 0\text{ V}$ , $V_{SCL} = 0\text{ V}$		0.6	5	$\mu\text{A}$
$V_{in}$	Input differential voltage range <sup>(1)</sup>			1	$V_{rms}$
$V_{oo}$	Output offset voltage No input signal	-500		+500	$\mu\text{V}$
$V_{out}$	Maximum output voltage, in-phase signals $R_L = 16\ \Omega$ , THD+N = 1% max, $f = 1\text{ kHz}$ $R_L = 47\ \Omega$ , THD+N = 1% max, $f = 1\text{ kHz}$ $R_L = 10\text{ k}\Omega$ , $R_s = 15\ \Omega$ , $C_L = 1\text{ nF}$ , THD+N = 1% max, $f = 1\text{ kHz}$	0.6 1.0 1.0	0.8 1.1 1.3		$V_{rms}$
THD+N	Total harmonic distortion + noise, $G = 0\text{ dB}$ $V_{out} = 700\text{ mV}_{rms}$ , $F = 1\text{ kHz}$ $V_{out} = 700\text{ mV}_{rms}$ , $20\text{ Hz} < F < 20\text{ kHz}$		0.006 0.05	0.02	%
PSRR	Power supply rejection ratio <sup>(1)</sup> , $V_{ripple} = 200\text{ mV}_{pp}$ , grounded inputs $F = 217\text{ Hz}$ , $G = 0\text{ dB}$ , $R_L \geq 16\ \Omega$ $F = 10\text{ kHz}$ , $G = 0\text{ dB}$ , $R_L \geq 16\ \Omega$	90	100 70		dB

**Table 6. Electrical characteristics of the amplifier**  
**for  $V_{CC} = +3.6\text{ V}$ ,  $AGND = 0\text{ V}$ ,  $R_L = 32\ \Omega + 15\ \Omega$ ,  $T_{amb} = 25^\circ\text{ C}$**   
**(unless otherwise specified) (continued)**

Symbol	Parameter	Min.	Typ.	Max.	Unit
CMRR	Common mode rejection ratio $F = 1\text{ kHz}$ , $G = 0\text{ dB}$ , $V_{ic} = 200\text{ mV}_{pp}$ $F = 20\text{ Hz to } 20\text{ kHz}$ , $G = 0\text{ dB}$ , $V_{ic} = 200\text{ mV}_{pp}$		65 45		dB
Crosstalk	Channel separation $R_L = 32\ \Omega + 15\ \Omega$ , $G = 0\text{ dB}$ , $F = 1\text{ kHz}$ , $P_o = 10\text{ mW}$ $R_L = 10\text{ k}\Omega$ , $G = 0\text{ dB}$ , $F = 1\text{ kHz}$ , $V_{out} = 1\text{ V}_{rms}$	60 80	100 110		dB
SNR	Signal-to-noise ratio, A-weighted, $V_{out} = 1\text{ V}_{rms}$ , $THD+N < 1\%$ , $F = 1\text{ kHz}^{(1)}$ $G = +4\text{ dB}$ $G = +0\text{ dB}$	99 100			dB
ONoise	Output noise voltage, A-weighted <sup>(1)</sup> $G = +4\text{ dB}$ $G = +0\text{ dB}$		9	11 9	$\mu\text{V}_{rms}$
G	Gain range with gain (dB) = $20 \times \log[(V_{outL/R}) / (\lnL/R+ - \lnL/R-)]$	-60		+4	dB
Mute	$\lnL/R+ - \lnL/R- = 1\text{ V}_{rms}$			-80	dB
-	Gain step size error	-0.5		+0.5	step-size
-	Gain error ( $G = +4\text{ dB}$ )	-0.45		+0.42	dB
$Z_{in}$	Differential input impedance	25	34		k $\Omega$
	Input impedance during wake-up phase (referred to ground)		2		k $\Omega$
$Z_{out}$	Output impedance when $CR1 = 00h$ (negative supply is ON and amplifier output stages are OFF) <sup>(1)</sup> $F < 40\text{ kHz}$ $F = 6\text{ MHz}$ $F = 36\text{ MHz}$	10 500 75			k $\Omega$ $\Omega$ $\Omega$
$t_{wu}$	Wake-up time <sup>(2)</sup>		12	16	ms
$t_{stby}$	Standby time		100		$\mu\text{s}$
$t_{atk}$	Attack time. Setup time between low rail buck voltage and high rail buck voltage		100		$\mu\text{s}$
$t_{dcy}$	Decay time		50		ms

1. Guaranteed by design and parameter correlation.

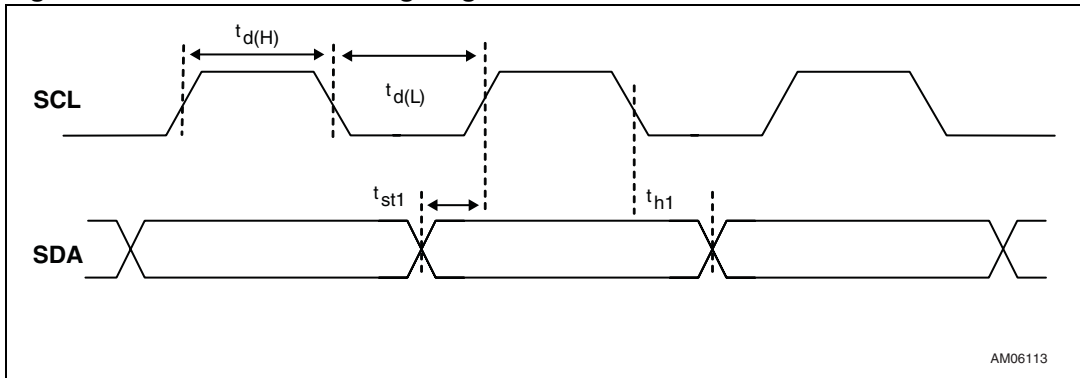
2. Refer to the application information in [Section 4.3 on page 27](#).



**Table 7. Timing characteristics of the I<sup>2</sup>C interface for I<sup>2</sup>C interface signals over recommended operating conditions (unless otherwise specified)**

Symbol	Parameter	Min.	Typ.	Max.	Unit
$f_{SCL}$	Frequency, SCL			400	kHz
$t_{d(H)}$	Pulse duration, SCL high	0.6			$\mu$ s
$t_{d(L)}$	Pulse duration, SCL low	1.3			$\mu$ s
$t_{st1}$	Setup time, SDA to SCL	100			ns
$t_{h1}$	Hold time, SCL to SDA	0			ns
$t_f$	Bus free time between stop and start condition	1.3			$\mu$ s
$t_{st2}$	Setup time, SCL to start condition	0.6			$\mu$ s
$t_{h2}$	Hold time, start condition to SCL	0.6			$\mu$ s
$t_{st3}$	Setup time, SCL to stop condition	0.6			$\mu$ s

**Figure 2. SCL and SDA timing diagram**



**Figure 3. Start and stop condition timing diagram**

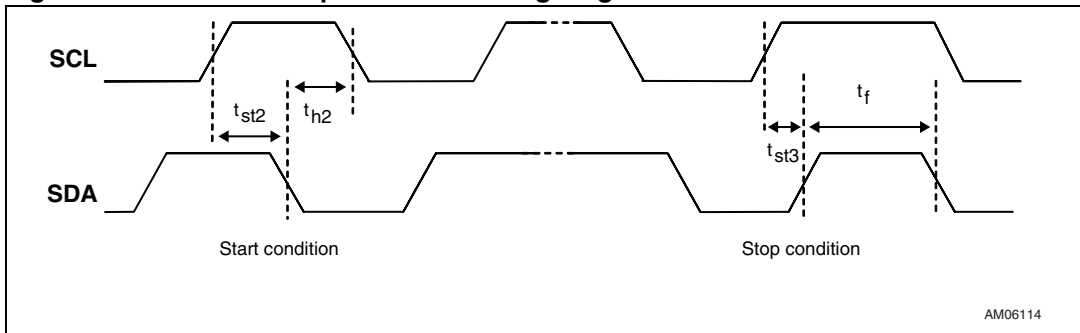


Figure 4. Current consumption vs. power supply voltage

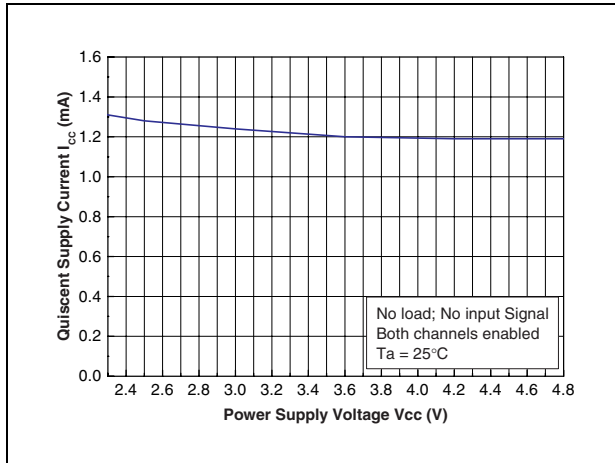


Figure 5. Standby current consumption vs. power supply voltage

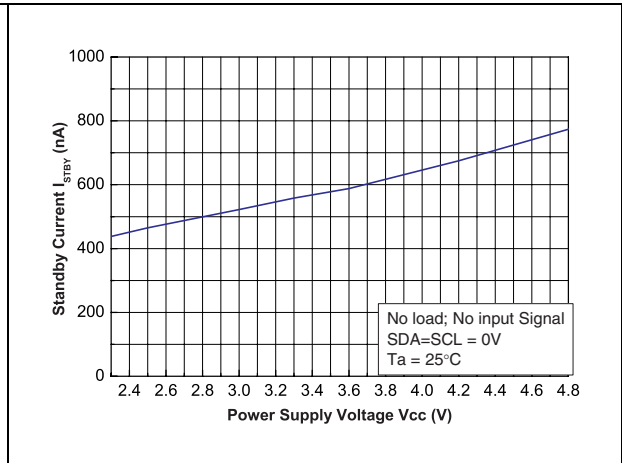


Figure 6. Maximum output power vs. load

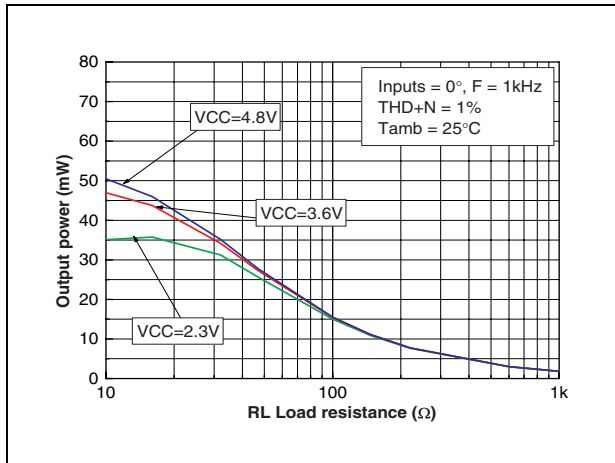


Figure 7. Maximum output power vs. load

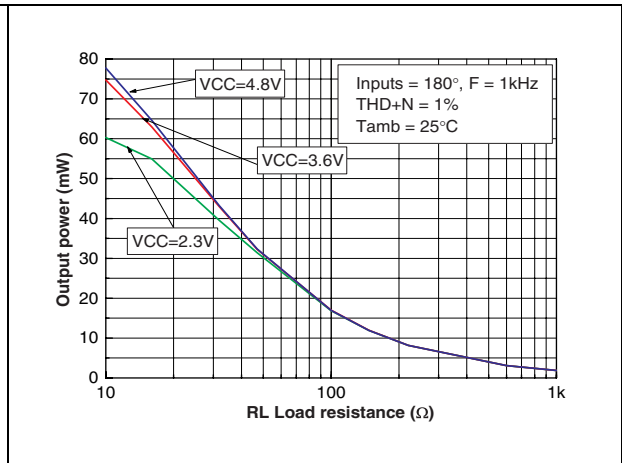


Figure 8. Maximum output power vs. power supply voltage

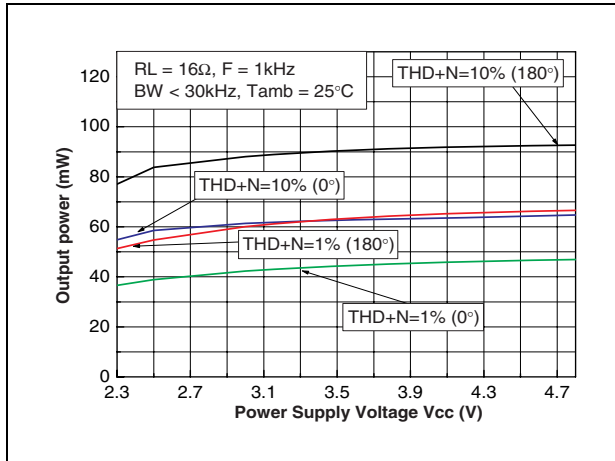


Figure 9. Maximum output power vs. power supply voltage

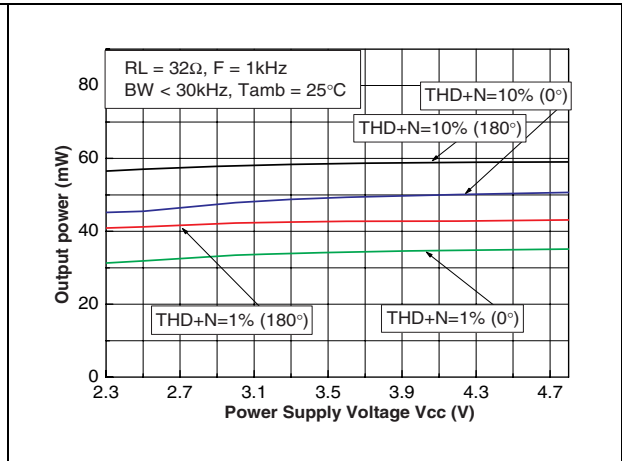


Figure 10. Maximum output power vs. power supply voltage

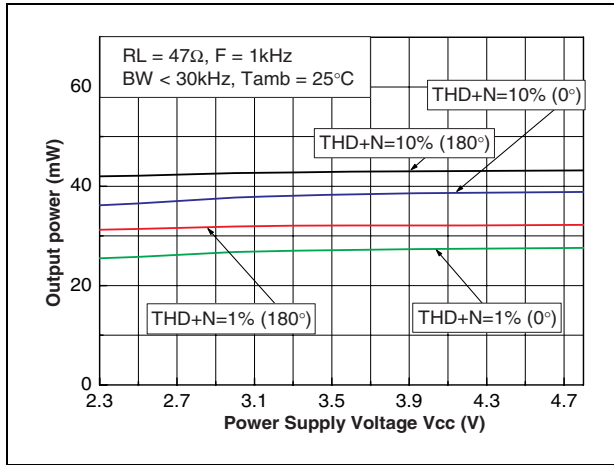


Figure 11. Maximum output voltage vs. power supply voltage

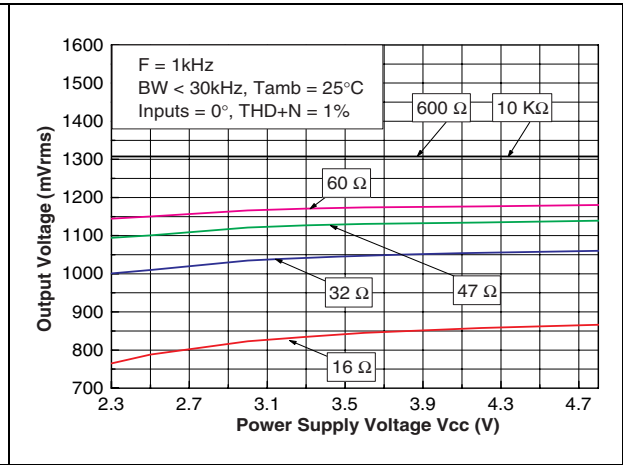


Figure 12. Maximum output voltage vs. power supply voltage

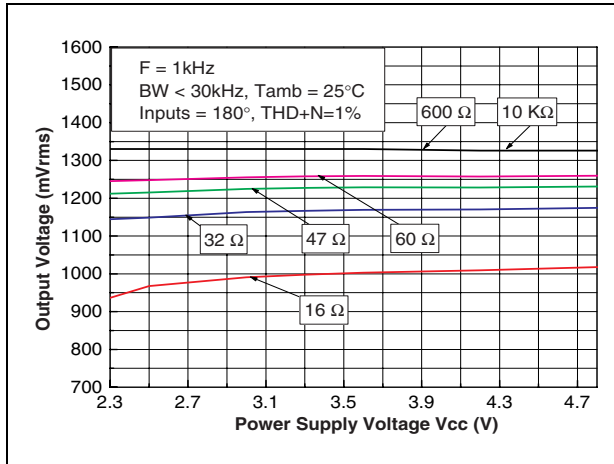


Figure 13. Current consumption vs. total output power

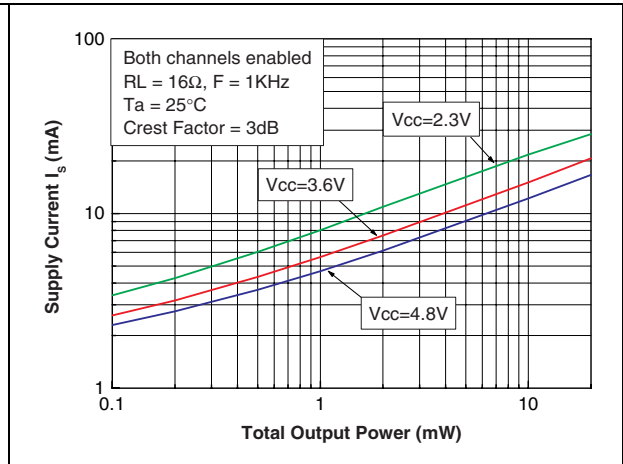


Figure 14. Current consumption vs. total output power

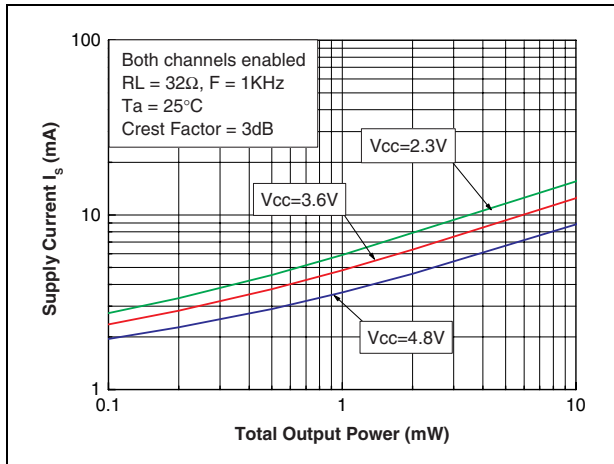


Figure 15. Current consumption vs. total output power

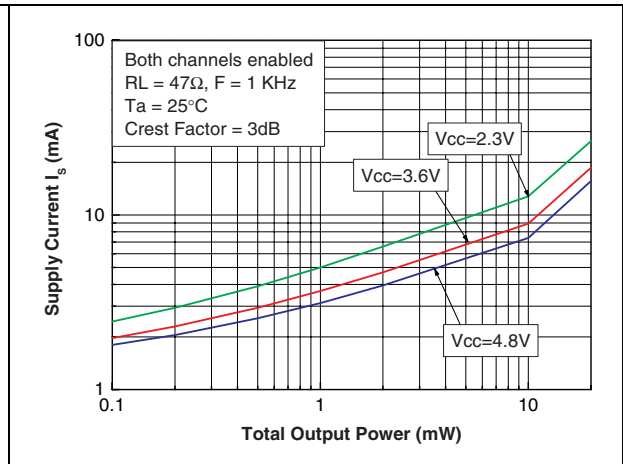


Figure 16. Current consumption vs. total output power

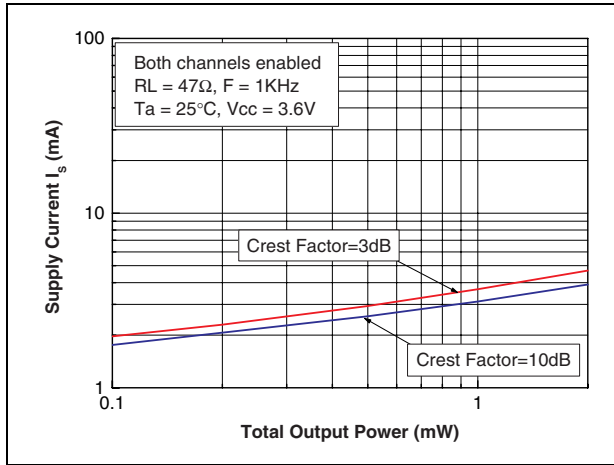


Figure 17. Power dissipation vs. total output power

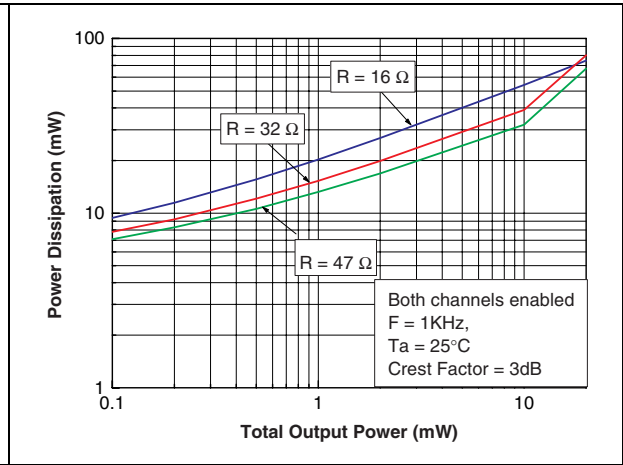


Figure 18. Output impedance vs. frequency

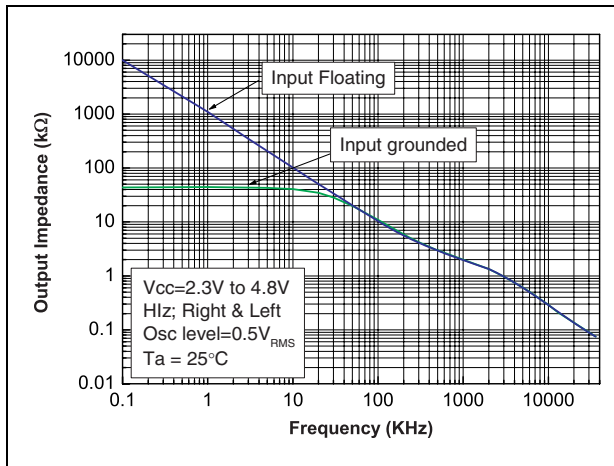


Figure 19. Differential input impedance vs. gain

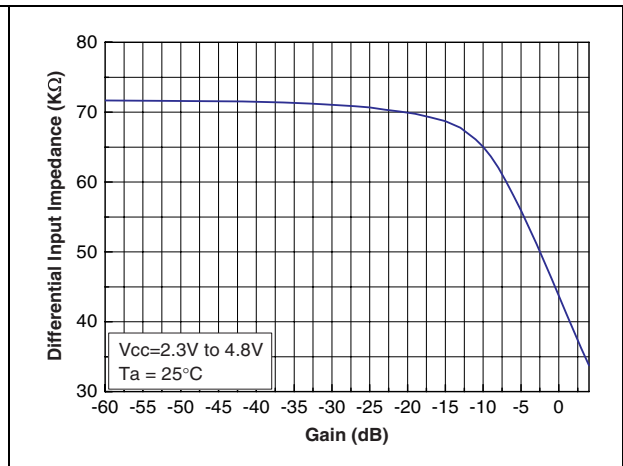


Figure 20. THD+N vs. output power

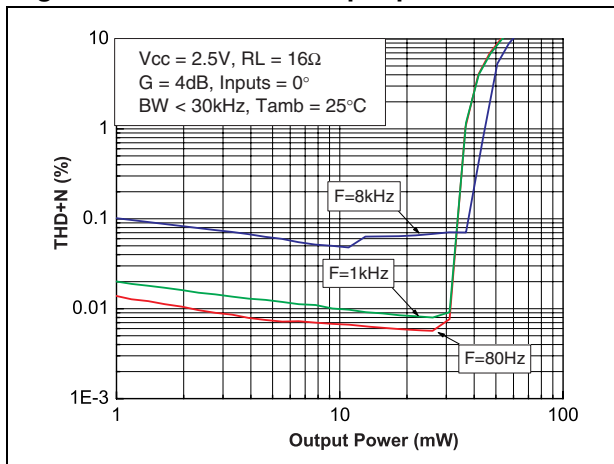


Figure 21. THD+N vs. output power

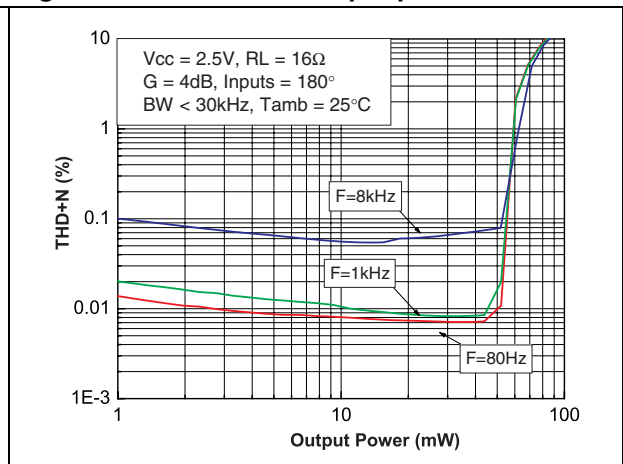


Figure 22. THD+N vs. output power

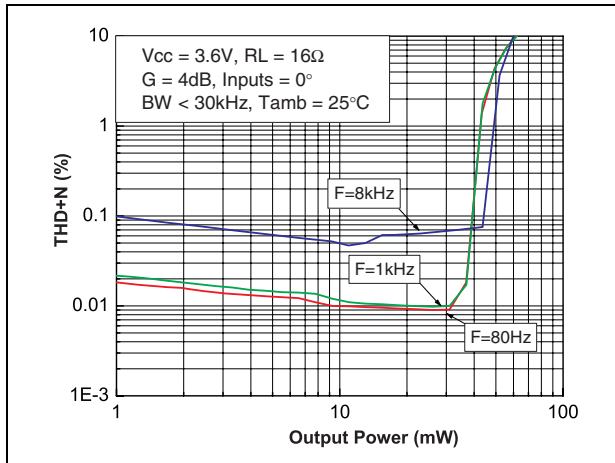


Figure 23. THD+N vs. output power

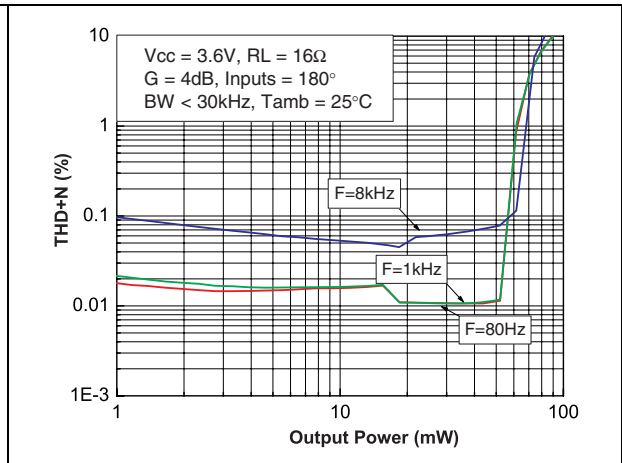


Figure 24. THD+N vs. output power

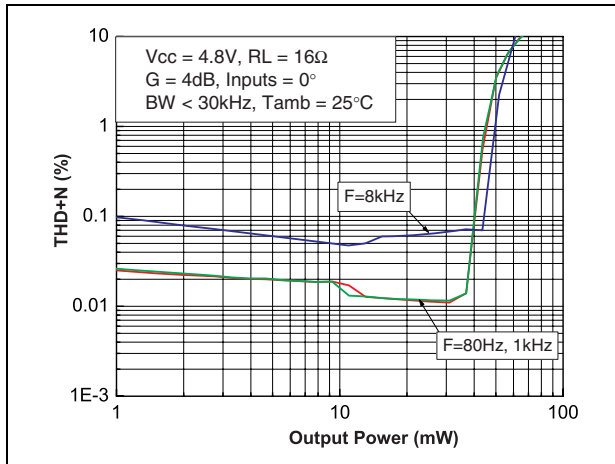


Figure 25. THD+N vs. output power

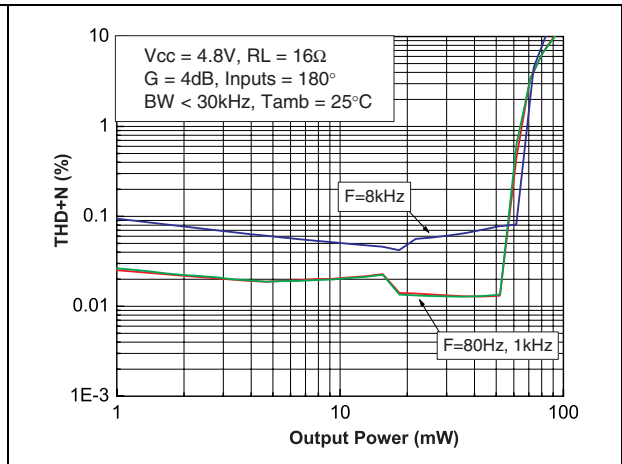


Figure 26. THD+N vs. output power

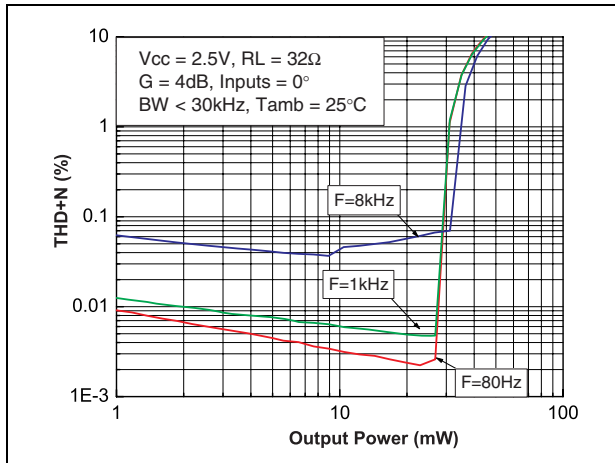


Figure 27. THD+N vs. output power

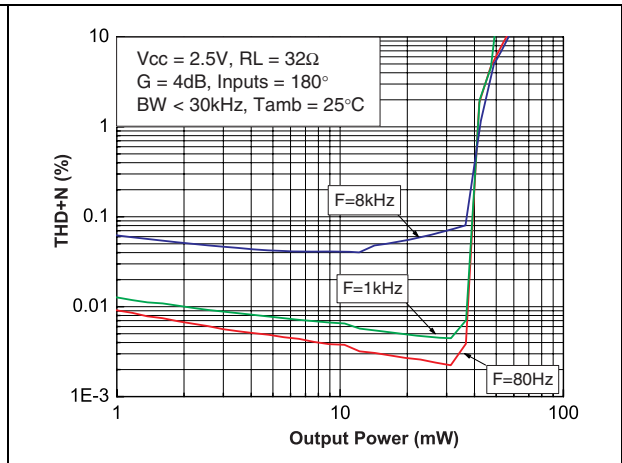


Figure 28. THD+N vs. output power

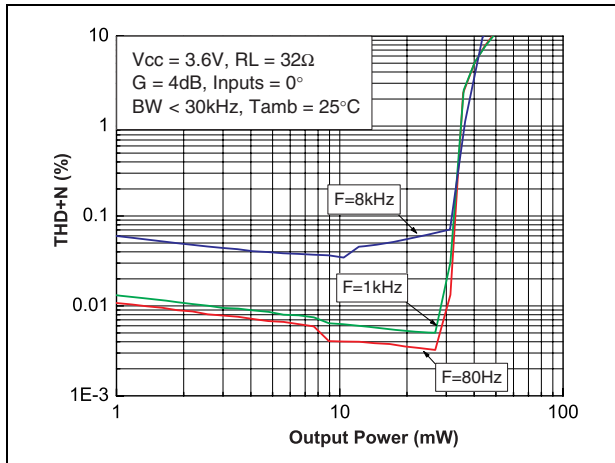


Figure 29. THD+N vs. output power

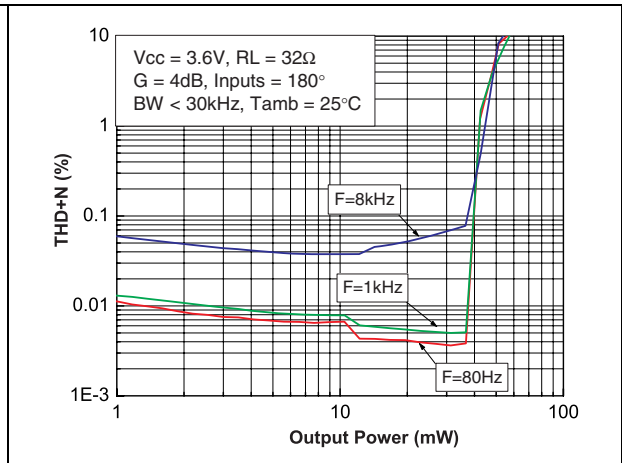


Figure 30. THD+N vs. output power

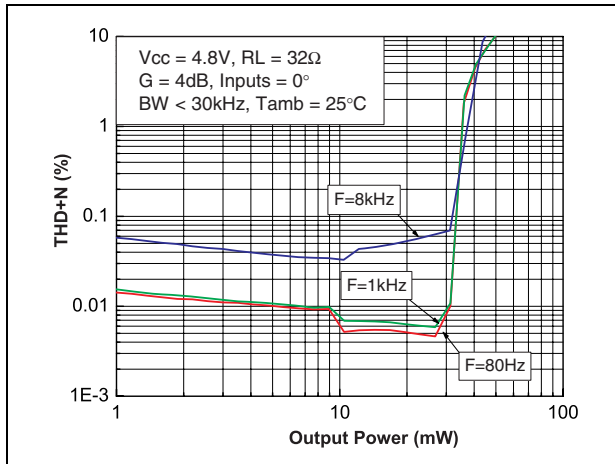


Figure 31. THD+N vs. output power

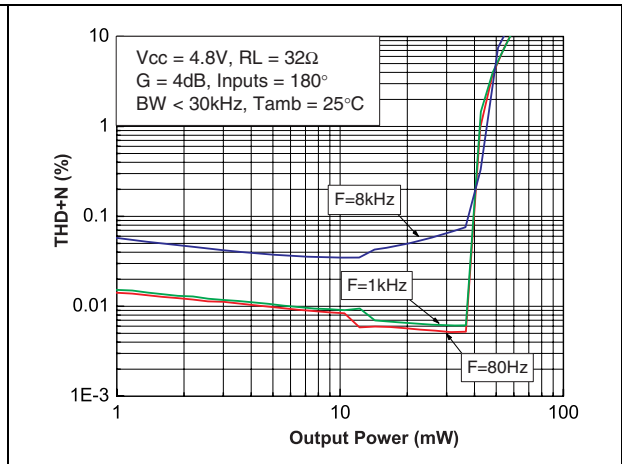


Figure 32. THD+N vs. output power

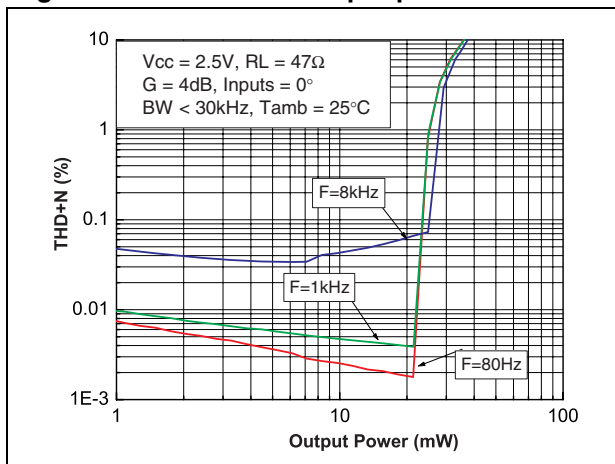


Figure 33. THD+N vs. output power

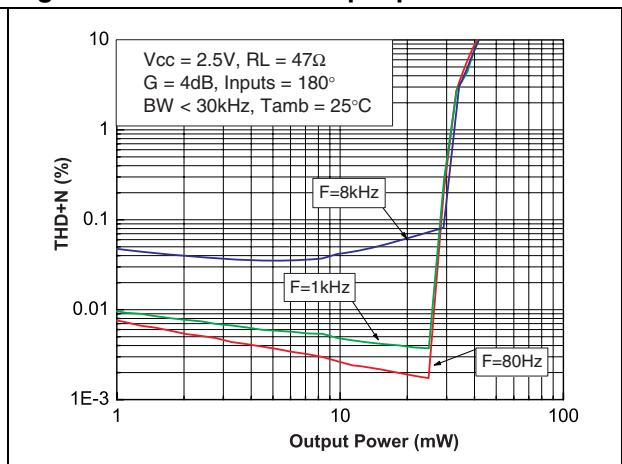


Figure 34. THD+N vs. output power

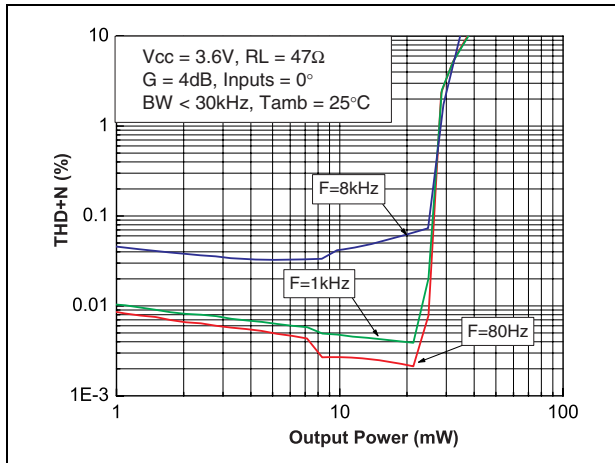


Figure 35. THD+N vs. output power

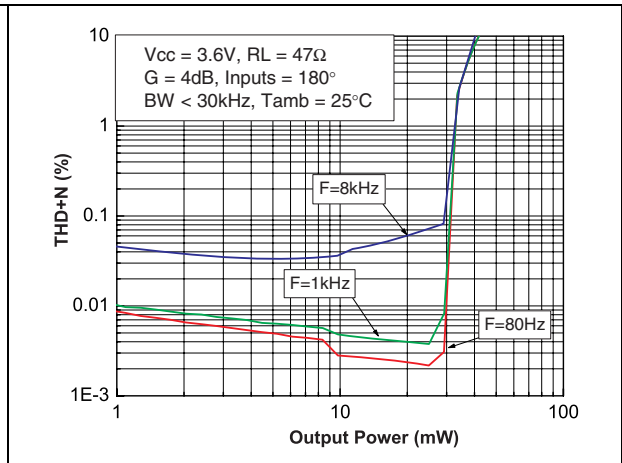


Figure 36. THD+N vs. output power

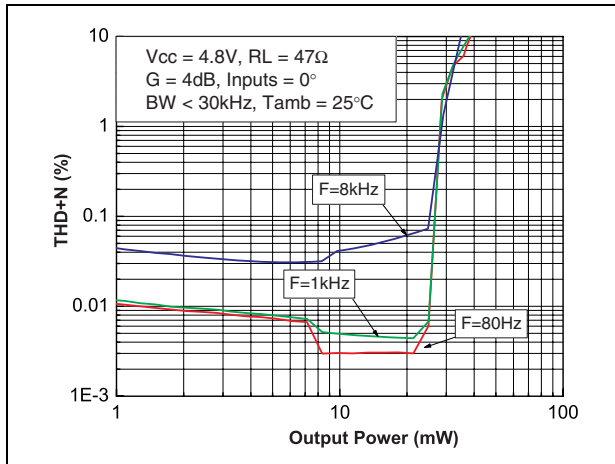


Figure 37. THD+N vs. output power

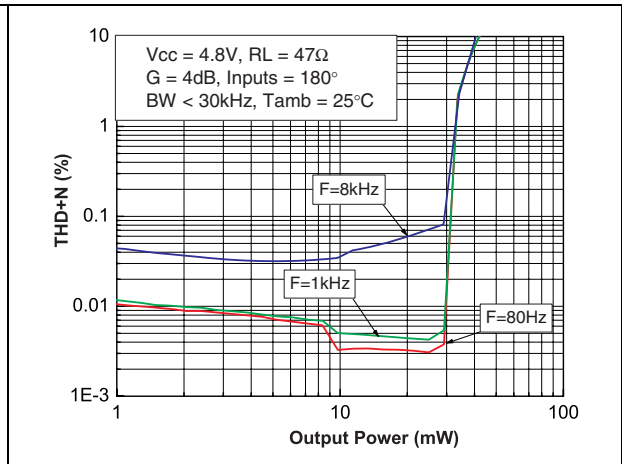


Figure 38. THD+N vs. frequency

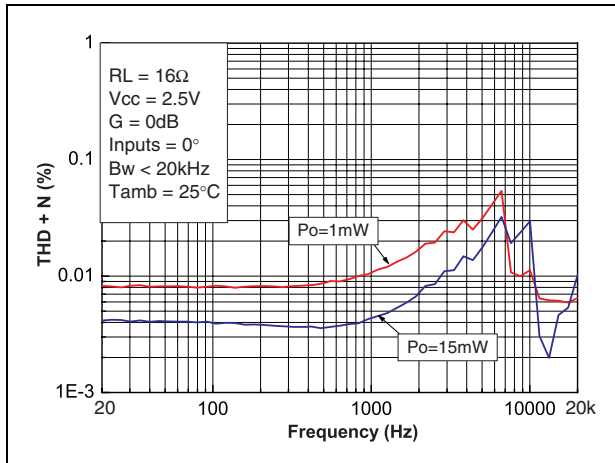


Figure 39. THD+N vs. frequency

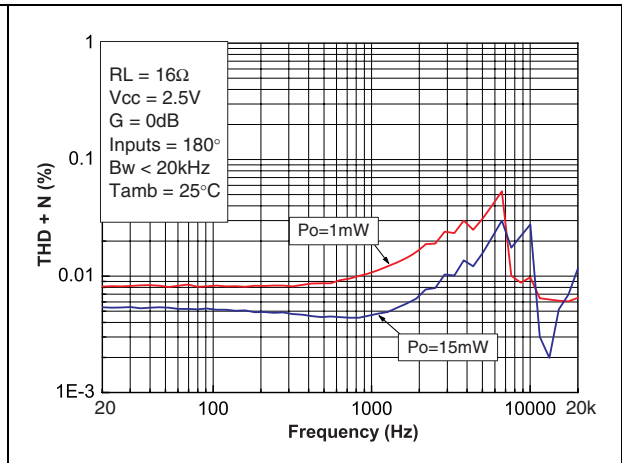


Figure 40. THD+N vs. frequency

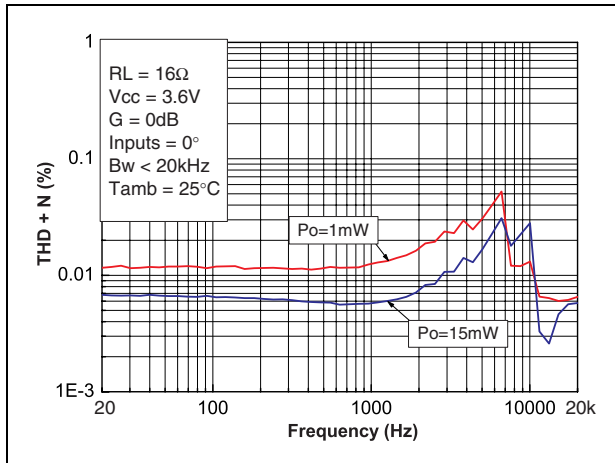


Figure 41. THD+N vs. frequency

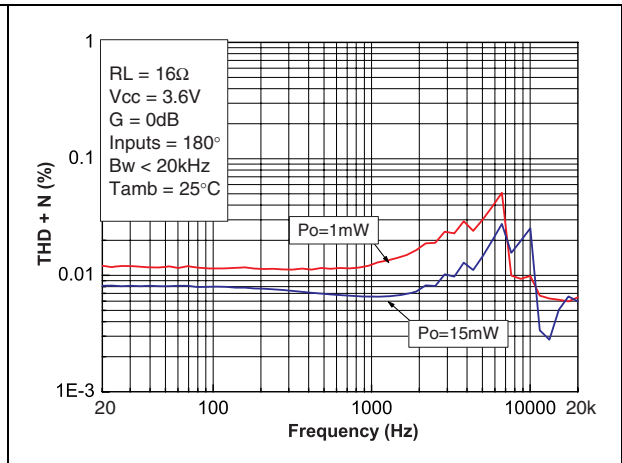


Figure 42. THD+N vs. frequency

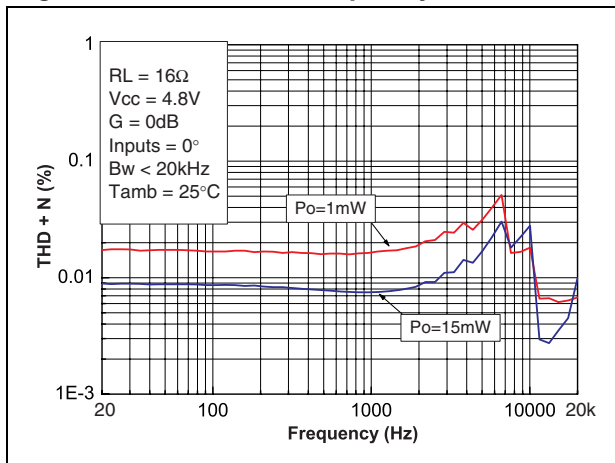


Figure 43. THD+N vs. frequency

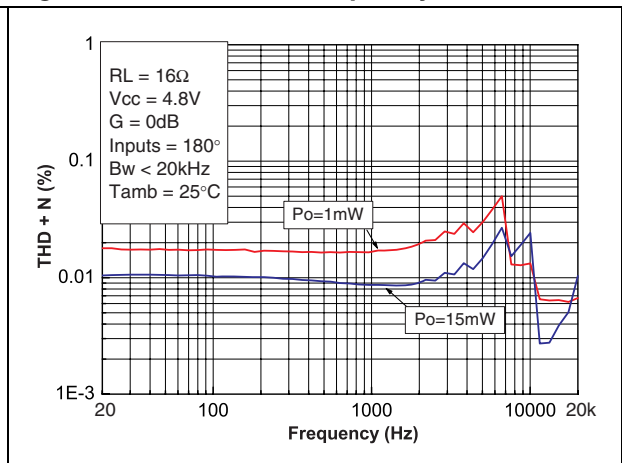


Figure 44. THD+N vs. frequency

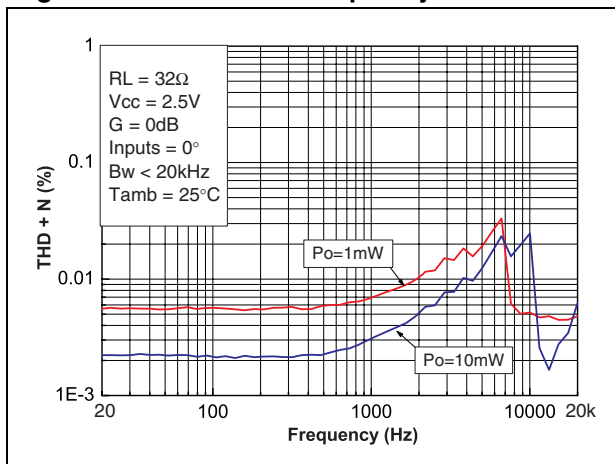


Figure 45. THD+N vs. frequency

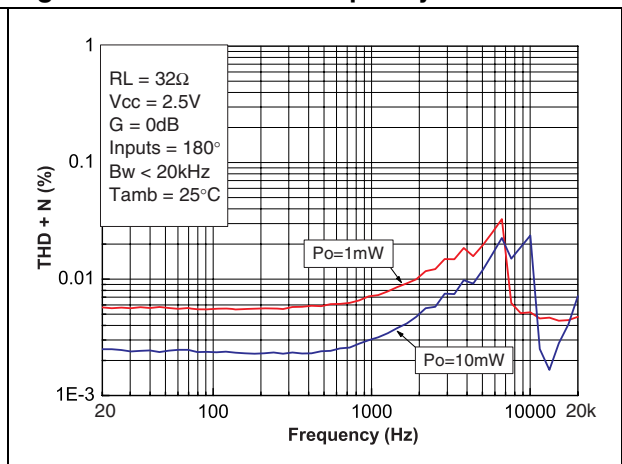




Figure 46. THD+N vs. frequency

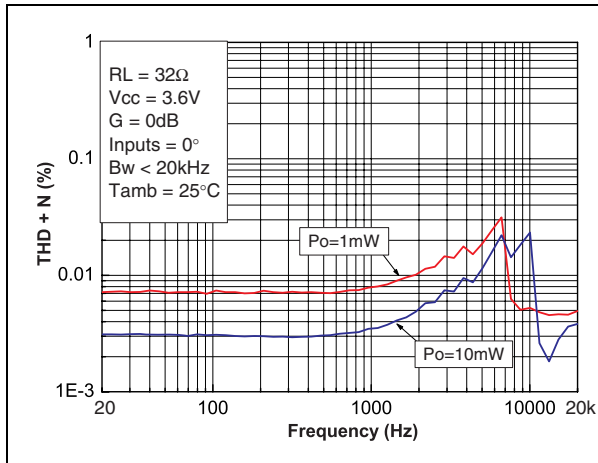


Figure 47. THD+N vs. frequency

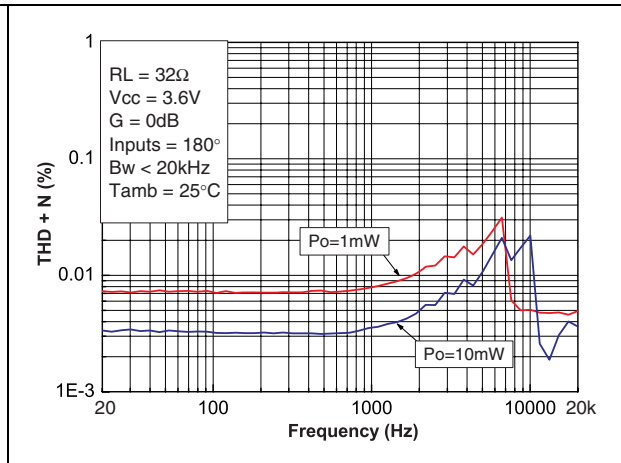


Figure 48. THD+N vs. frequency

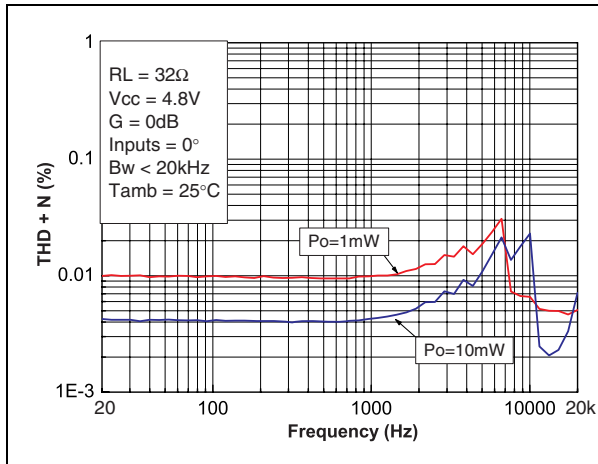


Figure 49. THD+N vs. frequency

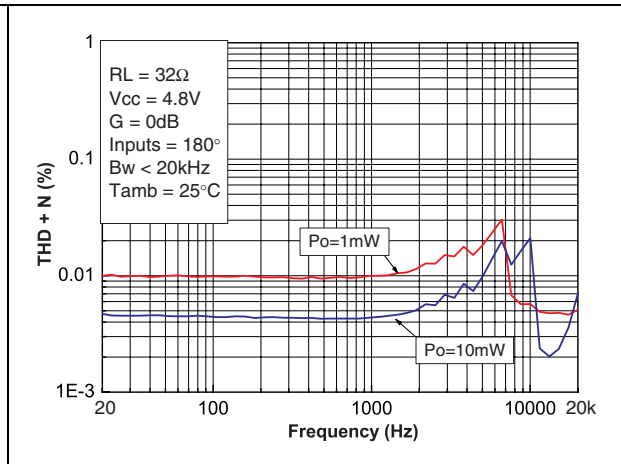


Figure 50. THD+N vs. frequency

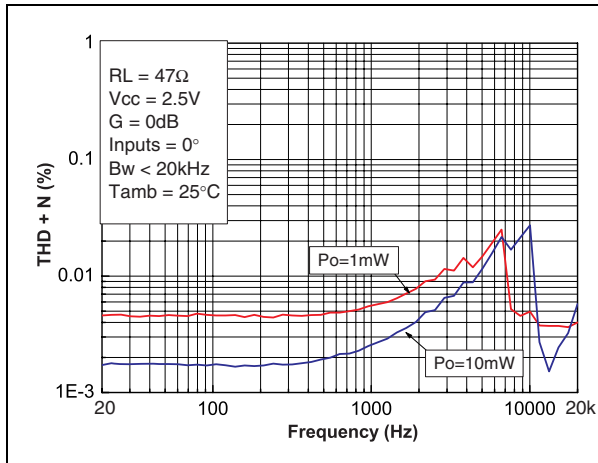


Figure 51. THD+N vs. frequency

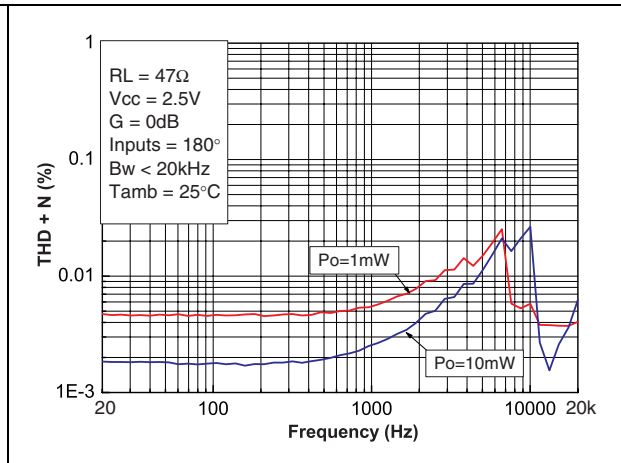


Figure 52. THD+N vs. frequency

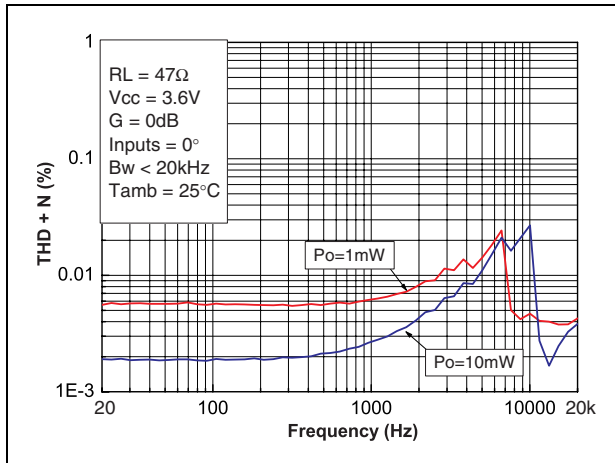


Figure 53. THD+N vs. frequency

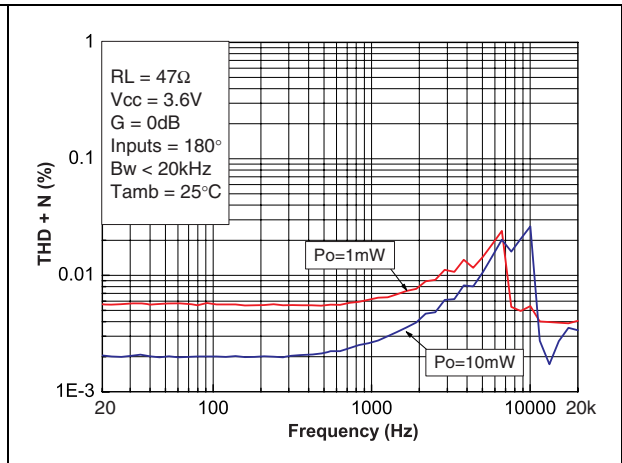


Figure 54. THD+N vs. frequency

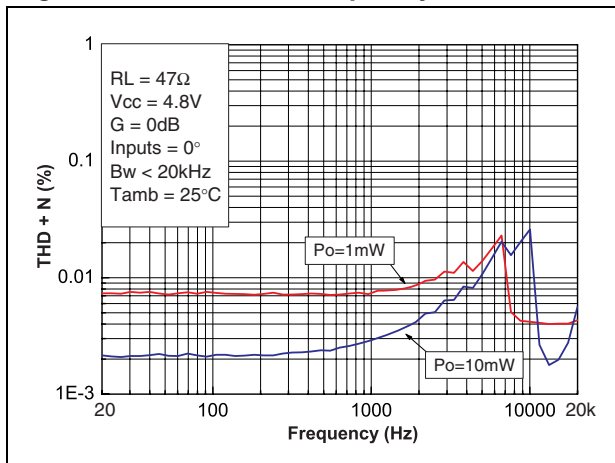


Figure 55. THD+N vs. frequency

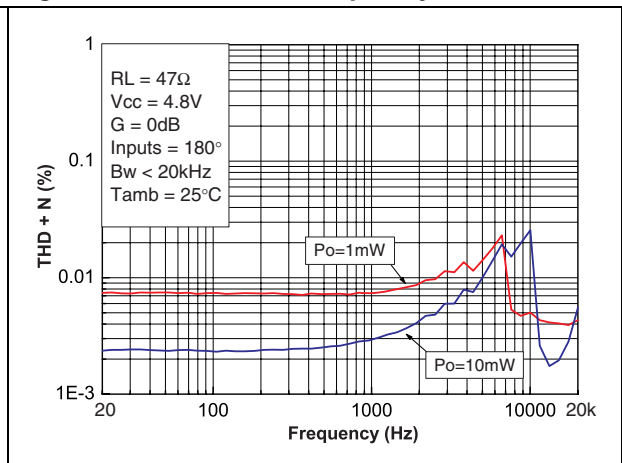


Figure 56. THD+N vs. frequency

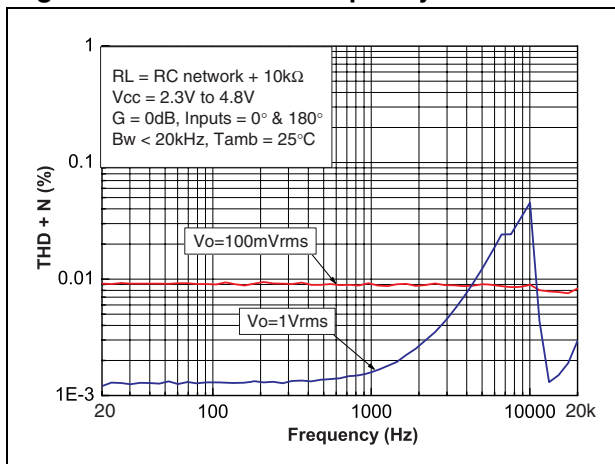


Figure 57. THD+N vs. frequency

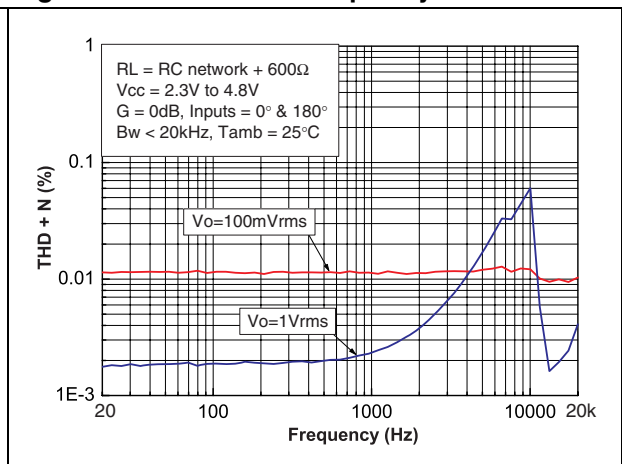


Figure 58. THD+N vs. output voltage

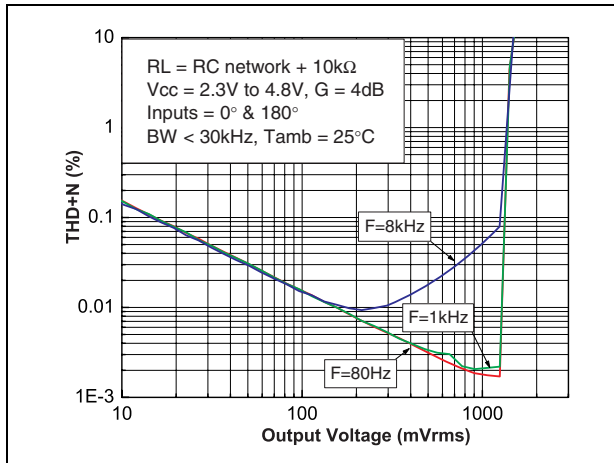


Figure 59. THD+N vs. output voltage

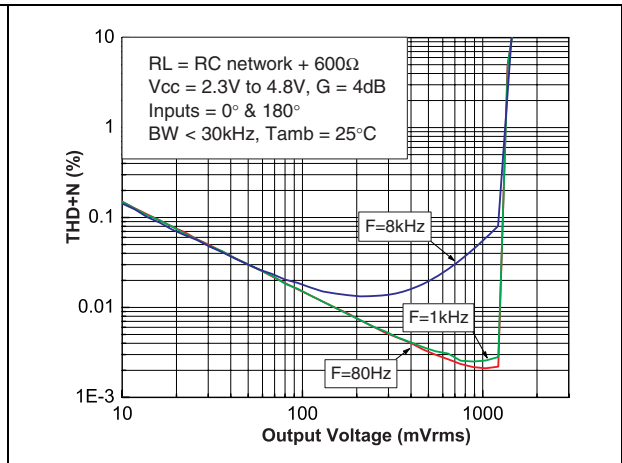


Figure 60. THD+N vs. input voltage, HiZ left and right

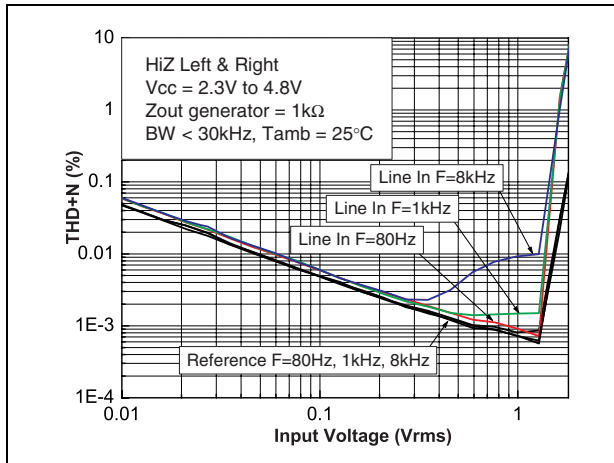


Figure 61. CMRR vs. frequency

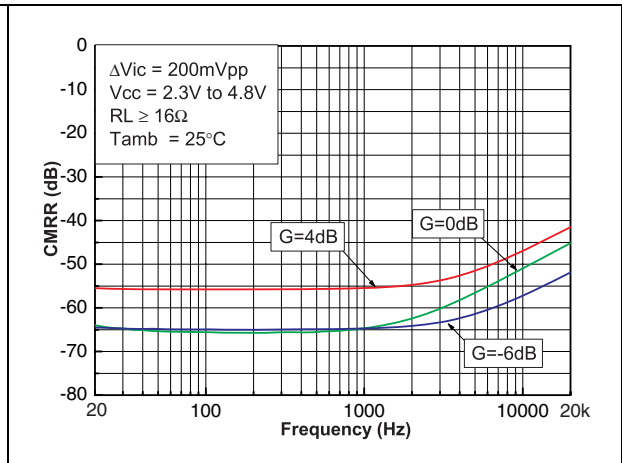


Figure 62. PSRR vs. frequency

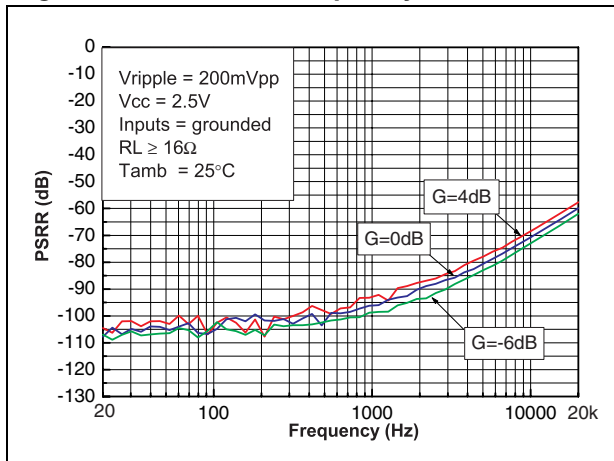


Figure 63. PSRR vs. frequency

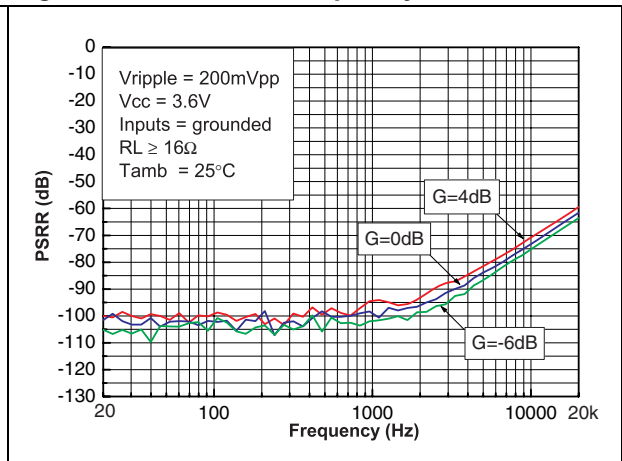


Figure 64. PSRR vs. frequency

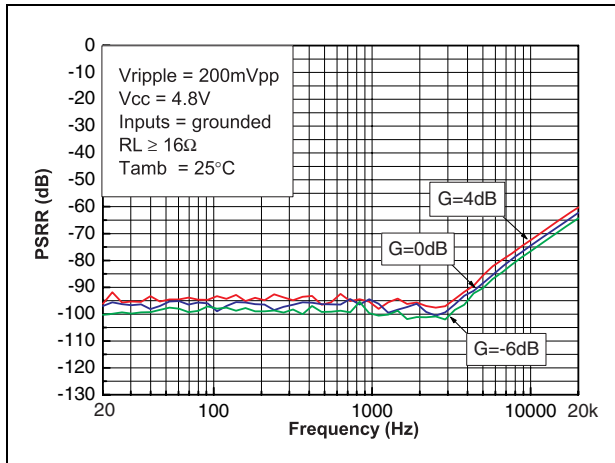


Figure 65. Output signal spectrum

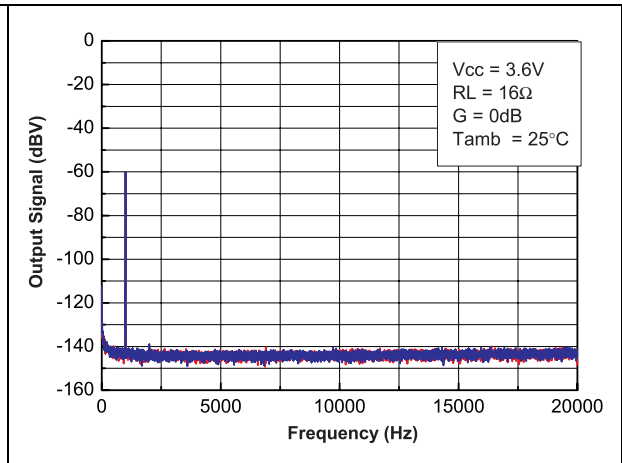


Figure 66. Crosstalk vs. frequency

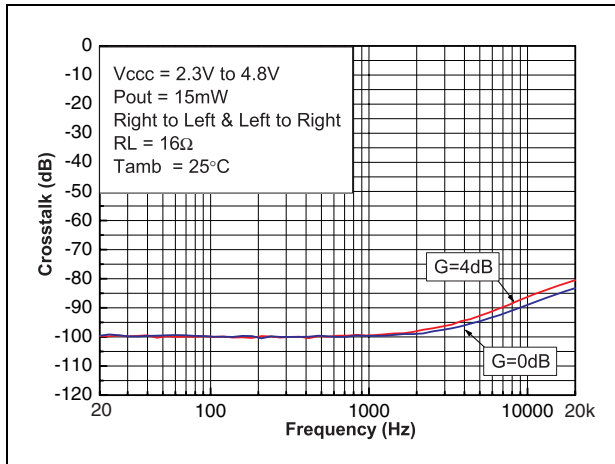


Figure 67. Crosstalk vs. frequency

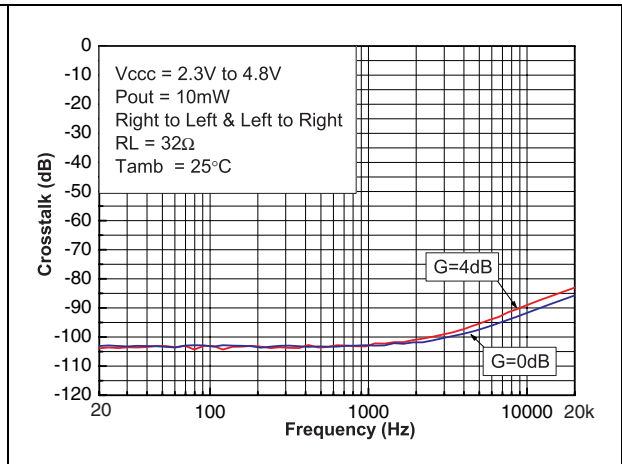


Figure 68. Crosstalk vs. frequency

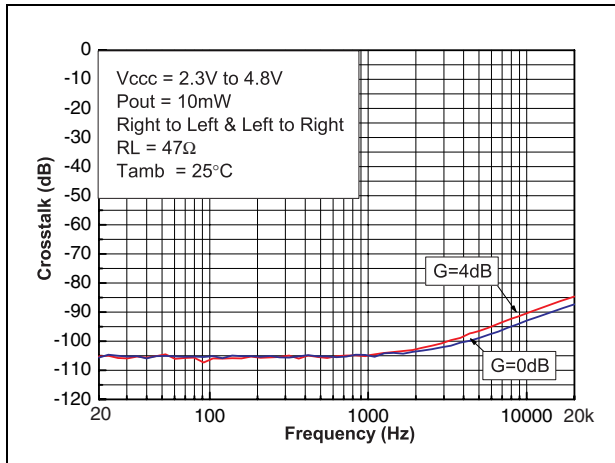


Figure 69. Crosstalk vs. frequency

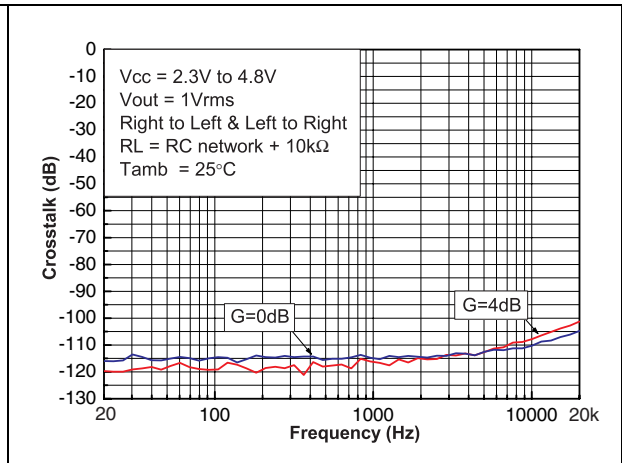


Figure 70. Wake-up time

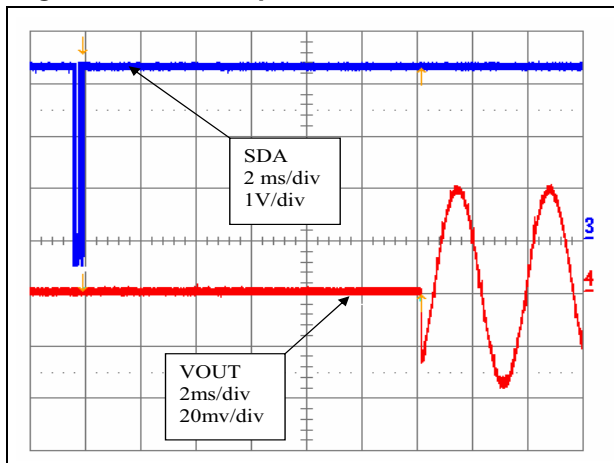
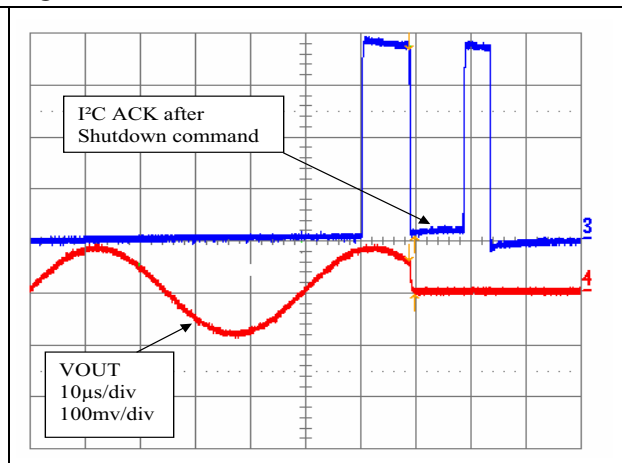


Figure 71. Shutdown time



## 4 Application information

### 4.1 I<sup>2</sup>C bus interface

In compliance with the I<sup>2</sup>C protocol, the TS4621E uses a serial bus to control the chip's functions with the clock (SCL) and data (SDA) wires. These two lines are bi-directional (open collector) and require an external pull-up resistor (typically 10 k $\Omega$ ). The maximum clock frequency in fast mode specified by the I<sup>2</sup>C standard is 400 kHz, which the TS4621E supports. In this application, the TS4621E is always the slave device and the controlling microcontroller MCU is the master device.

The slave address of the TS4621E is 1100 000x (C0h).

[Table 8](#) summarizes the pin descriptions for the I<sup>2</sup>C bus interface.

**Table 8. I<sup>2</sup>C bus interface pin descriptions**

Pin	Functional description
SDA	Serial data pin
SCL	Clock input pin

#### 4.1.1 I<sup>2</sup>C bus operation

The host MCU can write to the TS4621E control register to control the TS4621E, and read from the control register to obtain a configuration from the TS4621E. The TS4621E is addressed by the byte consisting of the 7-bit slave address and the R/ $\overline{W}$  bit.

**Table 9. First byte after the START message for addressing the device**

A6	A5	A4	A3	A2	A1	A0	R/ $\overline{W}$
1	1	0	0	0	0	0	X

There are four control registers ([Table 10](#)) named CR1 to CR4. In read mode, all the control registers can be accessed. In write mode, only CR1, CR2 and CR3 can be addressed.

**Table 10. Summary of control registers**

Description	Register address	D7	D6	D5	D4	D3	D2	D1	D0
CR1	1	HP_EN_L	HP_EN_R	0	0	SC_L	SC_R	T_SH	SWS
CR2 volume control	2	Mute_L	Mute_R	Volume control					0
CR3	3	0	0	0	0	0	0	HiZ_L	HiZ_R
CR4 identification	4	0	1	0	0	0	0	0	0

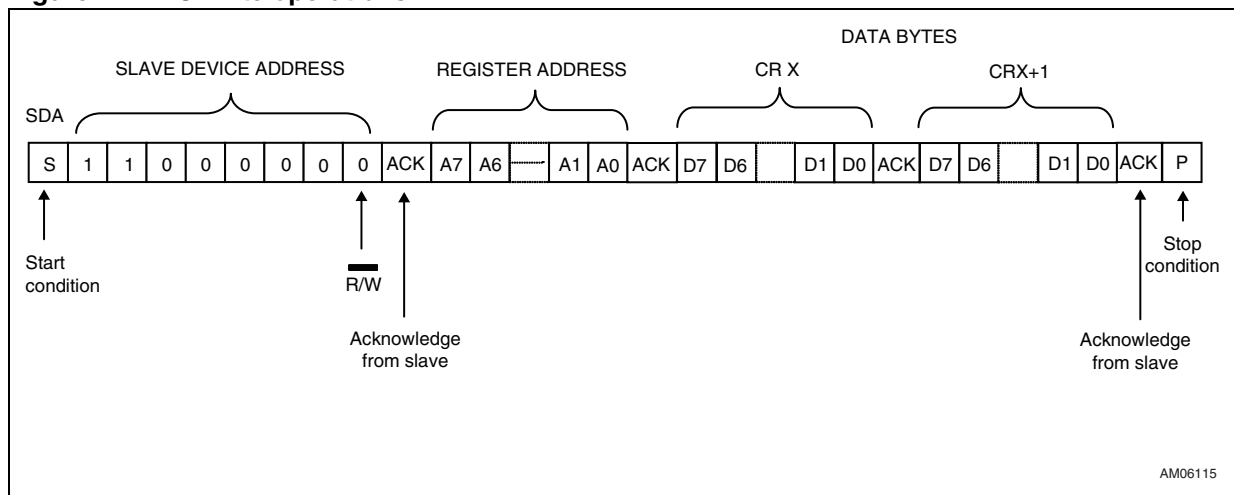
### Writing to the control registers

To write data to the TS4621E, after the "start" message the MCU must:

- send the I<sup>2</sup>C 7-bit slave address and a low level for the R/W bit.
- send the register address to write to.
- send the data bytes (control register settings).

All bytes are sent MSB first. The transfer of written data ends with a "stop" message. When transmitting several data bytes, the data can be written without having to repeat the "start" message or send the byte with the slave address. If several bytes are transmitted, they will be written repeatedly to CR1, CR2 and CR3.

Figure 72. I<sup>2</sup>C write operations



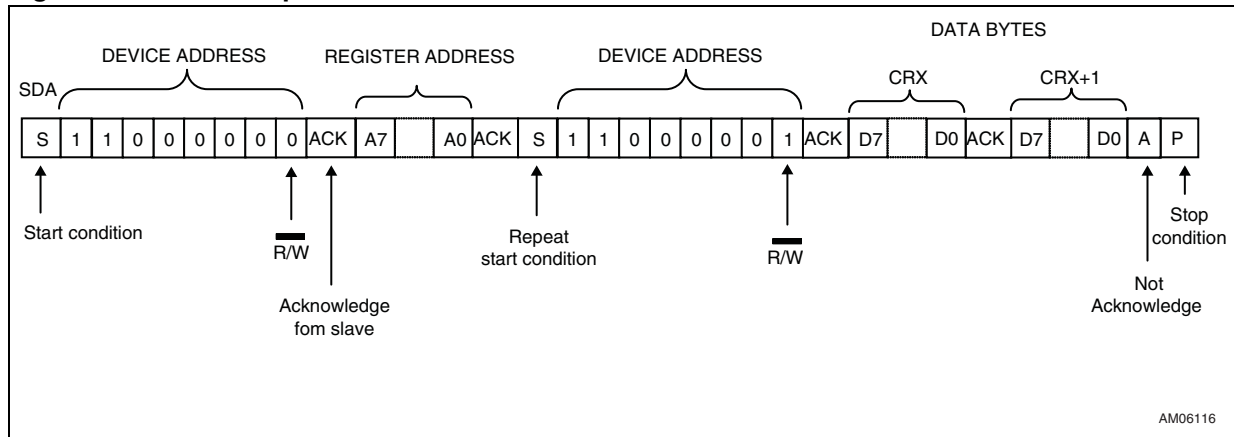
### Reading from the control registers

To read data from the TS4621E, after the "start" message the MCU must:

- send the I<sup>2</sup>C 7-bit slave address and a low level for the R/W bit.
- send the register address to write to.
- send the I<sup>2</sup>C 7-bit slave address and a high level for the R/W bit.
- receive the data (control register value).

All bytes are read MSB first. The transfer of read data ends with a "stop" message. When transmitting several data bytes, the data can be read without having to repeat the "start" message or send the byte with the slave address. If several bytes are transmitted, they will be read repeatedly from CR1, CR2, CR3 and CR4.

Figure 73. I<sup>2</sup>C read operations



### 4.1.2 Control register CR2 - address 2

Table 11. Volume control register CR2 - address 2

Volume control range: -60 dB to +4 dB											
D5	D4	D3	D2	D1	Gain (in dB)	D5	D4	D3	D2	D1	Gain (in dB)
0	0	0	0	0	-60 dB	1	0	0	0	0	-11 dB
0	0	0	0	1	-54 dB	1	0	0	0	1	-10 dB
0	0	0	1	0	-50.5 dB	1	0	0	1	0	-9 dB
0	0	0	1	1	-47 dB	1	0	0	1	1	-8 dB
0	0	1	0	0	-43 dB	1	0	1	0	0	-7 dB
0	0	1	0	1	-39 dB	1	0	1	0	1	-6 dB
0	0	1	1	0	-35 dB	1	0	1	1	0	-5 dB
0	0	1	1	1	-31 dB	1	0	1	1	1	-4 dB
0	1	0	0	0	-27 dB	1	1	0	0	0	-3 dB
0	1	0	0	1	-25 dB	1	1	0	0	1	-2 dB
0	1	0	1	0	-23 dB	1	1	0	1	0	-1 dB
0	1	0	1	1	-21 dB	1	1	0	1	1	0 dB
0	1	1	0	0	-19 dB	1	1	1	0	0	+1 dB
0	1	1	0	1	-17 dB	1	1	1	0	1	+2 dB
0	1	1	1	0	-15 dB	1	1	1	1	0	+3 dB
0	1	1	1	1	-13 dB	1	1	1	1	1	+4 dB

#### Mute function: bits MUTE\_L and MUTE\_R

In the volume register, MUTE\_L and MUTE\_R are dedicated to enabling the mute function, independently of the channel. When MUTE\_L and MUTE\_R are set to V<sub>IH</sub>, the mute function is enabled on the corresponding channel and the gain is set to -80 dB. When MUTE\_L and MUTE\_R are set to V<sub>IL</sub>, the I<sup>2</sup>C gain level is applied to the channel.



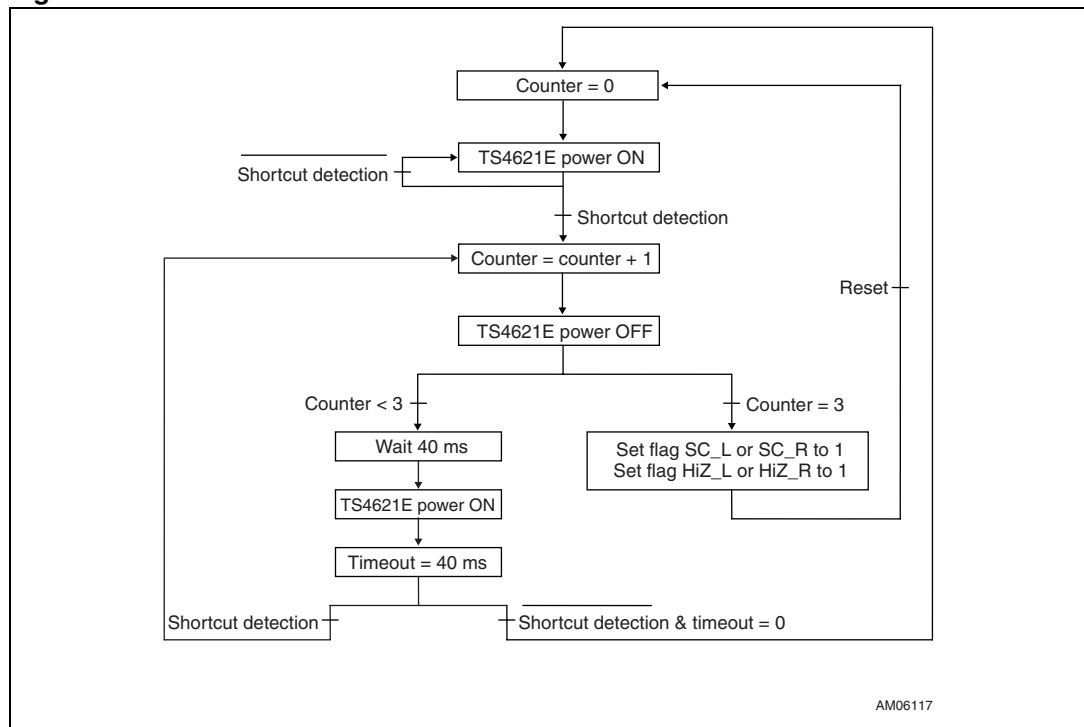
### 4.1.3 Control register CR1 - address 1

#### Amplifier output short-circuit detection: bits SC\_L and SC\_R

The amplifier's outputs are protected from short-circuits that might accidentally occur during manipulation of the device. In a typical application, if a short-circuit arises on the jack plug, there will be no detection because of the serial resistor present on the amplifier output, thus the output current threshold will not be reached.

To be active, the detection has to occur directly on the amplifier's output with a signal modulation on the inputs of the TS4621E. This detection is depicted in [Figure 74](#).

**Figure 74. Flowchart for short-circuit detection**



If a short-circuit is detected three consecutive times on one channel, a flag is raised in the I<sup>2</sup>C read register CR1.

- SC\_L: equals 0 during normal operation, equals 1 when a short-circuit is detected on the left channel.
- SC\_R: equals 0 during normal operation, equals 1 when a short-circuit is detected on the right channel.

The corresponding channel's output stage is then set to high impedance mode. An I<sup>2</sup>C read command allows the reading of the SC\_L and SC\_R flags but does not reset them. An I<sup>2</sup>C write command has to be sent to CR1 to reset the flags to 0 and restore normal operation.

**Thermal shutdown protection: bit T\_SH**

A thermal shutdown protection is implemented to protect the device from overheating. If the temperature rises above the thermal junction of 150°C, the device is put into standby mode and a flag is raised in the read register CR1.

- T\_SH: equals 0 during normal operation, equals 1 when a thermal shutdown is detected.

When the temperature decreases to safe levels, the circuit switches back to normal operation and the corresponding flag is cleared.

**Software shutdown: bit SWS**

When SWS equals 1, the device is set to I<sup>2</sup>C software shutdown. When SWS equals 0, the negative supply and buck converters are activated.

**Channel activation: bits HP\_EN\_L and HP\_EN\_R**

When HP\_EN\_L or HP\_EN\_R equals 1, the corresponding amplifier channel is enabled.

## 4.2 Wake-up and standby time definition

The wake-up time of the TS4621E is guaranteed at 12 ms typical (refer to [Chapter 3: Electrical characteristics on page 7](#)). However, since the TS4621E is activated with an I<sup>2</sup>C bus, the wake-up start procedure is as follows.

1. The master sends a start bit.
2. The master sends the device address.
3. The slave (TS4621E) answers by an acknowledge bit.
4. The master sends the register address.
5. The slave (TS4621E) answers by an acknowledge bit.
6. The master sends the output mode configuration (CR1).
7. If the TS4621E was previously in standby mode, the wake-up starts on the falling edge of the eighth clock signal (SCL) corresponding to the CR1 byte.
8. After 12 ms (de-pop sequence time), the TS4621E outputs are operational.

The standby time is guaranteed as 100 μs typical (refer to [Chapter 3: Electrical characteristics on page 7](#)). However, since the TS4621E is de-activated with an I<sup>2</sup>C bus, the standby time operates as follows.

1. The master sends a start bit.
2. The master sends the device address.
3. The slave (TS4621E) answers by an acknowledge bit.
4. The master sends the register address.
5. The slave (TS4621E) answers by an acknowledge bit.
6. The master sends the output mode configuration (CR1), which corresponds, in this case, to standby mode.
7. The standby time starts on the falling edge of the eighth clock signal (SCL) corresponding to the CR1 byte.
8. After 100 μs, the TS4621E is in standby mode.

### 4.3 Common mode sense

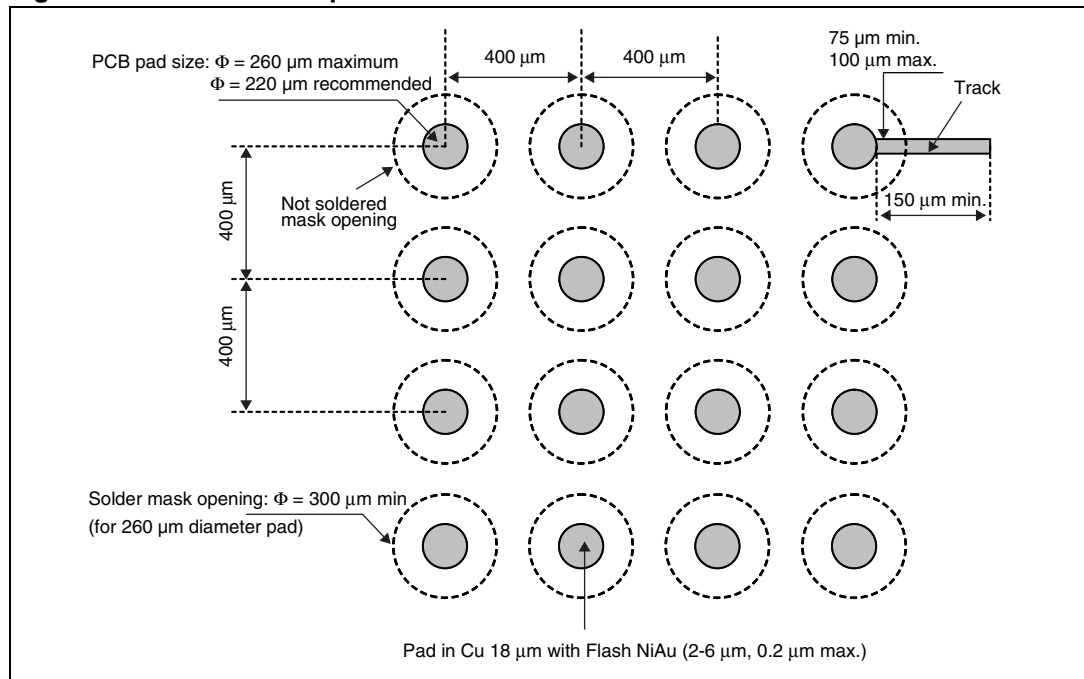
The TS4621E implements a common-mode sense pin to correct any voltage differences that might occur between the return of the headphone jack and the GND of the device and create parasitic noise in the headphone and/or line out.

The solution to strongly reduce and practically eliminate this noise consists in connecting the headphone jack ground to the CMS pin. This pin senses the difference of potential (voltage noise) between the TS4621E ground and the headphone ground. By way of the frequency response of the common-mode sense pin, this noise is removed from the TS4621E outputs.

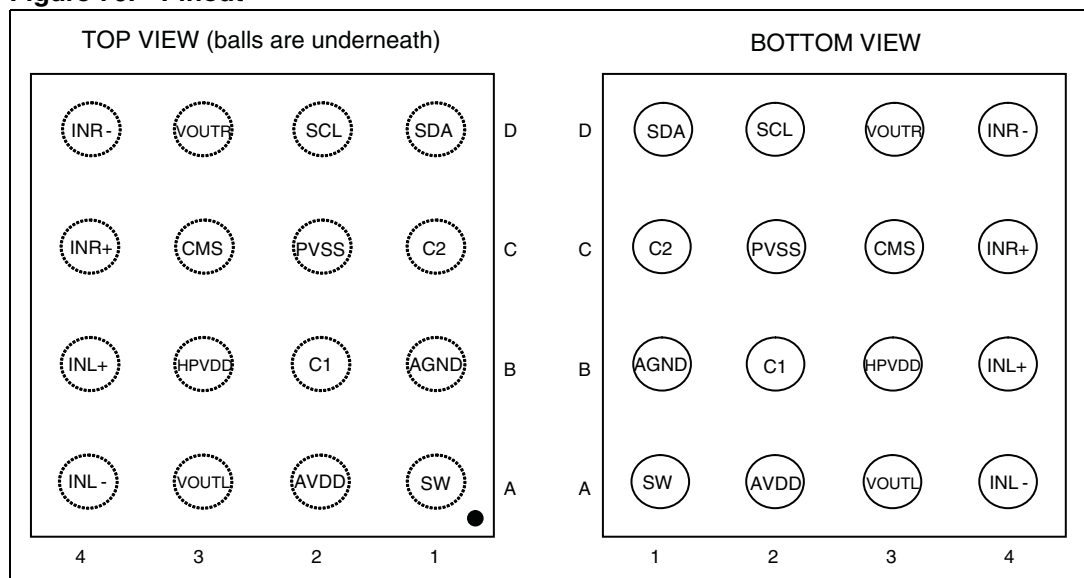
## 5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

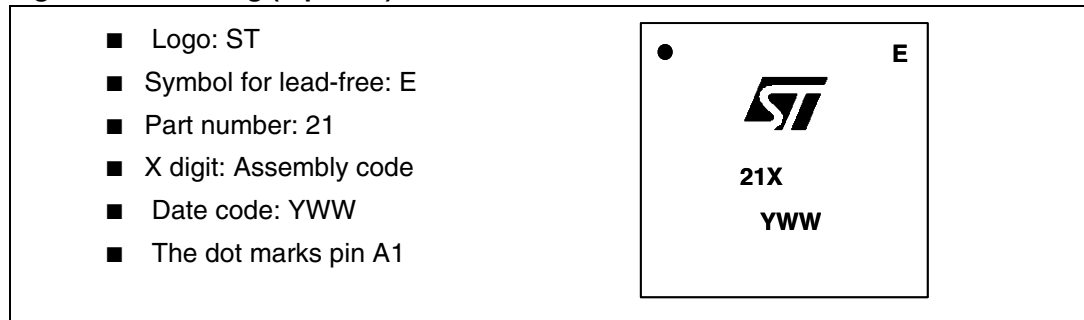
**Figure 75. TS4621E footprint recommendation**



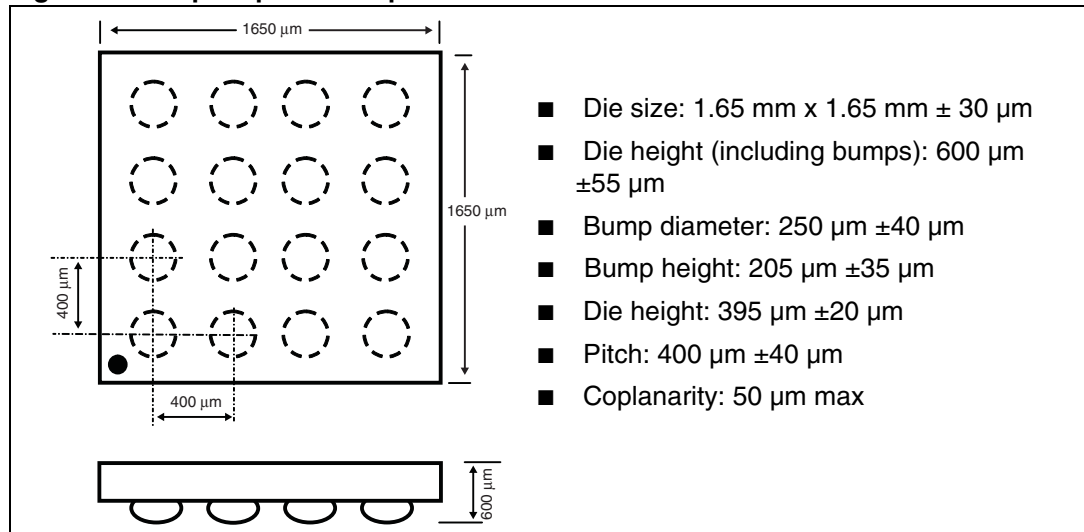
**Figure 76. Pinout**



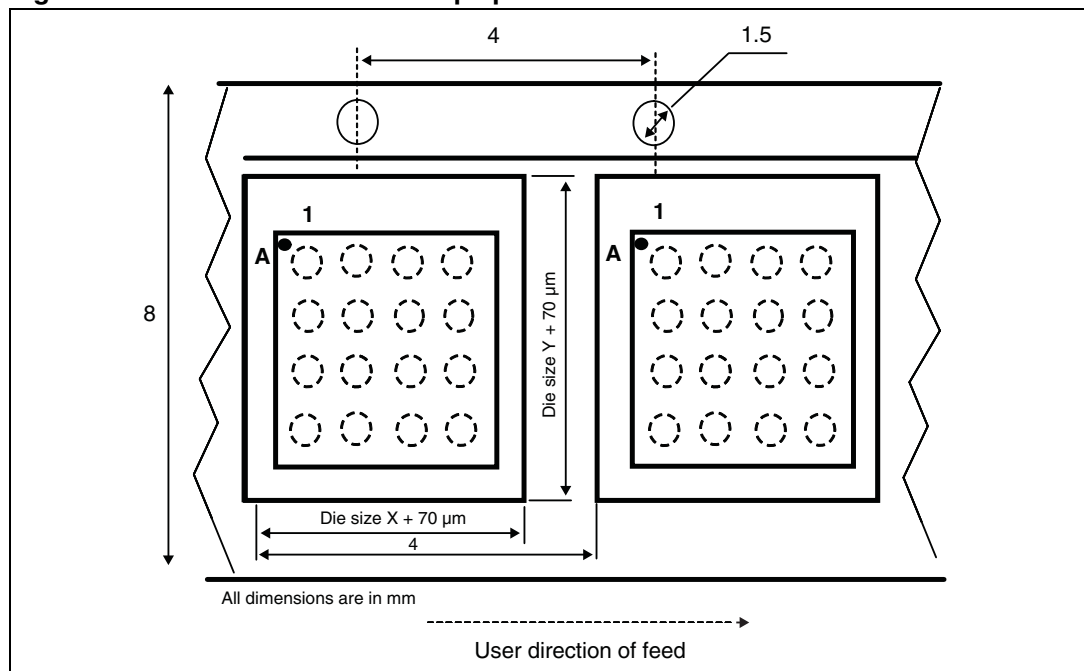
**Figure 77. Marking (top view)**



**Figure 78. Flip-chip - 16 bumps**



**Figure 79. Device orientation in tape pocket**



## 6 Ordering information

**Table 12. Order codes**

Order code	Temperature range	Package	Packing	Marking
TS4621EIJT	-40°C to +85°C	Flip-chip	Tape & reel	21

## 7 Revision history

**Table 13. Document revision history**

Date	Revision	Changes
06-Sep-2011	1	Initial release.

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