LF351

Wide bandwidth single JFET operational amplifiers

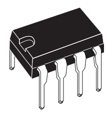
Features

- Internally adjustable input offset voltage
- Low power consumption
- Wide common-mode (up to V_{CC}^{+}) and differential voltage range
- Low input bias and offset current
- Output short-circuit protection
- High input impedance JFET input stage
- Internal frequency compensation
- Latch up free operation
- High slew rate 16 V/µs (typical)

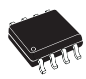
Description

These circuits are high speed JFET input single operational amplifiers incorporating well matched, high voltage JFET and bipolar transistors in a monolithic integrated circuit.

The devices feature high slew rates, low input bias and offset currents, and low offset voltage temperature coefficient.

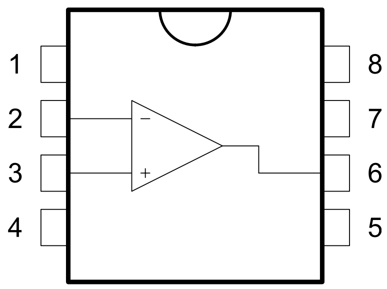


N
DIP8
(Plastic package)



D
SO-8
(Plastic micro package)

Pin connections
(top view)



1 - Offset null 1
2 - Inverting input
3 - Non-inverting input
4 - V_{CC}-
5 - Offset null 2
6 - Output
7 - V_{CC}+
8 - N.C.

1 Schematics

Figure 1. Schematic diagram

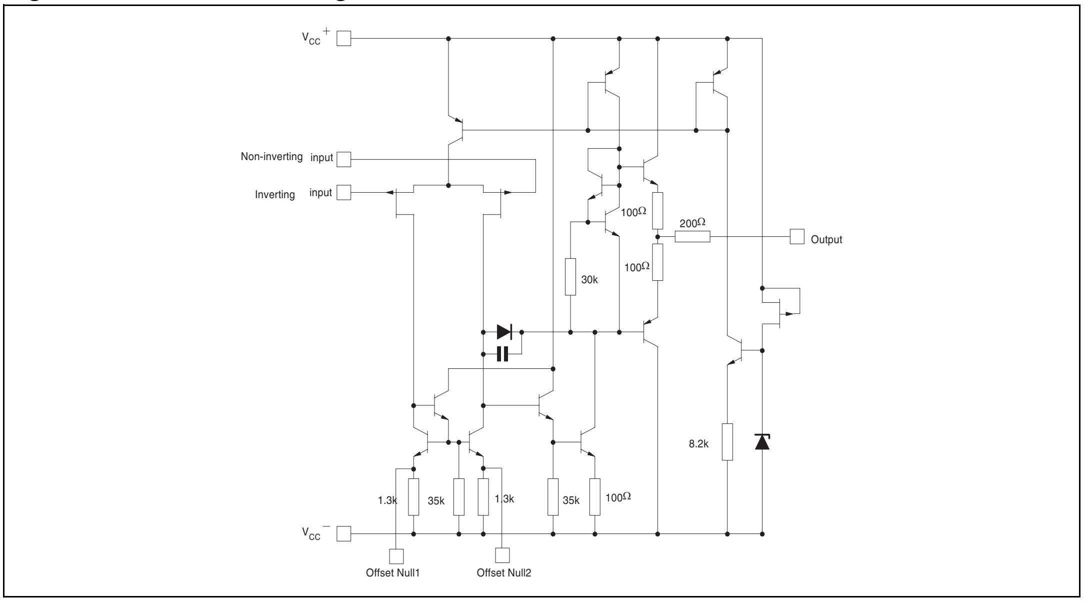
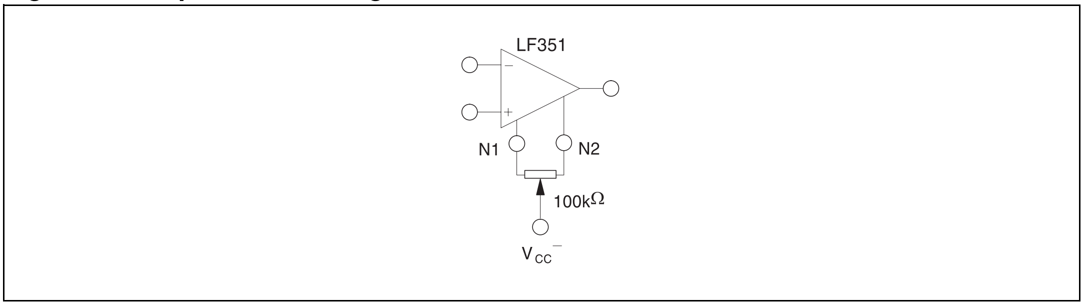


Figure 2. Input offset voltage null circuit



2 Absolute maximum ratings and operating conditions

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage(1)	±18	V
V_i	Input voltage(2)	±15	V
V_{id}	Differential input voltage(3)	±30	V
R_{thja}	Thermal resistance junction to ambient(4) SO-8 DIP8	 125 85	°C/W
R_{thjc}	Thermal resistance junction to case(4) SO-8 DIP8	 40 41	°C/W
	Output short-circuit duration(5)	Infinite	
T_{stg}	Storage temperature range	-65 to +150	°C
ESD	HBM: human body model(6)	500	V
	MM: machine model(7)	200	V
	CDM: charged device model(8)	1.5	kV

1. All voltage values, except differential voltage, are with respect to the zero reference level (ground) of the supply voltages where the zero reference level is the midpoint between V_{CC}^+ and V_{CC}^-.
2. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
3. Differential voltages are the non-inverting input terminal with respect to the inverting input terminal.
4. Short-circuits can cause excessive heating and destructive dissipation. Values are typical.
5. The output may be shorted to ground or to either supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded
6. Human body model: A 100 pF capacitor is charged to the specified voltage, then discharged through a 1.5 kΩ resistor between two pins of the device. This is done for all couples of connected pin combinations while the other pins are floating.
7. Machine model: A 200 pF capacitor is charged to the specified voltage, then discharged directly between two pins of the device with no external series resistor (internal resistor < 5 Ω). This is done for all couples of connected pin combinations while the other pins are floating.
8. Charged device model: all pins and the package are charged together to the specified voltage and then discharged directly to the ground through only one pin. This is done for all pins.

Table 2. Operating conditions

Symbol	Parameter	LF151	LF251	LF351	Unit
V_{CC}	Supply voltage		6 to 32		V
T_{oper}	Operating free-air temperature range	-55 to +125	-40 to +105	0 to +70	°C

3 Electrical characteristics

Table 3. Electrical characteristics at V_{CC} = ±15 V, T_{amb} = +25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{io}	Input offset voltage (R_s = 10kΩ) $T_{min} \leq T_{amb} \leq T_{max}$		3	10 13	mV
DV_{io}	Input offset voltage drift		10		µV/°C
I_{io}	Input offset current (1) $T_{min} \leq T_{amb} \leq T_{max}$		5	100 4	pA nA
I_{ib}	Input bias current (1) $T_{min} \leq T_{amb} \leq T_{max}$		20	200 20	pA nA
A_{vd}	Large signal voltage gain (R_L = 2kΩ, V_o = ±10V) $T_{min} \leq T_{amb} \leq T_{max}$	50 25	200		V/mV
SVR	Supply voltage rejection ratio (R_S = 10kΩ) $T_{min} \leq T_{amb} \leq T_{max}$	80 80	86		dB
I_{CC}	Supply current, no load $T_{min} \leq T_{amb} \leq T_{max}$		1.4	3.4 3.4	mA
V_{icm}	Input common mode voltage range	±11	+15 -12		V
CMR	Common mode rejection ratio (R_S = 10kΩ) $T_{min} \leq T_{amb} \leq T_{max}$	70 70	86		dB
I_{OS}	Output short-circuit current $T_{min} \leq T_{amb} \leq T_{max}$	10 10	40	60 60	mA
$\pm V_{opp}$	Output voltage swing R_L = 2kΩ R_L = 10kΩ $T_{min} \leq T_{amb} \leq T_{max}$ R_L = 2kΩ R_L = 10kΩ	 10 12 10 12	 12 13.5		V
SR	Slew rate, V_i = 10V, R_L = 2kΩ, C_L = 100pF, unity gain	12	16		V/µs
t_r	Rise time, V_i = 20mV, R_L = 2kΩ, C_L = 100pF, unity gain		0.1		µs
K_{ov}	Overshoot, V_i = 20mV, R_L = 2kΩ, C_L = 100pF, unity gain		10		%
GBP	Gain bandwidth product, f = 100kHz, V_{in} = 10mV, R_L = 2kΩ, C_L = 100pF	2.5	4		MHz
R_i	Input resistance		10^{12}		Ω
THD	Total harmonic distortion f= 1kHz, A_v= 20dB, R_L= 2kΩ, C_L=100pF, V_o= $2V_{pp}$		0.01		%
e_n	Equivalent input noise voltage R_S = 100Ω, f = 1KHz		15		$\frac{nV}{\sqrt{Hz}}$
Øm	Phase margin		45		Degrees

1. The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature.

Figure 3. Maximum peak-to-peak output voltage versus frequency

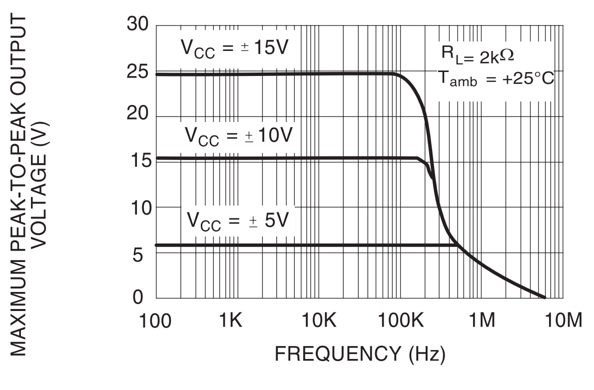


Figure 4. Maximum peak-to-peak output voltage versus frequency

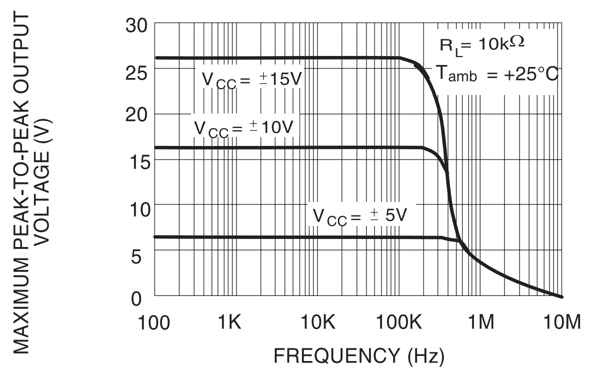


Figure 5. Maximum peak-to-peak output voltage versus frequency

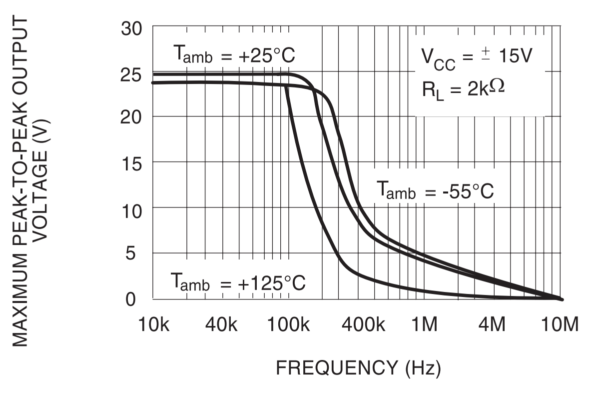


Figure 6. Maximum peak-to-peak output voltage versus free air temp.

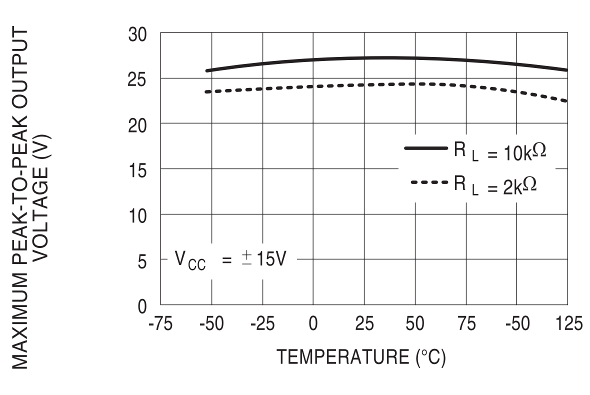


Figure 7. Maximum peak-to-peak output voltage versus load resistance

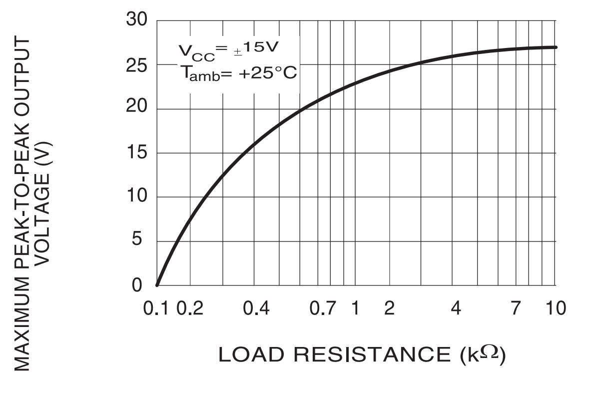


Figure 8. Maximum peak-to-peak output voltage versus supply voltage

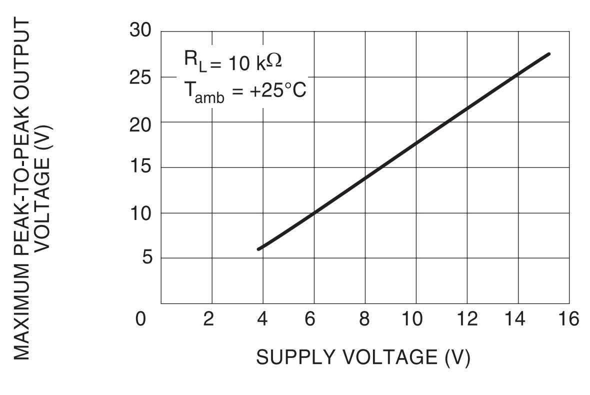


Figure 9. Input bias current versus free air temperature

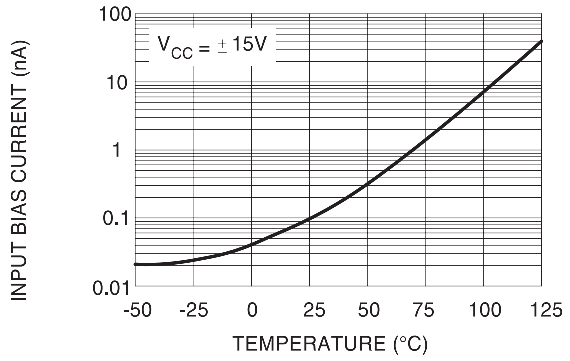


Figure 10. Large signal differential voltage amplification versus free air temp.

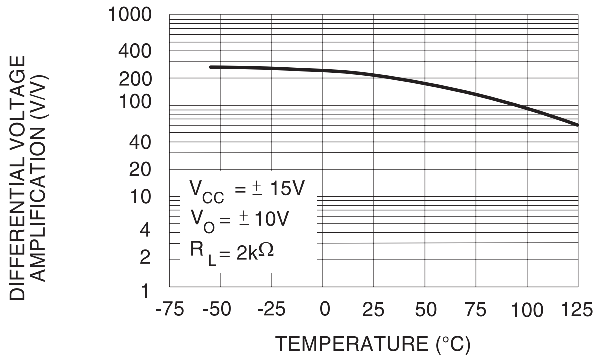


Figure 11. Large signal differential voltage amplification and phase shift versus frequency

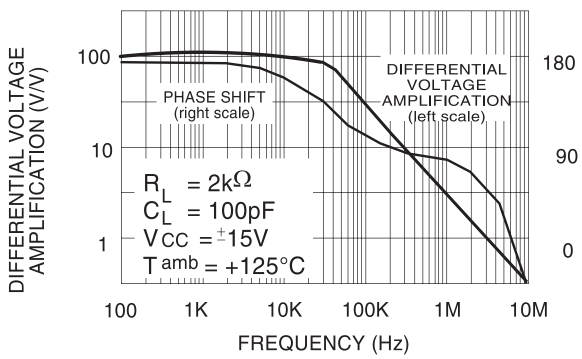


Figure 12. Total power dissipation versus free air temperature

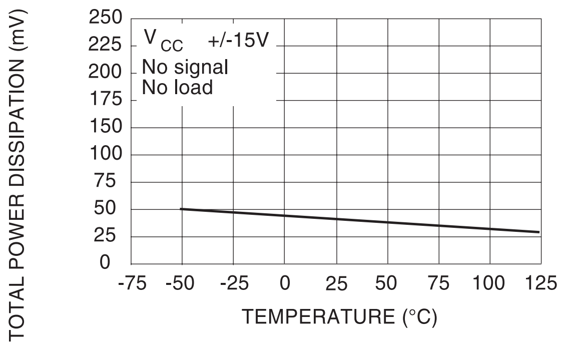


Figure 13. Supply current per amplifier versus free air temperature

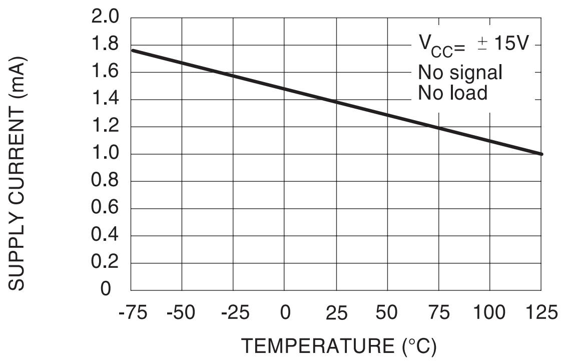


Figure 14. Supply current per amplifier versus supply voltage

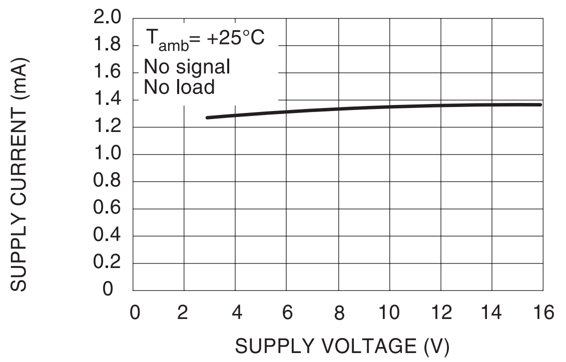


Figure 15. Common mode rejection ratio versus free air temperature

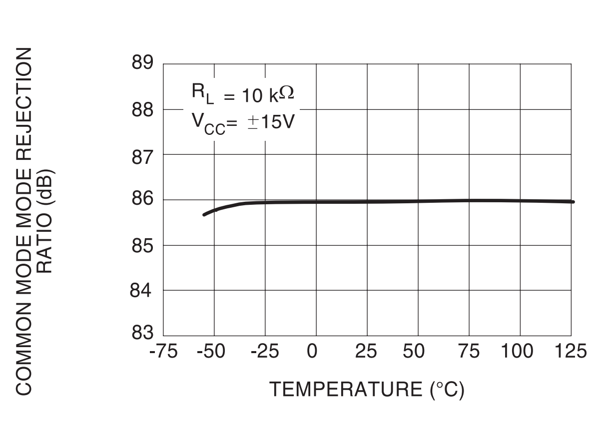


Figure 16. Voltage follower large signal pulse response

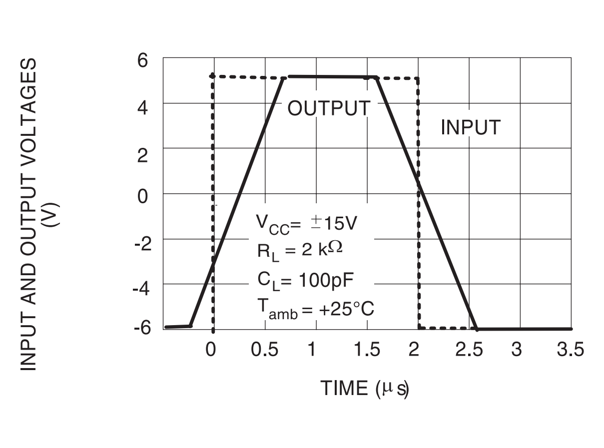


Figure 17. Output voltage versus elapsed time

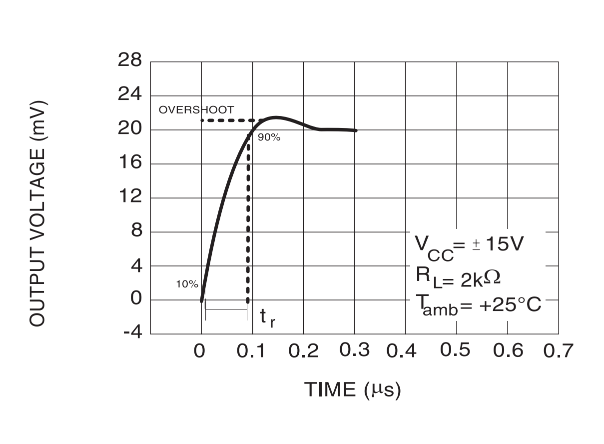


Figure 18. Equivalent input noise voltage versus frequency

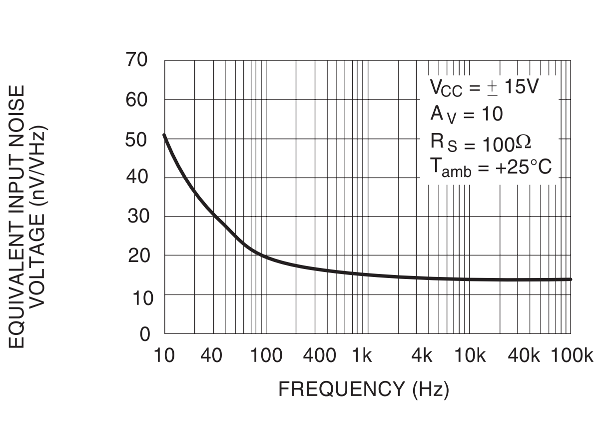
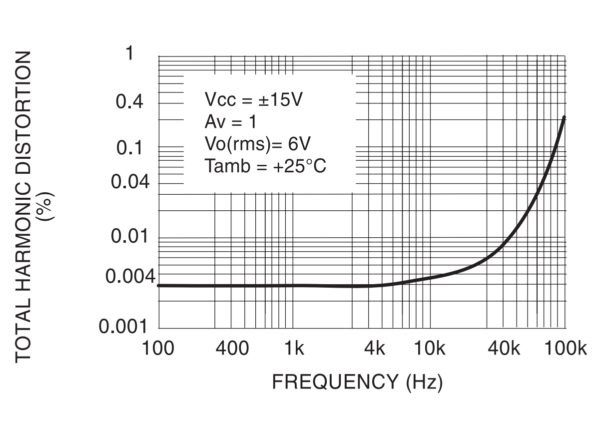


Figure 19. Total harmonic distortion versus frequency



4 Parameter measurement information

Figure 20. Voltage follower

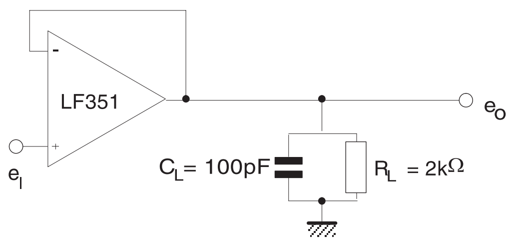
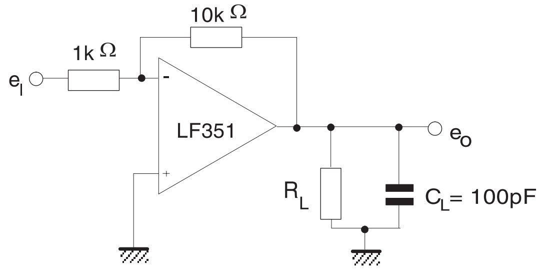


Figure 21. Gain-of-10 inverting amplifier



5 Typical application

Figure 22. Square wave oscillator (0.5 Hz)

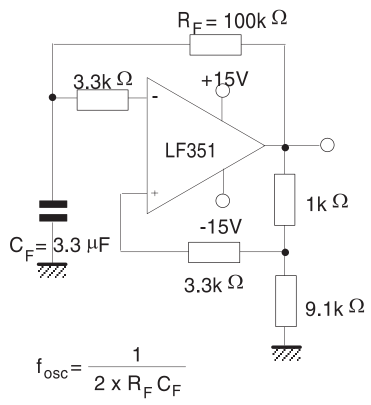
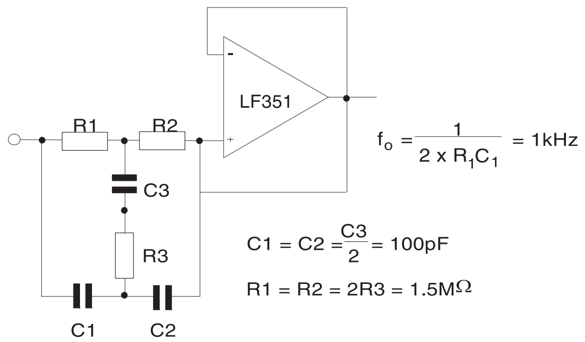


Figure 23. High Q notch filter



6 Package information

In order to meet environmental requirements, STMicroelectronics offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an STMicroelectronics trademark. ECOPACK specifications are available at: www.st.com.

6.1 DIP8 package information

Figure 24. DIP8 package mechanical drawing

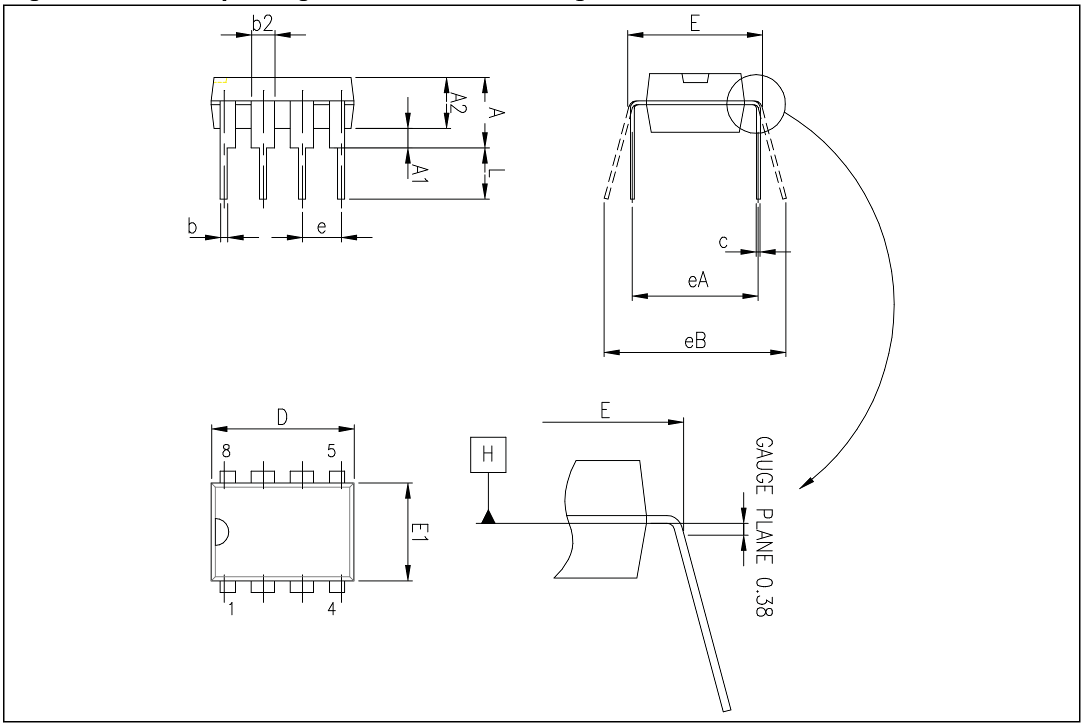


Table 4. DIP8 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			5.33			0.210
A1	0.38			0.015		
A2	2.92	3.30	4.95	0.115	0.130	0.195
b	0.36	0.46	0.56	0.014	0.018	0.022
b2	1.14	1.52	1.78	0.045	0.060	0.070
c	0.20	0.25	0.36	0.008	0.010	0.014
D	9.02	9.27	10.16	0.355	0.365	0.400
E	7.62	7.87	8.26	0.300	0.310	0.325
E1	6.10	6.35	7.11	0.240	0.250	0.280
e		2.54			0.100	
eA		7.62			0.300	
eB			10.92			0.430
L	2.92	3.30	3.81	0.115	0.130	0.150

6.2 SO-8 package information

Figure 25. SO-8 package mechanical drawing

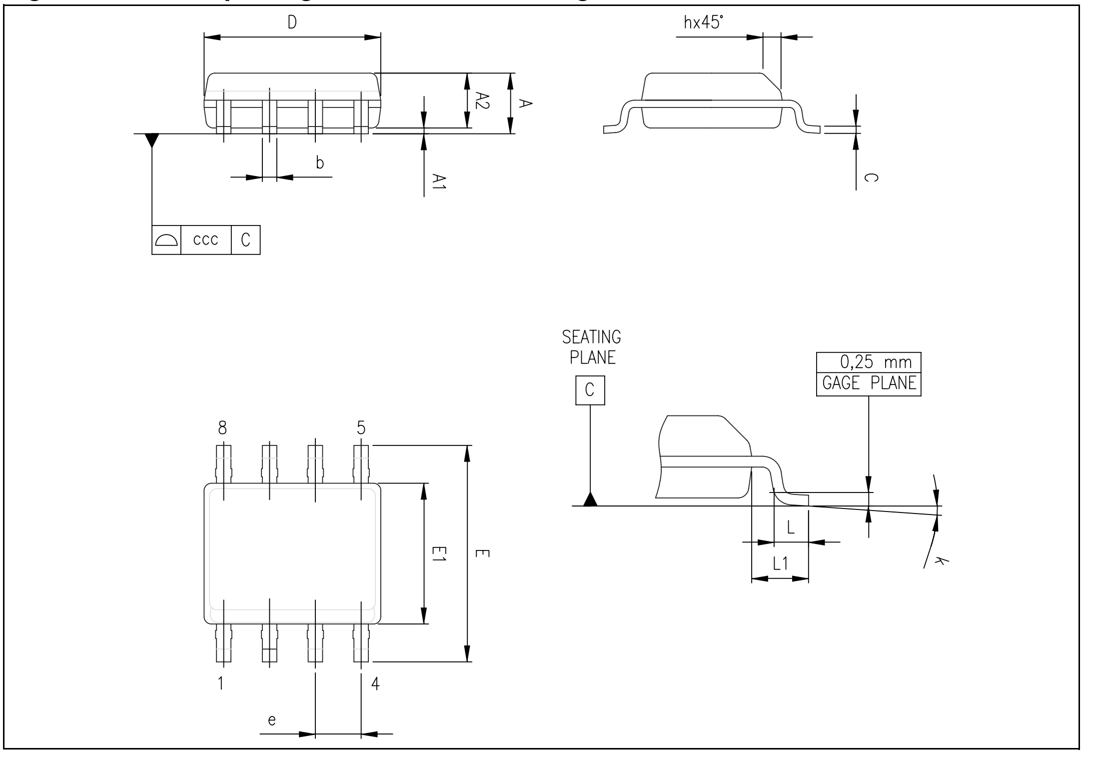


Table 5. SO-8 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.069
A1	0.10		0.25	0.004		0.010
A2	1.25			0.049		
b	0.28		0.48	0.011		0.019
c	0.17		0.23	0.007		0.010
D	4.80	4.90	5.00	0.189	0.193	0.197
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e		1.27			0.050	
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
k	1°		8°	1°		8°
ccc			0.10			0.004

7 Ordering information

Table 6. Order codes

Order code	Temperature range	Package	Packing	Marking
LF151N	-55°C, +125°C	DIP8	Tape	LF151N
LF151D LF151DT		SO-8	Tape or Tape & reel	151
LF251N	-40°C, +105°C	DIP8	Tape	LF251N
LF251D LF251DT		SO-8	Tape or Tape & reel	251
LF351N	0°C, +70°C	DIP8	Tape	LF351N
LF351D LF351DT		SO-8	Tape or Tape & reel	351

8 Revision history

Table 7. Document revision history

Date	Revision	Changes
17-May-2001	1	Initial release.
28-April-2008	2	Updated document format.