TS4962M

3 W filter-free class D audio power amplifier

Datasheet - production data

Features

- Operating from V_{CC} = 2.4 V to 5.5 V
- Standby mode active low
- Output power: 3 W into 4 Ω and 1.75 W into 8 Ω with 10% THD+N max. and 5 V power supply
- Output power: 2.3 W @5 V or 0.75 W @ 3.0 V into 4 Ω with 1% THD+N max.
- Output power: 1.4 W @5 V or 0.45 W @ 3.0 V into 8 Ω with 1% THD+N max.
- Adjustable gain via external resistors
- Low current consumption 2 mA @ 3 V
- Efficiency: 88% typ.
- Signal to noise ratio: 85 dB typ.
- PSRR: 63 dB typ. @217 Hz with 6 dB gain
- PWM base frequency: 250 kHz
- Low pop and click noise
- Available in Flip Chip 9 x 300 µm (Pb-free)

Related products

- See TS2007 for further gain settings e.g. 6 or 12 dB
- See TS2012 for stereo settings

Applications

- Portable gaming consoles
- VR headsets
- Smart phones
- Tablets

Description

The TS4962M is a differential Class-D BTL power amplifier. It is able to drive up to 2.3 W into a 4 Ω load and 1.4 W into a 8 Ω load at 5 V. It achieves outstanding efficiency (88% typ.) compared to classical Class-AB audio amps.

The gain of the device can be controlled via two external gain-setting resistors. Pop and click reduction circuitry provides low on/off switch noise while allowing the device to start within 5 ms. A standby function (active low) allows the reduction of current consumption to 10 nA typ.

Contents

1 Block diagram and pinout

Figure 1. Block diagram

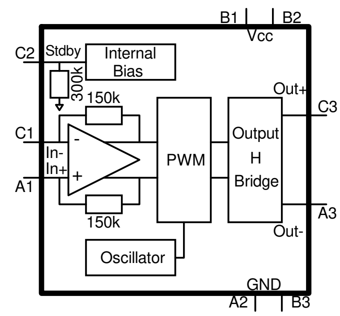
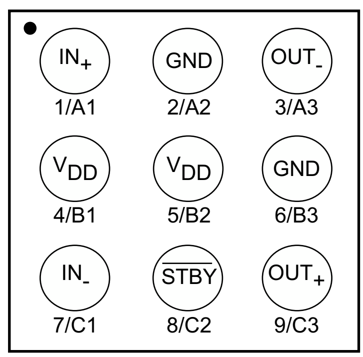


Figure 2. Pinout (top view)



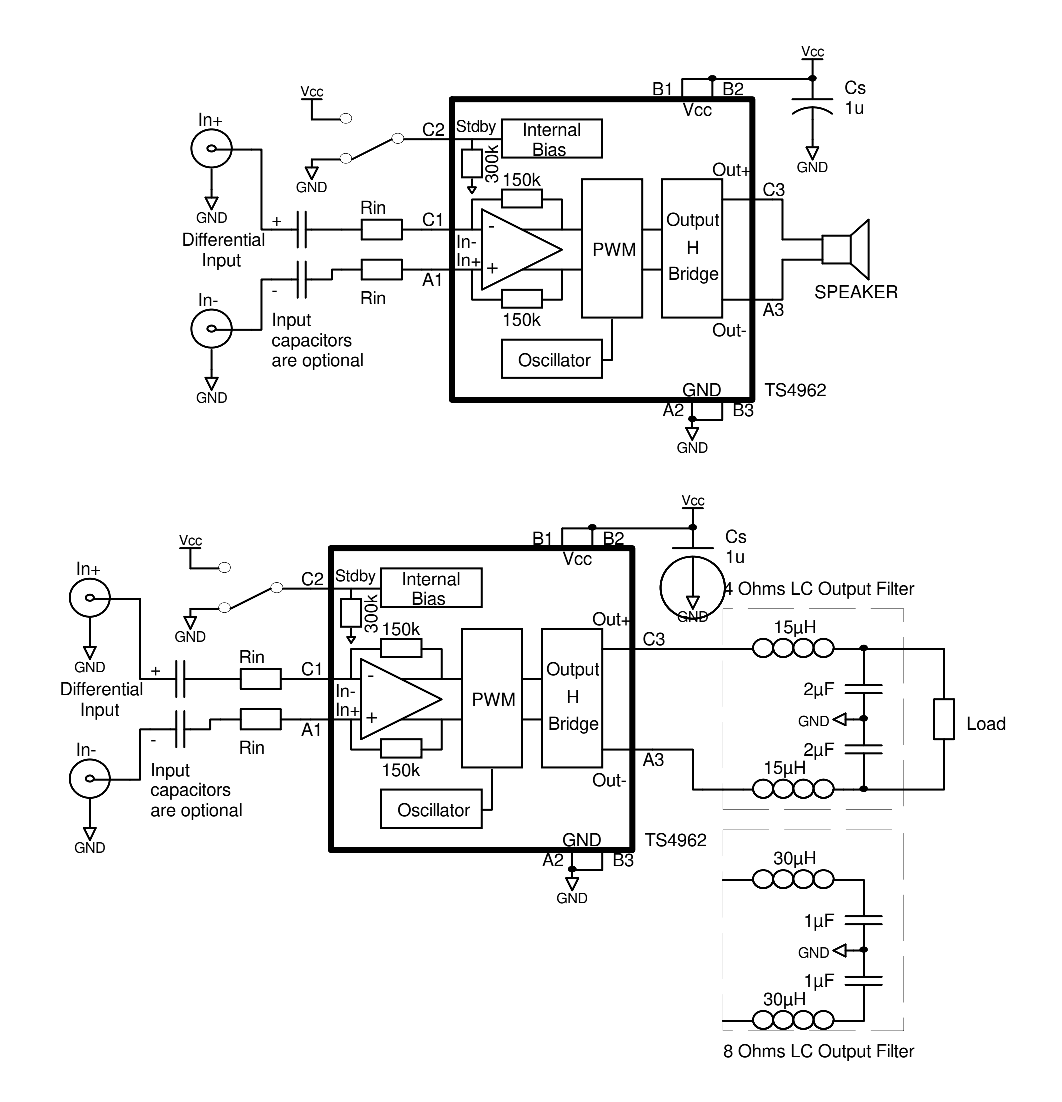
1. Legend:
   IN+ = positive differential input
   IN- = negative differential input
   VDD = analog power supply
   GND = power supply ground
   STBY = standby pin (active low)
   OUT+ = positive differential output
   OUT- = negative differential output
2. Bumps are underneath, bump diameter = 300 µm

2 Application component information

Table 1. Component information

Component	Functional description
C_s	Bypass supply capacitor. Install as close as possible to the TS4962M to minimize high-frequency ripple. A 100 nF ceramic capacitor should be added to enhance the power supply filtering at high frequency.
R_{in}	Input resistor to program the TS4962M differential gain (gain = 300 kΩ/R_{in} with R_{in} in kΩ).
Input capacitor	Due to common-mode feedback, these input capacitors are optional. However, they can be added to form with R_{in} a 1st order high-pass filter with -3 dB cut-off frequency = $1/(2*\pi*R_{in}*C_{in})$.

Figure 3. Typical application schematics



3 Absolute maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage (1) (2)	6	V
V_{in}	Input voltage (3)	GND to V_{CC}	V
T_{oper}	Operating free-air temperature range	-40 to + 85	°C
T_{stg}	Storage temperature	-65 to +150	°C
T_j	Maximum junction temperature	150	°C
R_{thja}	Thermal resistance junction to ambient	200	°C/W
P_{diss}	Power dissipation	Internally limited(4)	
ESD	Human body model	2	kV
ESD	Machine model	200	V
Latch-up	Latch-up immunity	200	mA
V_{STBY}	Standby pin voltage maximum voltage (5)	GND to V_{CC}	V
	Lead temperature (soldering, 10 s)	260	°C

1. Caution: this device is not protected in the event of abnormal operating conditions, such as for example, short-circuiting between any one output pin and ground, between any one output pin and V_{CC}, and between individual output pins.
2. All voltage values are measured with respect to the ground pin.
3. The magnitude of the input signal must never exceed V_{CC} + 0.3 V / GND - 0.3 V.
4. Exceeding the power derating curves during a long period causes abnormal operation.
5. The magnitude of the standby signal must never exceed V_{CC} + 0.3 V / GND - 0.3 V.

Table 3. Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage (1)	2.4 to 5.5	V
V_{IC}	Common-mode input voltage range (2)	0.5 to V_{CC} - 0.8	V
V_{STBY}	Standby voltage input: (3) Device ON Device OFF	 $1.4 \leq V_{STBY} \leq V_{CC}$ $GND \leq V_{STBY} \leq 0.4$ (4)	V
R_L	Load resistor	≥ 4	Ω
R_{thja}	Thermal resistance junction to ambient (5)	90	°C/W

1. For V_{CC} from 2.4 V to 2.5 V, the operating temperature range is reduced to 0 °C $\leq T_{amb} \leq$ 70 °C.
2. For V_{CC} from 2.4 V to 2.5 V, the common-mode input range must be set at $V_{CC}/2$.
3. Without any signal on V_{STBY}, the device is in standby.
4. Minimum current consumption is obtained when V_{STBY} = GND.
5. With heat sink surface = 125 mm^2.

4 Electrical characteristics

Table 4. V_{CC} = 5 V, GND = 0 V, V_{IC} = 2.5 V, t_{amb} = 25 °C (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_{CC}	Supply current	No input signal, no load		2.3	3.3	mA
I_{STBY}	Standby current (1)	No input signal, V_{STBY} = GND		10	1000	nA
V_{OO}	Output offset voltage	No input signal, R_L = 8 Ω		3	25	mV
P_{out}	Output power	G=6 dB THD = 1% max., F = 1 kHz, R_L = 4 Ω THD = 10% max., F = 1 kHz, R_L = 4 Ω THD = 1% max., F = 1 kHz, R_L = 8 Ω THD = 10% max., F = 1 kHz, R_L = 8 Ω		2.3 3 1.4 1.75		W
THD + N	Total harmonic distortion + noise	P_{out} = 900 mW_{RMS}, G = 6 dB, 20 Hz < F < 20 kHz R_L = 8 Ω + 15 μH, BW < 30 kHz P_{out} = 1 W_{RMS}, G = 6 dB, F = 1 kHz, R_L = 8 Ω + 15 μH, BW < 30 kHz		1 0.4		%
Efficiency	Efficiency	P_{out} = 2 W_{RMS}, R_L = 4 Ω + ≥ 15 μH P_{out} =1.2 W_{RMS}, R_L = 8 Ω+ ≥ 15 μH		78 88		%
PSRR	Power supply rejection ratio with inputs grounded (2)	F = 21 Hz, R_L = 8 Ω, G=6 dB, V_{ripple} = 200 mV_{pp}		63		dB
CMRR	Common-mode rejection ratio	F = 217 Hz, R_L = 8 Ω, G = 6 dB, ΔV_{icm} = 200 mV_{pp}		57		dB
Gain	Gain value	R_{in} in kΩ	$\frac{273k\Omega}{R_{in}}$	$\frac{300k\Omega}{R_{in}}$	$\frac{327k\Omega}{R_{in}}$	V/V
R_{STBY}	Internal resistance from Standby to GND		273	300	327	kΩ
F_{PWM}	Pulse width modulator base frequency		180	250	320	kHz
SNR	Signal to noise ratio	A-weighting, P_{out} = 1.2 W, R_L = 8 Ω		85		dB
t_{WU}	Wake-up time			5	10	ms
t_{STBY}	Standby time			5	10	ms

Table 4. V_{CC} = 5 V, GND = 0 V, V_{IC} = 2.5 V, t_{amb} = 25 °C (unless otherwise specified) (continued)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_N	Output voltage noise	F = 20 Hz to 20 kHz, G = 6 dB Unweighted R_L = 4 Ω A-weighted R_L = 4 Ω		 85 60		µV_{RMS}
		Unweighted R_L = 8 Ω A-weighted R_L = 8 Ω		86 62		
		Unweighted R_L = 4 Ω + 15 µH A-weighted R_L = 4 Ω + 15 µH		83 60		
		Unweighted R_L = 4 Ω + 30 µH A-weighted R_L = 4 Ω + 30 µH		88 64		
		Unweighted R_L = 8 Ω + 30 µH A-weighted R_L = 8 Ω + 30 µH		78 57		
		Unweighted R_L = 4 Ω + filter A-weighted R_L = 4 Ω + filter		87 65		
		Unweighted R_L = 4 Ω + filter A-weighted R_L = 4 Ω + filter		82 59		

1. Standby mode is active when V_{STBY} is tied to GND.
2. Dynamic measurements - 20*log(rms(V_{out})/rms(V_{ripple})). V_{ripple} is the superimposed sinusoidal signal to V_{CC} @ F = 217 Hz.

Table 5. V_{CC} = 4.2V, GND = 0V, V_{IC} = 2.5V, T_{amb} = 25°C (unless otherwise specified) (1)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_{CC}	Supply current	No input signal, no load		2.1	3	mA
I_{STBY}	Standby current (2)	No input signal, V_{STBY} = GND		10	1000	nA
V_{OO}	Output offset voltage	No input signal, R_L = 8 Ω		3	25	mV
P_{out}	Output power	G=6dB THD = 1% max, F = 1 kHz, R_L = 4 Ω THD = 10% max, F = 1 kHz, R_L = 4 Ω THD = 1% max, F = 1 kHz, R_L = 8 Ω THD = 10% max, F = 1 kHz, R_L = 8 Ω		1.6 2 0.95 1.2		W
THD + N	Total harmonic distortion + noise	P_{out} = 600mW$_{RMS}$, G = 6 dB, 20 Hz < F < 20k Hz R_L = 8 Ω + 15 µH, BW < 30 kHz P_{out} = 700 mW$_{RMS}$, G = 6 dB, F = 1 kHz, R_L = 8 Ω + 15 µH, BW < 30 kHz		1 0.35		%
Efficiency	Efficiency	P_{out} = 1.45 W$_{RMS}$, R_L = 4 Ω + ≥ 15 µH P_{out} =0.9 W$_{RMS}$, R_L = 8 Ω+ ≥ 15 µH		78 88		%
PSRR	Power supply rejection ratio with inputs grounded (3)	F = 217 Hz, R_L = 8 Ω, G=6 dB, V_{ripple} = 200 mV$_{pp}$		63		dB
CMRR	Common-mode rejection ratio	F = 217 Hz, R_L = 8 Ω, G = 6 dB, ΔV_{icm} = 200 mV$_{pp}$		57		dB
Gain	Gain value	R_{in} in kΩ	$\frac{273k\Omega}{R_{in}}$	$\frac{300k\Omega}{R_{in}}$	$\frac{327k\Omega}{R_{in}}$	V/V
R_{STBY}	Internal resistance from Standby to GND		273	300	327	kΩ
F_{PWM}	Pulse width modulator base frequency		180	250	320	kHz
SNR	Signal to noise ratio	A-weighting, P_{out} = 0.9 W, R_L = 8 Ω		85		dB
t_{WU}	Wake-uptime			5	10	ms
t_{STBY}	Standby time			5	10	ms

Table 5. V_{CC} = 4.2V, GND = 0V, V_{IC} = 2.5V, T_{amb} = 25°C (unless otherwise specified) (1)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_N	Output voltage noise	F = 20Hz to 20 kHz, G = 6 dB Unweighted R_L = 4 Ω A-weighted R_L = 4 Ω		85 60		µV_{RMS}
		Unweighted R_L = 8 Ω A-weighted R_L = 8 Ω		86 62		
		Unweighted R_L = 4 Ω + 15 µH A-weighted R_L = 4 Ω + 15 µH		83 60		
		Unweighted R_L = 4 Ω + 30 µH A-weighted R_L = 4 Ω + 30 µH		88 64		
		Unweighted R_L = 8 Ω + 30 µH A-weighted R_L = 8 Ω + 30 µH		78 57		
		Unweighted R_L = 4 Ω + filter A-weighted R_L = 4 Ω + filter		87 65		
		Unweighted R_L = 4 Ω + filter A-weighted R_L = 4 Ω + filter		82 59		

1. All electrical values are guaranteed with correlation measurements at 2.5 V and 5 V.
2. Standby mode is active when V_{STBY} is tied to GND.
3. Dynamic measurements - 20*log(rms(V_{out})/rms(V_{ripple})). V_{ripple} is the superimposed sinusoidal signal to V_{CC} @ F = 217 Hz.

Table 6. V_{CC} = 3.6 V, GND = 0 V, V_{IC} = 2.5 V, T_{amb} = 25 °C (unless otherwise specified) [(1)]

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_{CC}	Supply current	No input signal, no load		2	2.8	mA
I_{STBY}	Standby current [(2)]	No input signal, V_{STBY} = GND		10	1000	nA
V_{OO}	Output offset voltage	No input signal, R_L = 8 Ω		3	25	mV
P_{out}	Output power	G=6dB THD = 1% max., F = 1 kHz, R_L = 4 Ω THD = 10% max., F = 1 kHz, R_L = 4 Ω THD = 1% max., F = 1 kHz, R_L = 8 Ω THD = 10% max., F = 1 kHz, R_L = 8 Ω		1.15 1.51 0.7 0.9		W
THD + N	Total harmonic distortion + noise	P_{out} = 500 mW_{RMS}, G = 6 dB, 20 Hz < F< 20 kHz R_L = 8 Ω + 15 µH, BW < 30 kHz P_{out} = 500 mW_{RMS}, G = 6 dB, F = 1 kHz, R_L = 8 Ω + 15 µH, BW < 30 kHz		1 0.27		%
Efficiency	Efficiency	P_{out} = 1 W_{RMS}, R_L = 4 Ω + ≥ 15 µH P_{out} =0.65 W_{RMS}, R_L = 8 Ω+ ≥ 15 µH		78 88		%
PSRR	Power supply rejection ratio with inputs grounded [(3)]	F = 217 Hz, R_L = 8 Ω, G=6 dB, V_{ripple} = 200 mV_{pp}		62		dB
CMRR	Common-mode rejection ratio	F = 217 Hz, R_L = 8 Ω, G = 6 dB, ΔV_{icm} = 200 mV_{pp}		56		dB
Gain	Gain value	R_{in} in kΩ	$\frac{273k\Omega}{R_{in}}$	$\frac{300k\Omega}{R_{in}}$	$\frac{327k\Omega}{R_{in}}$	V/V
R_{STBY}	Internal resistance from Standby to GND		273	300	327	kΩ
F_{PWM}	Pulse width modulator base frequency		180	250	320	kHz
SNR	Signal to noise ratio	A-weighting, P_{out} = 0.6 W, R_L = 8 Ω		83		dB
t_{WU}	Wake-uptime			5	10	ms
t_{STBY}	Standby time			5	10	ms

Table 6. V_{CC} = 3.6 V, GND = 0 V, V_{IC} = 2.5 V, T_{amb} = 25 °C (unless otherwise specified) [(1)]

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_N	Output voltage noise	F = 20 Hz to 20 kHz, G = 6 dB Unweighted R_L = 4 Ω A-weighted R_L = 4 Ω		83 57		μV_{RMS}
		Unweighted R_L = 8 Ω A-weighted R_L = 8 Ω		83 61		
		Unweighted R_L = 4 Ω + 15 µH A-weighted R_L = 4 Ω + 15 µH		81 58		
		Unweighted R_L = 4 Ω + 30 µH A-weighted R_L = 4 Ω + 30 µH		87 62		
		Unweighted R_L = 8 Ω + 30 µH A-weighted R_L = 8 Ω + 30 µH		77 56		
		Unweighted R_L = 4 Ω + filter A-weighted R_L = 4 Ω + filter		85 63		
		Unweighted R_L = 4 Ω + filter A-weighted R_L = 4 Ω + filter		80 57		

1. All electrical values are guaranteed with correlation measurements at 2.5 V and 5 V.
2. Standby mode is active when V_{STBY} is tied to GND.
3. Dynamic measurements - 20*log(rms(V_{out})/rms(V_{ripple})). V_{ripple} is the superimposed sinusoidal signal to V_{CC} @ F = 217 Hz.

Table 7. V_{CC} = 3 V, GND = 0 V, V_{IC} = 2.5 V, T_{amb} = 25 °C (unless otherwise specified) (1)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_{CC}	Supply current	No input signal, no load		1.9	2.7	mA
I_{STBY}	Standby current (2)	No input signal, V_{STBY} = GND		10	1000	nA
V_{OO}	Output offset voltage	No input signal, R_L = 8Ω		3	25	mV
P_{out}	Output power	G=6dB THD = 1% max., F = 1 kHz, R_L = 4 Ω THD = 10% max., F = 1 kHz, R_L = 4 Ω THD = 1% max., F = 1 kHz, R_L = 8 Ω THD = 10% max., F = 1 kHz, R_L = 8 Ω		 0.75 1 0.5 0.6		W
THD + N	Total harmonic distortion + noise	P_{out} = 350 mW_{RMS}, G = 6 dB, 20 Hz < F < 20 kHz R_L = 8 Ω + 15 µH, BW < 30 kHz P_{out} = 350 mW_{RMS}, G = 6 dB, F = 1 kHz, R_L = 8 Ω + 15 µH, BW < 30 kHz		1 0.21		%
Efficiency	Efficiency	P_{out} = 0.7 W_{RMS}, R_L = 4 Ω + ≥ 15 µH P_{out} = 0.45 W_{RMS}, R_L = 8 Ω+ ≥ 15 µH		78 88		%
PSRR	Power supply rejection ratio with inputs grounded (3)	F = 217 Hz, R_L = 8 Ω, G=6 dB, V_{ripple} = 200 mV_{pp}		60		dB
CMRR	Common-mode rejection ratio	F = 217Hz, R_L = 8Ω, G = 6 dB, ΔV_{icm} = 200 mV_{pp}		54		dB
Gain	Gain value	R_{in} in kΩ	$\frac{273k\Omega}{R_{in}}$	$\frac{300k\Omega}{R_{in}}$	$\frac{327k\Omega}{R_{in}}$	V/V
R_{STBY}	Internal resistance from Standby to GND		273	300	327	kΩ
F_{PWM}	Pulse width modulator base frequency		180	250	320	kHz
SNR	Signal to noise ratio	A-weighting, P_{out} = 0.4 W, R_L = 8 Ω		82		dB
t_{WU}	Wake-up time			5	10	ms
t_{STBY}	Standby time			5	10	ms

Table 7. V_{CC} = 3 V, GND = 0 V, V_{IC} = 2.5 V, T_{amb} = 25 °C (unless otherwise specified) (1) (continued)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_N	Output Voltage Noise	f = 20 Hz to 20 kHz, G = 6 dB Unweighted R_L = 4 Ω A-weighted R_L = 4 Ω		83 57		μV_{RMS}
		Unweighted R_L = 8 Ω A-weighted R_L = 8 Ω		83 61		
		Unweighted R_L = 4 Ω + 15 µH A-weighted R_L = 4 Ω + 15 µH		81 58		
		Unweighted R_L = 4 Ω + 30 µH A-weighted R_L = 4 Ω + 30 µH		87 62		
		Unweighted R_L = 8 Ω + 30 µH A-weighted R_L = 8 Ω + 30 µH		77 56		
		Unweighted R_L = 4 Ω + filter A-weighted R_L = 4 Ω + filter		85 63		
		Unweighted R_L = 4 Ω + filter A-weighted R_L = 4 Ω + filter		80 57		

1. All electrical values are guaranteed with correlation measurements at 2.5 V and 5 V.
2. Standby mode is active when V_{STBY} is tied to GND.
3. Dynamic measurements - 20*log(rms(V_{out})/rms(V_{ripple})). V_{ripple} is the superimposed sinusoidal signal to V_{CC} @ F = 217 Hz.

Table 8. V_{CC} = 2.5 V, GND = 0 V, V_{IC} = 2.5 V, T_{amb} = 25 °C (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_{CC}	Supply current	No input signal, no load		1.7	2.4	mA
I_{STBY}	Standby current (1)	No input signal, V_{STBY} = GND		10	1000	nA
V_{OO}	Output offset voltage	No input signal, R_L = 8 Ω		3	25	mV
P_{out}	Output power	G=6dB THD = 1% max., F = 1 kHz, R_L = 4 Ω THD = 10% max., F = 1 kHz, R_L = 4 Ω THD = 1% max., F = 1 kHz, R_L = 8 Ω THD = 10% max., F = 1 kHz, R_L = 8 Ω		0.52 0.71 0.33 0.42		W
THD + N	Total harmonic distortion + noise	P_{out} = 200 mW_{RMS}, G = 6 dB, 20 Hz < F< 20 kHz R_L = 8 Ω + 15 µH, BW < 30 kHz P_{out} = 200 W_{RMS}, G = 6 dB, F = 1 kHz, R_L = 8 Ω + 15 µH, BW < 30 kHz		1 0.19		%
Efficiency	Efficiency	P_{out} = 0.47 W_{RMS}, R_L = 4 Ω + ≥ 15 µH P_{out} = 0.3 W_{RMS}, R_L = 8 Ω+ ≥ 15 µH		78 88		%
PSRR	Power supply rejection ratio with inputs grounded (2)	F = 217 Hz, R_L = 8 Ω, G=6 dB, V_{ripple} = 200 mV_{pp}		60		dB
CMRR	Common-mode rejection ratio	F = 217 Hz, R_L = 8 Ω, G = 6 dB, ΔV_{icm} = 200 mV_{pp}		54		dB
Gain	Gain value	R_{in} in kΩ	$\frac{273k\Omega}{R_{in}}$	$\frac{300k\Omega}{R_{in}}$	$\frac{327k\Omega}{R_{in}}$	V/V
R_{STBY}	Internal resistance from Standby to GND		273	300	327	kΩ
F_{PWM}	Pulse width modulator base frequency		180	250	320	kHz
SNR	Signal to noise ratio	A-weighting, P_{out} = 1.2 W, R_L = 8 Ω		80		dB
t_{WU}	Wake-up time			5	10	ms
t_{STBY}	Standby time			5	10	ms

Table 8. V_{CC} = 2.5 V, GND = 0 V, V_{IC} = 2.5 V, T_{amb} = 25 °C (unless otherwise specified) (continued)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_N	Output voltage noise	F = 20Hz to 20kHz, G = 6 dB Unweighted R_L = 4 Ω A-weighted R_L = 4 Ω		 85 60		μV_{RMS}
		Unweighted R_L = 8 Ω A-weighted R_L = 8 Ω		86 62		
		Unweighted R_L = 4 Ω + 15 μH A-weighted R_L = 4 Ω + 15 μH		76 56		
		Unweighted R_L = 4 Ω + 30 μH A-weighted R_L = 4 Ω + 30 μH		82 60		
		Unweighted R_L = 8 Ω + 30 μH A-weighted R_L = 8 Ω + 30 μH		67 53		
		Unweighted R_L = 4 Ω + filter A-weighted R_L = 4 Ω + filter		78 57		
		Unweighted R_L = 4 Ω + filter A-weighted R_L = 4 Ω + filter		74 54		

1. Standby mode is active when V_{STBY} is tied to GND.
2. Dynamic measurements - 20*log(rms(V_{out})/rms(V_{ripple})). V_{ripple} is the superimposed sinusoidal signal to V_{CC} @ F = 217 Hz.

Table 9. V_{CC} = 2.4 V, GND = 0 V, V_{IC} = 2.5 V, T_{amb} = 25 °C (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_{CC}	Supply current	No input signal, no load		1.7		mA
I_{STBY}	Standby current [(1)]	No input signal, V_{STBY} = GND		10		nA
V_{OO}	Output offset voltage	No input signal, R_L = 8 Ω		3		mV
P_{out}	Output power	G=6dB THD = 1% max., F = 1 kHz, R_L = 4 Ω THD = 10% max., F = 1 kHz, R_L = 4 Ω THD = 1% max., F = 1 kHz, R_L = 8 Ω THD = 10% max., F = 1 kHz, R_L = 8 Ω		 0.48 0.65 0.3 0.38		W
THD + N	Total harmonic distortion + noise	P_{out} = 200 mW_{RMS}, G = 6 dB, 20 Hz < F< 20 kHz R_L = 8 Ω + 15 µH, BW < 30 kHz		1		%
Efficiency	Efficiency	P_{out} = 0.38 W_{RMS}, R_L = 4 Ω + ≥ 15 µH P_{out} = 0.25 W_{RMS}, R_L = 8 Ω+ ≥ 15 µH		77 86		%
CMRR	Common-mode rejection ratio	F = 217 Hz, R_L = 8 Ω, G = 6 dB, ΔV_{icm} = 200 mV_{pp}		54		dB
Gain	Gain value	R_{in} in kΩ	$\frac{273k\Omega}{R_{in}}$	$\frac{300k\Omega}{R_{in}}$	$\frac{327k\Omega}{R_{in}}$	V/V
R_{STBY}	Internal resistance from Standby to GND		273	300	327	kΩ
F_{PWM}	Pulse width modulator base frequency			250		kHz
SNR	Signal to noise ratio	A Weighting, P_{out} = 1.2 W, R_L = 8 Ω		80		dB
t_{WU}	Wake-up time			5		ms
t_{STBY}	Standby time			5		ms
V_N	Output voltage noise	F = 20 Hz to 20 kHz, G = 6 dB Unweighted R_L = 4 Ω A-weighted R_L = 4 Ω		 85 60		μV_{RMS}
		Unweighted R_L = 8 Ω A-weighted R_L = 8 Ω		86 62		
		Unweighted R_L = 4 Ω + 15 µH A-weighted R_L = 4 Ω + 15 µH		76 56		
		Unweighted R_L = 4 Ω + 30 µH A-weighted R_L = 4 Ω + 30 µH		82 60		
		Unweighted R_L = 8 Ω + 30 µH A-weighted R_L = 8 Ω + 30 µH		67 53		
		Unweighted R_L = 4 Ω + Filter A-weighted R_L = 4 Ω + Filter		78 57		
		Unweighted R_L = 4 Ω + Filter A-weighted R_L = 4 Ω + Filter		74 54		

1. Standby mode is active when V_{STBY} is tied to GND.

5 Electrical characteristic curves

The graphs included in this section use the following abbreviations:

- R_L + 15 µH or 30 µH = pure resistor + very low series resistance inductor
- Filter = LC output filter (1 µF+30 µH for 4 Ω and 0.5 µF+60 µH for 8 Ω)
- All measurements made with C_{s1}=1 µF and C_{s2}=100 nF except for PSRR where Cs1 is removed.

Figure 4. Test diagram for measurements

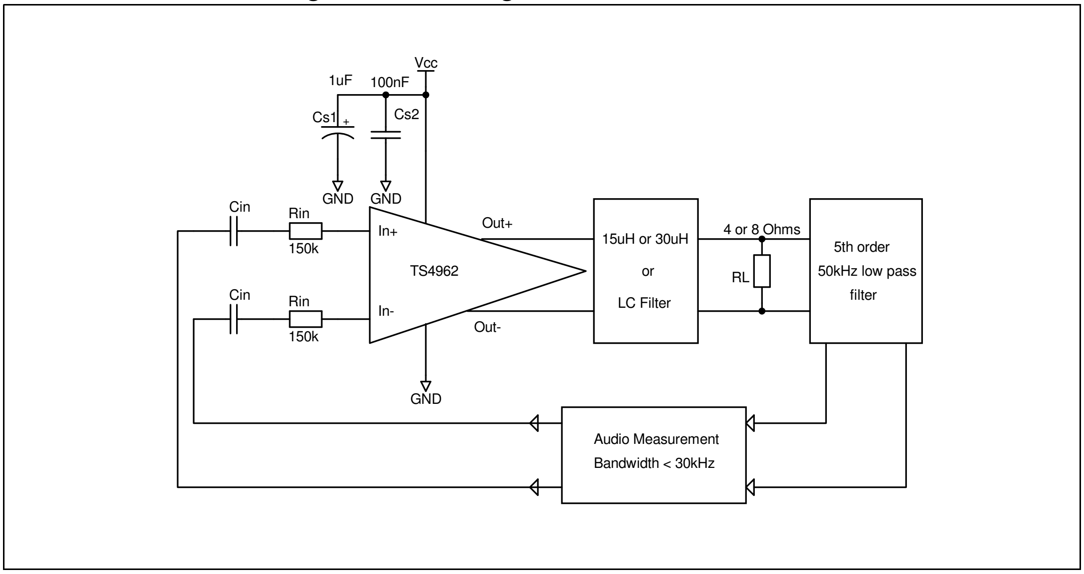


Figure 5. Test diagram for PSRR measurements

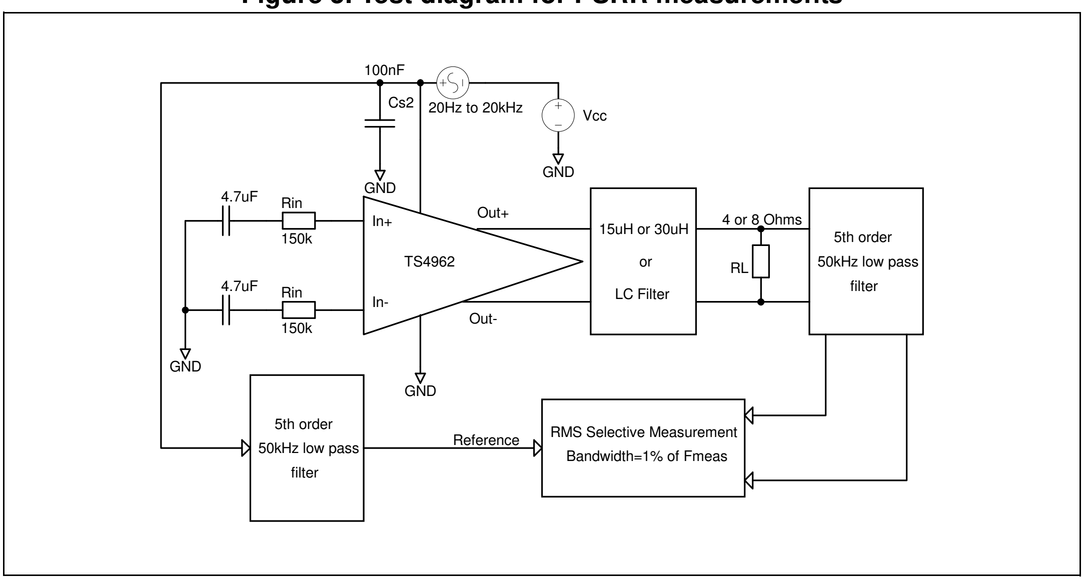


Figure 6. Current consumption vs. power supply voltage

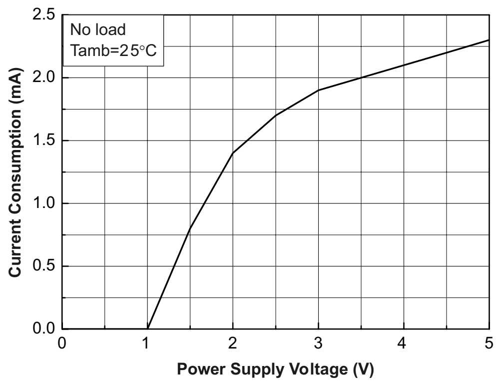


Figure 7. Current consumption vs. standby voltage at V_{CC} = 5 V

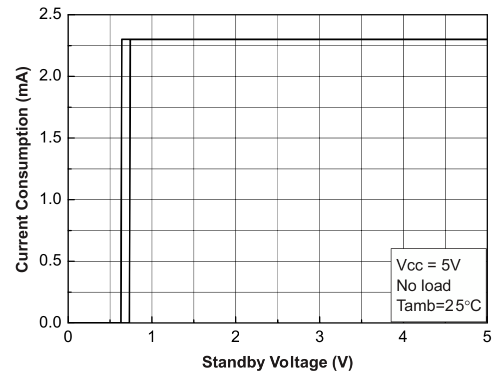


Figure 8. Current consumption vs. standby voltage at V_{CC} = 3 V

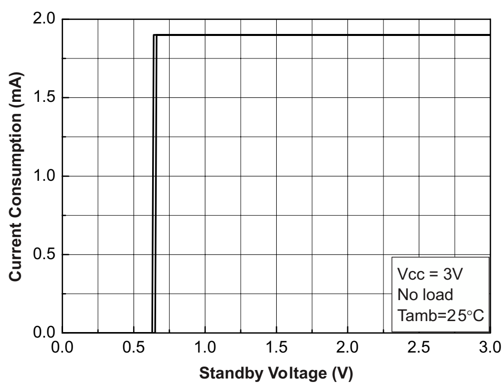


Figure 9. Output offset voltage vs. common-mode input voltage

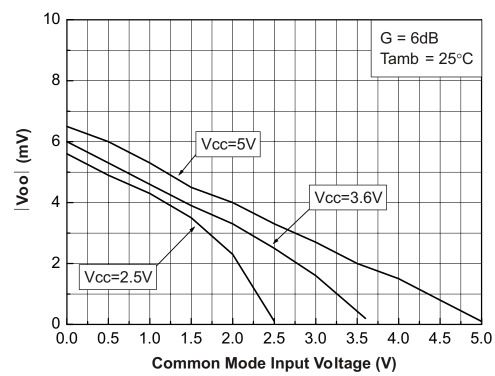


Figure 10. Efficiency vs. output power at V_{CC} = 5 V and R_L = 4 Ω

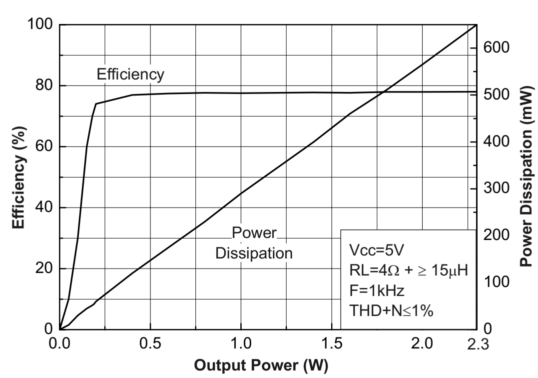


Figure 11. Efficiency vs. output power at V_{CC} = 3 V and R_L = 4 Ω

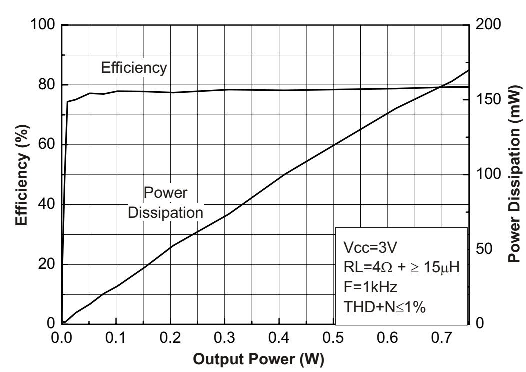


Figure 12. Efficiency vs. output power at V_{CC} = 5 V and R_L = 8 Ω

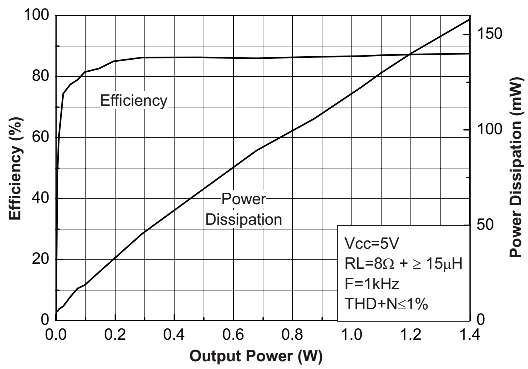


Figure 13. Efficiency vs. output power at V_{CC} = 3 V and R_L = 8 Ω

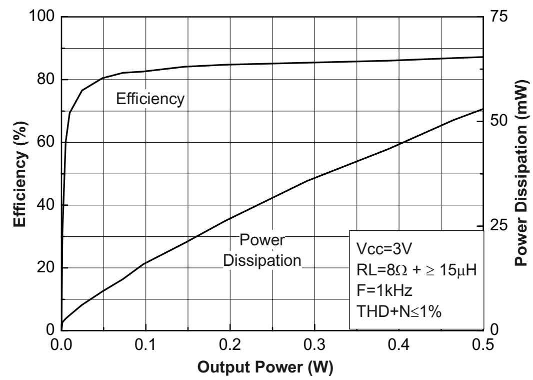


Figure 14. Output power vs. power supply voltage at R_L = 4 Ω

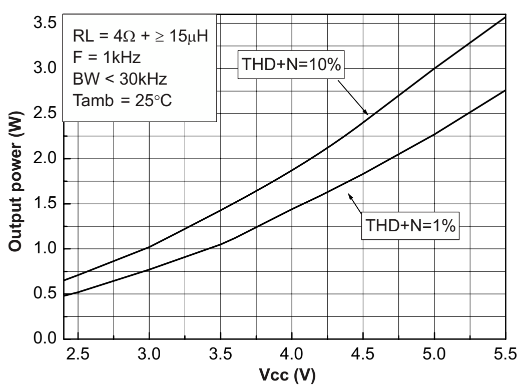


Figure 15. Output power vs. power supply voltage at R_L = 8 Ω

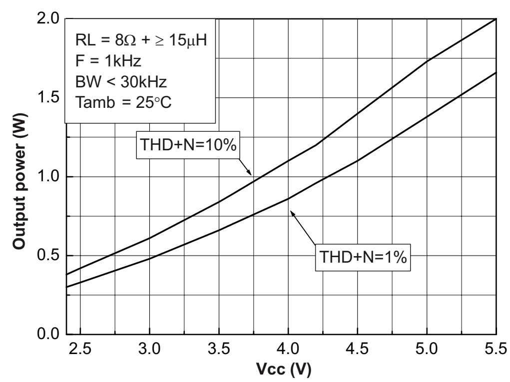


Figure 16. PSRR vs. frequency at R_L = 4 Ω + 15 µH

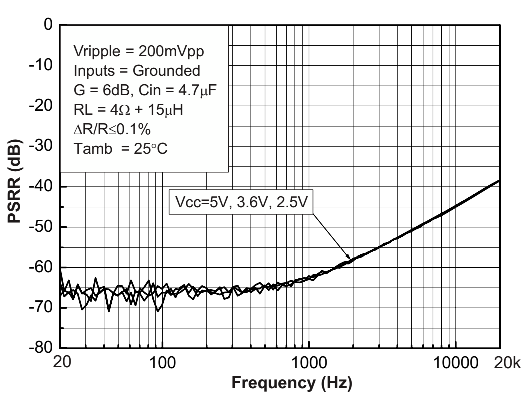


Figure 17. PSRR vs. frequency at R_L = 4 Ω + 30 µH

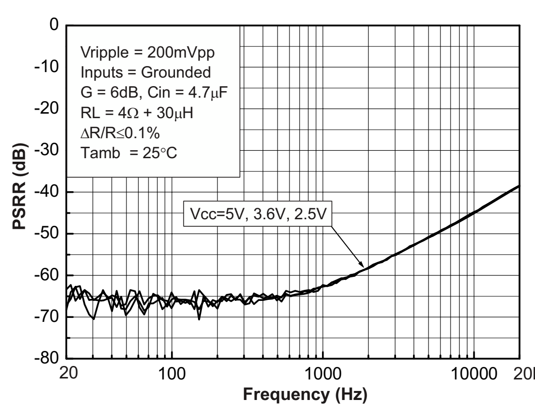


Figure 18. PSRR vs. frequency at R_L = 4 Ω + filter

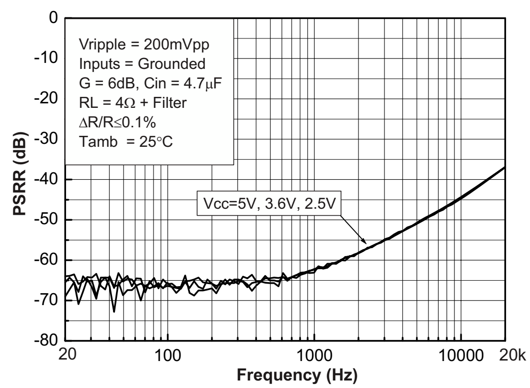


Figure 19. PSR R vs. frequency at R_L = 8 Ω + 15 µH

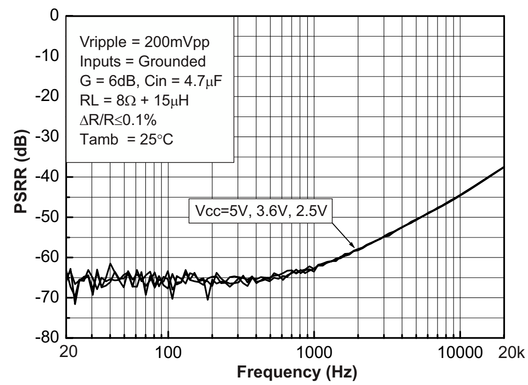


Figure 20. PSRR vs. frequency at R_L = 8 Ω + 30 µH

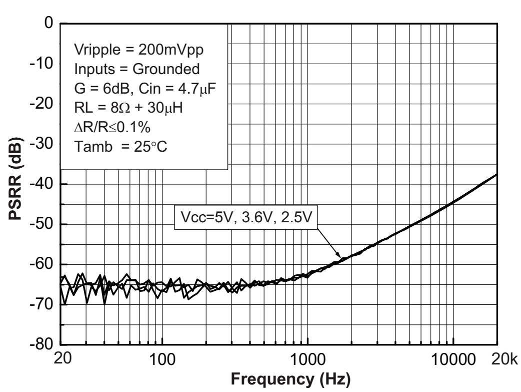


Figure 21. PSRR vs. frequency at R_L = 8 Ω + filter

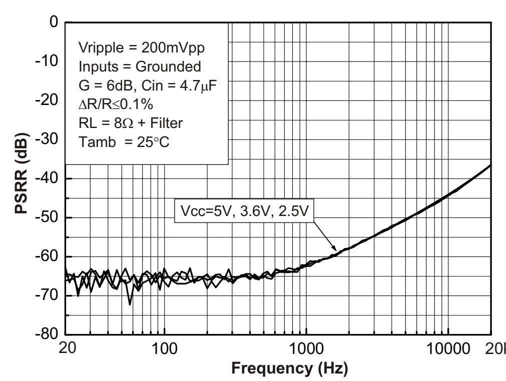


Figure 22. PSRR vs. common-mode input voltage

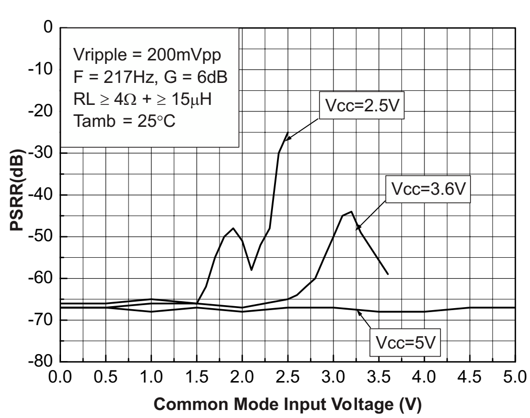


Figure 23. CMRR vs. frequency at R_L = 4 Ω + 15 µH

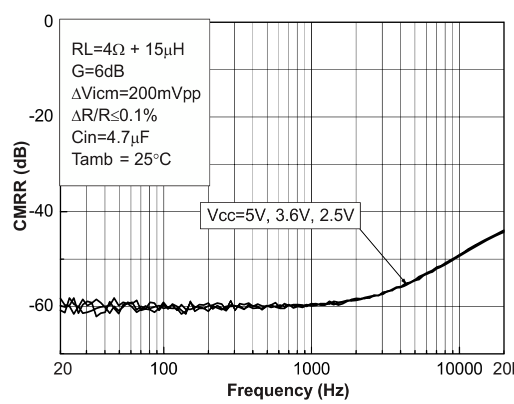


Figure 24. CMRR vs. frequency at R_L = 4 Ω + 30 µH

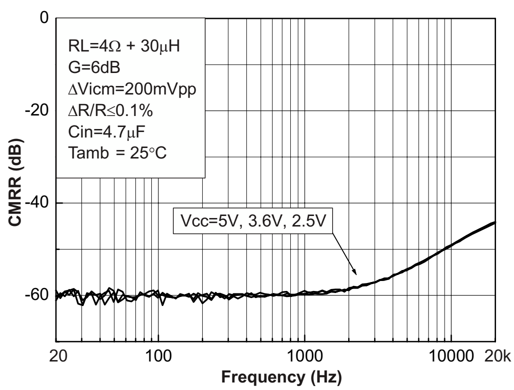


Figure 25. CMRR vs. frequency at R_L = 4 Ω + filter

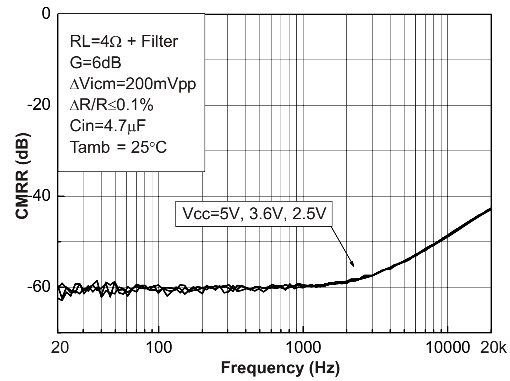


Figure 26. CMRR vs. frequency at R_L = 8 Ω + 15 µH

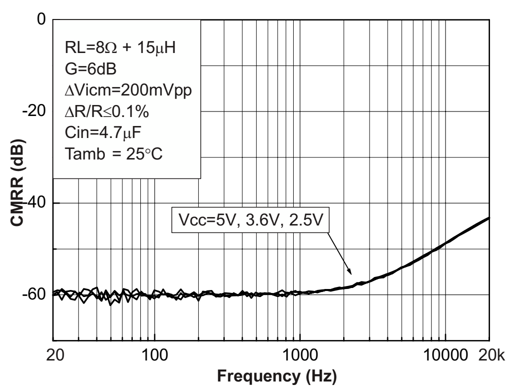


Figure 27. CMRR vs. frequency at R_L = 8 Ω + 30 µH

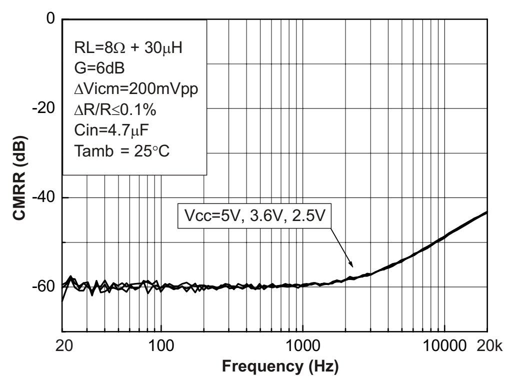


Figure 28. CMRR vs. frequency at R_L = 8 Ω + filter

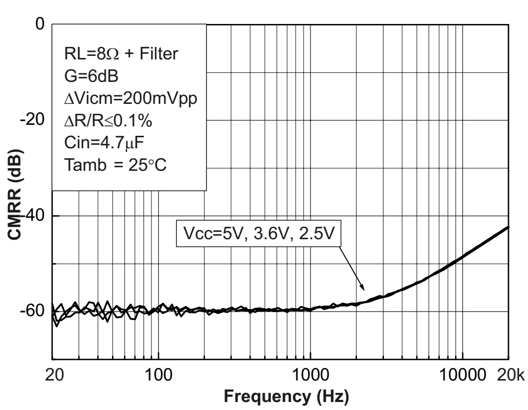


Figure 29. CMRR vs. common-mode input voltage

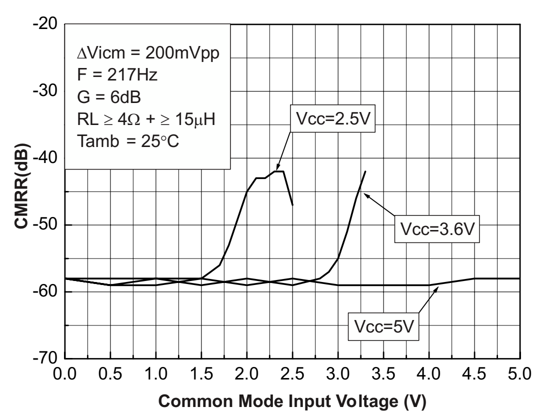


Figure 30. THD+N vs. output power at R_L = 4 Ω + 15 µH, F = 100 Hz

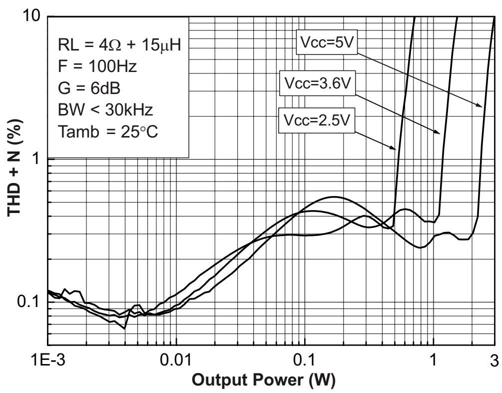


Figure 31. THD+N vs. output power at R_L = 4 Ω + 30 µH or filter, F = 100 Hz

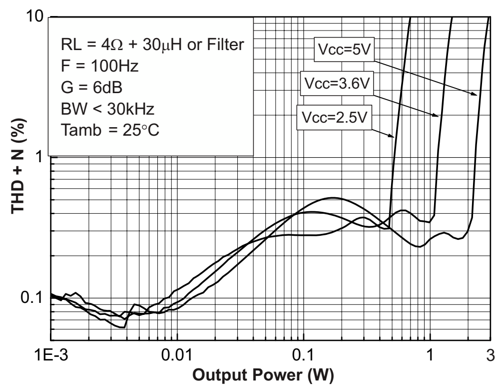


Figure 32. THD+N vs. output power at R_L = 8 Ω + 15 µH, F = 100 Hz

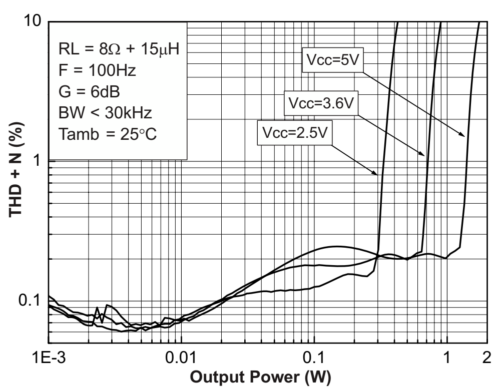


Figure 33. THD+N vs. output power at R_L = 8 Ω + 30 µH or filter, F = 100 Hz

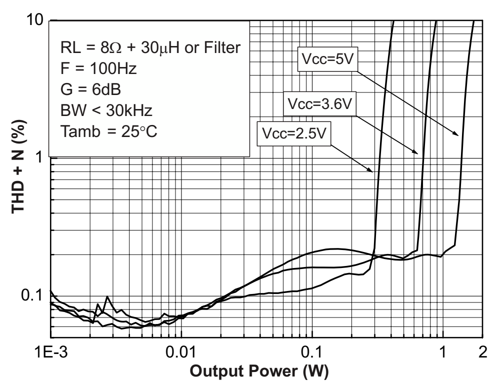


Figure 34. THD+N vs. output power at R_L = 4 Ω + 15 µH, F = 1 kHz

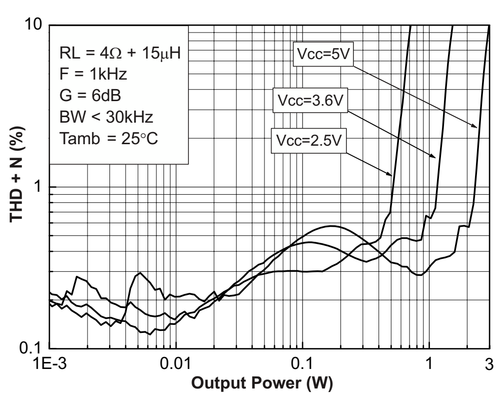


Figure 35. THD+N vs. output power at R_L = 4 Ω + 30 µH or filter, F = 1 kHz

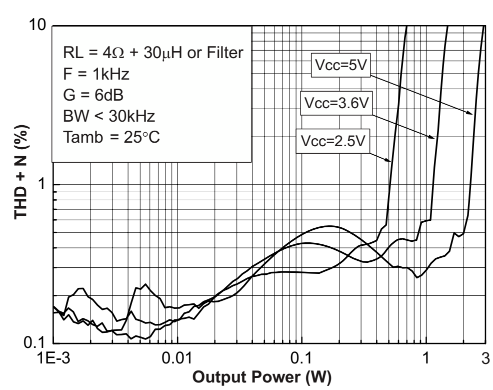


Figure 36. THD+N vs. output power at R_L = 8 Ω + 15 µH, F = 1 kHz

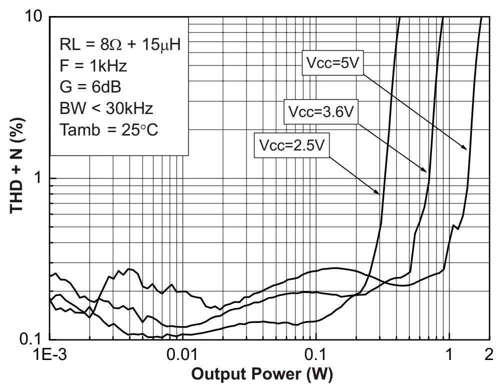


Figure 37. THD+N vs. output power at R_L = 8 Ω + 30 µH or filter, F = 1 kHz

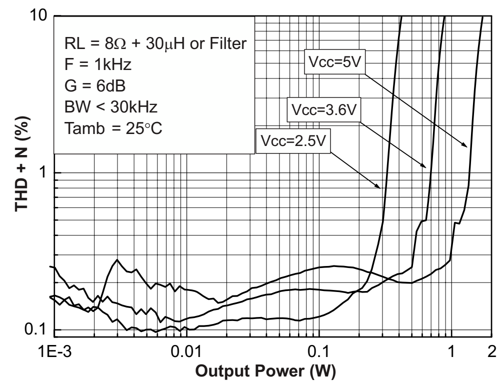


Figure 38. THD+N vs. frequency at R_L = 4 Ω + 15 µH, V_{CC} = 5 V

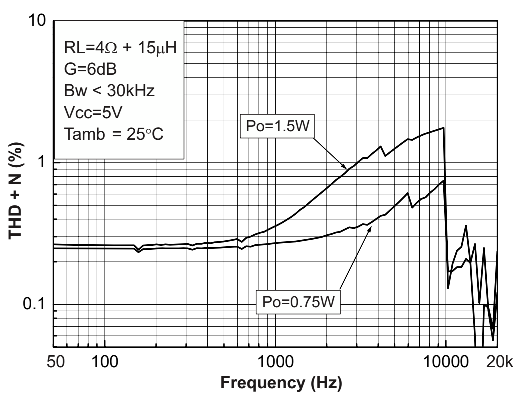


Figure 39. THD+N vs. frequency at R_L = 4 Ω + 30 µH or filter, V_{CC} = 5 V

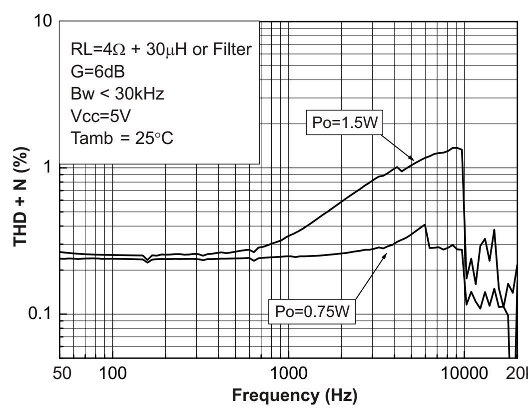


Figure 40. THD+N vs. frequency at R_L = 4 Ω + 15 µH, V_{CC} = 3.6 V

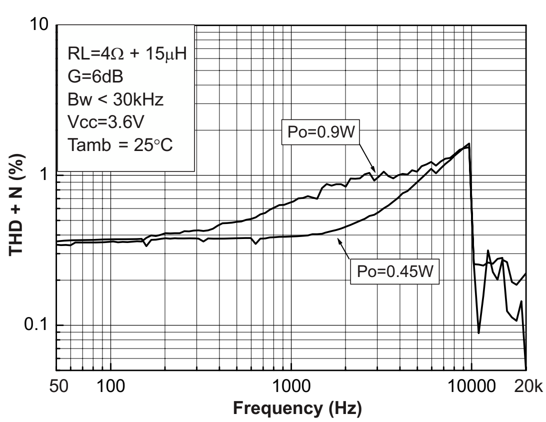


Figure 41. THD+N vs. frequency at R_L = 4 Ω + 30 H or filter, V_{CC} = 3.6 V

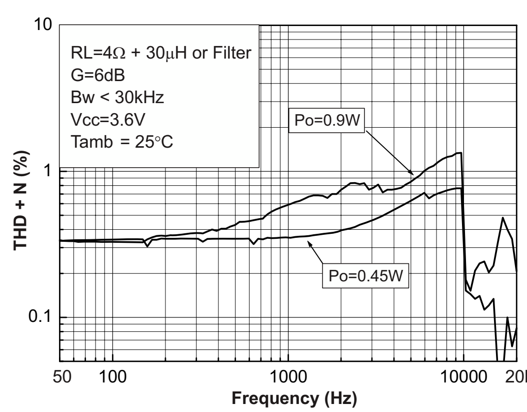


Figure 42. THD+N vs. frequency at R_L = 4 Ω + 15 µH, V_{CC} = 2.5 V

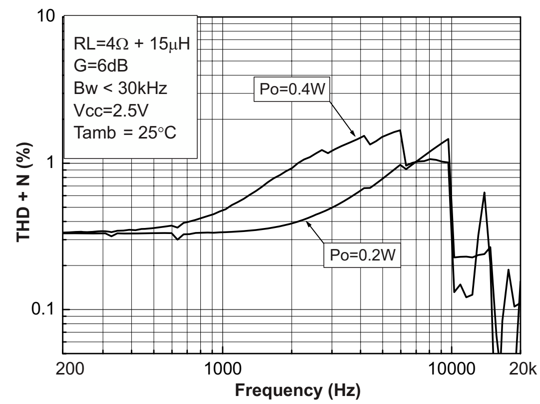


Figure 43. THD+N vs. frequency at R_L = 4 Ω + 30 µH or filter, V_{CC} = 2.5 V

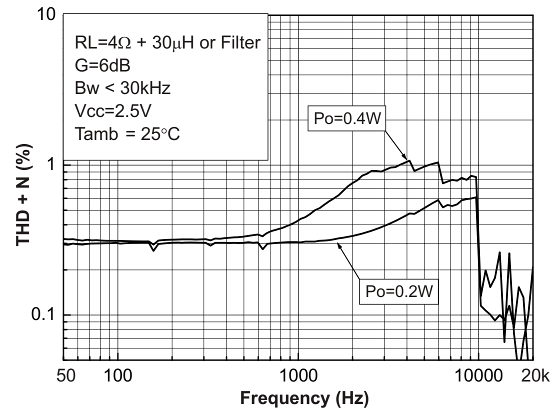


Figure 44. THD+N vs. frequency at R_L = 8 Ω + 15 µH, V_{CC} = 5 V

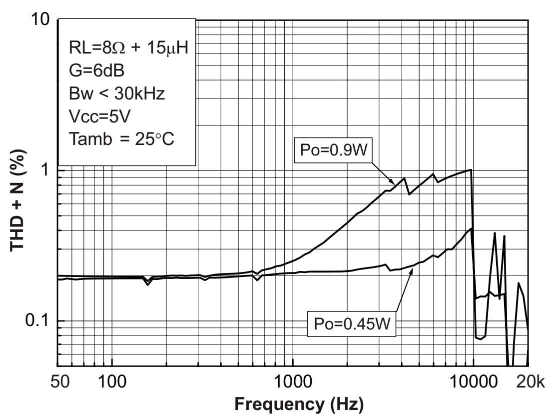


Figure 45. THD+N vs. frequency at R_L = 8 Ω + 30 µH or filter, V_{CC} = 5 V

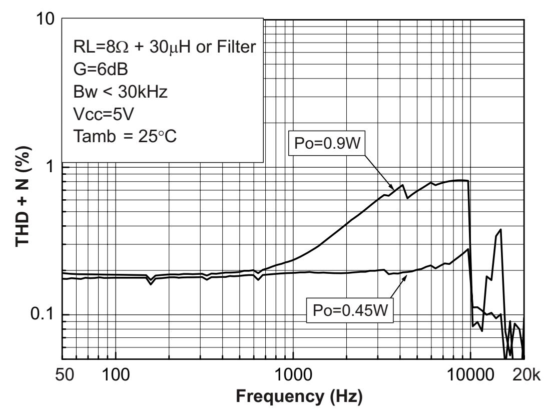


Figure 46. THD+N vs. frequency at R_L = 8 Ω + 15 µH, V_{CC} = 3.6 V

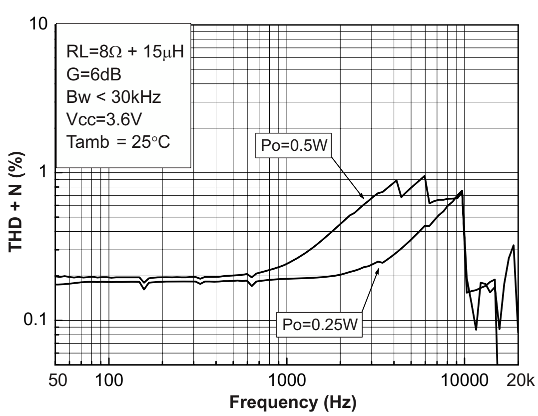


Figure 47. THD+N vs. frequency at R_L = 8 Ω + 30 µH or filter, V_{CC} = 3.6 V

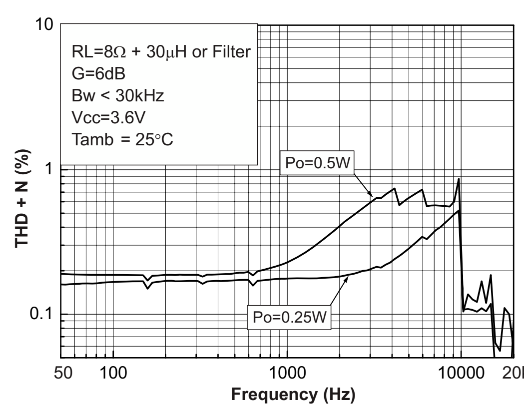


Figure 48. THD+N vs. frequency at R_L = 8 Ω + 15 µH, V_{CC} = 2.5 V

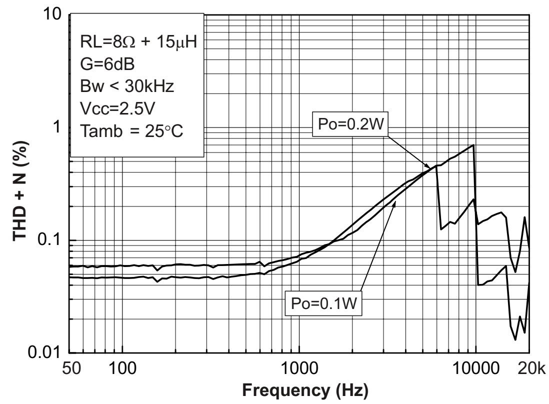


Figure 49. THD+N vs. frequency at R_L = 8 Ω + 30 µH or filter, V_{CC} = 2.5 V

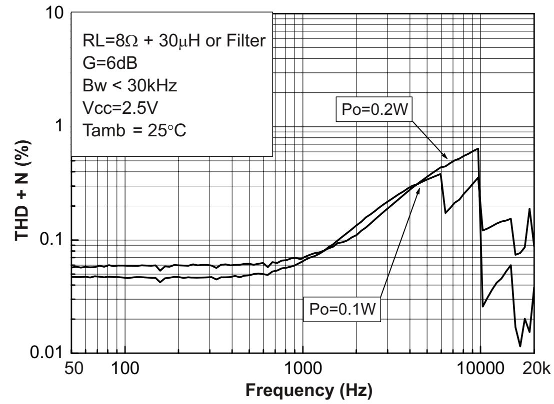


Figure 50. Gain vs. frequency at R_L = 4 Ω + 15 µH

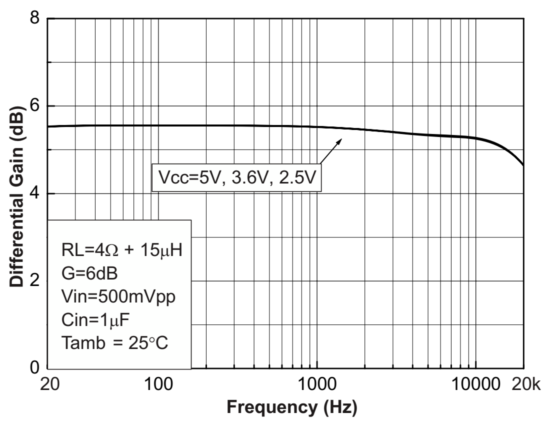


Figure 51. Gain vs. frequency at R_L = 4 Ω + 30 µH

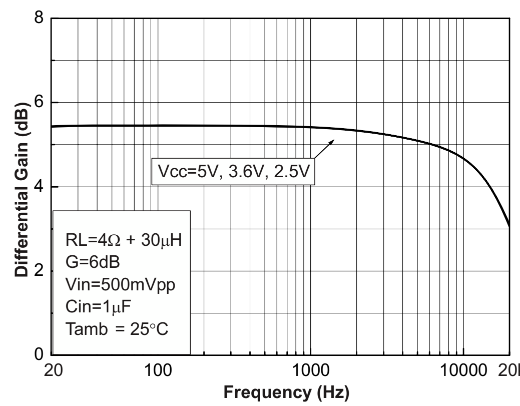


Figure 52. Gain vs. frequency at R_L = 4 Ω + filter

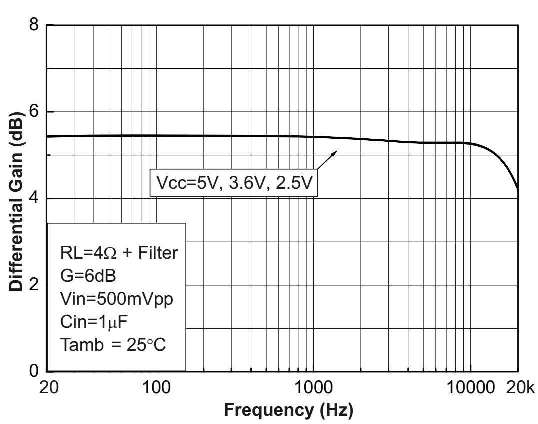


Figure 53. Gain vs. frequency at R_L = 8 Ω + 15 µH

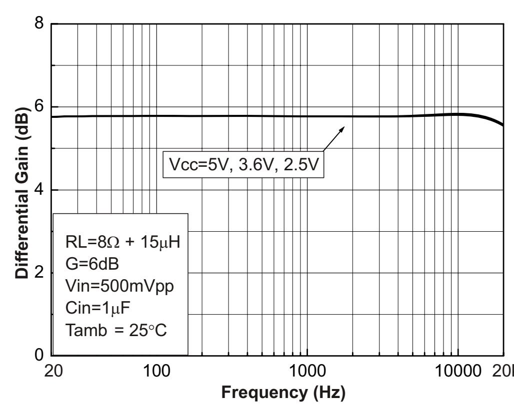


Figure 54. Gain vs. frequency at $R_L = 8\ \Omega + 30\ \mu H$

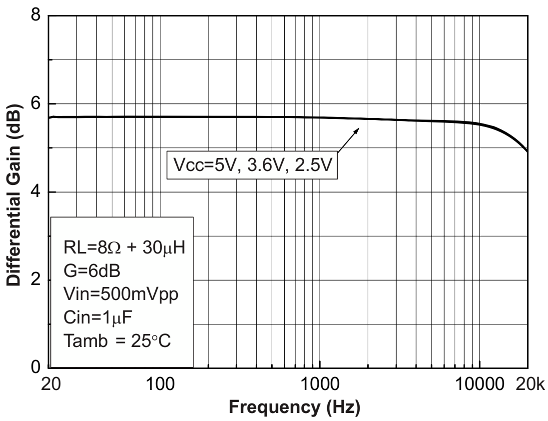


Figure 55. Gain vs. frequency at $R_L = 8\ \Omega$ + filter

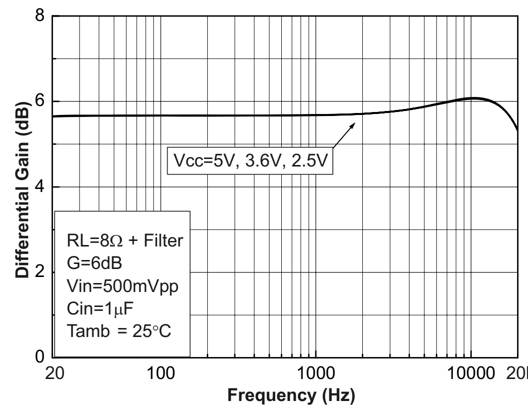


Figure 56. Gain vs. frequency at R_L = no load

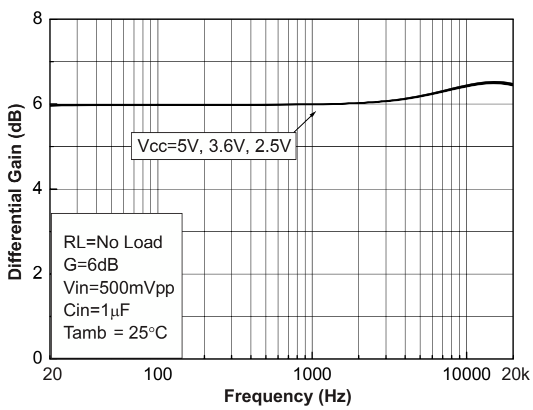


Figure 57. Startup and shutdown time $V_{CC} = 5$ V, G = 6 dB, $C_{in} = 1\ \mu F$ (5 ms/div)

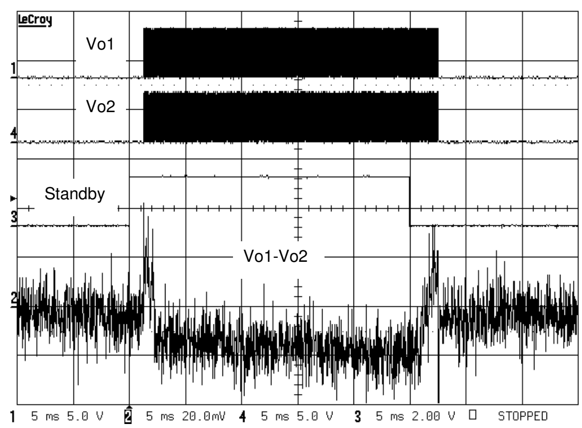


Figure 58. Startup and shutdown time $V_{CC} = 3$ V, G = 6 dB, $C_{in} = 1\ \mu F$ (5 ms/div)

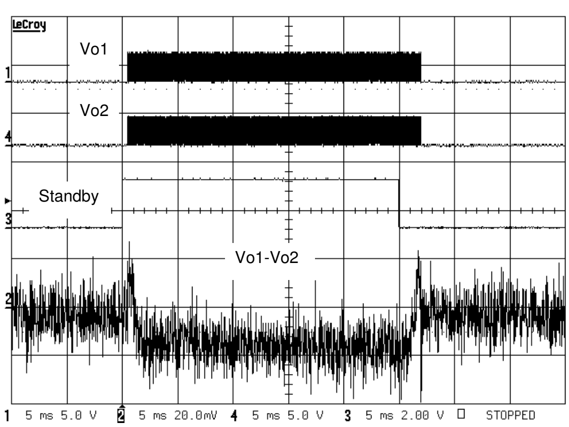


Figure 59. Startup and shutdown time $V_{CC} = 5$ V, G = 6 dB, $C_{in} = 100$ nF (5 ms/div)

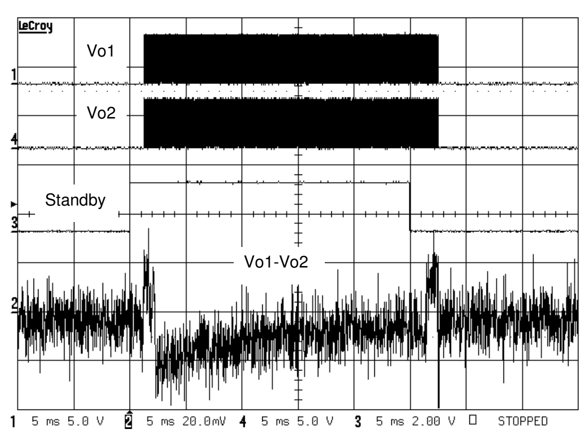


Figure 60. Startup and shutdown time V_{CC} = 3 V, G = 6 dB, C_{in} = 100 nF (5 ms/div)

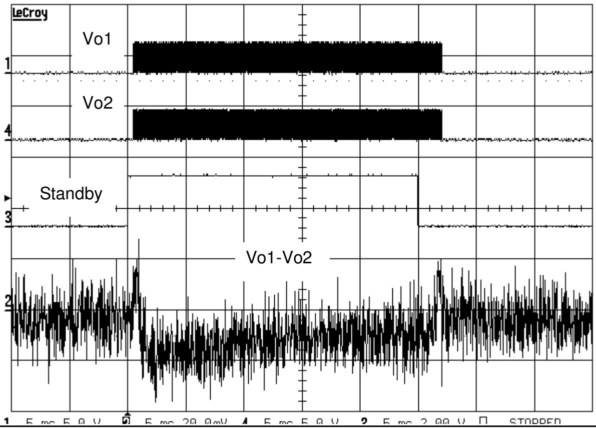


Figure 61. Startup and shutdown time V_{CC} = 5 V, G = 6 dB, No C_{in} (5 ms/div)

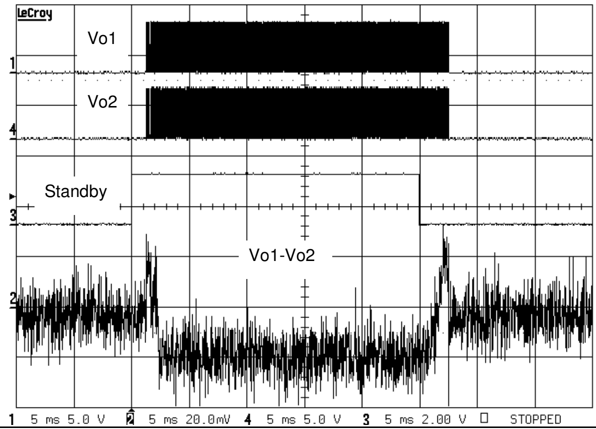
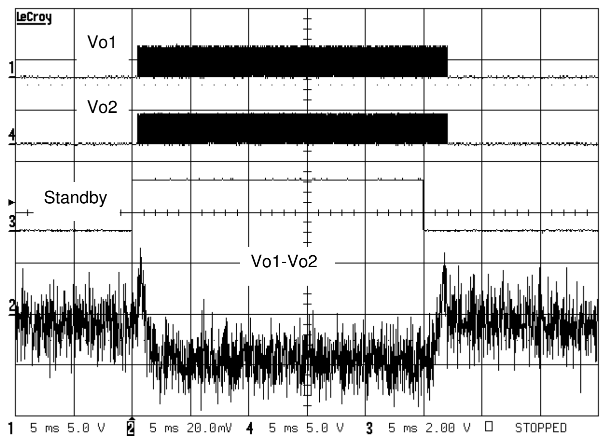


Figure 62. Startup and shutdown time V_{CC} = 3 V, G = 6 dB, no C_{in} (5 ms/div)



6 Application information

6.1 Differential configuration principle

The TS4962M is a monolithic fully-differential input/output class D power amplifier. The TS4962M also includes a common-mode feedback loop that controls the output bias value to average it at $V_{CC}/2$ for any DC common-mode input voltage. This allows the device to always have a maximum output voltage swing, and by consequence, maximizes the output power. Moreover, as the load is connected differentially compared to a single-ended topology, the output is four times higher for the same power supply voltage.

The advantages of a full-differential amplifier are:

- High PSRR (power supply rejection ratio)
- High common-mode noise rejection
- Virtually zero pop without additional circuitry, giving a faster start-up time compared to conventional single-ended input amplifiers.
- Easier interfacing with differential output audio DAC
- No input coupling capacitors required due to common-mode feedback loop

The main disadvantage is:

- As the differential function is directly linked to external resistor mismatching, particular attention to this mismatching is mandatory to obtain the best performance from the amplifier.

6.2 Gain in typical application schematic

Typical differential applications are shown in *Figure 3 on page 4*.

In the flat region of the frequency-response curve (no input coupling capacitor effect), the differential gain is expressed by the relation:

$$A_{V_{diff}} = \frac{Out^{+} - Out^{-}}{In^{+} - In^{-}} = \frac{300}{R_{in}}$$

with R_{in} expressed in kΩ.

Due to the tolerance of the internal 150 kΩ feedback resistor, the differential gain will be in the range (no tolerance on R_{in}):

$$\frac{273}{R_{in}} \leq A_{V_{diff}} \leq \frac{327}{R_{in}}$$

6.3 Common-mode feedback loop limitations

The common-mode feedback loop allows the output DC bias voltage to be averaged at $V_{CC}/2$ for any DC common-mode bias input voltage.

However, due to V_{icm} limitation in the input stage (see *Table 3: Operating conditions on page 5*), the common-mode feedback loop can ensure its role only within a defined range. This range depends upon the values of V_{CC} and R_{in} (A_{Vdiff}). To have a good estimation of the V_{icm} value, we can apply this formula (no tolerance on R_{in}):

$$V_{icm} = \frac{V_{CC} \times R_{in} + 2 \times V_{IC} \times 150k\Omega}{2 \times (R_{in} + 150k\Omega)} \quad (V)$$

with

$$V_{IC} = \frac{In^{+} + In^{-}}{2} \quad (V)$$

and the result of the calculation must be in the range:

$$0.5V \leq V_{icm} \leq V_{CC} - 0.8V$$

Due to the ±9% tolerance on the 150kΩ resistor, it is also important to check V_{icm} in these conditions:

$$\frac{V_{CC} \times R_{in} + 2 \times V_{IC} \times 136.5k\Omega}{2 \times (R_{in} + 136.5k\Omega)} \leq V_{icm} \leq \frac{V_{CC} \times R_{in} + 2 \times V_{IC} \times 163.5k\Omega}{2 \times (R_{in} + 163.5k\Omega)}$$

If the result of the V_{icm} calculation is not in the previous range, input coupling capacitors must be used (with V_{CC} from 2.4V to 2.5V, input coupling capacitors are mandatory).

Example

With V_{CC} = 3 V, R_{in} = 150 k and V_{IC} = 2.5 V, we typically find V_{icm} = 2 V and this is lower than 3V - 0.8 V = 2.2 V. With 136.5 kΩ we find 1.97 V, and with 163.5 kΩ we have 2.02 V. So, no input coupling capacitors are required.

6.4 Low frequency response

If a low frequency bandwidth limitation is requested, it is possible to use input coupling capacitors.

In the low frequency region, C_{in} (input coupling capacitor) starts to have an effect. C_{in} forms, with R_{in}, a first order high-pass filter with a -3dB cut-off frequency:

$$F_{CL} = \frac{1}{2\pi \times R_{in} \times C_{in}} \quad (Hz)$$

So, for a desired cut-off frequency we can calculate C_{in},

$$C_{in} = \frac{1}{2\pi \times R_{in} \times F_{CL}} \quad (F)$$

with R_{in} in Ω and F_{CL} in Hz.

6.5 Decoupling of the circuit

A power supply capacitor, referred to as $C_{S,}$ is needed to correctly bypass the TS4962M.

The TS4962M has a typical switching frequency at 250 kHz and an output fall and rise time about 5ns. Due to these very fast transients, careful decoupling is mandatory.

A 1 µF ceramic capacitor is enough, but it must be located very close to the TS4962M in order to avoid any extra parasitic inductance created by an overly long track wire. In relation with dI/dt, this parasitic inductance introduces an overvoltage that decreases the global efficiency and, if it is too high, may cause a breakdown of the device.

In addition, even if a ceramic capacitor has an adequate high-frequency ESR value, its current capability is also important. A 0603 size is a good compromise, particularly when a 4 Ω load is used.

Another important parameter is the rated voltage of the capacitor. A 1 µF/6.3 V capacitor used at 5 V, loses about 50% of its value. In fact, with a 5V power supply voltage, the decoupling value is about 0.5 µF instead of 1µF. As C_S has particular influence on the THD+N in the medium-high frequency region, this capacitor variation becomes decisive. In addition, less decoupling means higher overshoots, which can be problematic if they reach the power supply AMR value (6 V).

6.6 Wake-up time (t_{WU})

When the standby is released to set the device ON, there is a wait of about 5ms. The TS4962M has an internal digital delay that mutes the outputs and releases them after this time in order to avoid any pop noise.

6.7 Shutdown time (t_{STBY})

When the standby command is set, the time required to put the two output stages into high impedance and to put the internal circuitry in shutdown mode, is about 5 ms. This time is used to decrease the gain and avoid any pop noise during shutdown.

6.8 Consumption in shutdown mode

Between the shutdown pin and GND there is an internal 300 kΩ resistor. This resistor forces the TS4962M to be in standby mode when the standby input pin is left floating.

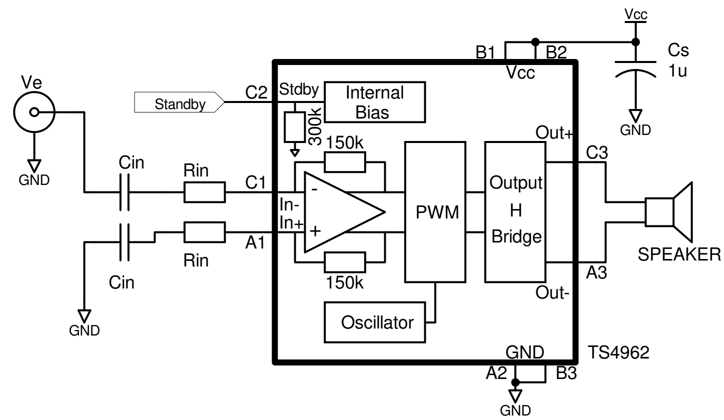
However, this resistor also introduces additional power consumption if the shutdown pin voltage is not 0 V.

For example, with a 0.4 V standby voltage pin, *Table 3: Operating conditions on page 5*, shows that you must add 0.4 V/300 kΩ = 1.3 µA in typical (0.4 V/273 kΩ = 1.46 µA in maximum) to the shutdown current specified in *Table 4 on page 6*.

6.9 Single-ended input configuration

It is possible to use the TS4962M in a single-ended input configuration. However, input coupling capacitors are needed in this configuration. The schematic in *Figure 63* shows a single-ended input typical application.

Figure 63. Single-ended input typical application



All formulas are identical except for the gain (with R_{in} in kΩ):

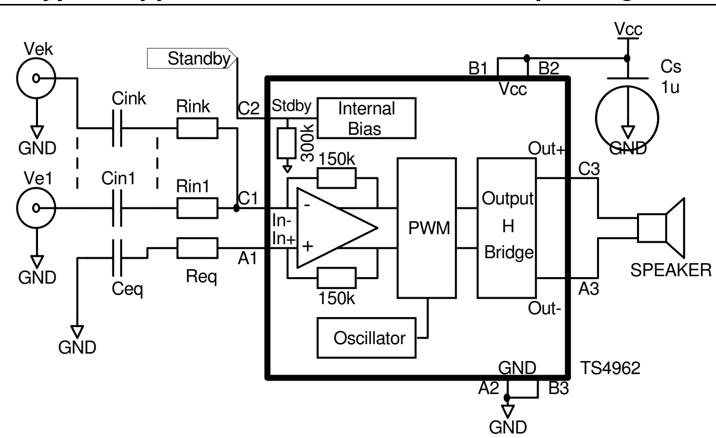
$$A_{V_{single}} = \frac{V_e}{Out^+ - Out^-} = \frac{300}{R_{in}}$$

And, due to the internal resistor tolerance we have:

$$\frac{273}{R_{in}} \leq A_{V_{single}} \leq \frac{327}{R_{in}}$$

In the event that multiple single-ended inputs are summed, it is important that the impedance on both TS4962M inputs (In^- and In^+) are equal.

Figure 64. Typical application schematic with multiple single-ended inputs



We have the following equations:

$$Out^{+} - Out^{-} = V_{e1} \times \frac{300}{R_{in1}} + \ldots + V_{ek} \times \frac{300}{R_{ink}} \quad \text{(V)}$$

$$C_{eq} = \sum_{j=1}^{k} C_{inj}$$

$$C_{inj} = \frac{1}{2 \times \pi \times R_{inj} \times F_{CLj}} \quad \text{(F)}$$

$$R_{eq} = \frac{1}{\sum_{j=1}^{k} \frac{1}{R_{inj}}}$$

In general, for mixed situations (single-ended and differential inputs), it is best to use the same rule, that is, to equalize impedance on both TS4962M inputs.

6.10 Output filter considerations

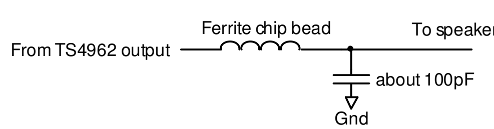
The TS4962M is designed to operate without an output filter. However, due to very sharp transients on the TS4962M output, EMI radiated emissions may cause some standard compliance issues.

These EMI standard compliance issues can appear if the distance between the TS4962M outputs and loudspeaker terminal is long (typically more than 50mm, or 100mm in both directions, to the speaker terminals). As the PCB layout and internal equipment device are different for each configuration, it is difficult to provide a one-size-fits-all solution.

However, to decrease the probability of EMI issues, there are several simple rules to follow:

- Reduce, as much as possible, the distance between the TS4962M output pins and the speaker terminals.
- Use ground planes for “shielding” sensitive wires
- Place, as close as possible to the TS4962M and in series with each output, a ferrite bead with a rated current at minimum 2A and impedance greater than 50Ω at frequencies above 30MHz. If, after testing, these ferrite beads are not necessary, replace them by a short-circuit. Murata BLM18EG221SN1 or BLM18EG121SN1 are possible examples of devices you can use.
- Allow enough of a footprint to place, if necessary, a capacitor to short perturbations to ground (see the schematics in *Figure 65*).

Figure 65. Method for shorting pertubations to ground

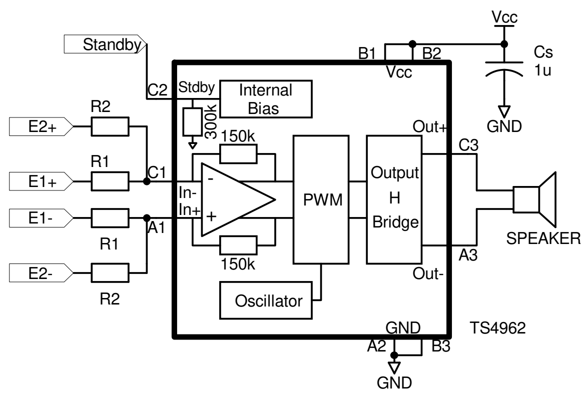


In the case where the distance between the TS4962M outputs and speaker terminals is high, it is possible to have low frequency EMI issues due to the fact that the typical operating frequency is 250kHz. In this configuration, we recommend using an output filter (as shown in *Figure 3: Typical application schematics on page 4*). It should be placed as close as possible to the device.

6.11 Different examples with summed inputs

Example 1: Dual differential inputs

Figure 66. Typical application schematic with dual differential inputs



With (R_i in kΩ):

$$A_{V_1} = \frac{Out^+ - Out^-}{E_1^+ - E_1^-} = \frac{300}{R_1}$$

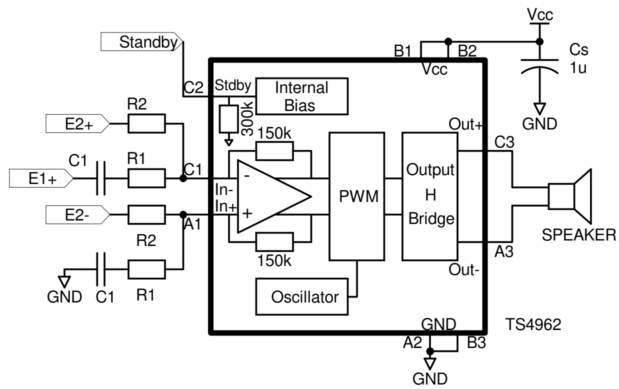
$$A_{V_2} = \frac{Out^+ - Out^-}{E_2^+ - E_2^-} = \frac{300}{R_2}$$

$$0.5V \leq \frac{V_{CC} \times R_1 \times R_2 + 300 \times (V_{IC1} \times R_2 + V_{IC2} \times R_1)}{300 \times (R_1 + R_2) + 2 \times R_1 \times R_2} \leq V_{CC} - 0.8V$$

$$V_{IC_1} = \frac{E_1^+ + E_1^-}{2} \quad \text{and} \quad V_{IC_2} = \frac{E_2^+ + E_2^-}{2}$$

Example 2: One differential input plus one single-ended input

Figure 67. Typical application schematic with one differential input plus one single-ended input



With (R_i in kΩ):

$$A_{V_1} = \frac{Out^+ - Out^-}{E_1^{\ +}} = \frac{300}{R_1}$$

$$A_{V_2} = \frac{Out^+ - Out^-}{E_2^{\ +} - E_2^{\ -}} = \frac{300}{R_2}$$

$$C_1 = \frac{1}{2\pi \times R_1 \times F_{CL}} \quad \text{(F)}$$

7 Evaluation board

An evaluation board for the TS4962M is available with a Flip Chip to DIP adapter. For more information about this board, refer to AN2134.

Figure 68. Schematic diagram of mono class D evaluation board for TS4962M

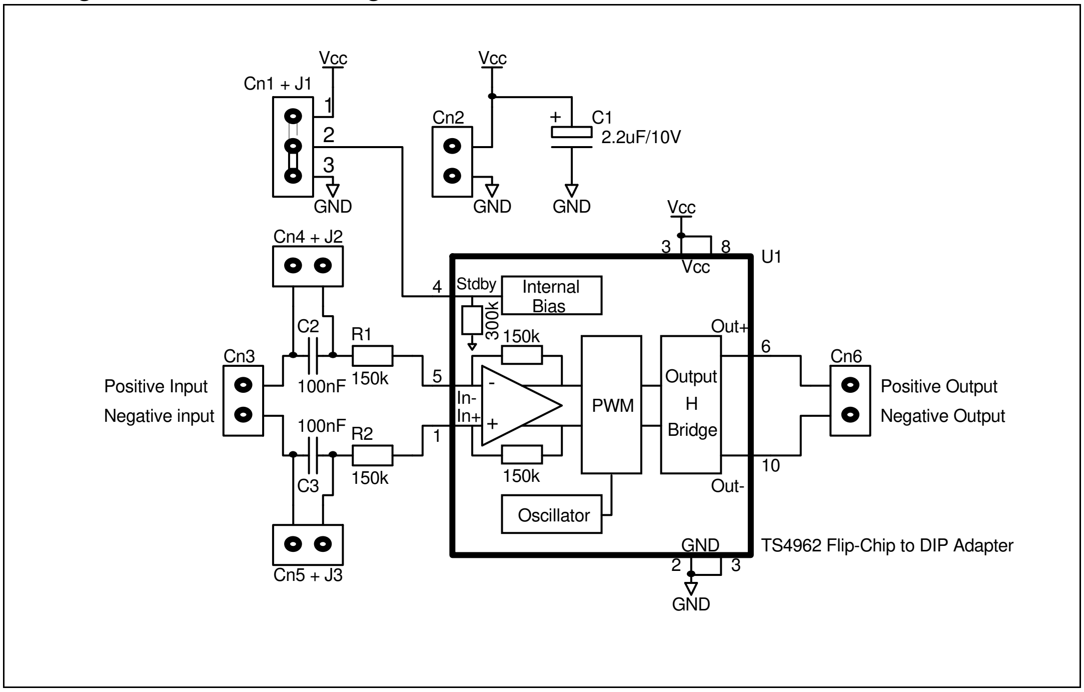


Figure 69. Diagram for Flip Chip to DIP adapter

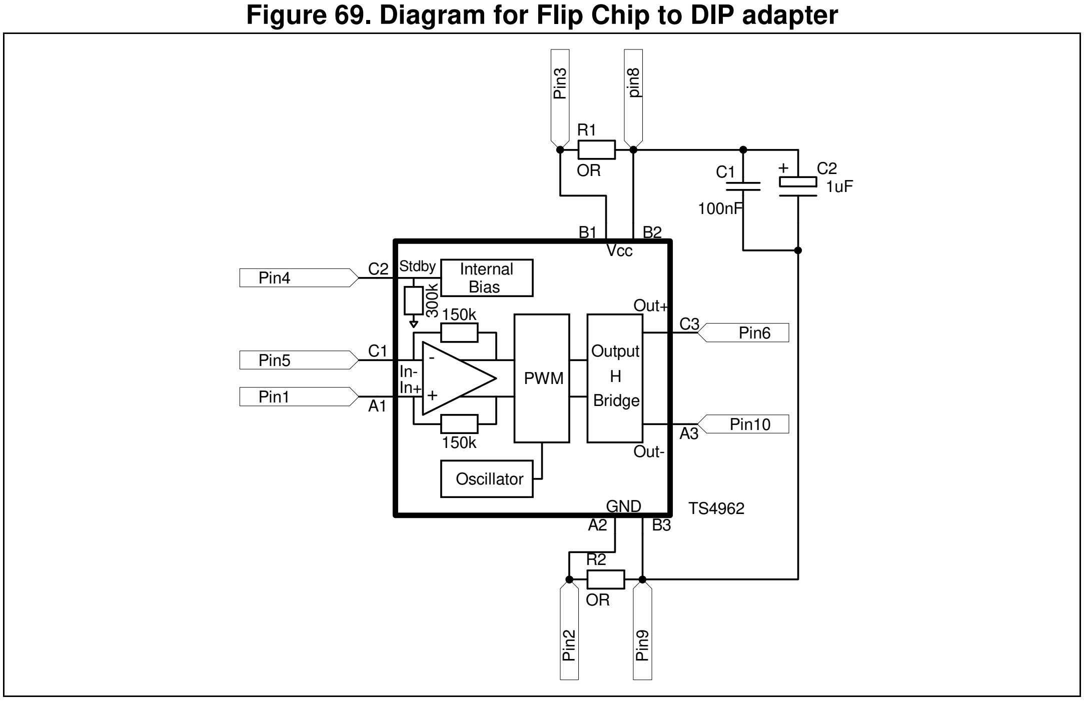


Figure 70. Top view

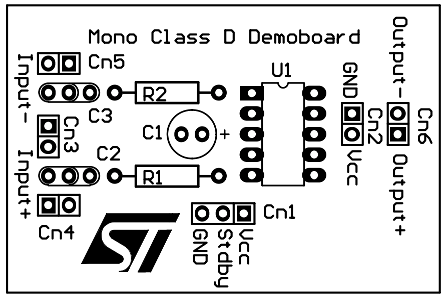


Figure 71. Bottom layer

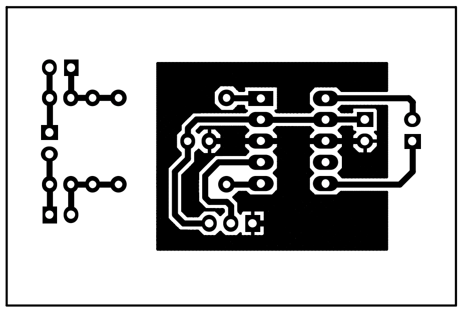
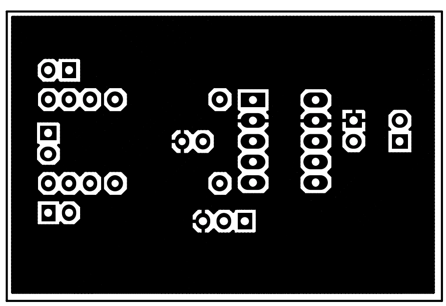


Figure 72. Top layer



8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

8.1 9-bump Flip Chip package information

Figure 73. 9-bump Flip Chip package outline

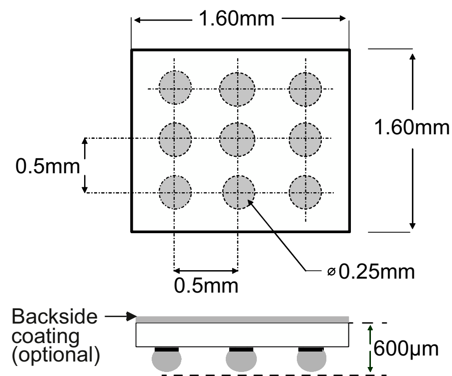
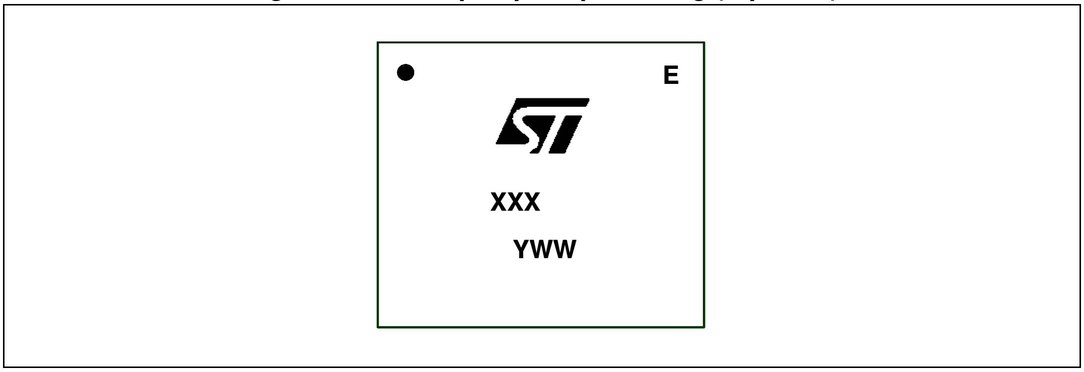


Table 10. 9-bump Flip Chip mechanical data

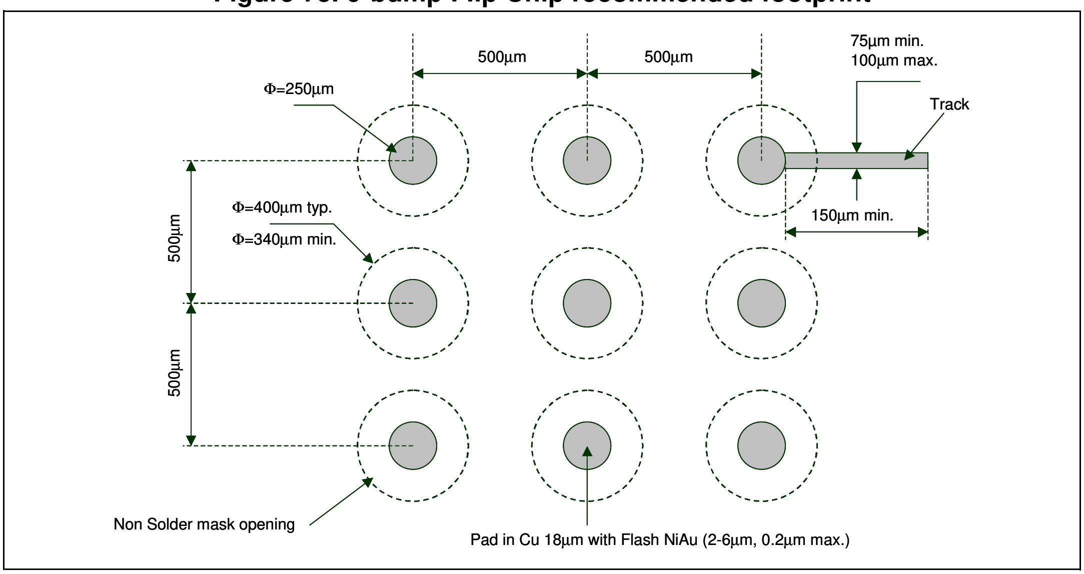
Parameter	Dimensions
Die size	1.6 mm x 1.6 mm ±30 µm
Die height (including bumps)	600 µm
Bump diameter	315 µm ±50 µm
Bump diameter before re-flow	300 µm ±10 µm
Bump height	250 µm ±40 µm
Die height	350 µm ±20 µm
Pitch	500 µm ±50 µm
Coplanarity	50 µm max.
Backside coating (optional, only for the TS4962MEIKJT)	25 µm ±3 µm

Figure 74. 9-bump Flip Chip marking (top view)



1. Legend:
   ST logo
   E = symbol for lead-free
   First two “XX” = product code = 62
   Third X = assembly code
   Three-digit date code, Y = year, WW = week
   Black dot is for marking pin A1

Figure 75. 9-bump Flip Chip recommended footprint



9 Ordering information

Table 11. Order code table

Part number	Temperature range	Package	Packing	Marking
TS4962MEIJT	-40 °C to 85 °C	Lead-free Flip Chip	Tape and reel	62L
TS4962MEIKJT		Lead-free Flip Chip with backside coating		

10 Revision history

Table 12. Document revision history

Date	Revision	Changes
Oct. 2005	1	First release corresponding to the product preview version.
Nov. 2005	2	Electrical data updated for output voltage noise, see Table 4, Table 5, Table 6, Table 7, Table 8 and Table 9 Formatting changes throughout.
Dec. 2005	3	Product in full production.
10-Jan-2007	4	Template update, no technical changes.
10-Oct-2016	5	Updated datasheet layout Added package silhouettes Added *Related products* Updated *Applications* *Section 5: Electrical characteristic curves*: updated titles of graphs which had same titles. *Figure 73: 9-bump Flip Chip package outline*: updated diagram to display the optional backside coating for order code TS4962MEIKJT. Added *Table 10* to display package mechanical data as a separate table (with information concerning the optional backside coating for order code TS4962MEIKJT). *Table 11: Order code table*: updated marking of order code TS4962MEIJT, added order code TS4962MEIKJT.
15-Jan-2018	6	Updated Table 10: 9-bump Flip Chip mechanical data.
17-Mar-2020	7	Removed feature on the cover page and footnote R_{thja} parameter in *Table 2*.