



The Future of Analog IC Technology®

MP1472

2A, 18V Synchronous Rectified Step-Down Converter

DESCRIPTION

The MP1472 is a monolithic synchronous buck regulator. The device integrates a 175mΩ high-side MOSFET and a 115mΩ low-side MOSFET that provide 2A of continuous load current over a wide input voltage of 4.75V to 18V. Current mode control provides fast transient response and cycle-by-cycle current limit.

An adjustable soft-start prevents inrush current at turn-on, and in shutdown mode the supply current drops to 1µA.

This device, available in an 8-pin TSOT23-8 package, provides a very compact solution with minimal external components.

FEATURES

- 2A Output Current
- Wide 4.75V to 18V Operating Input Range
- Integrated Power MOSFET Switches
- Output Adjustable from 0.923V to 15V
- Up to 95% Efficiency
- Programmable Soft-Start
- Stable with Low ESR Ceramic Output Capacitors
- Fixed 340kHz Frequency
- Cycle-by-Cycle Over Current Protection
- Input Under Voltage Lockout
- 8-Pin TSOT23-8

APPLICATIONS

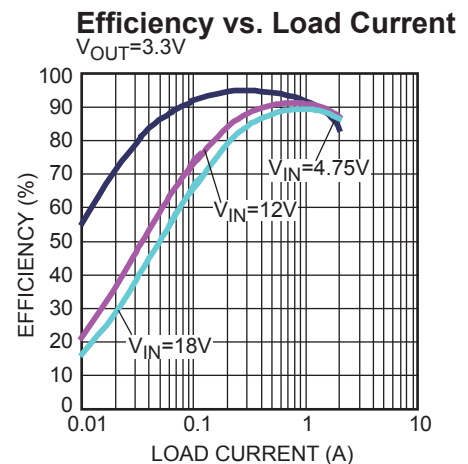
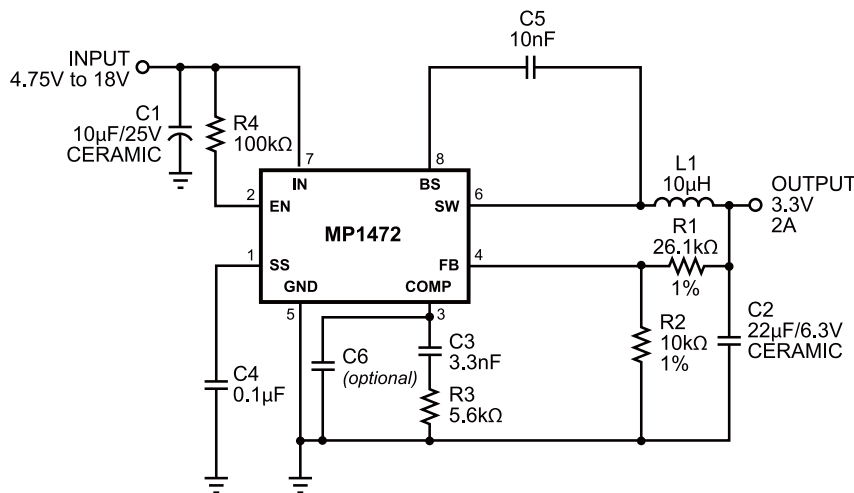
- Distributed Power Systems
- Networking Systems
- FPGA, DSP, ASIC Power Supplies
- Green Electronics/ Appliances
- Notebook Computers

EVALUATION BOARD REFERENCE

| Board Number | Dimensions |
|--------------|-----------------------|
| EV1472GJ-00A | 2.5"X x 2.5"Y x 0.5"Z |

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TYPICAL APPLICATION

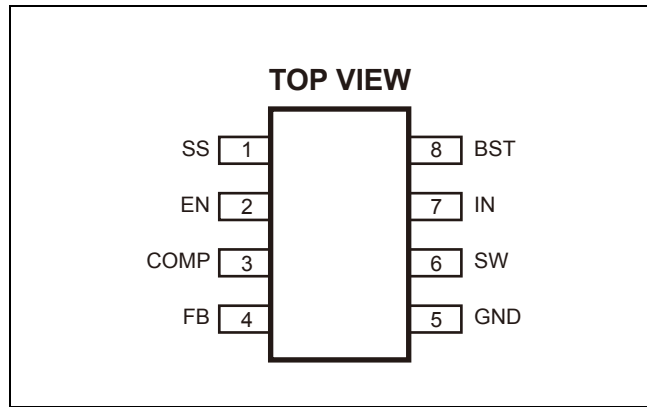


ORDERING INFORMATION

| Part Number | Package | Top Marking |
|-------------|----------|-------------|
| MP1472GJ* | TSOT23-8 | ACW |

*For Tape & Reel, add suffix -Z (e.g. MP1472GJ-Z);

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS ⁽¹⁾

| | |
|---|----------------------------------|
| Supply Voltage V_{IN} | -0.3V to +20V |
| Switch Node Voltage V_{SW} | 21V |
| Boost Voltage V_{BS} | $V_{SW} - 0.3V$ to $V_{SW} + 6V$ |
| All Other Pins | -0.3V to +6V |
| Junction Temperature | 150°C |
| Continuous Power Dissipation ($T_A = +25^\circ C$) ⁽²⁾ | 1.25W |
| Lead Temperature | 260°C |
| Storage Temperature | -65°C to +150°C |

Recommended Operating Conditions ⁽³⁾

| | |
|--|---------------|
| Input Voltage V_{IN} | 4.75V to 18V |
| Output Voltage V_{OUT} | 0.923V to 15V |
| Maximum Junction Temp. (T_J) | +125°C |

| | | |
|--|---------------|---------------|
| Thermal Resistance ⁽⁴⁾ | θ_{JA} | θ_{JC} |
| TSOT23-8 | 100 | 55... °C/W |

Notes:

- 1) Exceeding these ratings may damage the device.
- 2) The maximum allowable power dissipation is a function of the maximum junction temperature $T_J(MAX)$, the junction-to-ambient thermal resistance θ_{JA} , and the ambient temperature T_A . The maximum allowable continuous power dissipation at any ambient temperature is calculated by $P_D(MAX) = (T_J(MAX) - T_A) / \theta_{JA}$. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
- 3) The device is not guaranteed to function outside of its operating conditions.
- 4) Measured on JESD51-7 4-layer PCB.

ELECTRICAL CHARACTERISTICS

$V_{IN} = 12V$, $T_A = +25^{\circ}C$, unless otherwise noted.

| Parameter | Symbol | Condition | Min | Typ | Max | Units |
|--|---------------|-----------------------------------|-------|-------|-------|-------------|
| Shutdown Supply Current | | $V_{EN} = 0V$ | | 1 | 3.0 | μA |
| Supply Current | | $V_{EN} = 5.0V$; $V_{FB} = 1.0V$ | | 1.3 | 1.5 | mA |
| Feedback Voltage | V_{FB} | $4.75V \leq V_{IN} \leq 18V$ | 0.900 | 0.923 | 0.946 | V |
| Feedback Overvoltage Threshold | | | | 1.1 | | V |
| Error Amplifier Voltage Gain ⁽⁵⁾ | A_{EA} | | | 400 | | V/V |
| Error Amplifier Transconductance | G_{EA} | $\Delta I_C = \pm 10\mu A$ | | 800 | | $\mu A/V$ |
| High-Side Switch On Resistance ⁽⁵⁾ | $R_{DS(ON)1}$ | | | 175 | | m Ω |
| Low-Side Switch On Resistance ⁽⁵⁾ | $R_{DS(ON)2}$ | | | 115 | | m Ω |
| High-Side Switch Leakage Current | | $V_{EN} = 0V$, $V_{SW} = 0V$ | | | 10 | μA |
| Upper Switch Current Limit | | Minimum Duty Cycle | 3 | 4.1 | 5.3 | A |
| Lower Switch Current Limit | | From Drain to Source | | 1.1 | | A |
| COMP to Current Sense Transconductance | GCS | | | 3.5 | | A/V |
| Oscillation Frequency | F_{osc1} | | 305 | 340 | 375 | kHz |
| Short Circuit Oscillation Frequency | F_{osc2} | $V_{FB} = 0V$ | | 100 | | kHz |
| Maximum Duty Cycle | D_{MAX} | $V_{FB} = 0.8V$ | | 90 | | % |
| Minimum On Time ⁽⁵⁾ | | | | 220 | | ns |
| EN Shutdown Threshold Voltage | | V_{EN} Rising | 1.1 | 1.5 | 2.0 | V |
| EN Shutdown Threshold Voltage Hysteresis | | | | 210 | | mV |
| EN Lockout Threshold Voltage | | | 2.2 | 2.5 | 2.7 | V |
| EN Lockout Hysteresis | | | | 210 | | mV |
| Input Under Voltage Lockout Threshold | | V_{IN} Rising | 3.40 | 3.80 | 4.20 | V |
| Input Under Voltage Lockout Threshold Hysteresis | | | | 210 | | mV |
| Soft-Start Current | | $V_{SS} = 0V$ | | 6 | | μA |
| Soft-Start Period | | $C_{SS} = 0.1\mu F$ | | 15 | | ms |
| Thermal Shutdown ⁽⁵⁾ | | | | 160 | | $^{\circ}C$ |

Note:

5) Guaranteed by design, not tested.

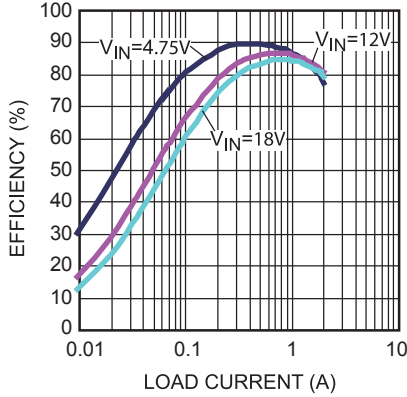
PIN FUNCTIONS

| Pin # | Name | Description |
|-------|------|--|
| 1 | SS | Soft-Start Control Input. SS controls the soft start period. Connect a capacitor from SS to GND to set the soft-start period. A 0.1 μ F capacitor sets the soft-start period to 15ms. To disable the soft-start feature, leave SS unconnected. |
| 2 | EN | Enable Input. EN is a digital input that turns the regulator on or off. Drive EN high to turn on the regulator, drive it low to turn it off. Pull up with 100k Ω resistor for automatic startup. |
| 3 | COMP | Compensation Node. COMP is used to compensate the regulation control loop. Connect a series RC network from COMP to GND to compensate the regulation control loop. In some cases, an additional capacitor from COMP to GND is required. See Compensation Components. |
| 4 | FB | Feedback Input. FB senses the output voltage to regulate that voltage. Drive FB with a resistive voltage divider from the output voltage. The feedback threshold is 0.923V. See Setting the Output Voltage. |
| 5 | GND | Ground. |
| 6 | SW | Power Switching Output. SW is the switching node that supplies power to the output. Connect the output LC filter from SW to the output load. Note that a capacitor is required from SW to BS to power the high-side switch. |
| 7 | IN | Power Input. IN supplies the power to the IC, as well as the step-down converter switches. Drive IN with a 4.75V to 18V power source. Bypass IN to GND with a suitably large capacitor to eliminate noise on the input to the IC. See Input Capacitor. |
| 8 | BS | High-Side Gate Drive Boost Input. BS supplies the drive for the high-side N-Channel MOSFET switch. Connect a 0.01 μ F or greater capacitor from SW to BS to power the high side switch. |

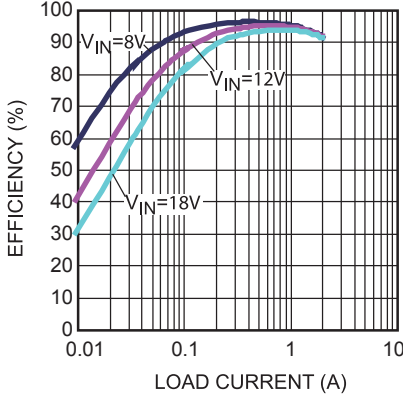
TYPICAL PERFORMANCE CHARACTERISTICS

$V_{IN} = 12V$, $V_O = 3.3V$, $C_{IN} = 10\mu F$, $C_{OUT} = 22\mu F$, $L = 10\mu H$, $T_A = +25^\circ C$, unless otherwise noted.

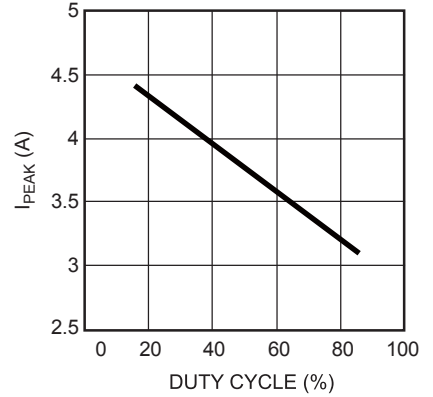
Efficiency vs. Load Current
 $V_{OUT} = 1.8V$



Efficiency vs. Load Current
 $V_{OUT} = 5.0V$

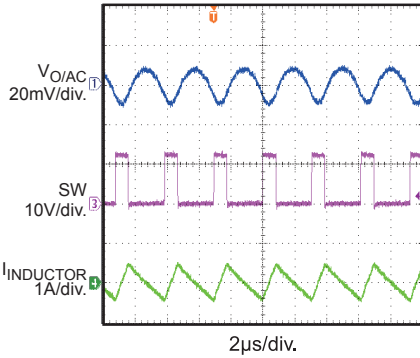


Peak Current vs. Duty Cycle



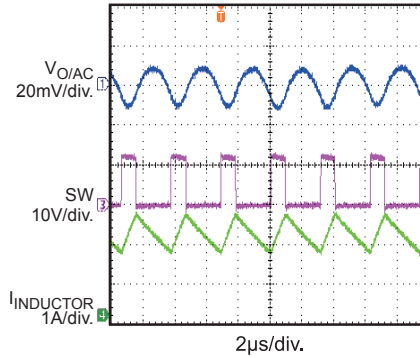
Output Ripple Voltage

$I_O = 0A$



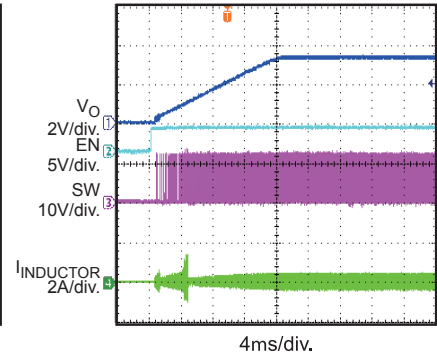
Output Ripple Voltage

$I_O = 2A$



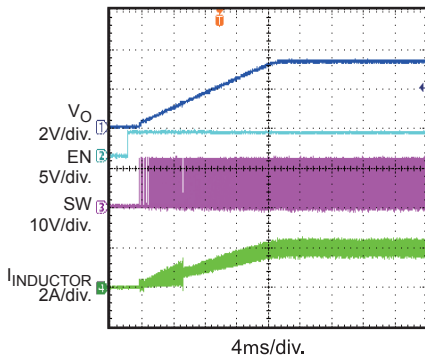
Enable Startup

$I_O = 0A$



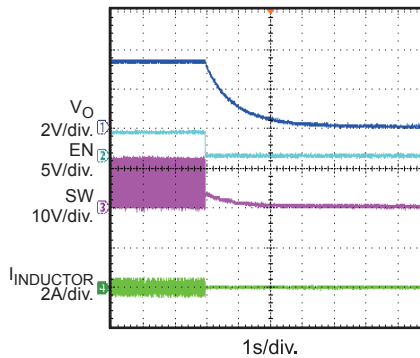
Enable Startup

$I_O = 2A$



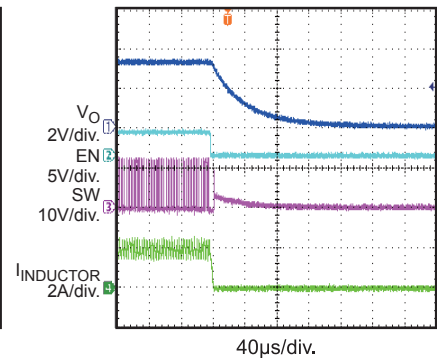
Enable Shutdown

$I_O = 0A$



Enable Shutdown

$I_O = 2A$



OPERATION

FUNCTIONAL DESCRIPTION

The MP1472 is a synchronous rectified, current-mode, step-down regulator. It regulates input voltages from 4.75V to 18V down to an output voltage as low as 0.923V, and supplies up to 2A of load current.

The MP1472 uses current-mode control to regulate the output voltage. The output voltage is measured at FB through a resistive voltage divider and amplified through the internal transconductance error amplifier. The voltage at the COMP pin is compared to the switch current measured internally to control the output voltage.

The converter uses internal N-Channel MOSFET switches to step-down the input voltage to the regulated output voltage. Since the high side MOSFET requires a gate voltage greater than the input voltage, a boost capacitor connected between SW and BS is needed to drive the high side gate. The boost capacitor is charged from the internal 5V rail when SW is low.

When the MP1472 FB pin exceeds 20% of the nominal regulation voltage of 0.923V, the over voltage comparator is tripped and the COMP pin and the SS pin are discharged to GND, forcing the high-side switch off.

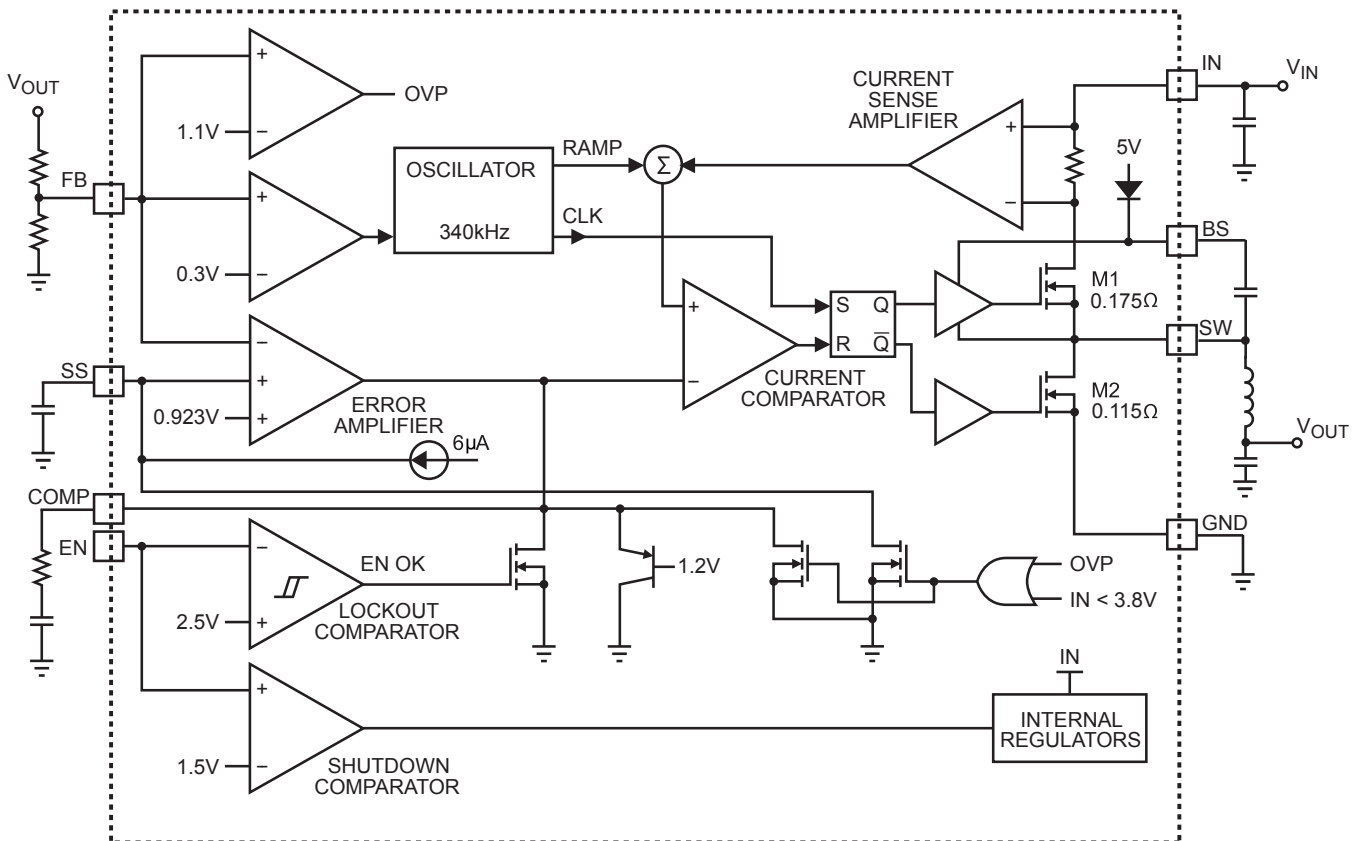


Figure 1—Functional Block Diagram

APPLICATIONS INFORMATION

COMPONENT SELECTION

Setting the Output Voltage

The output voltage is set using a resistive voltage divider from the output voltage to FB pin. The voltage divider divides the output voltage down to the feedback voltage by the ratio:

$$V_{FB} = V_{OUT} \frac{R2}{R1+R2}$$

Where V_{FB} is the feedback voltage and V_{OUT} is the output voltage.

Thus the output voltage is:

$$V_{OUT} = 0.923 \times \frac{R1+R2}{R2}$$

R2 can be as high as 100kΩ, but a typical value is 10kΩ. Using the typical value for R2, R1 is determined by:

$$R1 = 10.83 \times (V_{OUT} - 0.923) \text{ (k}\Omega\text{)}$$

For example, for a 3.3V output voltage, R2 is 10kΩ, and R1 is 26.1kΩ.

Inductor

The inductor is required to supply constant current to the output load while being driven by the switched input voltage. A larger value inductor will result in less ripple current that will result in lower output ripple voltage. However, the larger value inductor will have a larger physical

size, higher series resistance, and/or lower saturation current.

A good rule for determining the inductance to use is to allow the peak-to-peak ripple current in the inductor to be approximately 30% of the maximum switch current limit. Also, make sure that the peak inductor current is below the maximum switch current limit. The inductance value can be calculated by:

$$L = \frac{V_{OUT}}{f_s \times \Delta I_L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Where V_{OUT} is the output voltage, V_{IN} is the input voltage, f_s is the switching frequency, and ΔI_L is the peak-to-peak inductor ripple current.

Choose an inductor that will not saturate under the maximum inductor peak current. The peak inductor current can be calculated by:

$$I_{LP} = I_{LOAD} + \frac{V_{OUT}}{2 \times f_s \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Where I_{LOAD} is the load current.

Table 1 lists a number of suitable inductors from various manufacturers. The choice of which style inductor to use mainly depends on the price vs. size requirements and any EMI requirement.

Table 1—Inductor Selection Guide

| Part Number | Inductance (μH) | Max DCR (Ω) | Current Rating (A) | Dimensions L x W x H (mm ³) |
|--------------------------|-----------------|-------------|--------------------|--|
| Würth Electronics | | | | |
| 7440650068 | 6.8 | 0.033 | 3.6 | 10x10x2.8 |
| 744066100 | 10 | 0.035 | 3.6 | 10x10x3.8 |
| 744066150 | 15 | 0.050 | 3.2 | 10x10x3.8 |
| TDK | | | | |
| SLF10165T-6R8N4R33PF | 6.8 | 0.014 | 4.3 | 10x10x4.5 |
| SLF10165T-100M3R83PF | 10 | 0.0185 | 3.8 | 10x10x4.5 |
| SLF10165T-150M3R13PF | 15 | 0.027 | 3.1 | 10x10x4.5 |
| Toko | | | | |
| #B952AS-6R8N | 6.8 | 0.035 | 3.1 | 10.4x10.4x4.8 |
| #B892NAS-100M | 10 | 0.0225 | 4.2 | 12.3x12.3x4.5 |
| #B892NAS-150M | 15 | 0.0355 | 3.2 | 12.3x12.3x4.5 |

Optional Schottky Diode

During the transition between high-side switch and low-side switch, the body diode of the low-side power MOSFET conducts the inductor current. The forward voltage of this body diode is high. An optional Schottky diode may be paralleled between the SW pin and GND pin to improve overall efficiency. Table 2 lists example Schottky diodes and their Manufacturers.

Table 2—Diode Selection Guide

| Part Number | Voltage/Current Rating | Vendor |
|-------------|------------------------|-------------------------|
| B230 | 30V, 2A | Diodes, Inc. |
| SL23 | 30V, 2A | Vishay, Inc. |
| MBRS230 | 30V, 2A | International Rectifier |

Input Capacitor

The input current to the step-down converter is discontinuous, therefore a capacitor is required to supply the AC current to the step-down converter while maintaining the DC input voltage. Use low ESR capacitors for the best performance. Ceramic capacitors are preferred, but tantalum or low-ESR electrolytic capacitors may also suffice. Choose X5R or X7R dielectrics when using ceramic capacitors.

Since the input capacitor (C1) absorbs the input switching current it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated by:

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, where $I_{C1} = I_{LOAD}/2$. For simplification, choose the input capacitor whose RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum or ceramic. When using electrolytic or tantalum capacitors, a small, high quality ceramic capacitor, i.e. 0.1µF, should be placed as close to the IC as possible. When using ceramic capacitors, make sure that they have enough capacitance to provide sufficient charge to prevent excessive voltage ripple at input. The input voltage ripple for low ESR capacitors can be estimated by:

$$\Delta V_{IN} = \frac{I_{LOAD}}{C1 \times f_S} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Where C1 is the input capacitance value.

Output Capacitor

The output capacitor is required to maintain the DC output voltage. Ceramic, tantalum, or low ESR electrolytic capacitors are recommended. Low ESR capacitors are preferred to keep the output voltage ripple low. The output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_S \times C2}\right)$$

Where C2 is the output capacitance value and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

In the case of ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is mainly caused by the capacitance. For simplification, the output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_S^2 \times L \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

In the case of tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated to:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR}$$

The characteristics of the output capacitor also affect the stability of the regulation system. The MP1472 can be optimized for a wide range of capacitance and ESR values.

Compensation Components

MP1472 employs current mode control for easy compensation and fast transient response. The system stability and transient response are controlled through the COMP pin. COMP pin is the output of the internal transconductance error amplifier. A series capacitor-resistor combination sets a pole-zero combination to control the characteristics of the control system.

The DC gain of the voltage feedback loop is given by:

$$A_{VDC} = R_{LOAD} \times G_{CS} \times A_{EA} \times \frac{V_{FB}}{V_{OUT}}$$

Where A_{VEA} is the error amplifier voltage gain; G_{CS} is the current sense transconductance and R_{LOAD} is the load resistor value.

The system has two poles of importance. One is due to the compensation capacitor (C3) and the output resistor of the error amplifier, and the other is due to the output capacitor and the load resistor. These poles are located at:

$$f_{P1} = \frac{G_{EA}}{2\pi \times C3 \times A_{VEA}}$$

$$f_{P2} = \frac{1}{2\pi \times C2 \times R_{LOAD}}$$

Where G_{EA} is the error amplifier transconductance.

The system has one zero of importance, due to the compensation capacitor (C3) and the compensation resistor (R3). This zero is located at:

$$f_{Z1} = \frac{1}{2\pi \times C3 \times R3}$$

The system may have another zero of importance, if the output capacitor has a large capacitance and/or a high ESR value. The zero, due to the ESR and capacitance of the output capacitor, is located at:

$$f_{ESR} = \frac{1}{2\pi \times C2 \times R_{ESR}}$$

In this case, a third pole set by the compensation capacitor (C6) and the compensation resistor (R3) is used to compensate the effect of the ESR zero on the loop gain. This pole is located at:

$$f_{P3} = \frac{1}{2\pi \times C6 \times R3}$$

The goal of compensation design is to shape the converter transfer function to get a desired loop gain. The system crossover frequency where the feedback loop has the unity gain is important. Lower crossover frequencies result in slower line and load transient responses, while higher

crossover frequencies could cause system instability. A good rule of thumb is to set the crossover frequency below one-tenth of the switching frequency.

Table 3 lists the typical values of compensation components for some standard output voltages with various output capacitors and inductors. The values of the compensation components have been optimized for fast transient responses and good stability at given conditions.

Table 3—Compensation Values for Typical Output Voltage/Capacitor Combinations

| V _{OUT} | L1 | C2 | R3 | C3 | C6 |
|------------------|-------|-------------------|-------|-------|------|
| 1.8V | 6.8uH | 22μF/6.3V Ceramic | 3.3kΩ | 5.6nF | None |
| 3.3V | 10μH | 22μF/6.3V Ceramic | 5.6kΩ | 3.3nF | None |
| 5.0V | 15μH | 22μF/6.3V Ceramic | 10kΩ | 2.2nF | None |
| 12.0V | 22μH | 22μF/16V Ceramic | 15kΩ | 1.0nF | None |

To optimize the compensation components, the following procedure can be used.

1. Choose the compensation resistor (R3) to set the desired crossover frequency.

Determine the R3 value by the following equation:

$$R3 = \frac{2\pi \times C2 \times f_C}{G_{EA} \times G_{CS}} \times \frac{V_{OUT}}{V_{FB}} < \frac{2\pi \times C2 \times 0.1 \times f_S}{G_{EA} \times G_{CS}} \times \frac{V_{OUT}}{V_{FB}}$$

Where f_C is the desired crossover frequency which is typically below one tenth of the switching frequency.

2. Choose the compensation capacitor (C3) to achieve the desired phase margin. For applications with typical inductor values, setting the compensation zero, f_{Z1} , below one-fourth of the crossover frequency provides sufficient phase margin.

Determine the C3 value by the following equation:

$$C3 > \frac{4}{2\pi \times R3 \times f_C}$$

where R3 is the compensation resistor.

3. Determine if the second compensation capacitor (C6) is required. It is required if the ESR zero of the output capacitor is located at less than half of the switching frequency, or the following relationship is valid:

$$\frac{1}{2\pi \times C2 \times R_{ESR}} < \frac{f_s}{2}$$

If this is the case, then add the second compensation capacitor (C6) to set the pole f_{p3} at the location of the ESR zero. Determine the C6 value by the equation:

$$C6 = \frac{C2 \times R_{ESR}}{R3}$$

External Bootstrap Diode

An external bootstrap diode may enhance the efficiency of the regulator, and it will be a must if the applicable condition is:

- $V_{OUT}=5V$ or $3.3V$; and
- duty cycle is high: $D = \frac{V_{OUT}}{V_{IN}} > 65\%$

In these cases, an external BST diode is recommended from the output of the voltage regulator to BST pin, as shown in Figure 2

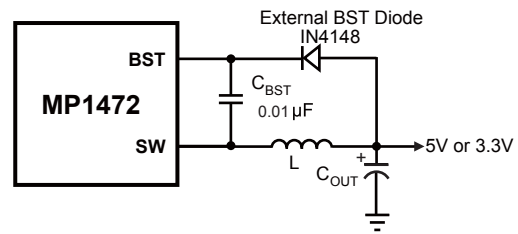
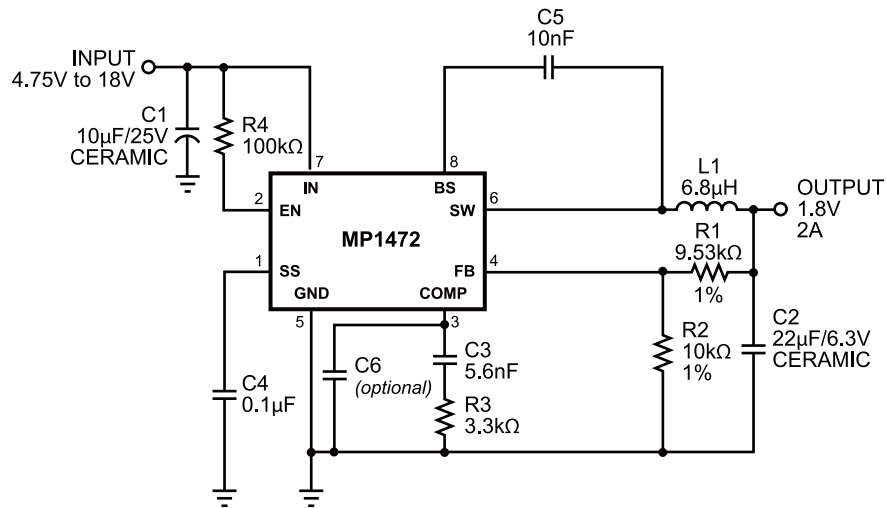
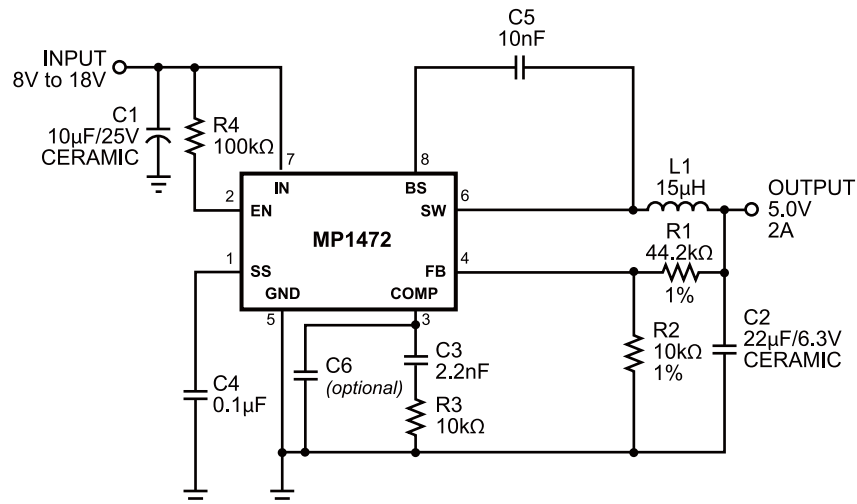


Figure 2—Add Optional External Bootstrap Diode to Enhance Efficiency

The recommended external BST diode is IN4148, and the BST cap is $0.01\mu F$.

typical Application circuit

Figure 3—MP1472 with 1.8V Output, 22µF/6.3V Ceramic Output Capacitor

Figure 4—MP1472 with 5.0V Output, 22µF/6.3V Ceramic Output Capacitor

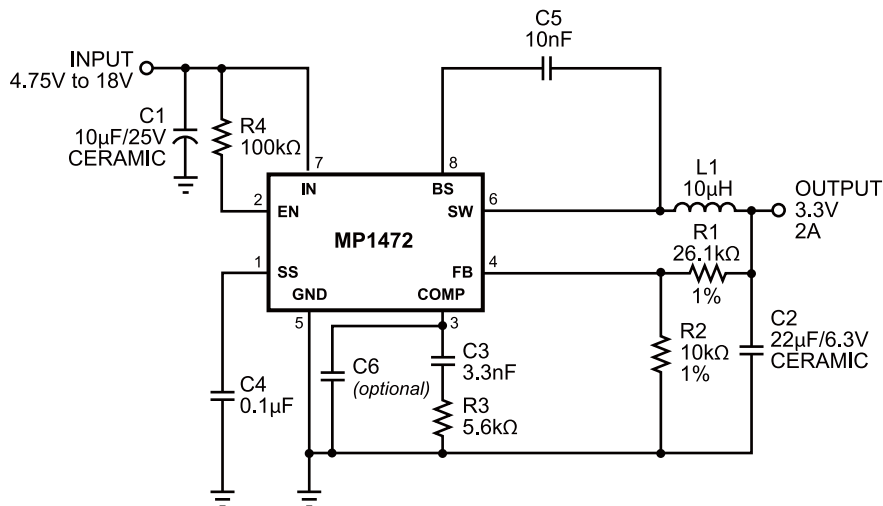
PCB LAYOUT GUIDE

PCB layout is very important to achieve stable operation. It is highly recommended to duplicate EVB layout for optimum performance.

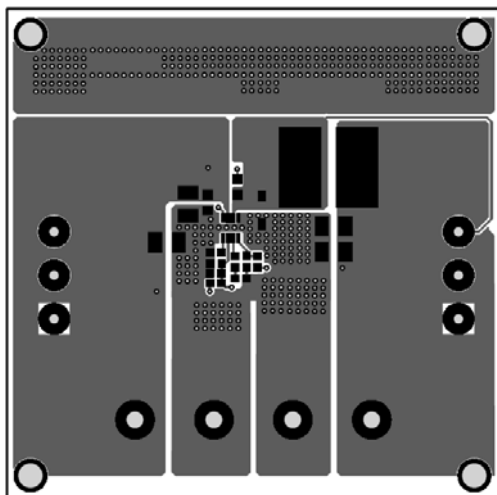
If change is necessary, please follow these guidelines and take Figure 5 for reference.

1) Keep the path of switching current short and minimize the loop area formed by input cap, high-side MOSFET and low-side MOSFET.

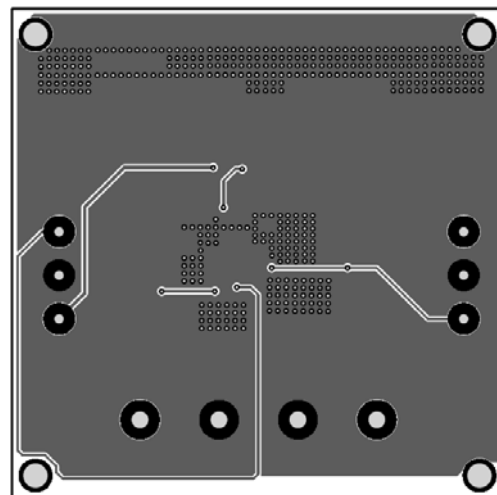
- 2) Bypass ceramic capacitors are suggested to be put close to the Vin Pin.
- 3) Ensure all feedback connections are short and direct. Place the feedback resistors and compensation components as close to the chip as possible.
- 4) Route SW away from sensitive analog areas such as FB.
- 5) Connect IN, SW, and especially GND respectively to a large copper area to cool the chip to improve thermal performance and long-term reliability.



MP1472 Typical Application Circuit

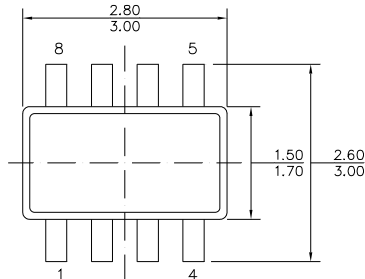
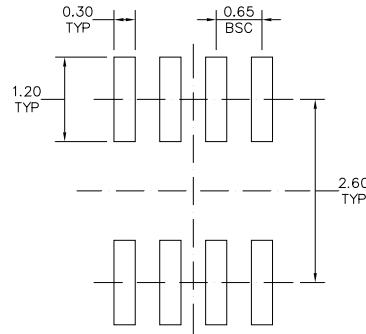
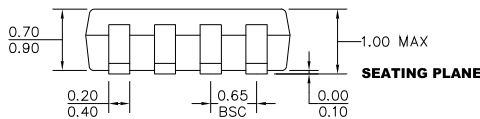
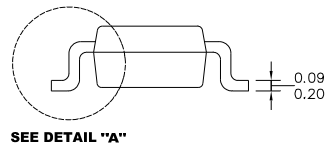
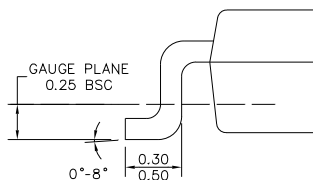


Top Layer



Bottom Layer

Figure 5—MP1472 Typical Application Circuit and PCB Layout Guide

PACKAGE INFORMATION
TSOT23-8

TOP VIEW

RECOMMENDED LAND PATTERN

FRONT VIEW

SIDE VIEW

DETAIL "A"
NOTE:

- 1) ALL DIMENSIONS ARE IN MILLIMETERS.
- 2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
- 3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
- 4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
- 5) JEDEC REFERENCE IS MO-193, VARIATION BA.
- 6) DRAWING IS NOT TO SCALE.

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