

**3A LOW NOISE STEP-DOWN DC-DC CONVERTER**

**Description**

The PAM2303 is a 3A step-down DC-DC converter. It operates in two different modes: PSM and PWM modes. At light load, it automatically enters into the PSM mode to improve efficiency. At heavy load, the constant frequency PWM control performs excellent stability and transient response. No external compensation components are required.

The PAM2303 supports a range of input voltages from 2.7V to 5.5V. The output voltage is adjustable from 0.6V to the input voltage. The PAM2303 employs internal power switch and synchronous rectifier to minimize external part count and realize high efficiency. During shutdown, the input is disconnected from the output and the shutdown current is less than 1µA. Other key features include over-temperature and short circuit protection, and under-voltage lockout to prevent deep battery discharge.

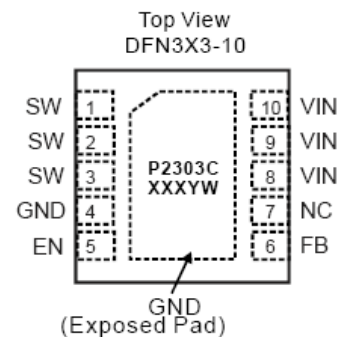
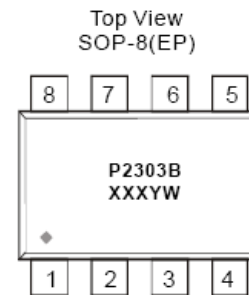
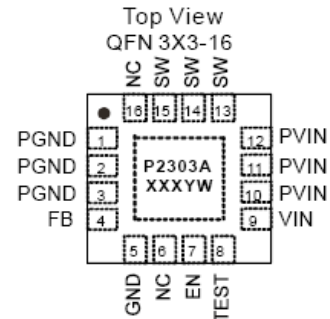
The PAM2303 delivers 3A maximum output current while consuming only 42µA of no-load quiescent current. Ultra-Low  $R_{DS(ON)}$  integrated MOSFETs and 100% duty cycle operation make the PAM2303 an ideal choice for high-output voltage, high-current applications which require a low dropout threshold.

The PAM2303 is available in SOP-8(EP), DFN3X3-10 and QFN3X3-16 package.

**Features**

- Output Current: Up to 3A
- Output Voltage: 0.6V to  $V_{IN}$
- Input Voltage: 2.7 to 5.5V
- Efficiency up to 95%
- 42µA (typ) No Load Quiescent Current
- Shutdown Current: <1A
- 100% Duty Cycle Operation
- 1.5MHz Switching Frequency
- Analog Soft Start
- No external Compensation Required
- Current Limit Protection
- Thermal Shutdown
- SOP-8(EP), DFN3X3-10 and QFN3X3-16 Package

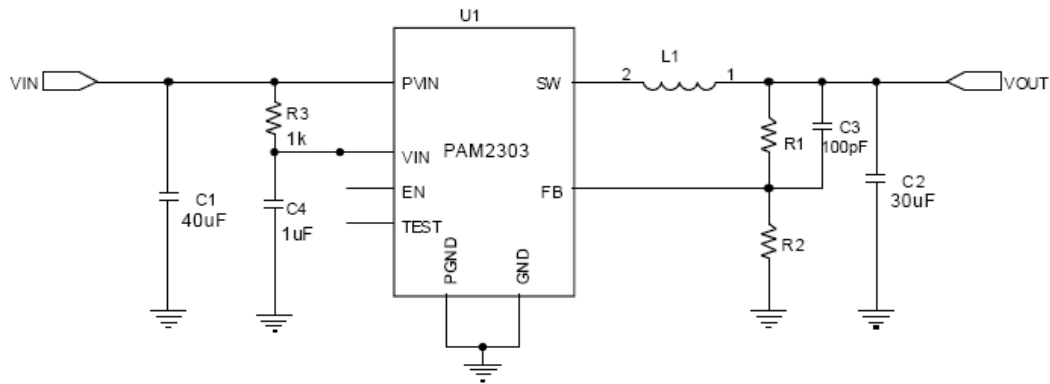
**Pin Assignments**



**Applications**

- 5V or 3.3V Point of Load Conversion
- Telecom/Networking Equipment
- Set Top Boxes
- Storage Equipment
- Video Cards
- DDR Power Supply

## Typical Applications Circuit

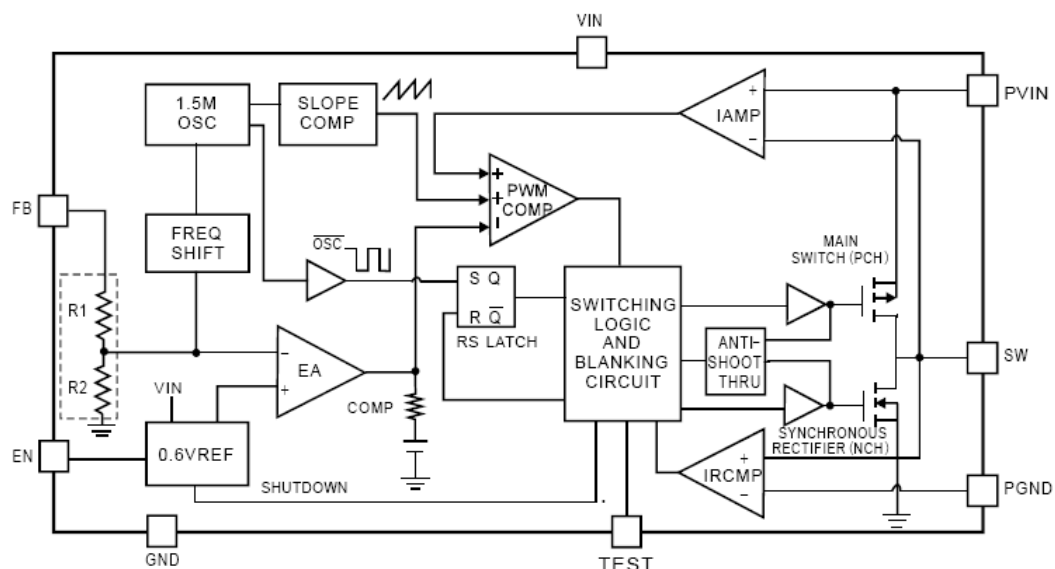


$$V_O = 0.6 \times \left( 1 + \frac{R_1}{R_2} \right)$$

## Pin Descriptions

Pin Name	Package Name			Function
	QFN3x3-16	SOP-8EP	DFN3x3-10	
PGND	1, 2, 3	2	—	Main power ground pin.
FB	4	3	6	Feedback voltage to internal error amplifier, the threshold voltage is 0.6V.
GND	5	4	4	Signal ground for small signal components.
NC	6, 16	—	7	Not connected.
EN	7	5	5	Enable control input. Force this pin voltage above 1.5V, enables the chip, and below 0.3V shuts down the device.
Test	8	6	—	Test mode. "Low" connection is recommended.
VIN	9	7	8, 9, 10	Bias supply. Chip main power supply pin.
PVIN	10, 11, 12	8	—	Input supply for power stage. Must be closely decoupled to PGND.
SW	13, 14, 15	1	1, 2, 3	The drains of the internal main and synchronous power MOSFET.

## Functional Block Diagram



## Absolute Maximum Ratings (@ $T_A = +25^\circ\text{C}$ , unless otherwise specified.)

These are stress ratings only and functional operation is not implied. Exposure to absolute maximum ratings for prolonged time periods may affect device reliability. All voltages are with respect to ground.

Parameter	Rating	Unit
Input Voltage $PV_{IN}, V_{IN}$	6	V
SW Pin Voltage	-0.3 to $(PV_{IN} + 0.3)$	V
FB Pin Voltage	-0.3 to $(V_{IN} + 0.3)$	V
EN Pin Voltage	-0.3 to +6.0	V
Maximum Junction Temperature	150	$^\circ\text{C}$
Storage Temperature Range	-65 to +150	$^\circ\text{C}$
Soldering Temperature	300, 5sec	$^\circ\text{C}$

## Recommended Operating Conditions (@ $T_A = +25^\circ\text{C}$ , unless otherwise specified.)

Parameter	Rating	Unit
Supply Voltage	2.7 to 5.5	V
Junction Temperature Range	-40 to +125	$^\circ\text{C}$
Ambient Temperature Range	-40 to +85	

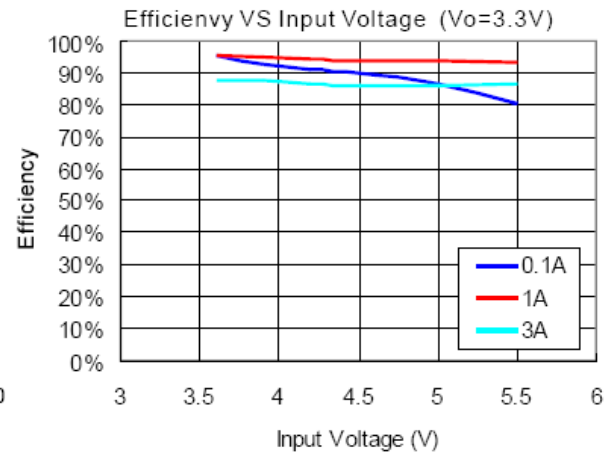
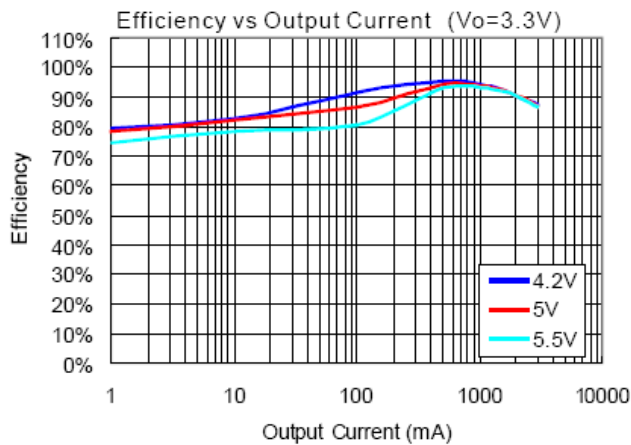
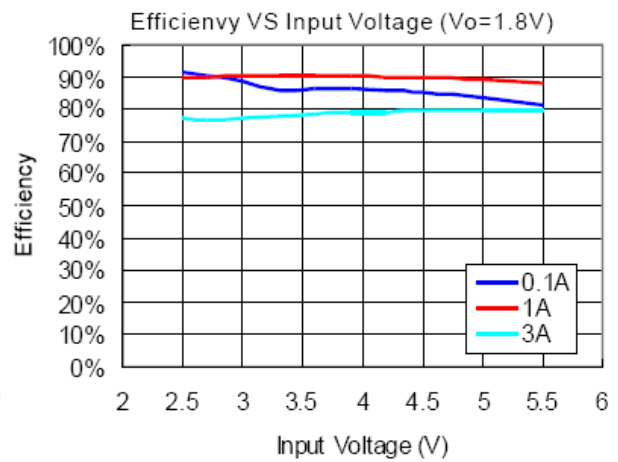
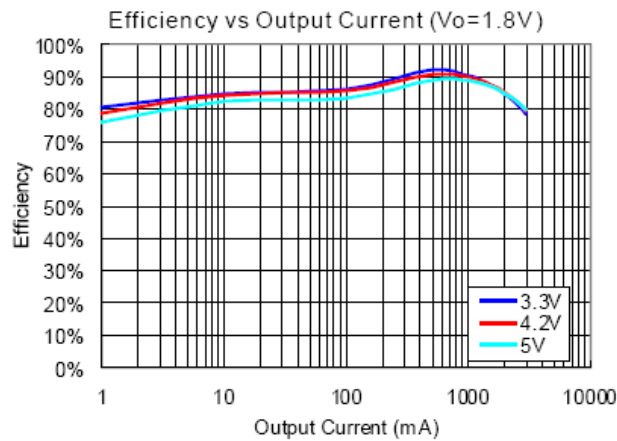
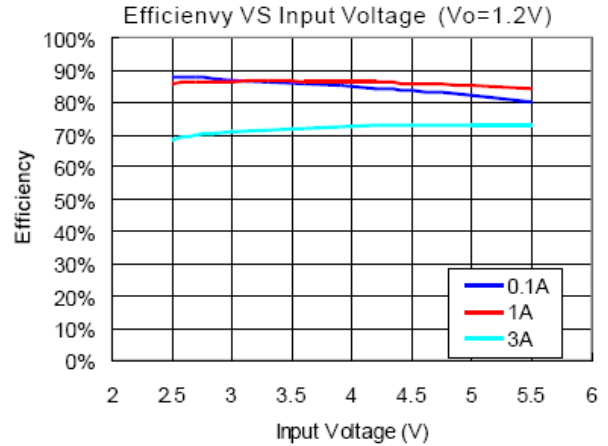
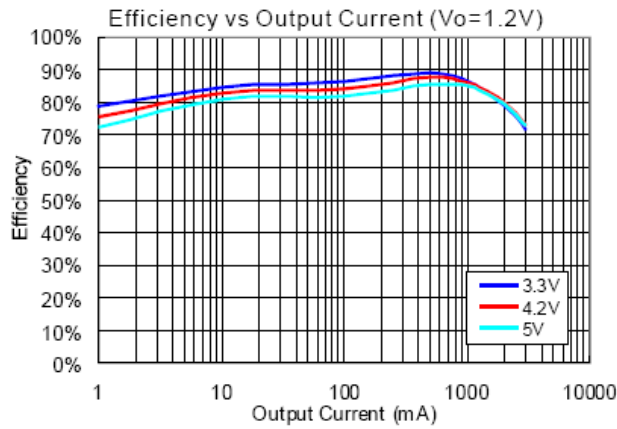
## Thermal Information

Parameter	Symbol	Package	Max	Unit
Thermal Resistance (Junction to Ambient)	$\theta_{JA}$	SOP-8EP	90	$^\circ\text{C}/\text{W}$
		DFN3x3-10	60	
		QFN3x3-16	35	
Thermal Resistance (Junction to Case)	$\theta_{JC}$	SOP-8EP	11	
		DFN3x3-10	8.5	
		QFN3x3-16	11	

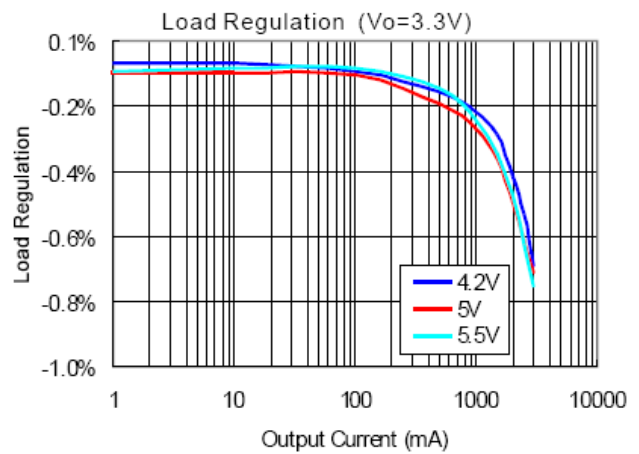
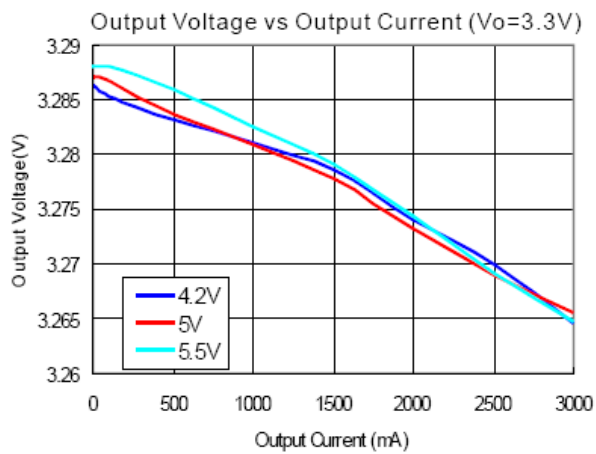
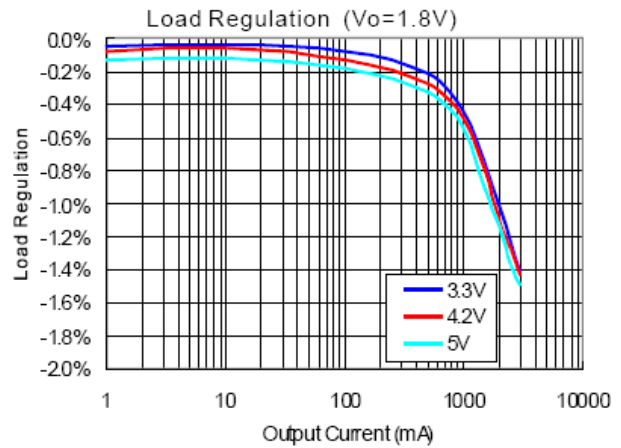
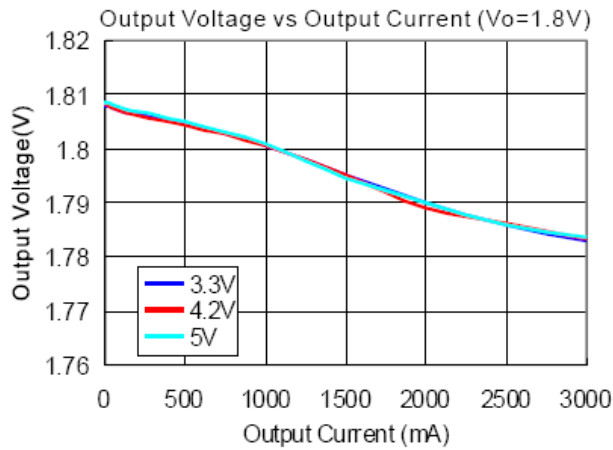
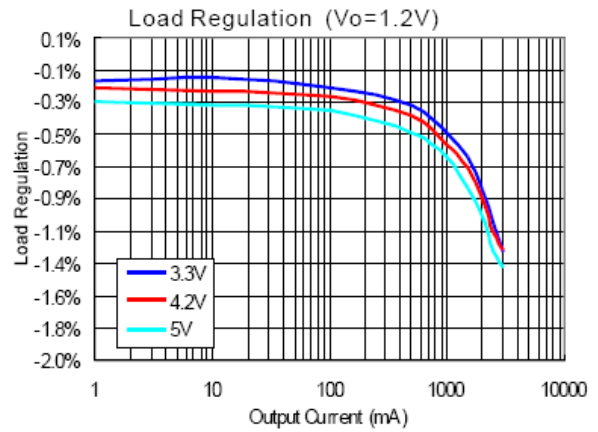
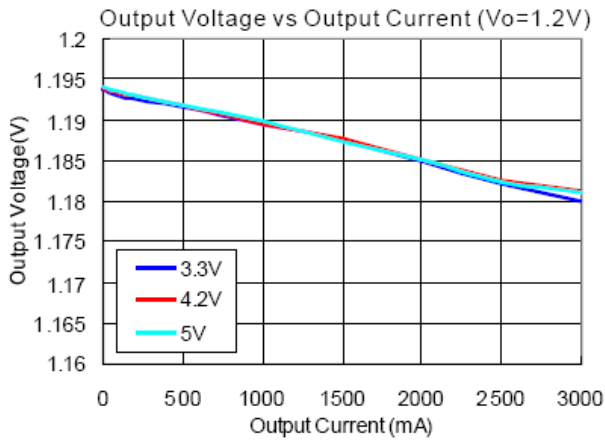
**Electrical Characteristics** (@ $T_A = +25^\circ\text{C}$ ,  $V_{IN} = 3.6\text{V}$ ,  $V_O = 1.8\text{V}$ ,  $C_{IN} = 33\mu\text{F}$ ,  $C_O = 22\mu\text{F}$ ,  $L = 2.2\mu\text{H}$  unless otherwise specified.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Input Voltage Range	$V_{IN}$		2.7		5.5	V
Output Voltage Range	$V_O$		0.6		$V_{IN}$	V
UVLO Threshold	$V_{UVLO}$	$V_{IN}$ Rising		2.4	2.5	V
		Hysteresis		240		mV
		$V_{IN}$ Falling	1.8			V
Regulated Output Voltage Accuracy	$V_O$	$I_O = 0$ to 3A	-3		+3	%
Regulated Feedback Voltage	$V_{FB}$		0.591	0.600	0.609	V
FB Leakage Current	$I_{FB}$	$V_O = 1\text{V}$	-50		+50	nA
Output Voltage Line Regulation	LNR	$V_{IN} = 2.5\text{V}$ to 5V		0.2		%/V
Output Voltage Load Regulation	LDR	$I_O = 0\text{A}$ to 3A		0.5		%/A
Quiescent Current	$I_Q$	No load		42	90	$\mu\text{A}$
Shutdown Current	$I_{SD}$	$V_{EN} = 0\text{V}$			1	$\mu\text{A}$
Current Limit	$I_{LIM}$			4		A
Oscillator Frequency	$f_{OSC}$		1.2	1.5	1.8	MHz
Drain-Source On-State Resistance	$R_{DS(ON)}$	High Side		85		m $\Omega$
		Low Side		60		
High Efficiency	$\eta$			95		%
PSM Threshold	$I_{TH}$	$V_{IN} = 3.3\text{V}$ , $V_O = 1.2\text{V}$ , $L = 1\mu\text{H}$			450	mA
Analog Soft Start Time	$t_s$	From enable to output regulation		0.5		ms
EN Threshold High	$V_{EH}$		1.5			V
EN Threshold Low	$V_{EL}$				0.3	V
EN Leakage Current	$I_{EN}$	$V_{IN} = V_{EN} = 0\text{V}$	-1.0		+1.0	$\mu\text{A}$
Over Temperature Protection	OTP			150		$^\circ\text{C}$
OTP Hysteresis	OTH			30		$^\circ\text{C}$

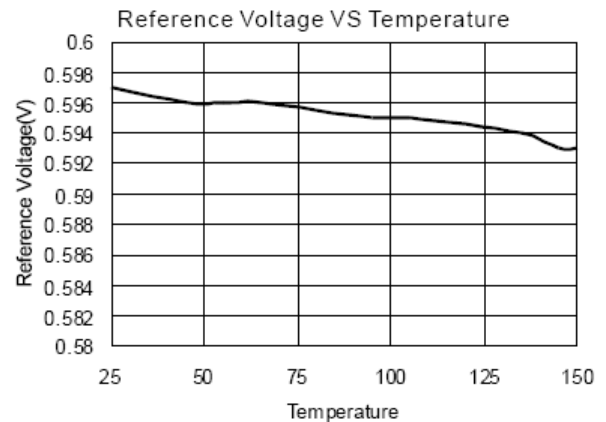
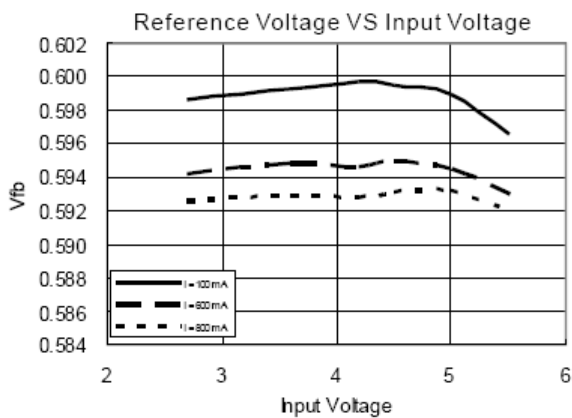
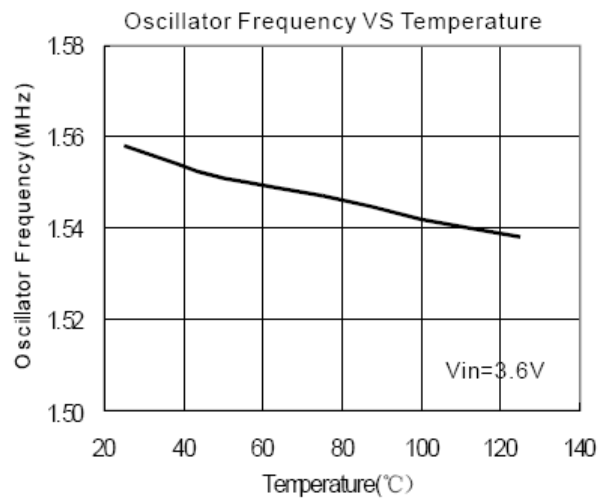
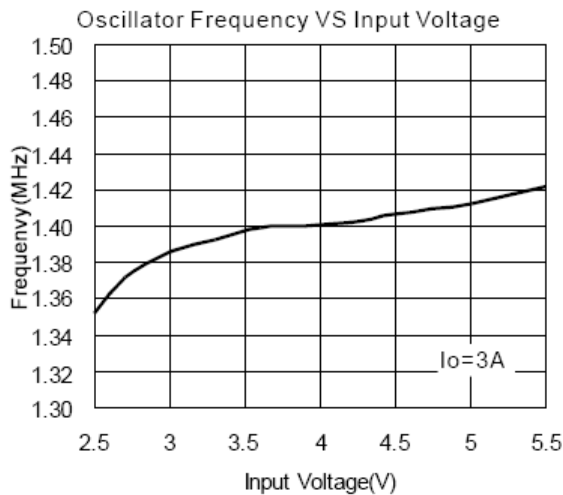
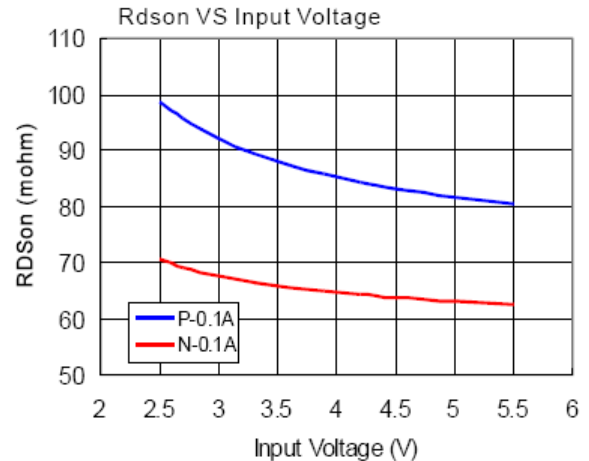
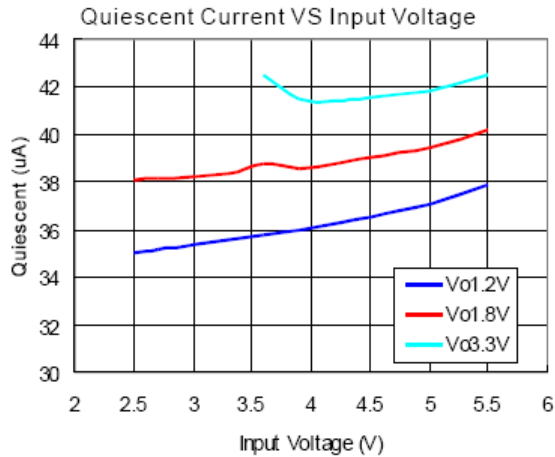
**Typical Performance Characteristics** (@ $T_A = +25^\circ\text{C}$ ,  $C_{IN} = 10\mu\text{F}$ ,  $C_O = 10\mu\text{F}$ ,  $L = 4.7\mu\text{H}$  unless otherwise specified.)



**Typical Performance Characteristics** (cont.) (@ $T_A = +25^\circ\text{C}$ ,  $C_{IN} = 10\mu\text{F}$ ,  $C_O = 10\mu\text{F}$ ,  $L = 4.7\mu\text{H}$  unless otherwise specified.)



**Typical Performance Characteristics** (cont.) @ $T_A = +25^\circ\text{C}$ ,  $C_{IN} = 10\mu\text{F}$ ,  $C_O = 10\mu\text{F}$ ,  $L = 4.7\mu\text{H}$  unless otherwise specified.)



## Application Information

The basic PAM2303 application circuit is shown in Page 1. External component selection is determined by the load requirement, selecting L first and then C<sub>IN</sub> and C<sub>OUT</sub>.

### Inductor Selection

For most applications, the value of the inductor will fall in the range of 1μH to 3.3μH. Its value is chosen based on the desired ripple current and efficiency. Large value inductors lower ripple current and small value inductors result in higher ripple currents. Higher V<sub>IN</sub> or V<sub>OUT</sub> also increases the ripple current as shown in equation 3A reasonable starting point for setting ripple current is ΔI<sub>L</sub> = 1.2A (40% of 3A).

$$\Delta I_L = \frac{1}{fL} V_{OUT} \left( 1 - \frac{V_{OUT}}{V_{IN}} \right) \quad \text{Equation 1}$$

The DC current rating of the inductor should be at least equal to the maximum load current plus half the ripple current to prevent core saturation. Thus, a 4.2A rated inductor should be enough for most applications (3A + 1.2A). For better efficiency, choose a low DC-resistance inductor.

V <sub>O</sub>	1.2V	1.5V	1.8V	2.5V	3.3V
L	1μH	1.5μH	2.2μH	2.2μH	3.3μH

### C<sub>IN</sub> and C<sub>OUT</sub> Selection

In continuous mode, the source current of the top MOSFET is a square wave of duty cycle V<sub>OUT</sub>/V<sub>IN</sub>. To prevent large voltage transients, allow ESR input capacitor sized for the maximum RMS current must be used. The maximum RMS capacitor current is given by:

$$C_{IN} \text{ required } I_{RMS} \cong I_{OMAX} \frac{[V_{OUT}(V_{IN} - V_{OUT})]^{1/2}}{V_{IN}}$$

This formula has a maximum at V<sub>IN</sub> = 2V<sub>OUT</sub>, where I<sub>RMS</sub> = I<sub>OUT</sub> / 2. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that the capacitor manufacturer's ripple current ratings are often based on 2000 hours of life. This makes it advisable to further derate the capacitor, or choose a capacitor rated at a higher temperature than required. Consult the manufacturer if there is any question.

The selection of C<sub>OUT</sub> is driven by the required effective series resistance (ESR).

Typically, once the ESR requirement for C<sub>OUT</sub> has been met, the RMS current rating generally far exceeds the I<sub>RIPPLE</sub> (P-P) requirement. The output ripple ΔV<sub>OUT</sub> is determined by:

$$\Delta V_{OUT} \approx \Delta I_L (ESR = 1/8fC_{OUT})$$

Where f = operating frequency, C = output capacitance and ΔI<sub>L</sub> = ripple current in the inductor. For a fixed output voltage, the output ripple is highest at maximum input voltage since ΔI<sub>L</sub> increases with input voltage.

### Using Ceramic Input and Output Capacitors

Higher values, lower cost ceramic capacitors are now becoming available in smaller case sizes. Their high ripple current, high voltage rating and low ESR make them ideal for switching regulator applications. Using ceramic capacitors can achieve very low output ripple and small circuit size.

When choosing the input and output ceramic capacitors, choose the X5R or X7R dielectric formulations. These dielectrics have the best temperature and voltage characteristics of all the ceramics for a given value and size.

### Thermal Consideration

Thermal protection limits power dissipation in the PAM2303. When the junction temperature exceeds +150°C, the OTP (Over Temperature Protection) starts the thermal shutdown and turns the pass transistor off. The pass transistor resumes operation after the junction temperature drops below +120°C.

For continuous operation, the junction temperature should be maintained below +125°C.

The power dissipation is defined as:

$$P_D = I_O^2 \frac{V_O R_{DS(ON)H} + (V_{IN} - V_O) R_{DS(ON)L}}{V_{IN}} + (t_{sw} F_s I_O + I_Q) V_{IN}$$

I<sub>Q</sub> is the step-down converter quiescent current. The term t<sub>sw</sub> is used to estimate the full load step-down converter switching losses.



## Application Information (cont.)

### Thermal Consideration (cont.)

For the condition where the step-down converter is in dropout at 100% duty cycle, the total device dissipation reduces to:

$$P_D = I_O^2 R_{DS(ON)H} + I_O V_{IN}$$

Since  $R_{DS(ON)}$ , quiescent current, and switching losses all vary with input voltage, the total losses should be investigated over the complete input voltage range. The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, the rate of surrounding airflow and temperature difference between junction and ambient. The maximum power dissipation can be calculated by the following formula:

$$P_D = \frac{T_{J(MAX)} - T_A}{\theta_{JA}}$$

Where  $T_J(max)$  is the maximum allowable junction temperature +125°C.  $T_A$  is the ambient temperature and  $\theta_{JA}$  is the thermal resistance from the junction to the ambient. Based on the standard JEDEC for a two layers thermal test board, the thermal resistance  $\theta_{JA}$  of QFN3X3-16 68°C/W and SOP-8(EP) 90°C/W, respectively. The maximum power dissipation at  $T_A = +25^\circ\text{C}$  can be calculated by the following formula:

$$P = (125^\circ\text{C} - 25^\circ\text{C})/68^\circ\text{C/W} = 1.47\text{W(QFN3X3-16)}$$

$$P = (125^\circ\text{C} - 25^\circ\text{C})/90^\circ\text{C/W} = 1.11\text{W(SOP-8)}$$

### Setting the Output Voltage

The internal reference is 0.6V (Typical). The output voltage is calculated as below:

The output voltage is given by Table 1.

$$V_O = 0.6 \times \left( 1 + \frac{R1}{R2} \right)$$

**Table 1:** Resistor recommended for output voltage setting

$V_O$	R1	R2
1.2V	150k	150k
1.5V	225k	150k
1.8V	300k	150k
2.5V	475k	150k
3.3V	680k	150k

### Pulse Skipping Mode (PSM) Description

When load current decreases, the peak switch current in Power-PMOS will be lower than skip current threshold and the device will enter into Pulse Skipping Mode.

In this mode, the device has two states, working state and idle state. First, the device enters into working state controlled by internal error amplifier. When the feedback voltage gets higher than internal reference voltage, the device will enter into low I idle state with most of internal blocks disabled. The output voltage will be reduced by loading or leakage current. When the feedback voltage gets lower than the internal reference voltage, the converter will start a working state again.

### 100% Duty Cycle Operation

As the input voltage approaches the output voltage, the converter turns the P-Channel transistor continuously on. In this mode the output voltage is equal to the input voltage minus the voltage drop across the P-Channel transistor:

$$V_{OUT} = V_{IN} - I_{LOAD} (R_{DS(ON)} + R_L)$$

where  $R_{DS(ON)}$  = P-Channel switch ON resistance,  $I_{LOAD}$  = Output current,  $R_L$  = Inductor DC resistance

### UVLO and Soft-Start

The reference and the circuit remain reset until the  $V_{IN}$  crosses its UVLO threshold.

The PAM2303 has an internal soft-start circuit that limits the in-rush current during start-up. This prevents possible voltage drops of the input voltage and eliminates the output voltage overshoot. The soft-start make the output voltage rise up smoothly.

## Application Information (cont.)

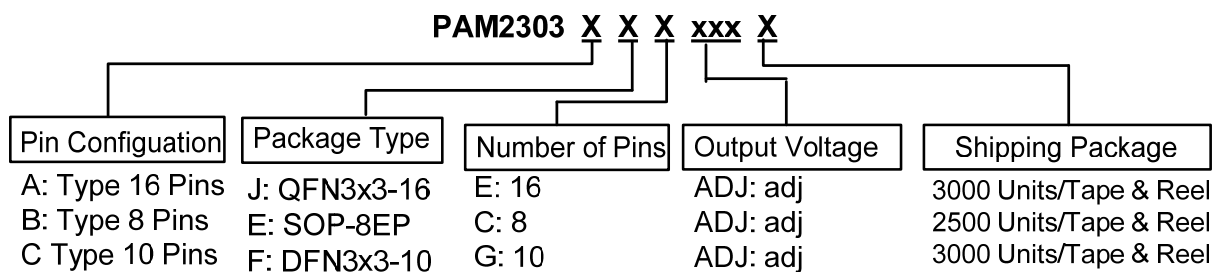
### Short Circuit Protection

The switch peak current is limited cycle-by-cycle to a typical value of 4A. In the event of an output voltage short circuit, the device operates with a frequency of 500kHz and minimum duty cycle, therefore the average input current is more smaller than current limit.

### Thermal Shutdown

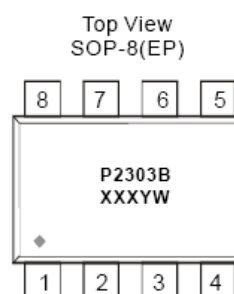
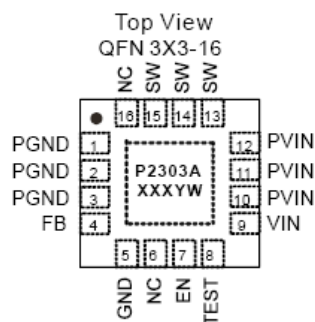
When the die temperature exceeds +150°C, a reset occurs and the reset remains until the temperature decrease to +120°C, at which time the circuit can be restarted.

## Ordering Information

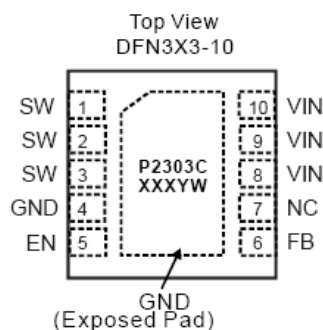


Part Number	Output Voltage	Package	Packaging
PAM2303AJEADJR	ADJ	QFN3x3-16	3000 Units/Tape & Reel
PAM2303BECADJR	ADJ	SOP-8EP	2500 Units/Tape & Reel
PAM2303CFGADJR	ADJ	DFN3x3-10	3000 Units/Tape & Reel

## Marking Information



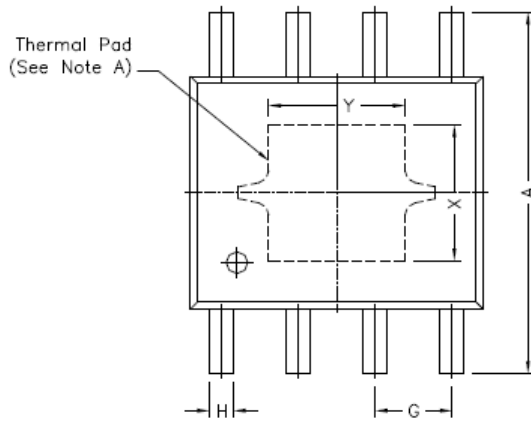
A/B: Pin Configuration  
Y: Year  
W: Week  
X: Internal Code



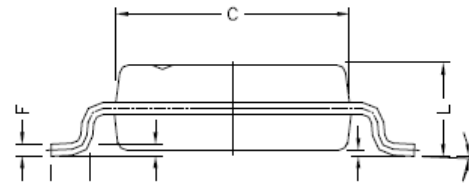
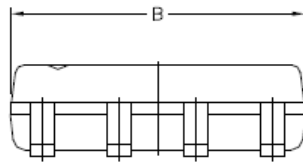
C: Pin Configuration  
Y: Year  
W: Week  
X: Internal Code

**Package Outline Dimensions** (All dimensions in mm.)

SOP-8EP

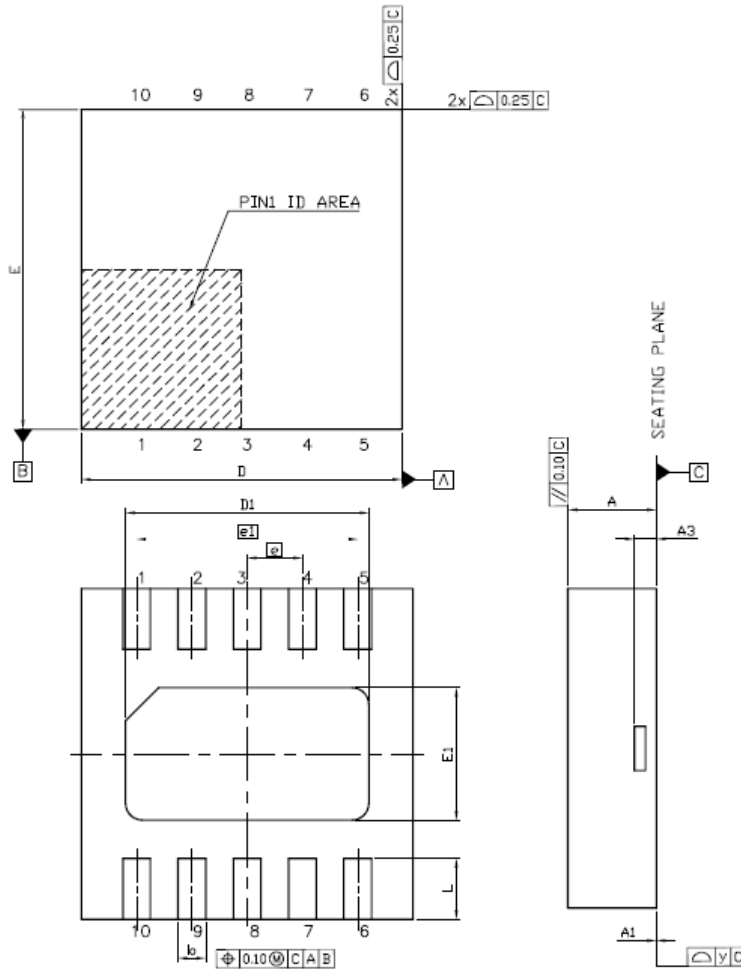


REF.	DIMENSIONS	
	Millimeters	
	Min.	Max.
A	5.80	6.20
B	4.80	5.00
C	3.80	4.00
D	0°	8°
E	0.40	0.90
F	0.19	0.25
M	0	0.15
H	0.35	0.49
L	1.35	1.75
G	1.27 TYP.	
Option1	X	2.28
	Y	2.28
Option2	X	2.41
	Y	3.30



**Package Outline Dimensions** (cont.) (All dimensions in mm.)

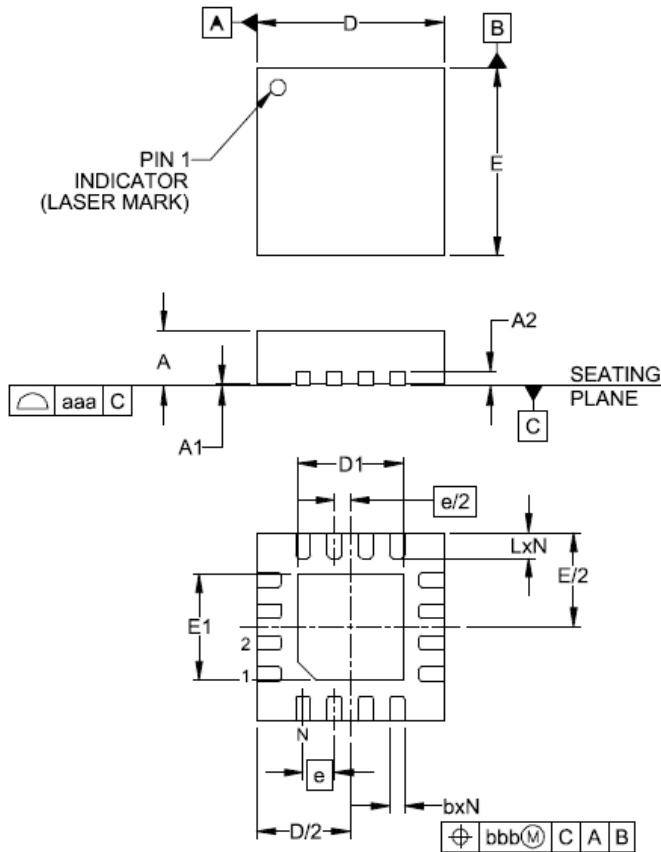
DFN3x3-10



SYMBOL	DIMENSION (MM)		
	MIN	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.203 REF		
b	0.18	0.25	0.30
D	2.90	3.00	3.10
D1	2.10	2.20	2.30
E	2.90	3.00	3.10
E1	1.10	1.20	1.30
L	0.45	0.55	0.65
E	0.50 BASIC		
e1	2.00 BASIC		
y	0		0.08

**Package Outline Dimensions** (cont.) (All dimensions in mm.)

QFN3x3-16



DIMENSIONS (Millimeters)			
	MIN	TYP	MAX
A	0.50	0.55	0.60
A1	0.00	0.02	0.05
A2	0.20		
b	0.18	0.25	0.30
D	2.90	3.00	3.10
D1	1.55	1.70	1.80
E	2.90	3.00	3.10
E1	1.55	1.70	1.80
e	0.50BSC		
L	0.30	0.40	0.50
N	16		
aaa	0.08		
bbb	0.10		

- Notes:
1. Controlling dimensions are millimeters (angles in degrees).
  2. Coplanarity applies to the exposed pads as well as the terminals.
  3. DAP is 1.90 x 1.90mm.

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