

## SN74LVC1G34 Single Buffer Gate

### 1 Features

- Available in the Ultra Small 0.64-mm<sup>2</sup> Package (DPW) with 0.5-mm Pitch
- Supports 5-V V<sub>CC</sub> Operation
- Inputs Accept Voltages to 5.5 V
- Provides Down Translation to V<sub>CC</sub>
- Max t<sub>pd</sub> of 3.5 ns at 3.3 V
- Low Power Consumption, 1-μA Max I<sub>CC</sub>
- ±24-mA Output Drive at 3.3 V
- I<sub>off</sub> Supports Live Insertion, Partial Power Down Mode, and Back Drive Protection
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

### 2 Applications

- AV Receiver
- Audio Dock: Portable
- Blu-ray Player and Home Theater
- DVD Recorder and Player
- Embedded PC
- MP3 Player/Recorder (Portable Audio)
- Personal Digital Assistant (PDA)
- Power: Telecom/Server AC/DC Supply: Single Controller: Analog and Digital
- Solid State Drive (SSD): Client and Enterprise
- TV: LCD/Digital and High-Definition (HDTV)
- Tablet: Enterprise
- Video Analytics: Server
- Wireless Headset, Keyboard, and Mouse

### 4 Simplified Schematic



### 3 Description

This single buffer gate is designed for 1.65-V to 5.5-V V<sub>CC</sub> operation.

The SN74LVC1G34 device performs the Boolean function  $Y = A$  in positive logic.

The CMOS device has high output drive while maintaining low static power dissipation over a broad V<sub>CC</sub> Operating range.

The SN74LVC1G34 is available in a variety of packages, including the ultra-small DPW package with a body size of 0.8 mm × 0.8 mm.

#### Device Information<sup>(1)</sup>

| DEVICE NAME    | PACKAGE (PINS) | BODY SIZE         |
|----------------|----------------|-------------------|
| SN74LVC1G34YFP | DSBGA (4)      | 0.76 mm × 0.76 mm |
| SN74LVC1G34YZP | DSBGA (5)      | 1.38 mm × 0.88 mm |
| SN74LVC1G34YZV | DSBGA (4)      | 0.88 mm × 0.88 mm |
| SN74LVC1G34DPW | X2SON (5)      | 0.80 mm × 0.80 mm |
| SN74LVC1G34DBV | SOT-23 (5)     | 2.90 mm × 2.80 mm |
| SN74LVC1G34DCK | SC70 (5)       | 2.00 mm × 2.10 mm |
| SN74LVC1G34DRL | SOT (5)        | 1.60 mm × 1.60 mm |
| SN74LVC1G34DRY | SON (6)        | 1.45 mm × 1.00 mm |
| SN74LVC1G34DSF | SON(6)         | 1.00 mm × 1.00 mm |

(1) For all available packages, see the orderable addendum at the end of the datasheet.



## Table of Contents

|          |   |          |           |   |           |
|----------|---|----------|-----------|---|-----------|
| <b>1</b> | <b>Features</b> .....   | <b>1</b> | <b>9</b>  | <b>Detailed Description</b> .....                             | <b>11</b> |
| <b>2</b> | <b>Applications</b> .....   | <b>1</b> | 9.1       | Overview .....  | 11        |
| <b>3</b> | <b>Description</b> .....  | <b>1</b> | 9.2       | Functional Block Diagram .....                                | 11        |
| <b>4</b> | <b>Simplified Schematic</b> .....   | <b>1</b> | 9.3       | Feature Description .....                                     | 11        |
| <b>5</b> | <b>Revision History</b> .....   | <b>2</b> | 9.4       | Device Functional Modes .....                                 | 11        |
| <b>6</b> | <b>Pin Configuration and Functions</b> .....                                | <b>4</b> | <b>10</b> | <b>Application and Implementation</b> .....                   | <b>12</b> |
| <b>7</b> | <b>Specifications</b> .....   | <b>5</b> | 10.1      | Application Information .....                                 | 12        |
| 7.1      | Absolute Maximum Ratings .....  | 5        | 10.2      | Typical Application .....                                     | 12        |
| 7.2      | ESD Ratings .....   | 5        | <b>11</b> | <b>Power Supply Recommendations</b> .....                     | <b>13</b> |
| 7.3      | Recommended Operating Conditions .....                                      | 6        | <b>12</b> | <b>Layout</b> .....   | <b>13</b> |
| 7.4      | Thermal Information .....   | 6        | 12.1      | Layout Guidelines .....                                       | 13        |
| 7.5      | Electrical Characteristics .....  | 7        | 12.2      | Layout Example .....  | 13        |
| 7.6      | Switching Characteristics, $C_L = 15$ pF .....                              | 8        | <b>13</b> | <b>Device and Documentation Support</b> .....                 | <b>14</b> |
| 7.7      | Switching Characteristics, $-40^\circ\text{C}$ to $85^\circ\text{C}$ .....  | 8        | 13.1      | Community Resources .....                                     | 14        |
| 7.8      | Switching Characteristics, $-40^\circ\text{C}$ to $125^\circ\text{C}$ ..... | 8        | 13.2      | Trademarks .....  | 14        |
| 7.9      | Operating Characteristics .....   | 8        | 13.3      | Electrostatic Discharge Caution .....                         | 14        |
| 7.10     | Typical Characteristics .....   | 8        | 13.4      | Glossary .....  | 14        |
| <b>8</b> | <b>Parameter Measurement Information</b> .....                              | <b>9</b> | <b>14</b> | <b>Mechanical, Packaging, and Orderable Information</b> ..... | <b>14</b> |

## 5 Revision History

### Changes from Revision L (April 2014) to Revision M

Page

|   |  |   |
|---|--|---|
| • | Changed X2SON from 4 pin to 5 pin on <i>Device Information</i> table .....                                   | 1 |
| • | Moved Storage temperature range from <i>ESD Ratings</i> table to <i>Absolute Maximum Ratings</i> table ..... | 5 |
| • | Added Junction temperature to <i>Absolute Maximum Ratings</i> table .....                                    | 5 |
| • | Added package temperature specification for DSBGA package .....  | 6 |

### Changes from Revision K (March 2014) to Revision L

Page

|   |  |    |
|---|--|----|
| • | Added Device Information table. ....               | 1  |
| • | Added Pin Functions table. ....                    | 4  |
| • | Updated Handling Ratings table. ....               | 5  |
| • | Updated operating temperature range. ....          | 6  |
| • | Added Thermal Information table. ....              | 6  |
| • | Added Typical Characteristics. ....                | 8  |
| • | Added Detailed Description section. ....           | 11 |
| • | Added Application and Implementation section. .... | 12 |

### Changes from Revision J (December 2013) to Revision K

Page

|   |   |   |
|---|---|---|
| • | Added Applications. ....                        | 1 |
| • | DPW Package. ....                               | 4 |
| • | Moved $T_{stg}$ to Handling Ratings table. .... | 5 |

---

**Changes from Revision I (June2011) to Revision J****Page**

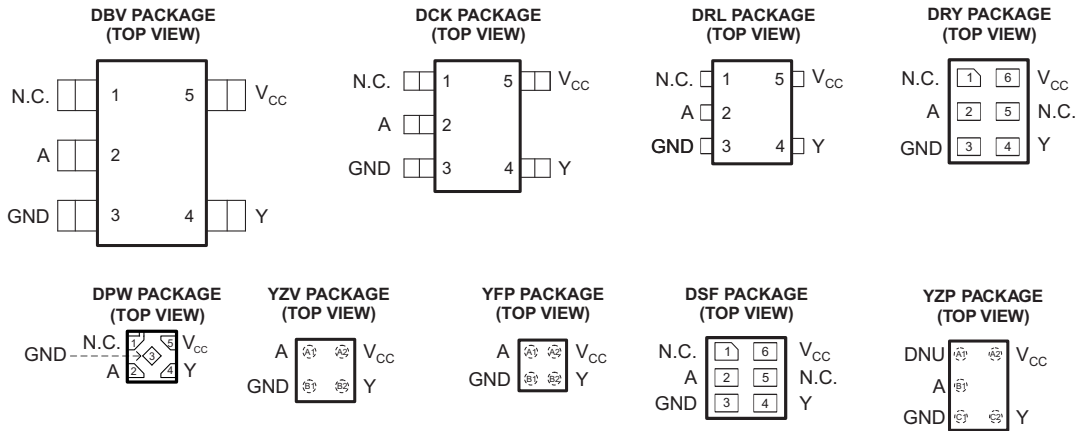
- 
- Updated document to new TI data sheet format ..... 1
  - Removed Ordering Information table. .... 1
-

# SN74LVC1G34

SCES519M – DECEMBER 2003 – REVISED APRIL 2016

www.ti.com

## 6 Pin Configuration and Functions



See mechanical drawings for dimensions.  
 N.C. – No internal connection  
 DNU – Do not use

### Pin Functions

| NAME            | PIN           |     |          |     |          | DESCRIPTION   |
|-----------------|---------------|-----|----------|-----|----------|---------------|
|                 | DRL, DCK, DBV | DPW | DRY, DSF | YZP | YFP, YZV |               |
| NC              | 1             | 1   | 1, 5     | A1  | –        | Not connected |
| A               | 2             | 2   | 2        | B1  | A1       | Input         |
| GND             | 3             | 3   | 3        | C1  | B1       | Ground        |
| Y               | 4             | 4   | 4        | C2  | B2       | Output        |
| V <sub>CC</sub> | 5             | 5   | 6        | A2  | A2       | Power pin     |

## 7 Specifications

### 7.1 Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

|           |   | MIN       | MAX            | UNIT |
|-----------|---|-----------|----------------|------|
| $V_{CC}$  | Supply voltage range  | -0.5      | 6.5            | V    |
| $V_I$     | Input voltage range   | -0.5      | 6.5            | V    |
| $V_O$     | Voltage range applied to any output in the high-impedance or power-off state <sup>(2)</sup> | -0.5      | 6.5            | V    |
| $V_O$     | Voltage range applied to any output in the high or low state <sup>(2)(3)</sup>              | -0.5      | $V_{CC} + 0.5$ | V    |
| $I_{IK}$  | Input clamp current   | $V_I < 0$ | -50            | mA   |
| $I_{OK}$  | Output clamp current  | $V_O < 0$ | -50            | mA   |
| $I_O$     | Continuous output current   |           | ±50            | mA   |
|           | Continuous current through $V_{CC}$ or GND  |           | ±100           | mA   |
| $T_{stg}$ | Storage temperature range   | -65       | 150            | °C   |
| $T_J$     | Max Junction temperature  |           | 150            | °C   |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The value of  $V_{CC}$  is provided in the *Recommended Operating Conditions* table.

### 7.2 ESD Ratings

|             |                         | MIN  | MAX | UNIT |
|-------------|-------------------------|--|-----|------|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>              | ±2  | kV   |
|             |                         | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup> | ±1  |      |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

**SN74LVC1G34**

SCES519M – DECEMBER 2003 – REVISED APRIL 2016

[www.ti.com](http://www.ti.com)
**7.3 Recommended Operating Conditions<sup>(1)</sup>**

|                 |                                    | MIN   | MAX                    | UNIT                   |      |
|-----------------|------------------------------------|---|------------------------|------------------------|------|
| V <sub>CC</sub> | Supply voltage                     | Operating                                       | 1.65                   | 5.5                    | V    |
|                 |                                    | Data retention only                             | 1.5                    |                        |      |
| V <sub>IH</sub> | High-level input voltage           | V <sub>CC</sub> = 1.65 V to 1.95 V              | 0.65 × V <sub>CC</sub> |                        | V    |
|                 |                                    | V <sub>CC</sub> = 2.3 V to 2.7 V                | 1.7                    |                        |      |
|                 |                                    | V <sub>CC</sub> = 3 V to 3.6 V                  | 2                      |                        |      |
|                 |                                    | V <sub>CC</sub> = 4.5 V to 5.5 V                | 0.7 × V <sub>CC</sub>  |                        |      |
| V <sub>IL</sub> | Low-level input voltage            | V <sub>CC</sub> = 1.65 V to 1.95 V              |                        | 0.35 × V <sub>CC</sub> | V    |
|                 |                                    | V <sub>CC</sub> = 2.3 V to 2.7 V                |                        | 0.7                    |      |
|                 |                                    | V <sub>CC</sub> = 3 V to 3.6 V                  |                        | 0.8                    |      |
|                 |                                    | V <sub>CC</sub> = 4.5 V to 5.5 V                |                        | 0.3 × V <sub>CC</sub>  |      |
| V <sub>I</sub>  | Input voltage                      | 0   | 5.5                    | V                      |      |
| V <sub>O</sub>  | Output voltage                     | 0   | V <sub>CC</sub>        | V                      |      |
| I <sub>OH</sub> | High-level output current          | V <sub>CC</sub> = 1.65 V                        |                        | –4                     | mA   |
|                 |                                    | V <sub>CC</sub> = 2.3 V                         |                        | –8                     |      |
|                 |                                    | V <sub>CC</sub> = 3 V                           |                        | –16                    |      |
|                 |                                    | V <sub>CC</sub> = 4.5 V                         |                        | –24                    |      |
| I <sub>OL</sub> | Low-level output current           | V <sub>CC</sub> = 1.65 V                        |                        | 4                      | mA   |
|                 |                                    | V <sub>CC</sub> = 2.3 V                         |                        | 8                      |      |
|                 |                                    | V <sub>CC</sub> = 3 V                           |                        | 16                     |      |
|                 |                                    | V <sub>CC</sub> = 4.5 V                         |                        | 24                     |      |
| Δt/Δv           | Input transition rise or fall rate | V <sub>CC</sub> = 1.8 V ± 0.15 V, 2.5 V ± 0.2 V |                        | 20                     | ns/V |
|                 |                                    | V <sub>CC</sub> = 3.3 V ± 0.3 V                 |                        | 10                     |      |
|                 |                                    | V <sub>CC</sub> = 5 V ± 0.5 V                   |                        | 10                     |      |
| T <sub>A</sub>  | Operating free-air temperature     | DSBGA package                                   | –40                    | 85                     | °C   |
|                 |                                    | All other packages                              | –40                    | 125                    | °C   |

(1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).

**7.4 Thermal Information**

| THERMAL METRIC <sup>(1)</sup> | SN74LVC1G34                                  |        |        |        |        |        | UNIT |      |
|-------------------------------|--|--------|--------|--------|--------|--------|------|------|
|                               | DBV  | DCK    | DRL    | DRY    | YZP    | DPW    |      |      |
|                               | 5 PINS                                       | 5 PINS | 5 PINS | 6 PINS | 5 PINS | 4 PINS |      |      |
| R <sub>θJA</sub>              | Junction-to-ambient thermal resistance       | 229    | 278    | 243    | 439    | 130    | 340  | °C/W |
| R <sub>θJC(top)</sub>         | Junction-to-case (top) thermal resistance    | 164    | 93     | 78     | 277    | 54     | 215  |      |
| R <sub>θJB</sub>              | Junction-to-board thermal resistance         | 62     | 65     | 78     | 271    | 51     | 294  |      |
| Ψ <sub>JT</sub>               | Junction-to-top characterization parameter   | 44     | 2      | 10     | 84     | 1      | 41   |      |
| Ψ <sub>JB</sub>               | Junction-to-board characterization parameter | 62     | 64     | 77     | 271    | 50     | 294  |      |
| R <sub>θJC(bot)</sub>         | Junction-to-case (bottom) thermal resistance | –      | –      | –      | –      | –      | 250  |      |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

## 7.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER        | TEST CONDITIONS   | V <sub>CC</sub> | –40°C to 85°C         |                    |     | –40°C to 125°C        |                    |     | UNIT |
|------------------|---|-----------------|-----------------------|--------------------|-----|-----------------------|--------------------|-----|------|
|                  |   |                 | MIN                   | TYP <sup>(1)</sup> | MAX | MIN                   | TYP <sup>(1)</sup> | MAX |      |
| V <sub>OH</sub>  | I <sub>OH</sub> = –100 μA   | 1.65 V to 5.5 V | V <sub>CC</sub> – 0.1 |                    |     | V <sub>CC</sub> – 0.1 |                    |     | V    |
|                  | I <sub>OH</sub> = –4 mA   | 1.65 V          | 1.2                   |                    |     | 1.2                   |                    |     |      |
|                  | I <sub>OH</sub> = –8 mA   | 2.3 V           | 1.9                   |                    |     | 1.9                   |                    |     |      |
|                  | I <sub>OH</sub> = –16 mA  | 3 V             | 2.4                   |                    |     | 2.4                   |                    |     |      |
|                  | I <sub>OH</sub> = –24 mA  |                 | 2.3                   |                    |     | 2.3                   |                    |     |      |
|                  | I <sub>OH</sub> = –32 mA  | 4.5 V           | 3.8                   |                    |     | 3.8                   |                    |     |      |
| V <sub>OL</sub>  | I <sub>OL</sub> = 100 μA  | 1.65 V to 5.5 V | 0.1                   |                    |     | 0.1                   |                    |     | V    |
|                  | I <sub>OL</sub> = 4 mA  | 1.65 V          | 0.45                  |                    |     | 0.45                  |                    |     |      |
|                  | I <sub>OL</sub> = 8 mA  | 2.3 V           | 0.3                   |                    |     | 0.3                   |                    |     |      |
|                  | I <sub>OL</sub> = 16 mA   | 3 V             | 0.4                   |                    |     | 0.4                   |                    |     |      |
|                  | I <sub>OL</sub> = 24 mA   |                 | 0.55                  |                    |     | 0.55                  |                    |     |      |
|                  | I <sub>OL</sub> = 32 mA   | 4.5 V           | 0.55                  |                    |     | 0.55                  |                    |     |      |
| I <sub>I</sub>   | V <sub>I</sub> = 5.5 V or GND   | 0 to 5.5 V      | ±1                    |                    |     | ±2                    |                    |     | μA   |
| I <sub>off</sub> | V <sub>I</sub> or V <sub>O</sub> = 5.5 V  | 0               | ±10                   |                    |     | ±10                   |                    |     | μA   |
| I <sub>CC</sub>  | V <sub>I</sub> = 5.5 V or GND, I <sub>O</sub> = 0                               | 1.65 V to 5.5 V | 1                     |                    |     | 10                    |                    |     | μA   |
| ΔI <sub>CC</sub> | One input at V <sub>CC</sub> – 0.6 V,<br>Other inputs at V <sub>CC</sub> or GND | 3 V to 5.5 V    | 500                   |                    |     | 500                   |                    |     | μA   |
| C <sub>i</sub>   | V <sub>I</sub> = V <sub>CC</sub> or GND   | 3.3 V           | 3.5                   |                    |     |                       |                    |     | pF   |

(1) All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

## SN74LVC1G34

SCES519M – DECEMBER 2003 – REVISED APRIL 2016

www.ti.com

### 7.6 Switching Characteristics, $C_L = 15\text{ pF}$

over recommended operating free-air temperature range,  $C_L = 15\text{ pF}$  (unless otherwise noted) (see Figure 3)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | -40°C to 85°C                             |     |  |     |  |     |  |     | UNIT |
|-----------|--------------|-------------|---|-----|--|-----|--|-----|--|-----|------|
|           |              |             | $V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$ |     | $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ |     | $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ |     | $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ |     |      |
|           |              |             | MIN                                       | MAX | MIN                                      | MAX | MIN                                      | MAX | MIN                                    | MAX |      |
| $t_{pd}$  | A            | Y           | 2   | 9.9 | 1.5                                      | 6   | 1  | 3.5 | 1                                      | 2.9 | ns   |

### 7.7 Switching Characteristics, -40°C to 85°C

over recommended operating free-air temperature range,  $C_L = 30\text{ pF}$  or  $50\text{ pF}$  (unless otherwise noted) (see Figure 4)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | -40°C to 85°C                             |     |  |     |  |     |  |     | UNIT |
|-----------|--------------|-------------|---|-----|--|-----|--|-----|--|-----|------|
|           |              |             | $V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$ |     | $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ |     | $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ |     | $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ |     |      |
|           |              |             | MIN                                       | MAX | MIN                                      | MAX | MIN                                      | MAX | MIN                                    | MAX |      |
| $t_{pd}$  | A            | Y           | 3.2                                       | 8.6 | 1.5                                      | 4.4 | 1.5                                      | 4.1 | 1                                      | 3.2 | ns   |

### 7.8 Switching Characteristics, -40°C to 125°C

over recommended operating free-air temperature range,  $C_L = 30\text{ pF}$  or  $50\text{ pF}$  (unless otherwise noted) (see Figure 4)

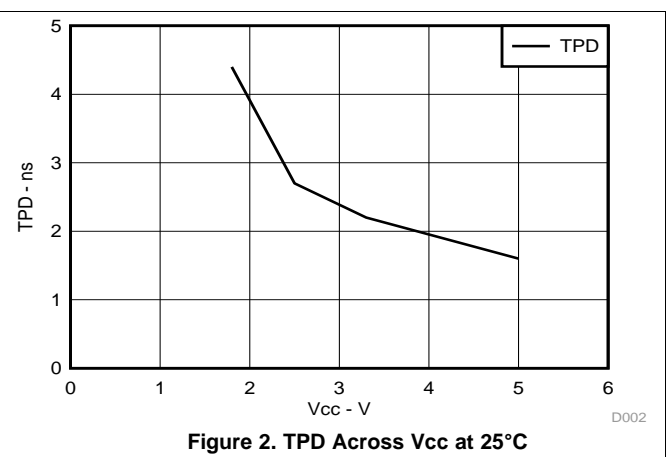
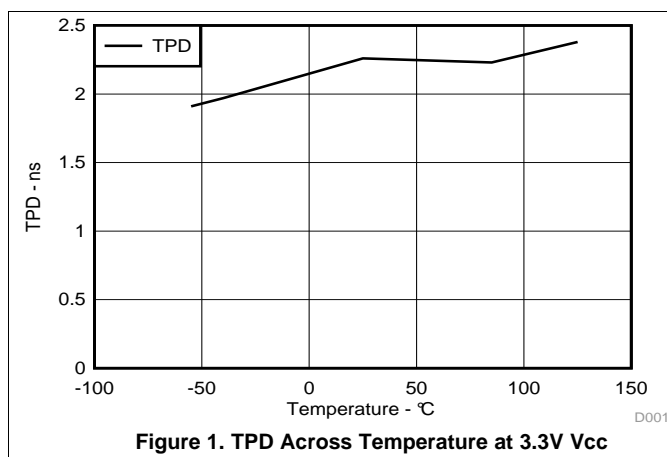
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | -40°C to 125°C                            |     |  |     |  |     |  |     | UNIT |
|-----------|--------------|-------------|---|-----|--|-----|--|-----|--|-----|------|
|           |              |             | $V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$ |     | $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ |     | $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ |     | $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ |     |      |
|           |              |             | MIN                                       | MAX | MIN                                      | MAX | MIN                                      | MAX | MIN                                    | MAX |      |
| $t_{pd}$  | A            | Y           | 3.2                                       | 9.5 | 1.5                                      | 5.1 | 1.5                                      | 4.7 | 1                                      | 3.9 | ns   |

### 7.9 Operating Characteristics

$T_A = 25^\circ\text{C}$

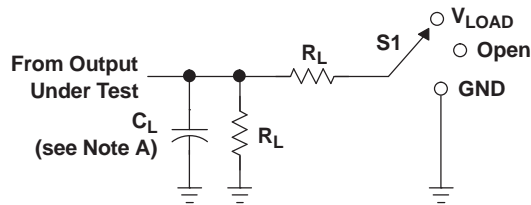
| PARAMETER                              | TEST CONDITIONS     | $V_{CC} = 1.8\text{ V}$ | $V_{CC} = 2.5\text{ V}$ | $V_{CC} = 3.3\text{ V}$ | $V_{CC} = 5\text{ V}$ | UNIT |
|--|---------------------|-------------------------|-------------------------|-------------------------|-----------------------|------|
|  |                     | TYP                     | TYP                     | TYP                     | TYP                   |      |
| $C_{pd}$ Power dissipation capacitance | $f = 10\text{ MHz}$ | 16                      | 16                      | 16                      | 18                    | pF   |

### 7.10 Typical Characteristics





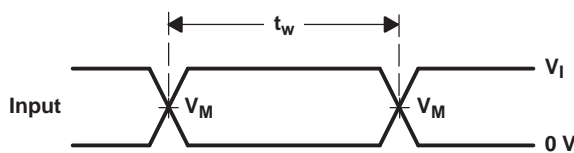
## 8 Parameter Measurement Information



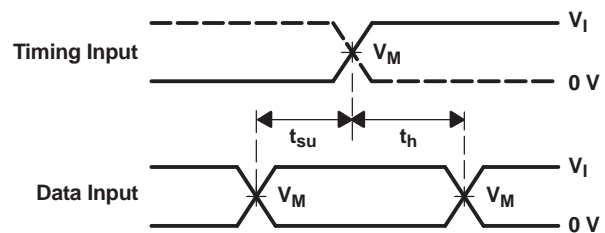
LOAD CIRCUIT

| TEST              | S1         |
|-------------------|------------|
| $t_{PLH}/t_{PHL}$ | Open       |
| $t_{PLZ}/t_{PZL}$ | $V_{LOAD}$ |
| $t_{PHZ}/t_{PZH}$ | GND        |

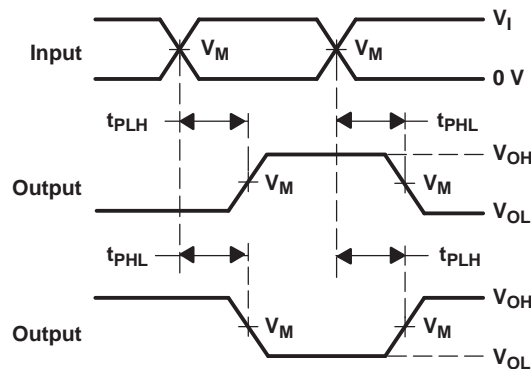
| $V_{CC}$                         | INPUTS   |                      | $V_M$      | $V_{LOAD}$        | $C_L$ | $R_L$        | $V_{\Delta}$ |
|----------------------------------|----------|----------------------|------------|-------------------|-------|--------------|--------------|
|                                  | $V_I$    | $t_r/t_f$            |            |                   |       |              |              |
| $1.8\text{ V} \pm 0.15\text{ V}$ | $V_{CC}$ | $\leq 2\text{ ns}$   | $V_{CC}/2$ | $2 \times V_{CC}$ | 15 pF | 1 M $\Omega$ | 0.15 V       |
| $2.5\text{ V} \pm 0.2\text{ V}$  | $V_{CC}$ | $\leq 2\text{ ns}$   | $V_{CC}/2$ | $2 \times V_{CC}$ | 15 pF | 1 M $\Omega$ | 0.15 V       |
| $3.3\text{ V} \pm 0.3\text{ V}$  | 3 V      | $\leq 2.5\text{ ns}$ | 1.5 V      | 6 V               | 15 pF | 1 M $\Omega$ | 0.3 V        |
| $5\text{ V} \pm 0.5\text{ V}$    | $V_{CC}$ | $\leq 2.5\text{ ns}$ | $V_{CC}/2$ | $2 \times V_{CC}$ | 15 pF | 1 M $\Omega$ | 0.3 V        |



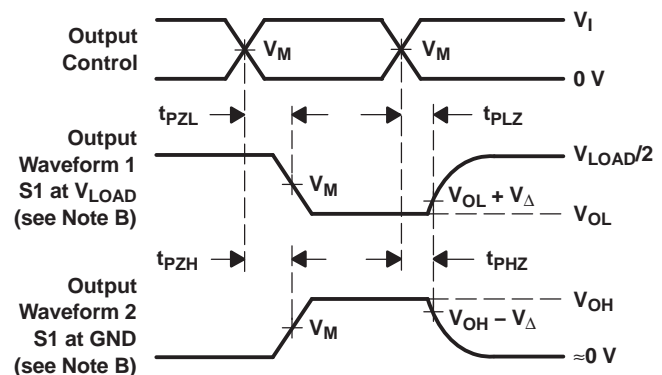
VOLTAGE WAVEFORMS PULSE DURATION



VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES INVERTING AND NONINVERTING OUTPUTS

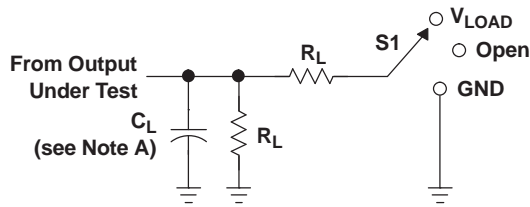


VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ .
  - D. The outputs are measured one at a time, with one transition per measurement.
  - E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
  - H. All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuit and Voltage Waveforms

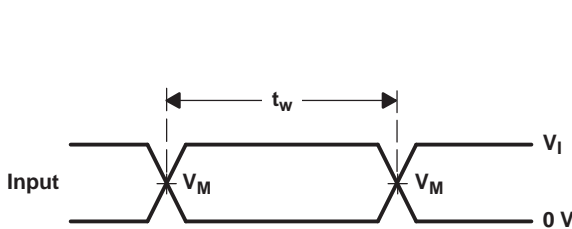
Parameter Measurement Information (continued)



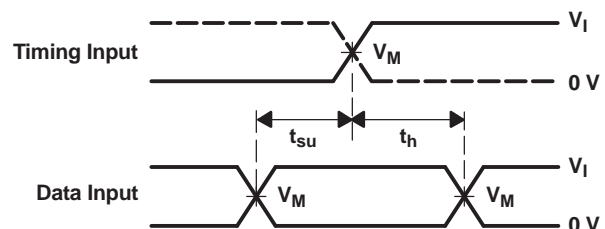
LOAD CIRCUIT

| TEST              | S1         |
|-------------------|------------|
| $t_{PLH}/t_{PHL}$ | Open       |
| $t_{PLZ}/t_{PZL}$ | $V_{LOAD}$ |
| $t_{PHZ}/t_{PZH}$ | GND        |

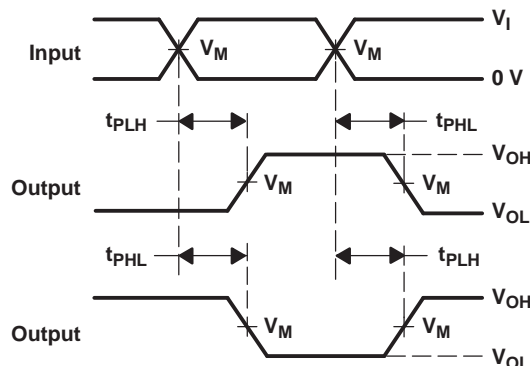
| $V_{CC}$                         | INPUTS   |                      | $V_M$      | $V_{LOAD}$        | $C_L$ | $R_L$        | $V_{\Delta}$ |
|----------------------------------|----------|----------------------|------------|-------------------|-------|--------------|--------------|
|                                  | $V_I$    | $t_r/t_f$            |            |                   |       |              |              |
| $1.8\text{ V} \pm 0.15\text{ V}$ | $V_{CC}$ | $\leq 2\text{ ns}$   | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 1 k $\Omega$ | 0.15 V       |
| $2.5\text{ V} \pm 0.2\text{ V}$  | $V_{CC}$ | $\leq 2\text{ ns}$   | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 500 $\Omega$ | 0.15 V       |
| $3.3\text{ V} \pm 0.3\text{ V}$  | 3 V      | $\leq 2.5\text{ ns}$ | 1.5 V      | 6 V               | 50 pF | 500 $\Omega$ | 0.3 V        |
| $5\text{ V} \pm 0.5\text{ V}$    | $V_{CC}$ | $\leq 2.5\text{ ns}$ | $V_{CC}/2$ | $2 \times V_{CC}$ | 50 pF | 500 $\Omega$ | 0.3 V        |



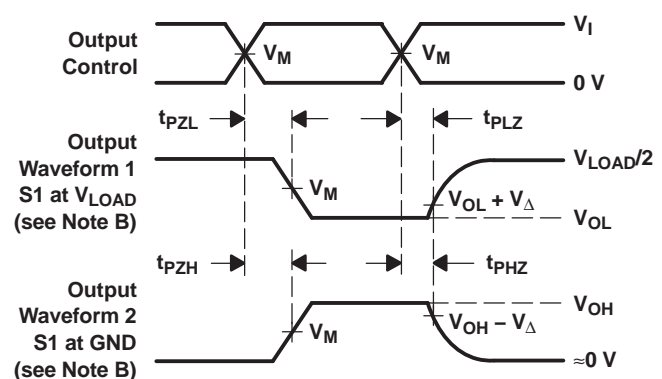
VOLTAGE WAVEFORMS PULSE DURATION



VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ .
  - D. The outputs are measured one at a time, with one transition per measurement.
  - E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
  - H. All parameters and waveforms are not applicable to all devices.

Figure 4. Load Circuit and Voltage Waveforms

## 9 Detailed Description

### 9.1 Overview

The SN74LVC1G34 device contains one buffer gate device and performs the Boolean function  $Y = A$ . This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

The DPW package technology is a major breakthrough in IC packaging. Its tiny 0.64 mm square footprint saves significant board space over other package options while still retaining the traditional manufacturing friendly lead pitch of 0.5 mm.

### 9.2 Functional Block Diagram



### 9.3 Feature Description

- Wide operating voltage range.
  - Operates from 1.65 V to 5.5 V.
- Allows down voltage translation.
- Inputs accept voltages to 5.5 V.
- $I_{off}$  feature allows voltages on the inputs and outputs when  $V_{CC}$  is 0 V.

### 9.4 Device Functional Modes

**Function Table**

| INPUT<br>A | OUTPUT<br>Y |
|------------|-------------|
| H          | H           |
| L          | L           |

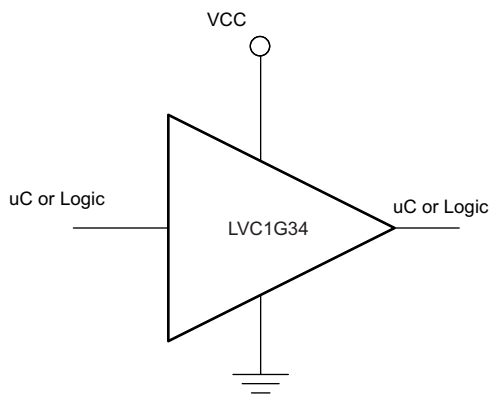
## 10 Application and Implementation

### 10.1 Application Information

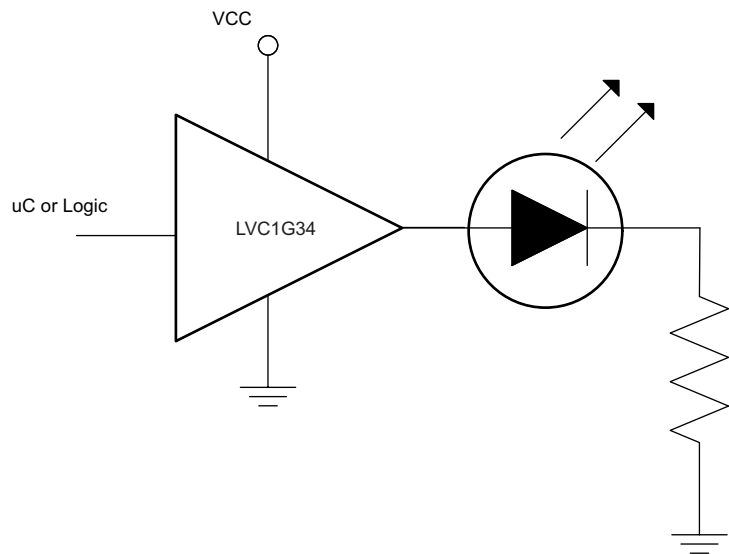
The SN74LVC1G34 is a high drive CMOS device that can be used as a buffer with a high output drive, such as an LED application. It can produce 24 mA of drive current at 3.3 V making it ideal for driving multiple outputs and good for high speed applications up to 100 MHz. The inputs are 5.5 V tolerant allowing it to translate down to  $V_{CC}$ .

### 10.2 Typical Application

Buffer Function



Basic LED Driver



#### 10.2.1 Design Requirements

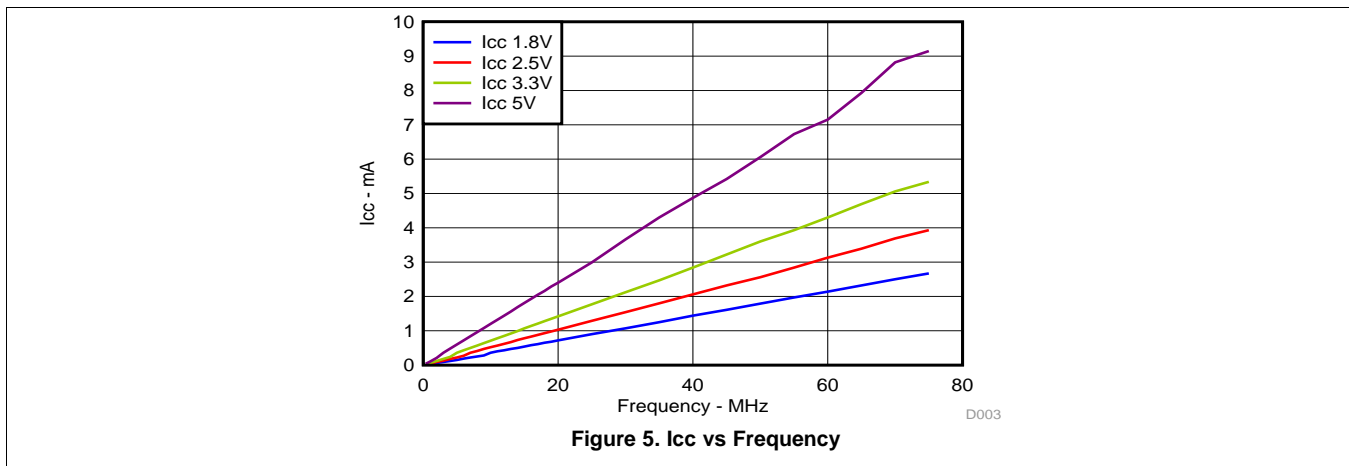
This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads so routing and load conditions should be considered to prevent ringing.

#### 10.2.2 Detailed Design Procedure

1. Recommended Input Conditions
  - Rise time and fall time specs. See  $(\Delta t/\Delta V)$  in the [Recommended Operating Conditions](#) table.
  - Specified high and low levels. See  $(V_{IH}$  and  $V_{IL})$  in the [Recommended Operating Conditions](#) table.
  - Inputs are overvoltage tolerant allowing them to go as high as  $(VI \text{ max})$  in the [Recommended Operating Conditions](#) table at any valid  $V_{CC}$ .
2. Recommend Output Conditions
  - Load currents should not exceed  $(I_O \text{ max})$  per output and should not exceed (Continuous current through  $V_{CC}$  or GND) total current for the part. These limits are located in the [Absolute Max Ratings](#) table.
  - Outputs should not be pulled above  $V_{CC}$ .

## Typical Application (continued)

### 10.2.3 Application Curves



## 11 Power Supply Recommendations

The power supply can be any voltage between the min and max supply voltage rating located in the [Recommended Operating Conditions](#) table.

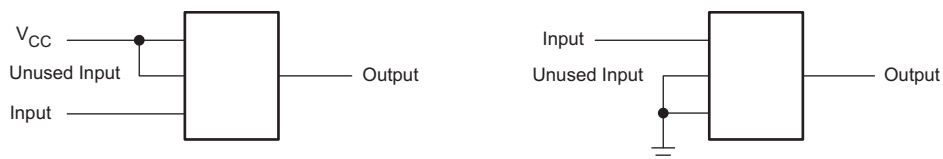
Each V<sub>CC</sub> pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply a 0.1- $\mu$ F capacitor is recommended and if there are multiple V<sub>CC</sub> pins then a 0.01- $\mu$ F or 0.022- $\mu$ F capacitor is recommended for each power pin. It is ok to parallel multiple bypass caps to reject different frequencies of noise. 0.1- $\mu$ F and 1- $\mu$ F capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

## 12 Layout

### 12.1 Layout Guidelines

When using multiple bit logic devices inputs should not ever float. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified below are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to Gnd or V<sub>CC</sub> whichever make more sense or is more convenient.

### 12.2 Layout Example



## 13 Device and Documentation Support

### 13.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](http://e2e.ti.com), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 13.2 Trademarks

E2E is a trademark of Texas Instruments.  
All other trademarks are the property of their respective owners.

### 13.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 13.4 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

| Orderable Device  | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2) | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5)                                 | Samples                 |
|-------------------|---------------|--------------|--------------------|------|----------------|-----------------|--------------------------------------|----------------------|--------------|---|-------------------------|
| SN74LVC1G34DBVR   | ACTIVE        | SOT-23       | DBV                | 5    | 3000           | RoHS & Green    | NIPDAU   SN                          | Level-1-260C-UNLIM   | -40 to 125   | (C345, C34F, C34J,<br>C34K, C34R)<br>(C34H, C34P, C34S) | <a href="#">Samples</a> |
| SN74LVC1G34DBVRE4 | ACTIVE        | SOT-23       | DBV                | 5    | 3000           | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | C345<br>C34S  | <a href="#">Samples</a> |
| SN74LVC1G34DBVRG4 | ACTIVE        | SOT-23       | DBV                | 5    | 3000           | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | C345<br>C34S  | <a href="#">Samples</a> |
| SN74LVC1G34DBVT   | ACTIVE        | SOT-23       | DBV                | 5    | 250            | RoHS & Green    | NIPDAU   SN                          | Level-1-260C-UNLIM   | -40 to 125   | (C345, C34J, C34K,<br>C34R)<br>(C34H, C34S)             | <a href="#">Samples</a> |
| SN74LVC1G34DBVTE4 | ACTIVE        | SOT-23       | DBV                | 5    | 250            | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | C345<br>C34S  | <a href="#">Samples</a> |
| SN74LVC1G34DBVTG4 | ACTIVE        | SOT-23       | DBV                | 5    | 250            | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | C345<br>C34S  | <a href="#">Samples</a> |
| SN74LVC1G34DCKR   | ACTIVE        | SC70         | DCK                | 5    | 3000           | RoHS & Green    | NIPDAU   SN                          | Level-1-260C-UNLIM   | -40 to 125   | (C95, C9F, C9J, C9<br>K, C9R)<br>(C9H, C9P, C9S)        | <a href="#">Samples</a> |
| SN74LVC1G34DCKRE4 | ACTIVE        | SC70         | DCK                | 5    | 3000           | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | C95<br>C9S  | <a href="#">Samples</a> |
| SN74LVC1G34DCKRG4 | ACTIVE        | SC70         | DCK                | 5    | 3000           | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | C95<br>C9S  | <a href="#">Samples</a> |
| SN74LVC1G34DCKT   | ACTIVE        | SC70         | DCK                | 5    | 250            | RoHS & Green    | NIPDAU   SN                          | Level-1-260C-UNLIM   | -40 to 125   | (C95, C9J, C9K, C9<br>R)<br>(C9H, C9S)                  | <a href="#">Samples</a> |
| SN74LVC1G34DCKTG4 | ACTIVE        | SC70         | DCK                | 5    | 250            | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | C95<br>C9S  | <a href="#">Samples</a> |
| SN74LVC1G34DPWR   | ACTIVE        | X2SON        | DPW                | 5    | 3000           | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | P4  | <a href="#">Samples</a> |
| SN74LVC1G34DRLR   | ACTIVE        | SOT-5X3      | DRL                | 5    | 4000           | RoHS & Green    | NIPDAU   NIPDAUAG                    | Level-1-260C-UNLIM   | -40 to 125   | (C97, C9R)  | <a href="#">Samples</a> |
| SN74LVC1G34DRYR   | ACTIVE        | SON          | DRY                | 6    | 5000           | RoHS & Green    | NIPDAU   NIPDAUAG                    | Level-1-260C-UNLIM   | -40 to 125   | C9  | <a href="#">Samples</a> |
| SN74LVC1G34DSFR   | ACTIVE        | SON          | DSF                | 6    | 5000           | RoHS & Green    | NIPDAU   NIPDAUAG                    | Level-1-260C-UNLIM   | -40 to 125   | C9  | <a href="#">Samples</a> |

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2) | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| SN74LVC1G34YFPR  | ACTIVE        | DSBGA        | YFP             | 4    | 3000        | RoHS & Green    | SNAGCU                               | Level-1-260C-UNLIM   | -40 to 85    | C9<br>N                 | <a href="#">Samples</a> |
| SN74LVC1G34YZPR  | ACTIVE        | DSBGA        | YZP             | 5    | 3000        | RoHS & Green    | SNAGCU                               | Level-1-260C-UNLIM   | -40 to 85    | C9N                     | <a href="#">Samples</a> |
| SN74LVC1G34YZVR  | ACTIVE        | DSBGA        | YZV             | 4    | 3000        | RoHS & Green    | SNAGCU                               | Level-1-260C-UNLIM   | -40 to 85    | C9<br>N                 | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

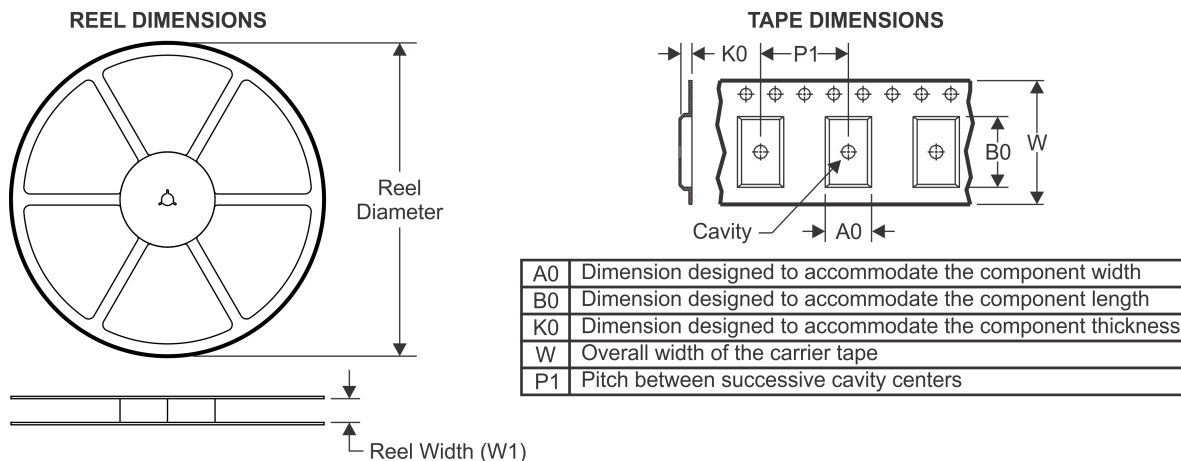
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.



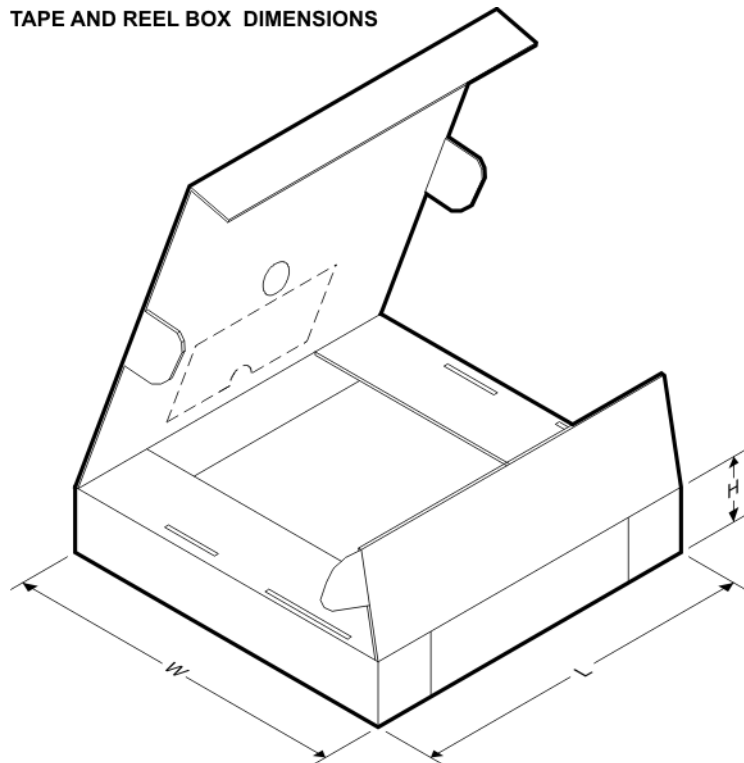


**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

| Device            | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74LVC1G34DBVR   | SOT-23       | DBV             | 5    | 3000 | 180.0              | 8.4                | 3.23    | 3.17    | 1.37    | 4.0     | 8.0    | Q3            |
| SN74LVC1G34DBVR   | SOT-23       | DBV             | 5    | 3000 | 178.0              | 9.0                | 3.3     | 3.2     | 1.4     | 4.0     | 8.0    | Q3            |
| SN74LVC1G34DBVR   | SOT-23       | DBV             | 5    | 3000 | 178.0              | 9.2                | 3.3     | 3.23    | 1.55    | 4.0     | 8.0    | Q3            |
| SN74LVC1G34DBVRG4 | SOT-23       | DBV             | 5    | 3000 | 178.0              | 9.2                | 3.3     | 3.23    | 1.55    | 4.0     | 8.0    | Q3            |
| SN74LVC1G34DBVT   | SOT-23       | DBV             | 5    | 250  | 180.0              | 8.4                | 3.23    | 3.17    | 1.37    | 4.0     | 8.0    | Q3            |
| SN74LVC1G34DBVT   | SOT-23       | DBV             | 5    | 250  | 178.0              | 9.2                | 3.3     | 3.23    | 1.55    | 4.0     | 8.0    | Q3            |
| SN74LVC1G34DBVT   | SOT-23       | DBV             | 5    | 250  | 178.0              | 9.0                | 3.3     | 3.2     | 1.4     | 4.0     | 8.0    | Q3            |
| SN74LVC1G34DBVTG4 | SOT-23       | DBV             | 5    | 250  | 178.0              | 9.2                | 3.3     | 3.23    | 1.55    | 4.0     | 8.0    | Q3            |
| SN74LVC1G34DCKR   | SC70         | DCK             | 5    | 3000 | 178.0              | 9.2                | 2.4     | 2.4     | 1.22    | 4.0     | 8.0    | Q3            |
| SN74LVC1G34DCKR   | SC70         | DCK             | 5    | 3000 | 178.0              | 9.0                | 2.4     | 2.5     | 1.2     | 4.0     | 8.0    | Q3            |
| SN74LVC1G34DCKR   | SC70         | DCK             | 5    | 3000 | 180.0              | 8.4                | 2.47    | 2.3     | 1.25    | 4.0     | 8.0    | Q3            |
| SN74LVC1G34DCKRG4 | SC70         | DCK             | 5    | 3000 | 178.0              | 9.2                | 2.4     | 2.4     | 1.22    | 4.0     | 8.0    | Q3            |
| SN74LVC1G34DCKT   | SC70         | DCK             | 5    | 250  | 178.0              | 9.0                | 2.4     | 2.5     | 1.2     | 4.0     | 8.0    | Q3            |
| SN74LVC1G34DCKT   | SC70         | DCK             | 5    | 250  | 178.0              | 9.2                | 2.4     | 2.4     | 1.22    | 4.0     | 8.0    | Q3            |
| SN74LVC1G34DCKT   | SC70         | DCK             | 5    | 250  | 180.0              | 8.4                | 2.47    | 2.3     | 1.25    | 4.0     | 8.0    | Q3            |
| SN74LVC1G34DCKTG4 | SC70         | DCK             | 5    | 250  | 178.0              | 9.2                | 2.4     | 2.4     | 1.22    | 4.0     | 8.0    | Q3            |
| SN74LVC1G34DPWR   | X2SON        | DPW             | 5    | 3000 | 178.0              | 8.4                | 0.91    | 0.91    | 0.5     | 2.0     | 8.0    | Q3            |
| SN74LVC1G34DRLR   | SOT-5X3      | DRL             | 5    | 4000 | 180.0              | 8.4                | 1.98    | 1.78    | 0.69    | 4.0     | 8.0    | Q3            |

| Device          | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74LVC1G34DRYR | SON          | DRY             | 6    | 5000 | 180.0              | 9.5                | 1.15    | 1.6     | 0.75    | 4.0     | 8.0    | Q1            |
| SN74LVC1G34DSFR | SON          | DSF             | 6    | 5000 | 180.0              | 9.5                | 1.16    | 1.16    | 0.5     | 4.0     | 8.0    | Q2            |
| SN74LVC1G34YFPR | DSBGA        | YFP             | 4    | 3000 | 178.0              | 9.2                | 0.89    | 0.89    | 0.58    | 4.0     | 8.0    | Q1            |
| SN74LVC1G34YZPR | DSBGA        | YZP             | 5    | 3000 | 178.0              | 9.2                | 1.02    | 1.52    | 0.63    | 4.0     | 8.0    | Q1            |
| SN74LVC1G34YZVR | DSBGA        | YZV             | 4    | 3000 | 178.0              | 9.2                | 1.0     | 1.0     | 0.63    | 4.0     | 8.0    | Q1            |

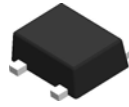
**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

| Device            | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74LVC1G34DBVR   | SOT-23       | DBV             | 5    | 3000 | 202.0       | 201.0      | 28.0        |
| SN74LVC1G34DBVR   | SOT-23       | DBV             | 5    | 3000 | 180.0       | 180.0      | 18.0        |
| SN74LVC1G34DBVR   | SOT-23       | DBV             | 5    | 3000 | 180.0       | 180.0      | 18.0        |
| SN74LVC1G34DBVRG4 | SOT-23       | DBV             | 5    | 3000 | 180.0       | 180.0      | 18.0        |
| SN74LVC1G34DBVT   | SOT-23       | DBV             | 5    | 250  | 202.0       | 201.0      | 28.0        |
| SN74LVC1G34DBVT   | SOT-23       | DBV             | 5    | 250  | 180.0       | 180.0      | 18.0        |
| SN74LVC1G34DBVT   | SOT-23       | DBV             | 5    | 250  | 180.0       | 180.0      | 18.0        |
| SN74LVC1G34DBVTG4 | SOT-23       | DBV             | 5    | 250  | 180.0       | 180.0      | 18.0        |
| SN74LVC1G34DCKR   | SC70         | DCK             | 5    | 3000 | 180.0       | 180.0      | 18.0        |
| SN74LVC1G34DCKR   | SC70         | DCK             | 5    | 3000 | 180.0       | 180.0      | 18.0        |
| SN74LVC1G34DCKR   | SC70         | DCK             | 5    | 3000 | 202.0       | 201.0      | 28.0        |
| SN74LVC1G34DCKRG4 | SC70         | DCK             | 5    | 3000 | 180.0       | 180.0      | 18.0        |

| Device            | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74LVC1G34DCKT   | SC70         | DCK             | 5    | 250  | 180.0       | 180.0      | 18.0        |
| SN74LVC1G34DCKT   | SC70         | DCK             | 5    | 250  | 180.0       | 180.0      | 18.0        |
| SN74LVC1G34DCKT   | SC70         | DCK             | 5    | 250  | 202.0       | 201.0      | 28.0        |
| SN74LVC1G34DCKTG4 | SC70         | DCK             | 5    | 250  | 180.0       | 180.0      | 18.0        |
| SN74LVC1G34DPWR   | X2SON        | DPW             | 5    | 3000 | 205.0       | 200.0      | 33.0        |
| SN74LVC1G34DRLR   | SOT-5X3      | DRL             | 5    | 4000 | 202.0       | 201.0      | 28.0        |
| SN74LVC1G34DRYR   | SON          | DRY             | 6    | 5000 | 184.0       | 184.0      | 19.0        |
| SN74LVC1G34DSFR   | SON          | DSF             | 6    | 5000 | 184.0       | 184.0      | 19.0        |
| SN74LVC1G34YFPR   | DSBGA        | YFP             | 4    | 3000 | 220.0       | 220.0      | 35.0        |
| SN74LVC1G34YZPR   | DSBGA        | YZP             | 5    | 3000 | 220.0       | 220.0      | 35.0        |
| SN74LVC1G34YZVR   | DSBGA        | YZV             | 4    | 3000 | 220.0       | 220.0      | 35.0        |

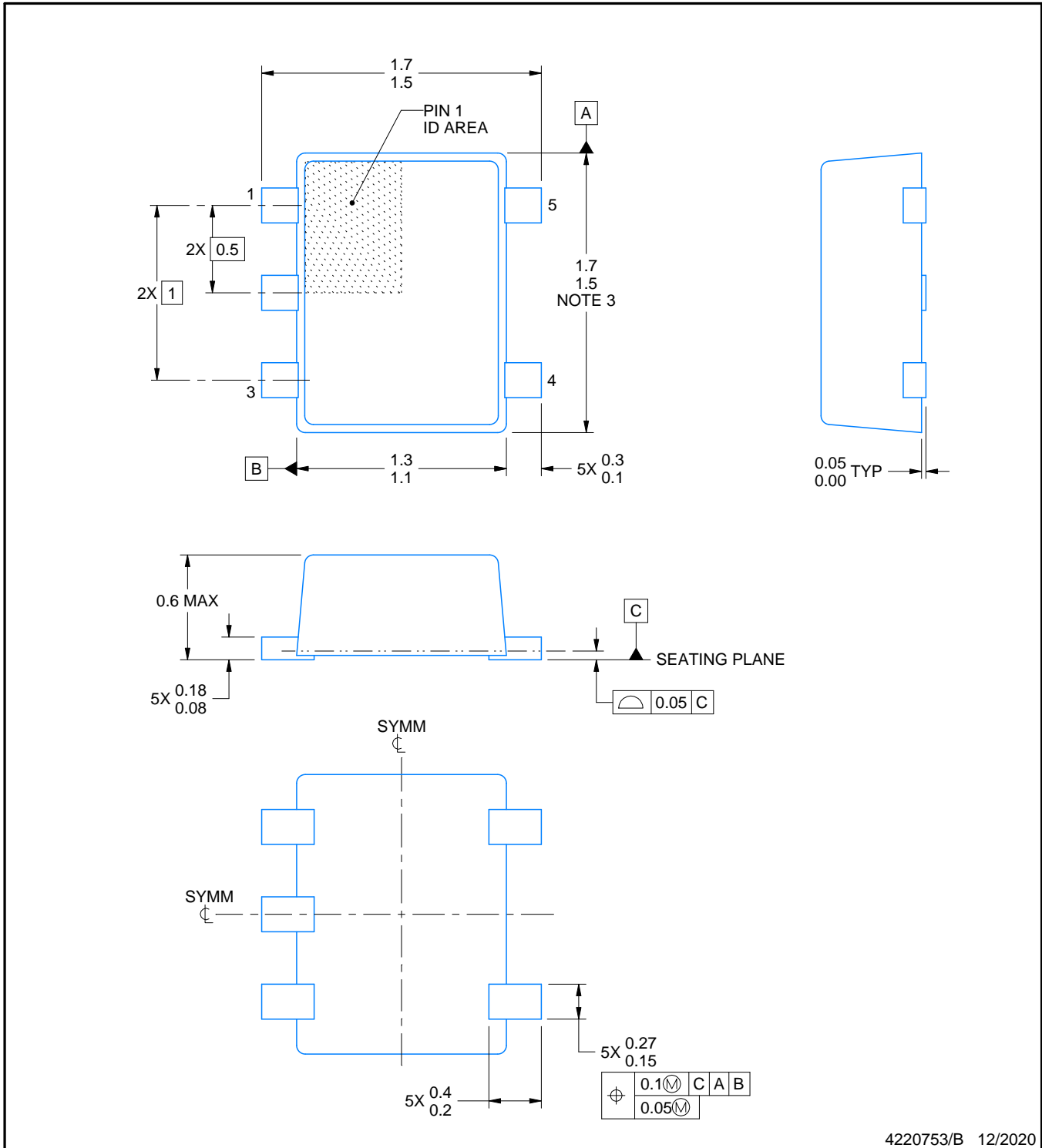
DRL0005A



# PACKAGE OUTLINE

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



4220753/B 12/2020

## NOTES:

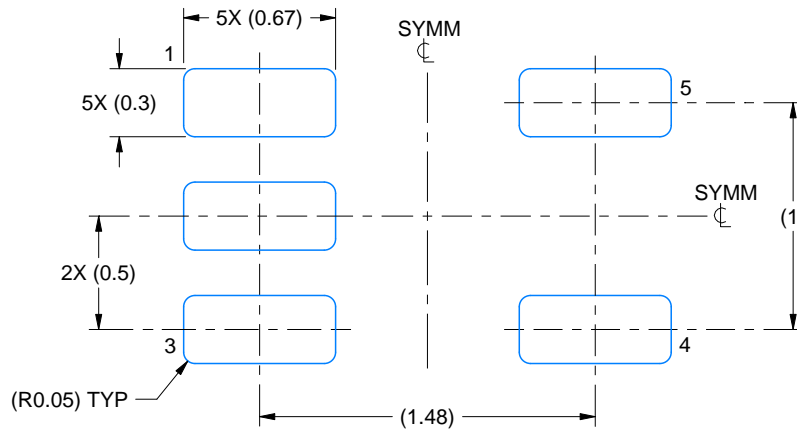
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-293 Variation UAAD-1

# EXAMPLE BOARD LAYOUT

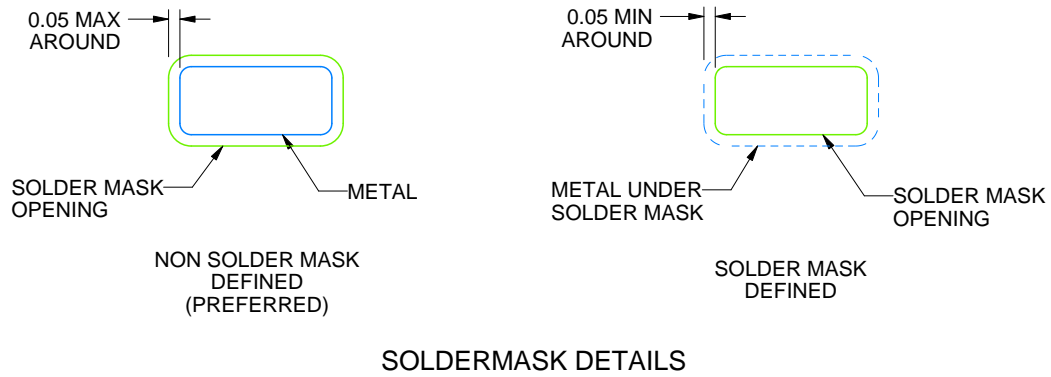
DRL0005A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE  
SCALE:30X



SOLDERMASK DETAILS

4220753/B 12/2020

NOTES: (continued)

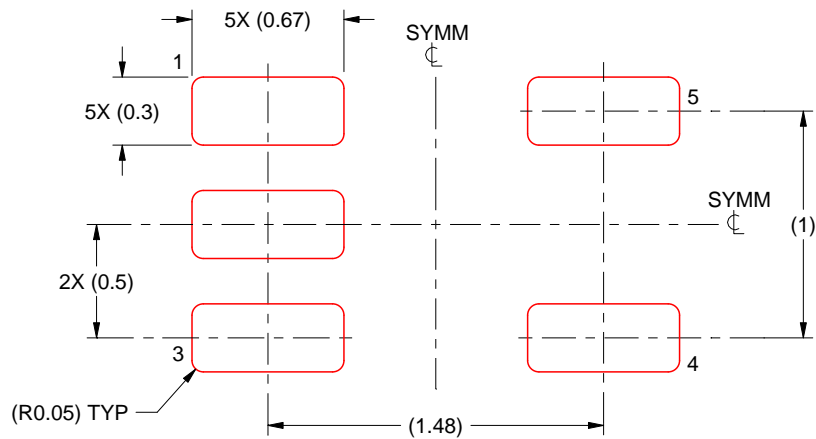
- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DRL0005A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE  
BASED ON 0.1 mm THICK STENCIL  
SCALE:30X

4220753/B 12/2020

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

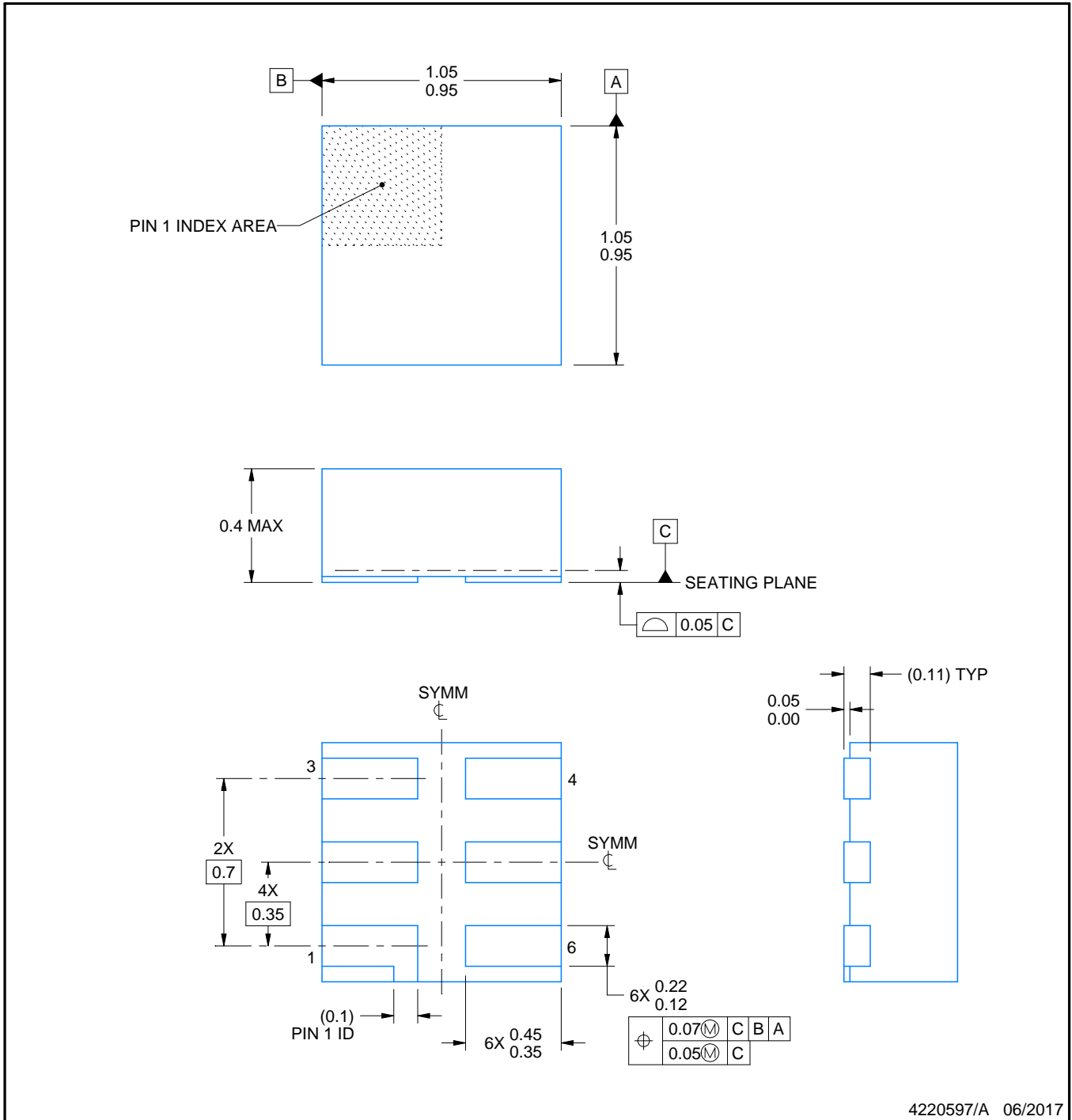


# DSF0006A

# PACKAGE OUTLINE

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



4220597/A 06/2017

**NOTES:**

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MO-287, variation X2AAF.

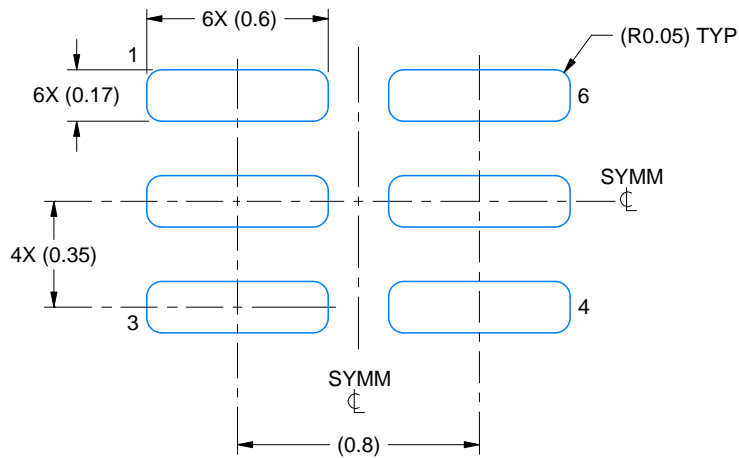


# EXAMPLE BOARD LAYOUT

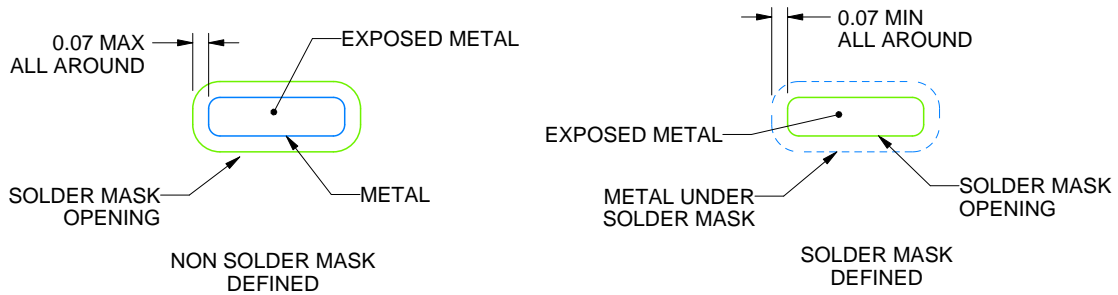
DSF0006A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:40X



SOLDER MASK DETAILS

4220597/A 06/2017

NOTES: (continued)

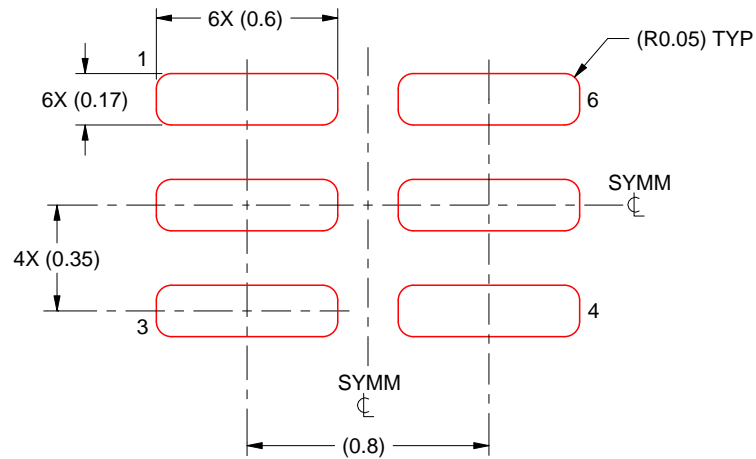
4. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).

# EXAMPLE STENCIL DESIGN

DSF0006A

X2SON - 0.4 mm max height

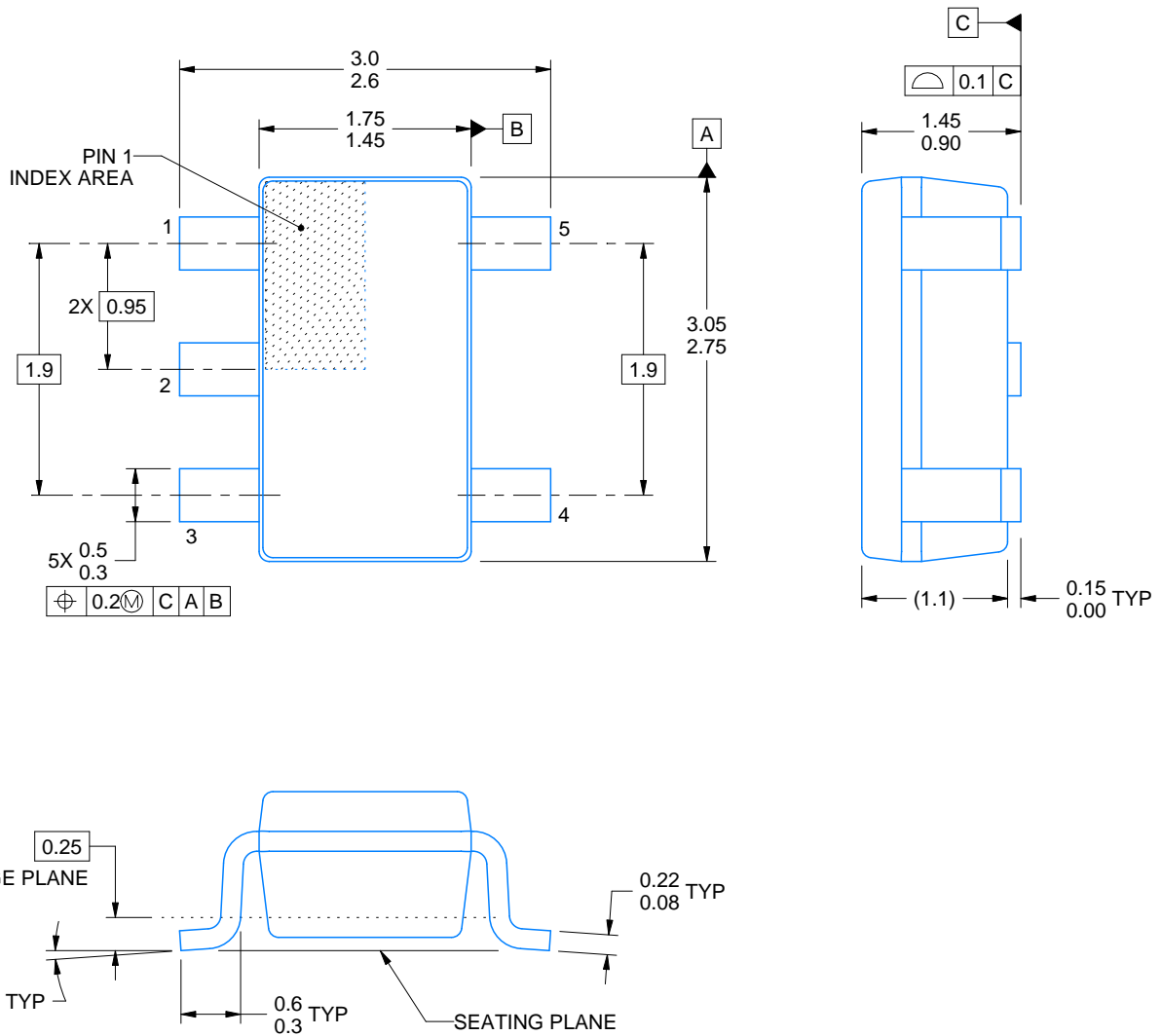
PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
SCALE:40X

4220597/A 06/2017

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



4214839/E 09/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.

# EXAMPLE BOARD LAYOUT

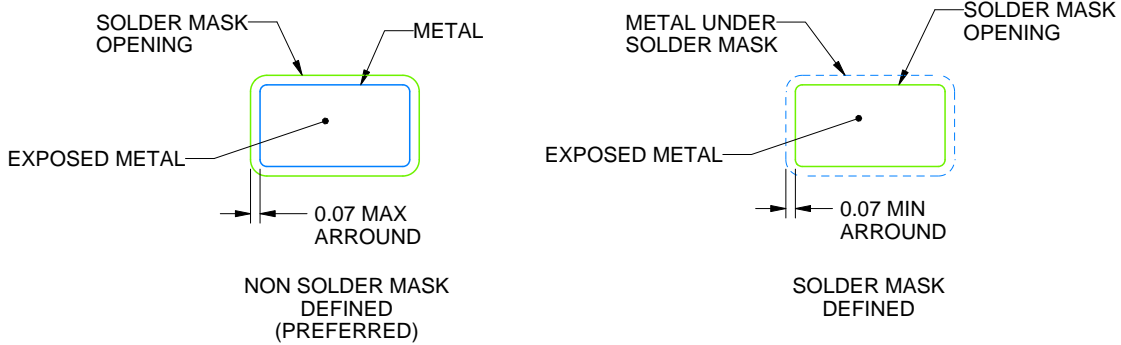
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

4214839/E 09/2019

NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

4214839/E 09/2019

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

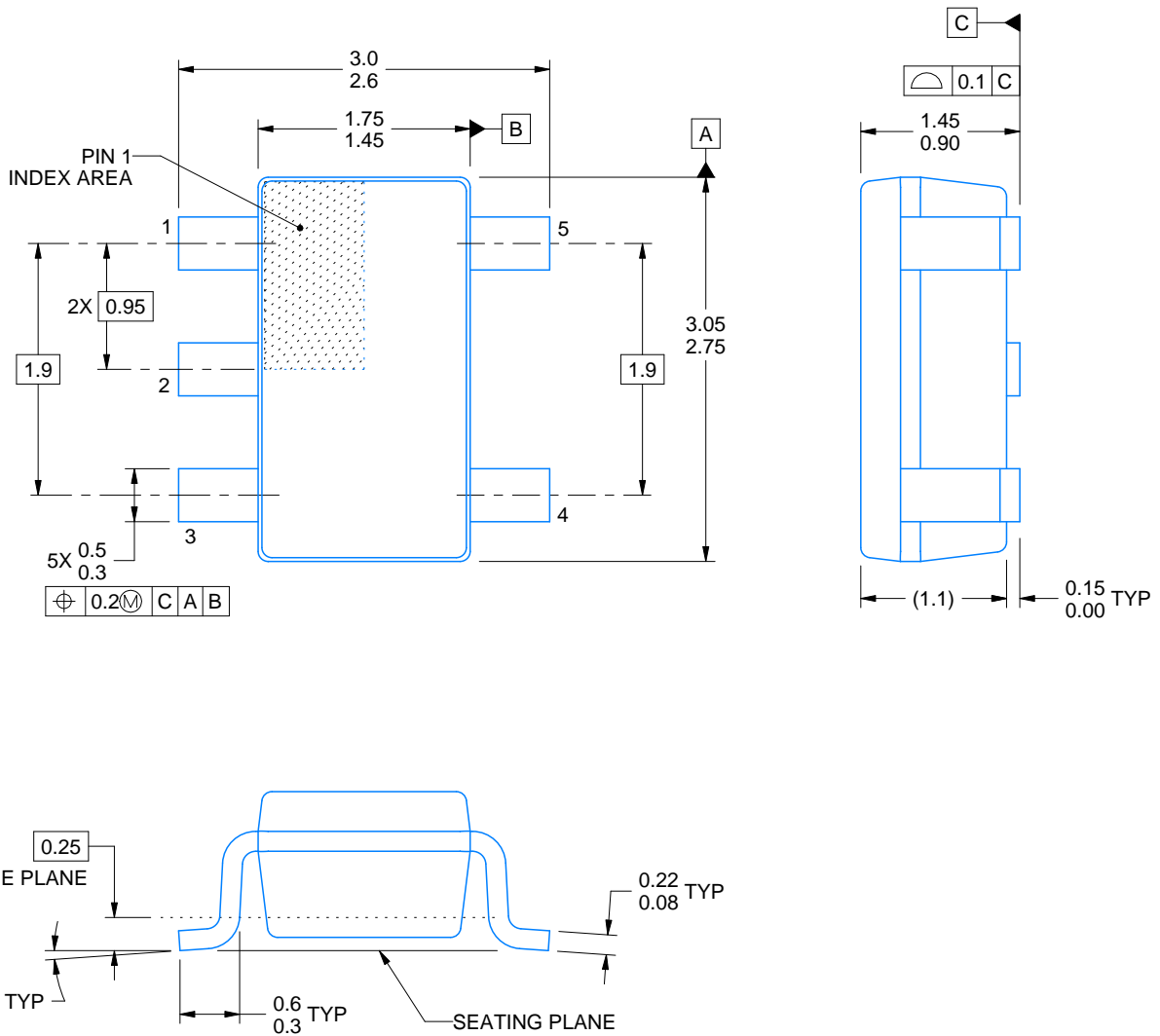


DBV0005A

# PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



4214839/F 06/2021

## NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.

# EXAMPLE BOARD LAYOUT

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

4214839/F 06/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

4214839/F 06/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.



## GENERIC PACKAGE VIEW

DPW 5

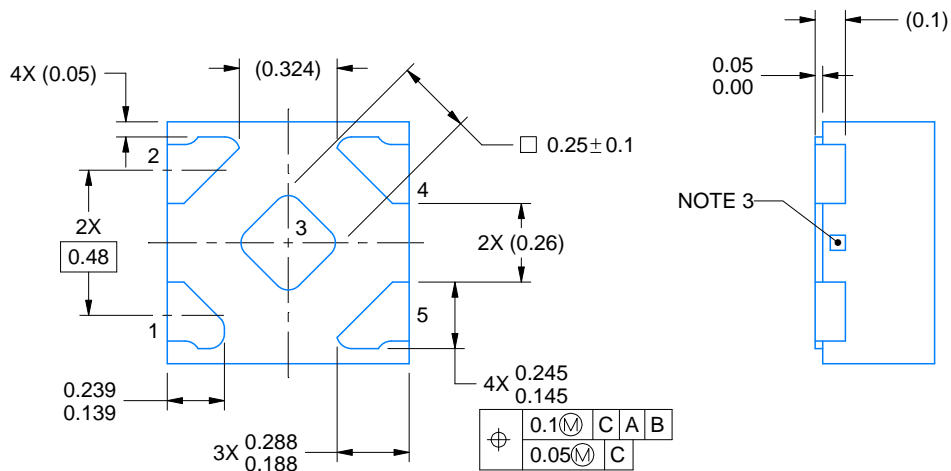
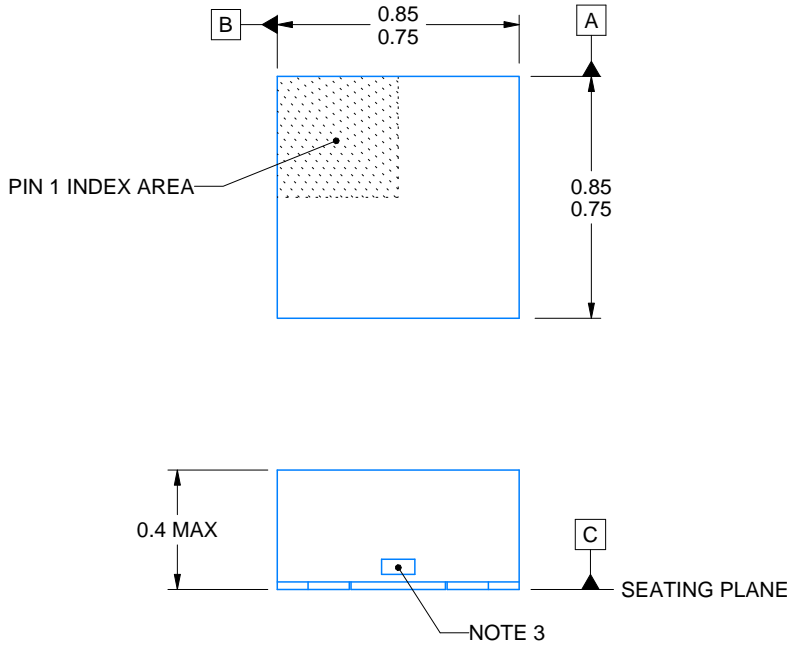
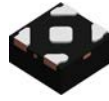
X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4211218-3/D



4223102/C 06/2021

NOTES:

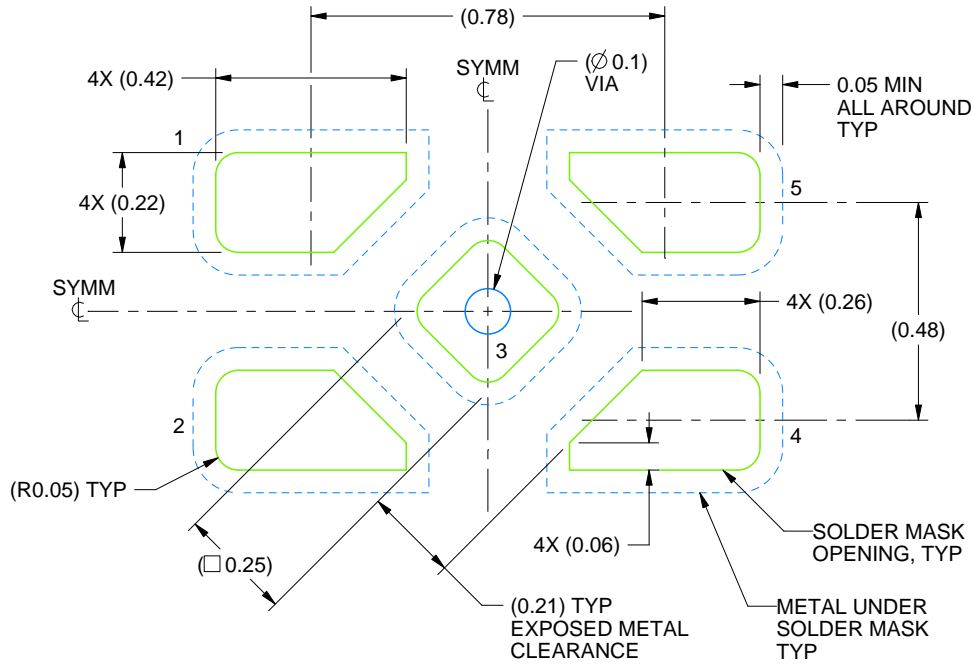
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The size and shape of this feature may vary.

# EXAMPLE BOARD LAYOUT

DPW0005A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE  
SOLDER MASK DEFINED  
SCALE:60X

4223102/C 06/2021

NOTES: (continued)

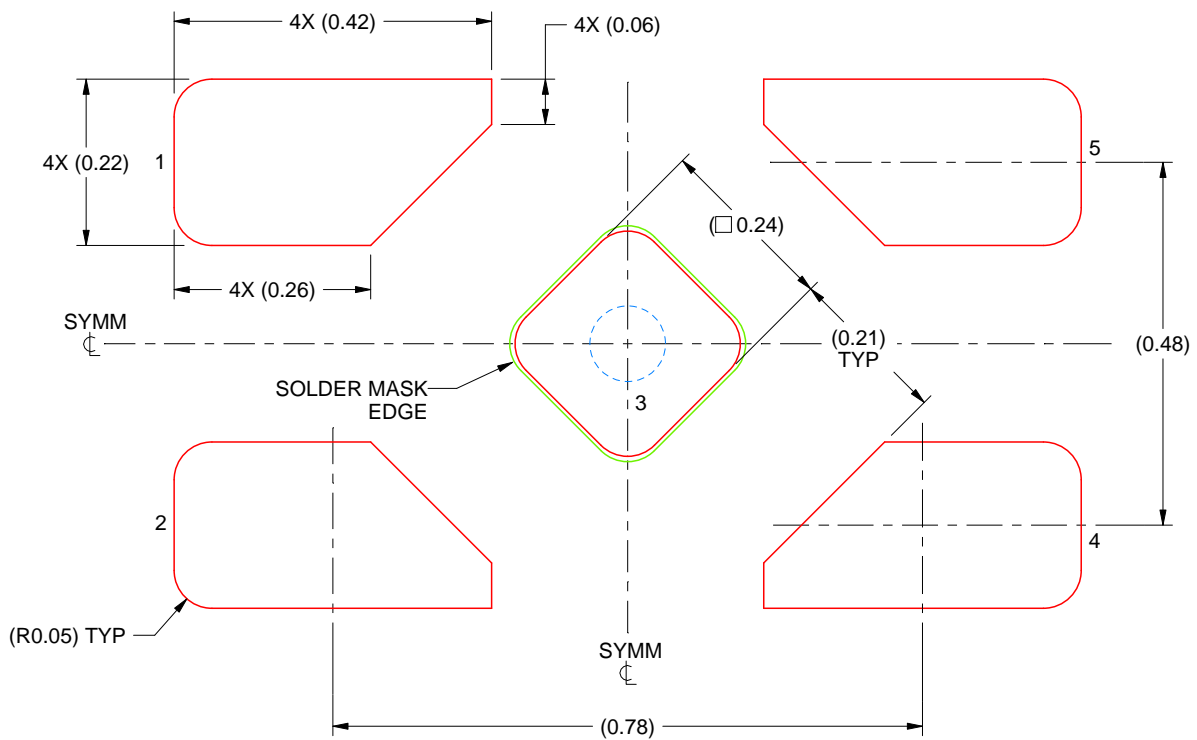
4. This package is designed to be soldered to a thermal pad on the board. For more information, refer to QFN/SON PCB application note in literature No. SLUA271 ([www.ti.com/lit/sl原因271](http://www.ti.com/lit/sl原因271)).

# EXAMPLE STENCIL DESIGN

DPW0005A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.1 mm THICK STENCIL

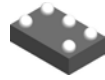
EXPOSED PAD 3  
92% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
SCALE:100X

4223102/C 06/2021

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

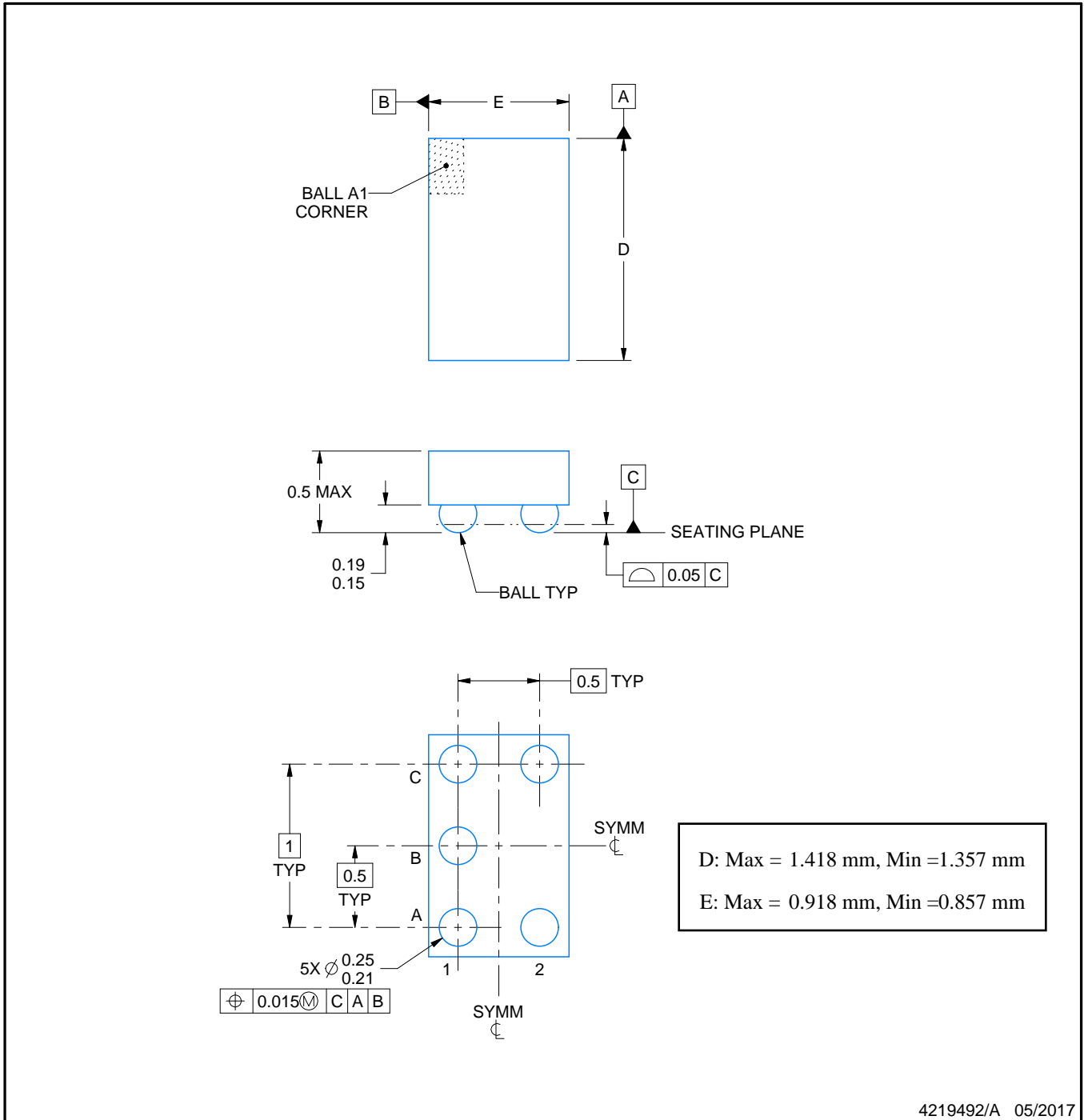
YZP0005



# PACKAGE OUTLINE

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



4219492/A 05/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

# EXAMPLE BOARD LAYOUT

YZP0005

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE  
SCALE:40X



SOLDER MASK DETAILS  
NOT TO SCALE

4219492/A 05/2017

NOTES: (continued)

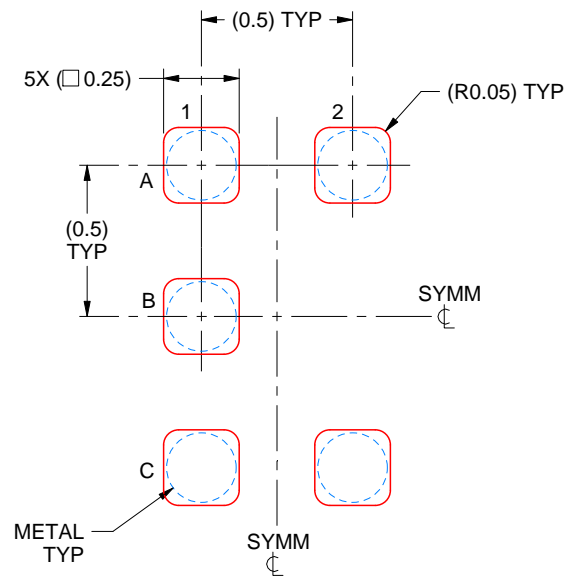
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 ([www.ti.com/lit/snva009](http://www.ti.com/lit/snva009)).

# EXAMPLE STENCIL DESIGN

YZP0005

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE  
BASED ON 0.1 mm THICK STENCIL  
SCALE:40X

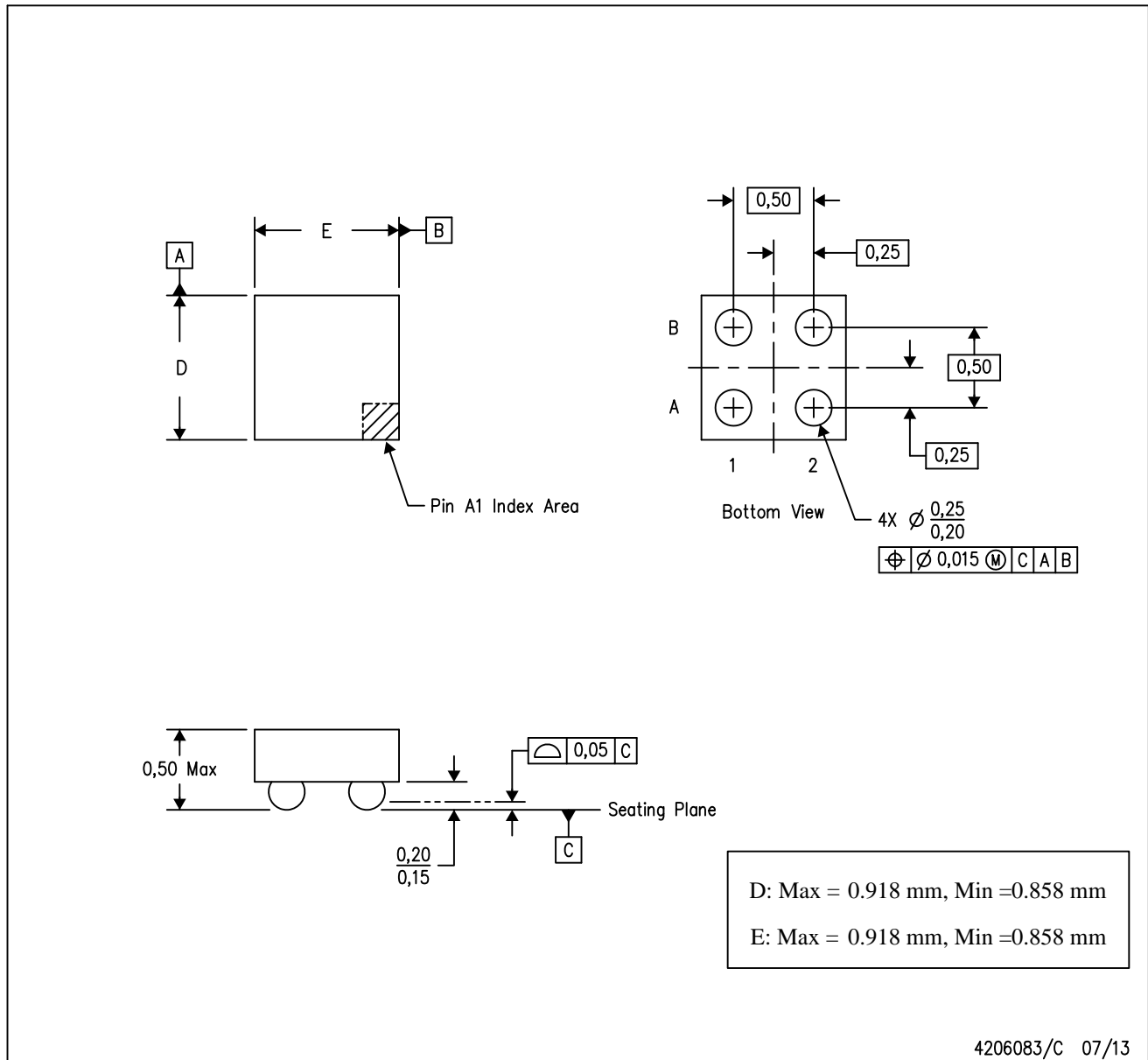
4219492/A 05/2017

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

YZV (S-XBGA-N4)

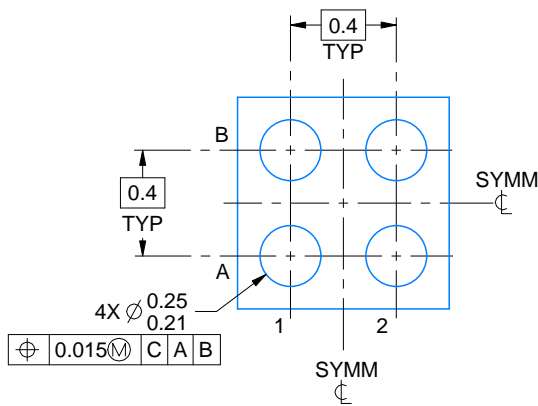
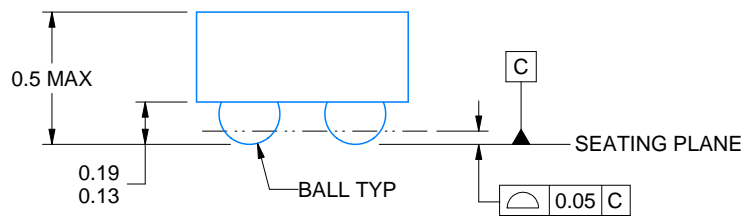
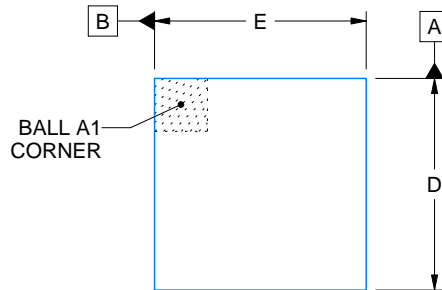
DIE-SIZE BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. NanoFree™ package configuration.

NanoFree is a trademark of Texas Instruments.





D: Max = 0.79 mm, Min = 0.73 mm  
 E: Max = 0.79 mm, Min = 0.73 mm

4223507/A 01/2017

NOTES:

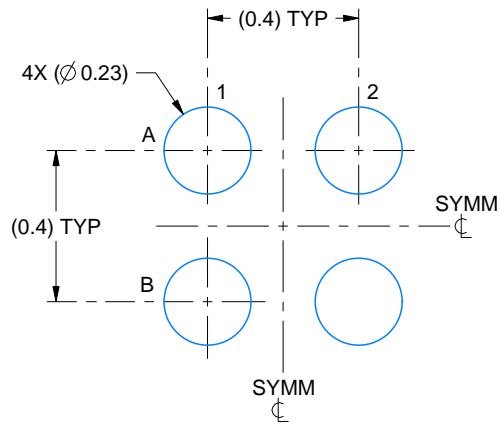
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

# EXAMPLE BOARD LAYOUT

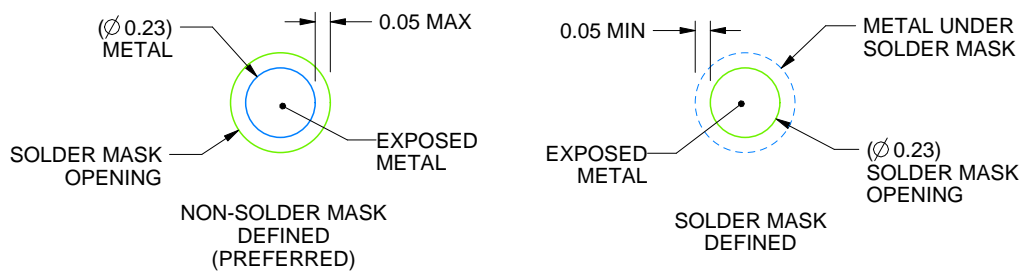
YFP0004

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:50X



SOLDER MASK DETAILS  
NOT TO SCALE

4223507/A 01/2017

NOTES: (continued)

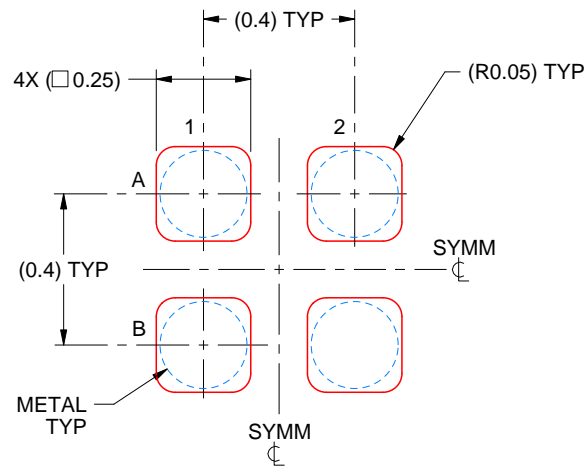
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 ([www.ti.com/lit/snva009](http://www.ti.com/lit/snva009)).

# EXAMPLE STENCIL DESIGN

YFP0004

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE  
BASED ON 0.1 mm THICK STENCIL  
SCALE:50X

4223507/A 01/2017

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

DCK (R-PDSO-G5)

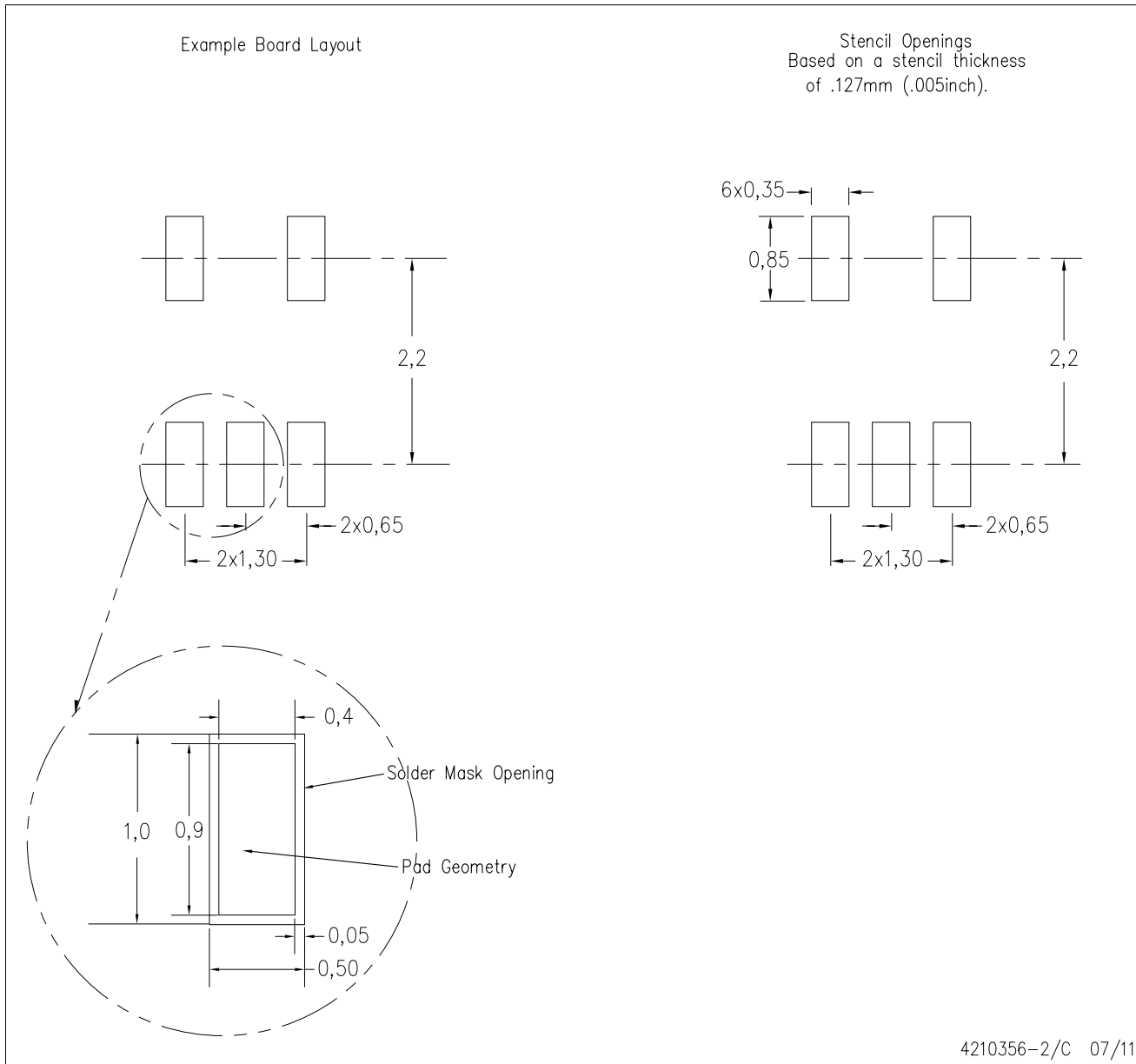
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
  - D. Falls within JEDEC MO-203 variation AA.

DCK (R-PDSO-G5)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

## GENERIC PACKAGE VIEW

**DRY 6**

**USON - 0.6 mm max height**

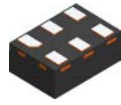
PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4207181/G

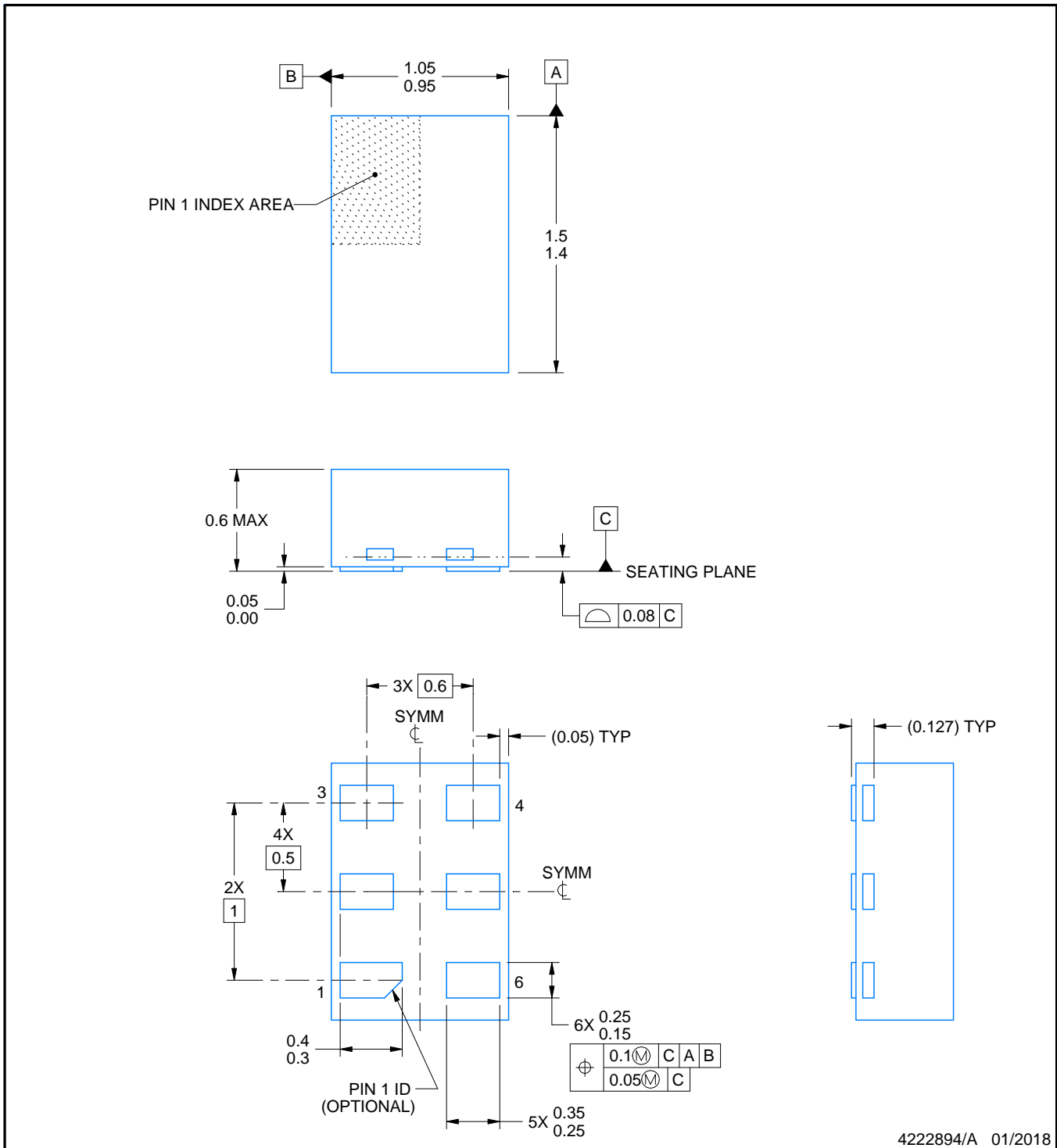
# DRY0006A



# PACKAGE OUTLINE

USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



4222894/A 01/2018

## NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

# EXAMPLE BOARD LAYOUT

DRY0006A

USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



**LAND PATTERN EXAMPLE**  
1:1 RATIO WITH PKG SOLDER PADS  
EXPOSED METAL SHOWN  
SCALE:40X



**SOLDER MASK DETAILS**

4222894/A 01/2018

NOTES: (continued)

3. For more information, see QFN/SON PCB application report in literature No. SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).



# EXAMPLE STENCIL DESIGN

DRY0006A

USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.075 - 0.1 mm THICK STENCIL  
SCALE:40X

4222894/A 01/2018

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale (<https://www.ti.com/legal/termsofsale.html>) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2021, Texas Instruments Incorporated