DS90UA101-Q1 Multi-Channel Digital Audio Link

Check for Samples: DS90UA101-Q1

FEATURES

- **Digital Audio Serializer**
- **Flexible Digital Audio Inputs, supporting I^2S (Stereo) or TDM (Multi-Channel) Formats**
- **Coaxial or Single Differential Pair Interconnect**
- **High Speed Serial Output Interface**
- **Very Low Latency (<15µs)**
- **Bidirectional Control Interface Channel with I^2C-Compatible Serial Control Bus**
- **Supports up to 8 Stereo I^2S or TDM Audio Inputs**
- **Supports Audio System Clocks from 10MHz to 50MHz**
- **Single 1.8V Supply**
- **1.8V or 3.3V I/O Interface**
- **4/4 Dedicated General Purpose Inputs/Outputs**
- **AC-Coupled STP or Coaxial Cable up to 15m**
- **DC-Balanced & Scrambled Data w/ Embedded Clock**
- **Automotive Grade Product: AEC-Q100 Grade 2 Qualified**
- **Temperature Range: -40°C to 105°C**
- **ISO 10605 and IEC 61000-4-2 ESD Compliant**

APPLICATIONS

- **Automotive Infotainment Systems**
- **Active Noise Cancellation Systems**
- **Distributed Multi-Channel Audio Systems**

DESCRIPTION

The DS90UA101-Q1 Serializer, in conjunction with the DS90UA102-Q1 Deserializer, provides a solution for distribution of digital audio in multi-channel audio systems. It transmits a high-speed serialized interface with an embedded clock over a single shielded twisted pair or coaxial cable. The serial bus scheme supports high speed forward data transmission and low speed bidirectional control channel over the link. Consolidation of digital audio, general-purpose IO, and control signals over a single differential pair reduces the interconnect size and weight, while also reducing design challenges related to skew and system latency.

The DS90UA101-Q1 Serializer embeds the clock and level shifts the signals to high-speed low-voltage differential signaling. The device serializes up to eight digital audio data inputs, word/frame sync, bit clock, and system clock.

Four dedicated general purpose input pins and four general purpose output pins allow flexible implementation of control and interrupt signals to and from remote devices.

Applications Diagrams

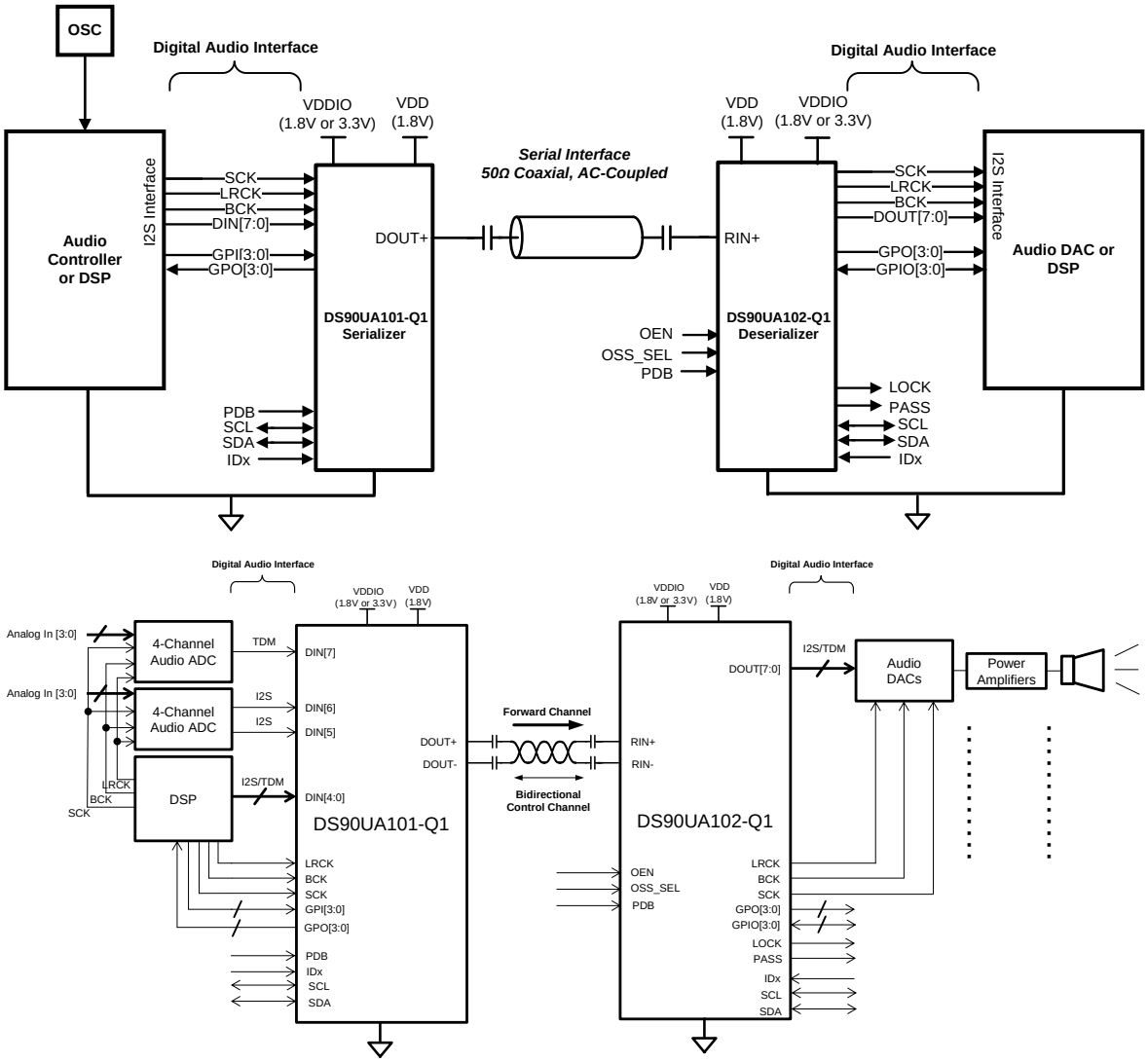


Figure 1. Applications Diagrams

Block Diagram

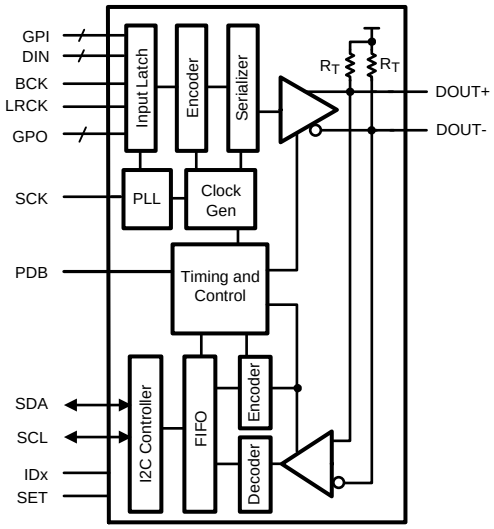


Figure 2. Block Diagram

DS90UA101-Q1 Pin Diagram

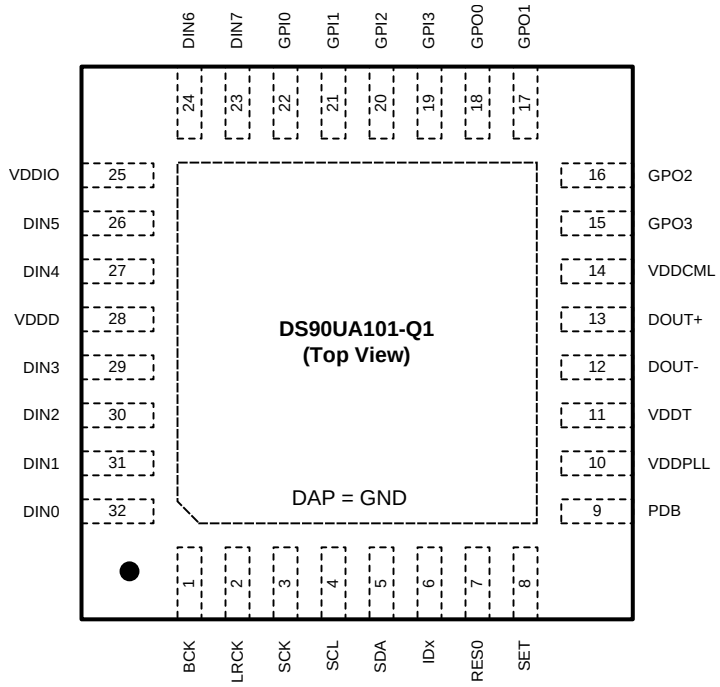


Figure 3. DS90UA101-Q1 — Top View

Pin Descriptions

Pin Name	Pin #	I/O, Type	Description
Digital Audio Interface			
SCK	3	Input, LVCMOS w/ pull down	System clock input. Forward channel audio data is clocked from this pin.
LRCK	2	Input, LVCMOS w/ pull down	Word clock input.
BCK	1	Input, LVCMOS w/ pull down	Bit clock input.
DIN[7:0]	23, 24, 26, 27, 29, 30, 31, 32	Inputs, LVCMOS w/ pull down	Digital audio data inputs. Each input can be in I^2S, TDM, LJ, or RJ format.
LVCMOS Parallel Interface			
GPI[3:0]	19, 20, 21, 22	Inputs, LVCMOS w/ pull down	General purpose inputs.
GPO[3:0]	15, 16, 17, 18	Outputs, LVCMOS	General purpose outputs.
Control and Configuration			
SCL	4	Input/Output, Open Drain	I^2C clock line. Must have an external pull-up to V_{DDIO}. DO NOT FLOAT. Recommended pull-up: 4.7 kΩ.
SDA	5	Input/Output, Open Drain	I^2C data input/output line. Must have an external pull-up to V_{DDIO}. DO NOT FLOAT. Recommended pull-up: 4.7 kΩ.
IDx	6	Input, Analog	Device I^2C address select. The IDx pin on the Serializer is used to assign its I^2C device address. See Table 2. DO NOT FLOAT.
SET	8	Input, Analog	Device SET. Connect to external 10 kΩ pull-up to 1.8V rail and 100kΩ pull-down to GND. DO NOT FLOAT.

Pin Name	Pin #	I/O, Type	Description
PDB	9	Input, LVCMOS w/ pull down	Power down mode input pin. PDB = H, device is enabled and is ON. PDB = L, device is powered down. When the device is in the powered down state, the transmitter outputs are both HIGH, the PLL is shutdown, and IDD is minimized. Control registers are RESET.
Serial Interface			
DOUT+	13	Input/Output, LVDS	True serial interface output. The interconnection must be AC-coupled to this pin with a 0.1 µF capacitor.
DOUT-	12	Input/Output, LVDS	Inverting serial interface output. The interconnection must be AC-coupled to this pin with a 0.1 µF capacitor.
Power and Ground			
VDDPLL	10	Power	1.8V (±5%) PLL power.
VDDT	11	Power	1.8V (±5%) analog core power.
VDDCML	14	Power	1.8V (±5%) CML driver power.
VDDIO	25	Power	LVCMOS I/O power. 1.8V (±5%) or 3.3V (±10%).
VDDD	28	Power	1.8V (±5%) digital power.
GND	DAP	Ground	DAP is the large metal contact located at the bottom center of the LLP package. Connect to the GND plane with at least 9 vias.
Other			
RES0	7	Reserved	Reserved. Connect to GND.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS(1)

Supply Voltage – V_{DDn} (1.8V)	−0.3V to +2.5V
Supply Voltage – V_{DDIO}	−0.3V to +4.0V
LVCMOS I/O Voltage	−0.3V to + (V_{DDIO} + 0.3V)
CML Driver I/O Voltage (V_{DDCML})	−0.3V to +(V_{DDCML} + 0.3V)
Junction Temperature	+150°C
Storage Temperature	−65°C to +150°C
Maximum Package Power Dissipation Capacity	1/θ_{JA} °C/W above +25°
Package Derating: DS90UA101-Q1 32L WQFN	
θ_{JA}*(based on 16 thermal vias)*	38.4°C/W
θ_{JC}*(based on 16 thermal vias)*	6.9°C/W
ESD Rating (IEC 61000-4-2)	R_D = 330Ω, C_S = 150pF
Air Discharge (DOUT+, DOUT-)	≥±25 kV
Contact Discharge (DOUT+, DOUT-)	≥±7 kV
ESD Rating (ISO10605)	R_D = 330Ω, C_S = 150/330pF
ESD Rating (ISO10605)	R_D = 2KΩ, C_S = 150/330pF
Air Discharge (DOUT+, DOUT–)	≥±15 kV
Contact Discharge (DOUT+, DOUT-)	≥±8 kV
ESD Rating (HBM)	≥±8 kV
ESD Rating (CDM)	≥±1 kV
ESD Rating (MM)	≥±250 V

For soldering specifications: see product folder at www.ti.com and www.ti.com/lit/an/snoa549c/snoa549c.pdf

(1) "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional; the device should not be operated beyond such conditions.

RECOMMENDED OPERATING CONDITIONS

	Min	Nom	Max	Units
Supply Voltage (V_{DDn})	1.71	1.8	1.89	V
LVCMOS Supply Voltage (V_{DDIO}) OR	1.71	1.8	1.89	V
LVCMOS Supply Voltage (V_{DDIO})	3.0	3.3	3.6	V
Supply Noise(1)				
V_{DDn} (1.8V)			25	mVp-p
V_{DDIO} (1.8V)			25	mVp-p
V_{DDIO} (3.3V)			50	mVp-p
Operating Free Air Temperature (T_A)	–40	+25	+105	°C
SCK Clock Frequency (STP Cable)	10		50	MHz
SCK Clock Frequency (Coaxial Cable)	25		50	MHz

(1) Supply noise testing was done with minimum capacitors (as shown on Figure 32 and Figure 33 on the PCB. A sinusoidal signal is AC coupled to the V_{DDn} (1.8V) supply with amplitude = 25 mVp-p measured at the device V_{DDn} pins. Bit error rate testing of input to the Ser and output of the Des with 10 meter cable shows no error when the noise frequency on the Ser is less than 1 MHz. The Des on the other hand shows no error when the noise frequency is less than 750 kHz.

ELECTRICAL CHARACTERISTICS

Over recommended operating supply and temperature ranges unless otherwise specified. (1)(2)(3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
LVCMOS DC SPECIFICATIONS 3.3V I/O (SER INPUTS, GPI, GPO, CONTROL INPUTS AND OUTPUTS)							
V_{IH}	High Level Input Voltage	V_{IN} = 3.0V to 3.6V		2.0		V_{IN}	V
V_{IL}	Low Level Input Voltage	V_{IN} = 3.0V to 3.6V		GND		0.8	V
I_{IN}	Input Current	V_{IN} = 0V or 3.6V V_{IN} = 3.0V to 3.6V		-20	±1	+20	µA
V_{OH}	High Level Output Voltage	V_{DDIO} = 3.0V to 3.6V I_{OH} = −4 mA		2.4		V_{DDIO}	V
V_{OL}	Low Level Output Voltage	V_{DDIO} = 3.0V to 3.6V I_{OL} = +4 mA		GND		0.4	V
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V	Serializer GPO Outputs		-15		mA
I_{OZ}	TRI-STATE Output Current	PDB = 0V, V_{OUT} = 0V or V_{DD}	LVCMOS Outputs	-20		+20	µA
LVCMOS DC SPECIFICATIONS 1.8V I/O (SER INPUTS, GPI, GPO, CONTROL INPUTS AND OUTPUTS)							
V_{IH}	High Level Input Voltage	V_{IN} = 1.71V to 1.89V		0.65 V_{IN}		V_{IN}	V
V_{IL}	Low Level Input Voltage	V_{IN} = 1.71V to 1.89V		GND		0.35 V_{IN}	
I_{IN}	Input Current	V_{IN} = 0V or 1.89V V_{IN} = 1.71V to 1.89V		-20	±1	+20	µA
V_{OH}	High Level Output Voltage	V_{DDIO} = 1.71V to 1.89V I_{OH} = −4 mA		V_{DDIO} - 0.45		V_{DDIO}	V
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V	Serializer GPO Outputs		-11		mA
I_{OZ}	TRI-STATE Output Current	PDB = 0V, V_{OUT} = 0V or V_{DD}	LVCMOS Outputs	-20		+20	µA
CML DRIVER DC SPECIFICATIONS (DOUT+, DOUT-)							
$\|V_{OD}\|$	Output Differential Voltage	R_L = 100Ω (Figure 8)		268	340	412	mV
ΔV_{OD}	Output Differential Voltage Unbalance	R_L = 100Ω			1	50	mV
V_{OS}	Output Differential Offset Voltage	R_L = 100Ω (Figure 8)			V_{DD} - $V_{OD/2}$		V
ΔV_{OS}	Offset Voltage Unbalance	R_L = 100Ω			1	50	mV
I_{OS}	Output Short Circuit Current	DOUT± = 0V			-26		mA
R_T	Differential Internal Termination Resistance	Differential across DOUT+ and DOUT-		80	100	120	Ω
	Single-ended Termination Resistance	DOUT+ or DOUT–		40	50	60	

(1) The Electrical Characteristics tables list verified specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not verified.
(2) Current into device pins is defined as positive. Current out of a device pin is defined as negative. Voltages are referenced to ground except V_{OD}, ΔV_{OD}, V_{TH} and V_{TL} which are differential voltages.
(3) Typical values represent most likely parametric norms at 1.8V or 3.3V, T_A = +25°C, and at the Recommended Operation Conditions at the time of product characterization and are not verified.

ELECTRICAL CHARACTERISTICS (continued)

Over recommended operating supply and temperature ranges unless otherwise specified.[1][2][3]

Symbol	Parameter	Conditions		Min	Typ	Max	Units
SUPPLY CURRENT, DIGITAL, PLL, AND ANALOG VDD							
I_{DDIOT}	Serializer (Tx) V_{DDIO} Supply Current (includes load current)	R_L = 100Ω WORST CASE Pattern (Figure 5)	V_{DDIO} = 1.89V f = 50 MHz Default Registers		1.5	3	mA
			V_{DDIO} = 3.6V f = 50 MHz Default Registers		5	8	
		R_L = 100Ω Random Pattern	V_{DDIO} = 1.8V f = 24.576 MHz Default Registers		1.5		
			V_{DDIO} 1.8V f = 12.288 MHz Default Registers		1.5		
			V_{DDIO} = 3.3V f = 24.576 MHz Default Registers		5		
			V_{DDIO} = 3.3V *f* = 12.288 MHz Default Registers		5		
I_{DDT}	Serializer (Tx) V_{DDn} Core Supply Current	R_L = 100Ω WORST CASE Pattern (Figure 5)	V_{DDn} = 1.89V, V_{DDIO} = 3.6V f = 50 MHz Default Registers		61	80	mA
		R_L = 100Ω Random Pattern	V_{DDn} = 1.8V, V_{DDIO} = 3.3V f = 24.576 MHz Default Registers		51		
			V_{DDn} = 1.8V, V_{DDIO} = 3.3V f = 12.288 MHz Default Registers		49		
I_{DDTZ}	Serializer (Tx) Supply Current Power-down	PDB = 0V; All other LVCMOS Inputs = 0V	V_{DDIO} = 1.89V Default Registers		300	1000	µA
			V_{DDIO} = 3.6V Default Registers		300	1000	µA
I_{DDIOTZ}	Serializer (Tx) V_{DDIO} Supply Current Power-down	PDB = 0V; All other LVCMOS Inputs = 0V	V_{DDIO} = 1.89V Default Registers		15	100	µA
			V_{DDIO} = 3.6V Default Registers		15	100	µA

ELECTRICAL CHARACTERISTICS: Recommended Timing for SCK

Over recommended operating supply and temperature ranges unless otherwise specified. (1)(2)(3)(4)

Symbol	Parameter	Conditions	Pin	Min	Typ	Max	Units
t_{TCP}	Transmit Clock Period	STP Cable	SCK	20	T	100	ns
		Coaxial Cable	SCK	20	T	40	
t_{TCIH}	Transmit Clock Input High Time	f = 10 MHz – 50 MHz	SCK	0.4	0.5	0.6	T
t_{TCIL}	Transmit Clock Input Low Time	f = 10 MHz – 50 MHz	SCK	0.4	0.5	0.6	T
t_{CLKT}	SCK Input Transition Time (Figure 9)	f = 10 MHz – 50 MHz	SCK	0.05	0.25	0.3	T
t_{JIT0}	SCK Input Jitter	Refer to Jitter freq>f/40, f = 10 MHz – 50 MHz	SCK		0.1		T

(1) The Electrical Characteristics tables list verified specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not verified.
(2) Current into device pins is defined as positive. Current out of a device pin is defined as negative. Voltages are referenced to ground except V_{OD}, ΔV_{OD}, V_{TH} and V_{TL} which are differential voltages.
(3) Typical values represent most likely parametric norms at 1.8V or 3.3V, T_A = +25°C, and at the Recommended Operation Conditions at the time of product characterization and are not verified.
(4) Recommended Input Timing Requirements are input specifications and not tested in production.

ELECTRICAL CHARACTERISTICS: Serializer Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified. (1)(2)(3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{LHT}	CML Low-to-High Transition Time	R_L = 100Ω (Figure 6)		150	330	ps
t_{HLT}	CML High-to-Low Transition Time	R_L = 100Ω (Figure 6)		150	330	ps
t_{DIS}	Data Input Setup to SCK	Serializer Data Inputs (Figure 10)	2			ns
t_{DIH}	Data Input Hold from SCK		2			ns
t_{PLD}	Serializer PLL Lock Time	R_L = 100Ω (4) (5), (Figure 11)		1	2	ms
t_{SD}	Serializer Delay (5)	R_T = 100Ω Register 0x03h b[0] (TRFB = 1) (Figure 12)	11.75T	13T	15T	ns
t_{JIND}	Serializer Output Deterministic Jitter	Serializer output intrinsic deterministic jitter . Measured (cycle-cycle) with PRBS-7 test pattern (3) (6)		0.13		UI
t_{JINR}	Serializer Output Random Jitter	Serializer output intrinsic random jitter (cycle-cycle). Alternating-1,0 pattern. (3) (6)		0.04		UI
t_{JINT}	Peak-to-peak Serializer Output Jitter	Serializer output peak-to-peak jitter includes deterministic jitter, random jitter, and jitter transfer from Serializer input. Measured (cycle-cycle) with PRBS-7 test pattern. (3) (6)		0.396		UI
λ_{STXBW}	Serializer Jitter Transfer Function -3 dB Bandwidth (7)	SCK = 50MHz		2.2		MHz
δ_{STX}	Serializer Jitter Transfer Function (Peaking) (7)	SCK = 50MHz		1.16		dB
δ_{STXf}	Serializer Jitter Transfer Function (Peaking Frequency) (7)	SCK = 50MHz		600		kHz

(1) The Electrical Characteristics tables list verified specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not verified.
(2) Current into device pins is defined as positive. Current out of a device pin is defined as negative. Voltages are referenced to ground except V_{OD}, ΔV_{OD}, V_{TH} and V_{TL} which are differential voltages.
(3) Typical values represent most likely parametric norms at 1.8V or 3.3V, T_A = +25°C, and at the Recommended Operation Conditions at the time of product characterization and are not verified.
(4) t_{PLD} and t_{DDLT} is the time required by the Serializer and Deserializer to obtain lock when exiting power-down state with an active SCK.
(5) Specification is verified by design.
(6) UI – Unit Interval is equivalent to one ideal serialized data bit width. The UI scales with SCK frequency.
(7) Specification is by characterization and is not tested in production.

BIDIRECTIONAL CONTROL BUS TIMING SPECIFICATIONS

Bidirectional Control Bus: AC Timing Specifications (SCL, SDA) - I²C Compliant

Over recommended supply and temperature ranges unless otherwise specified. (Figure 4)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Recommended Input Timing Requirements						
f_{SCL}	SCL Clock Frequency	Standard Mode			100	kHz
		Fast Mode			400	kHz
t_{LOW}	SCL Low Period	Standard Mode	4.7			µs
		Fast Mode	1.3			µs
t_{HIGH}	SCL High Period	Standard Mode	4.0			µs
		Fast Mode	0.6			µs
$t_{HD:STA}$	Hold time for a start or a repeated start condition	Standard Mode	4.0			µs
		Fast Mode	0.6			µs
$t_{SU:STA}$	Set Up time for a start or a repeated start condition	Standard Mode	4.7			µs
		Fast Mode	0.6			µs
$t_{HD:DAT}$	Data Hold Time	Standard Mode	0		3.45	µs
		Fast Mode	0		900	ns
$t_{SU:DAT}$	Data Set Up Time	Standard Mode	250			ns
		Fast Mode	100			ns
$t_{SU:STO}$	Set Up Time for STOP Condition	Standard Mode	4.0			µs
		Fast Mode	0.6			µs
t_{BUF}	Bus Free time between Stop and Start	Standard Mode	4.7			µs
		Fast Mode	1.3			µs
t_r	SCL & SDA Rise Time	Standard Mode			1000	ns
		Fast Mode			300	ns
t_f	SCL & SDA Fall Time	Standard Mode			300	ns
		Fast Mode			300	ns

Bidirectional Control Bus: DC Timing Specifications (SCL, SDA) - I²C Compliant(1)

Over recommended supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Recommended Input Timing Requirements						
V_{IH}	Input High Level	SDA and SCL	0.7*V_{DDIO}		V_{DDIO}	V
V_{IL}	Input Low Level	SDA and SCL	GND		0.3*V_{DDIO}	V
V_{HY}	Input Hysteresis			>50		mV
V_{OL}	Output Low Level	SDA, I_{OL}=0.5mA	0		0.4	V
I_{IN}	Input Current	SDA or SCL, V_{IN}=V_{DDIO} OR GND	-10		10	µA
t_R	SDA Rise Time-READ	SDA, RPU = 10kΩ, Cb ≤ 400pF(Figure 4)		430		ns
t_F	SDA Fall Time-READ			20		ns
$t_{SU;DAT}$		(Figure 4)		560		ns
$t_{HD;DAT}$		(Figure 4)		615		ns
t_{SP}				50		ns
C_{IN}		SDA or SCL		<5		pF

(1) Specification is verified by design.

TIMING AND CIRCUIT DIAGRAMS

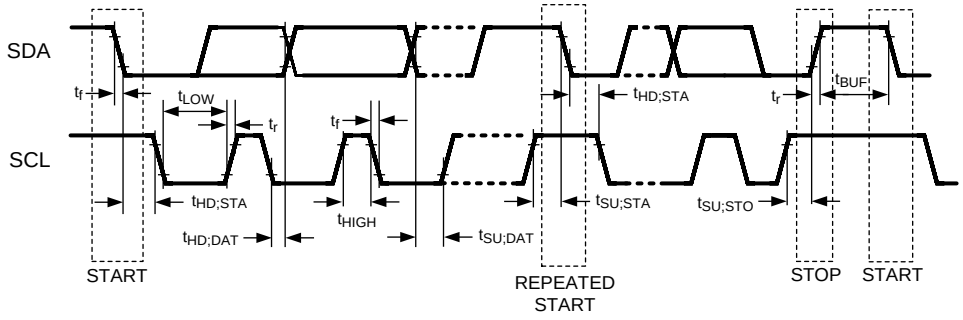


Figure 4. Bidirectional Control Bus Timing

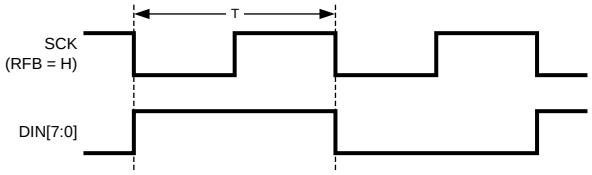


Figure 5. "Worst Case" Test Pattern

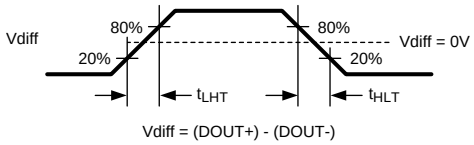


Figure 6. Serializer CML Output Transition Times

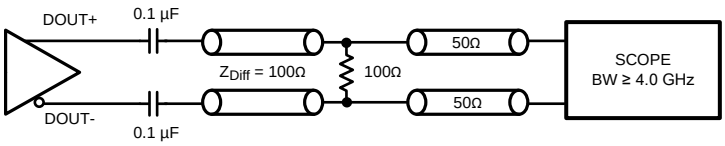


Figure 7. Serializer CML Output Load

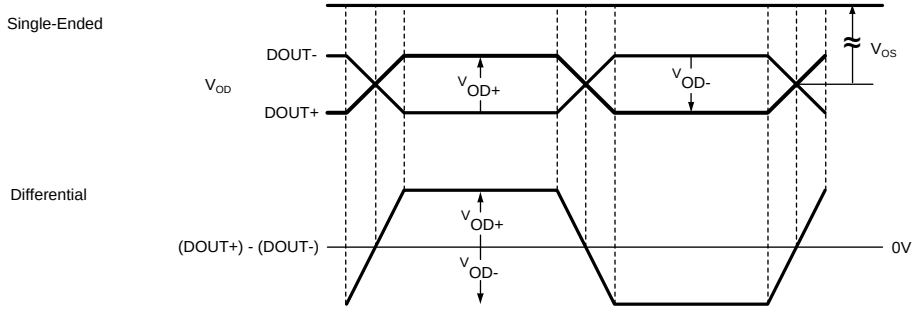


Figure 8. Serializer VOD and Differential Diagram

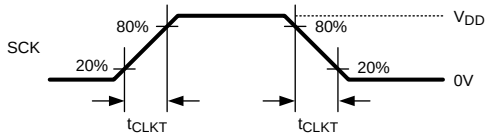


Figure 9. Serializer Input Clock Transition Times

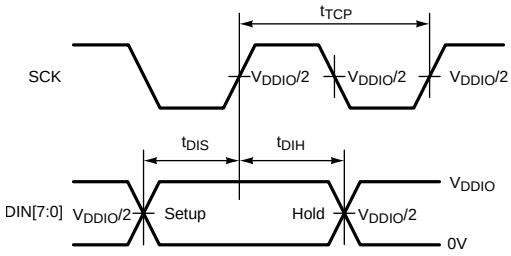


Figure 10. Serializer Setup/Hold Times

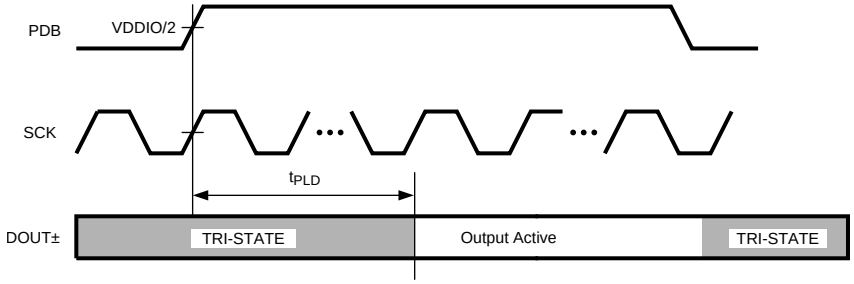


Figure 11. Serializer PLL Lock Time

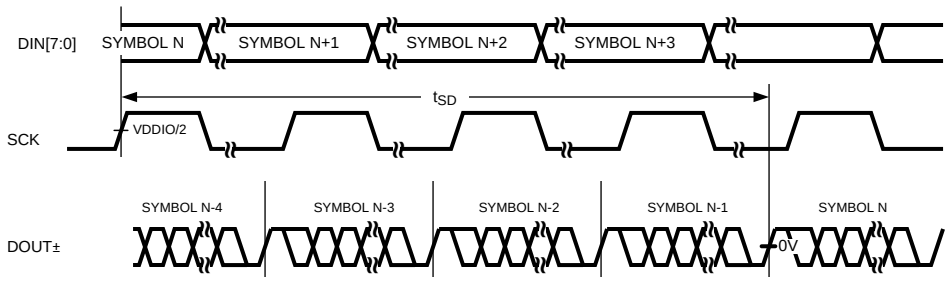


Figure 12. Serializer Delay

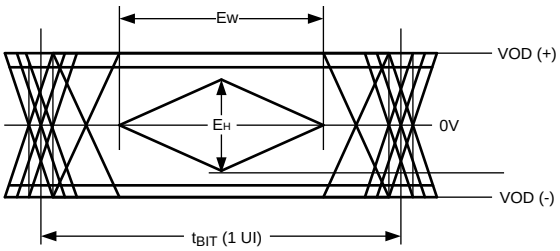


Figure 13. CML Output Driver

DS90UA101-Q1 REGISTER INFORMATION

The table below contains information on the DS90UA101-Q1 control registers. These registers are accessible locally via the I^2C control interface, or remotely via the Bidirectional Control Channel. Addresses not listed are reserved. Fields listed as reserved should not be changed from the listed default value.

Addr (Hex)	Name	Bits	Field	R/W	Default (Hex)	Description
0x00	I^2C Device ID	7:1	DEVICE ID	RW	0xB0	7-bit address of Serializer. 0x58'h (0101_100X'b) default.
		0	SER ID SEL	RW		0: Serializer DEVICE ID is from IDx. 1: Register I^2C DEVICE ID overrides IDx.
0x01	Power and Reset	7	RSVD		0x30	Reserved.
		6	RDS	RW		Digital output drive strength. 1: High drive strength. 0: Low drive strength.
		5	V_{DDIO} Control	RW		Auto voltage control. 1: Enable (auto-detect mode). 0: Disable.
		4	V_{DDIO} Mode	RW		V_{DDIO} voltage set. 1: Sets V_{DDIO} mode to 3.3V. 0: Sets V_{DDIO} mode to 1.8V.
		3	ANAPWDN	RW		This register can be set only through local I^2C access. 1: Analog power-down: Powers down the analog block in the Serializer. 0: Analog power-up: Powers up the analog block in the Serializer.
		2	RSVD			Reserved.
		1	Digital Reset 1	RW		1: Resets the digital block except for register values. This bit is self-clearing. 0: Normal operation.
		0	Digital Reset 0	RW		1: Resets the entire digital block including all register values. This bit is self-clearing. 0: Normal operation.

Addr (Hex)	Name	Bits	Field	R/W	Default (Hex)	Description
0x03	General Configuration	7	RX CRC Checker Enable	RW	0xC5	Back channel CRC Checker enable. 1:Enable. 0:Disable.
		6	TX Parity Generator Enable	RW		Forward channel Parity Generator enable. 1: Enable. 0: Disable.
		5	CRC Error Reset	RW		Clear CRC error counters. This bit is NOT self-clearing. 1: Clear counters. 0: Normal operation.
		4	I^2C Remote Write Auto Acknowledge	RW		Automatically acknowledge I^2C remote writes. This mode should only be used when the system is LOCKED. 1: Enable: When enabled, I^2C writes to the Deserializer (or any remote I^2C slave, if I^2C Pass All is enabled) are immediately acknowledged without waiting for the Deserializer to acknowledge the write. The accesses are then remapped to the address specified in 0x06. 0: Disable.
		3	I^2C Pass All	RW		Pass-through all I^2C transactions. For an explanation of I^2C pass-through, refer to I^2C Pass-Through and Multiple Device Addressing. 1: Enable pass-through of all I^2C accesses to I^2C IDs that do not match the Serializer I^2C ID. The I^2C accesses are then remapped to the address specified in register 0x06. 0: Enable pass-through only of I^2C accesses to I^2C IDs matching either the remote Deserializer I^2C ID or the remote slave I^2C ID.
		2	I^2C Pass-Through	RW		I^2C pass-through mode. 1: Pass-through enabled. Refer to I^2C Pass-Through and Multiple Device Addressing. 0: Pass-through disabled.
		1	RSVD	RW		Reserved.
		0	TRFB	RW		SCK clock edge select. 1: Parallel interface data is strobed on the rising clock edge. 0: Parallel interface data is strobed on the falling clock edge.
0x06	DES ID	7:1	Deserializer Device ID	RW		This field stores the 7-bit I^2C address of the remote Deserializer. If an I^2C transaction (originating from the Serializer side) is addressed to DES Alias, the transaction will be remapped to this address before it is passed across the Bidirectional Control Channel to the remote Deserializer. This field is automatically configured by the Bidirectional Control Channel once RX LOCK has been detected. Software may overwrite this value, but the Freeze Device ID bit should also be asserted to prevent overwriting by the Bidirectional Control Channel. A value of 0 in this field disables I^2C access to the remote Deserializer. Refer to I^2C Pass-Through and Multiple Device Addressing.
		0	Freeze Device ID	RW		Freeze Deserializer Device ID. 1: Prevents auto-loading of the Deserializer Device ID from the back channel. The ID will be frozen at the value written. 0: Allows auto-loading of the Deserializer Device ID from the back channel.

Addr (Hex)	Name	Bits	Field	R/W	Default (Hex)	Description
0x07	DES Alias	7:1	Deserializer Alias ID	RW	0x00	This field stores a 7-bit I^2C address. Once set, it configures the Serializer to accept any transaction designated for the I^2C address stored in this field. The transaction will then be remapped to the I^2C address specified in the DES ID register. A value of 0 in this field disables I^2C access to the remote Deserializer. Refer to I^2C Pass-Through and Multiple Device Addressing.
		0	RSVD			Reserved.
0x08	Slave ID	7:1	Slave ID	RW	0x00	This field stores the 7-bit I^2C address of the remote slave attached to the remote Deserializer. If an I^2C transaction (originating from the Serializer side) is addressed to Slave Alias, the transaction will be remapped to this address before it is passed across the Bidirectional Control Channel to the remote Deserializer, where it is then passed to the remote slave. A value of 0 in this field disables I^2C access to the remote slave. Refer to I^2C Pass-Through and Multiple Device Addressing.
		0	RSVD			Reserved.
0x09	Slave Alias	7:1	Slave Alias ID	RW	0x00	This field stores a 7-bit I^2C address. Once set, it configures the Serializer to accept any transaction designated for the I^2C address stored in this field. The transaction will then be remapped to the I^2C address specified in the Slave ID register. A value of 0 in this field disables I^2C access to the remote slave. Refer to I^2C Pass-Through and Multiple Device Addressing.
		0	RSVD			Reserved.
0x0A	CRC Errors	7:0	CRC Error Byte 0	R	0x00	Number of back-channel CRC errors during normal operation. Least significant byte.
0x0B	CRC Errors	7:0	CRC Error Byte 1	R	0x00	Number of back-channel CRC errors during normal operation. Most significant byte.
0x0C	General Status	7:5	Rev-ID	R		Revision ID. 0x00: Production.
		4	RX Lock Detect	R		1: RX LOCKED. 0: RX not LOCKED.
		3	BIST CRC Error Status	R		1: CRC errors in BIST mode. 0: No CRC errors in BIST mode.
		2	SCK Detect	R		1: Valid SCK detected. 0: Valid SCK not detected.
		1	DES Error	R		1: CRC error is detected during communication with the Deserializer. This bit is cleared upon loss of link or assertion of CRC Error Reset bit in register 0x03[5]. 0: No errors detected.
		0	Link Detect	R		1: Cable link detected. 0: Cable link not detected. This includes any of the following faults: — Cable open. — '+' and '-' shorted. — Short to GND. — Short to battery.

Addr (Hex)	Name	Bits	Field	R/W	Default (Hex)	Description
0x0D	GPO3 and GPO2 Configuration	7	GPO2 Output Value	RW	0x55	Local GPO2 Output Value. This value is output on the GPO2 pin when GPO2 is enabled, the local GPO2 direction is set to output, and remote GPO2 control is disabled.
		6	GPO2 Remote Enable	RW		Remote GPO2 control: 1: Enable GPO2 control from the remote Deserializer. The GPO2 pin needs to be an output, and the value is received from the remote Deserializer. 0: Disable GPO2 control from the remote Deserializer.
		5	GPO2 Direction	RW		Local GPO2 direction: 1: Input. 0: Output.
		4	GPO2 Enable	RW		GPO2 enable: 1: Enable GPO2 operation. 0: TRI-STATE.
		3	GPO3 Output Value	RW		Local GPO3 Output Value. This value is output on the GPO3 pin when GPO3 is enabled, the local GPO3 direction is set to output, and remote GPO3 control is disabled.
		2	GPO3 Remote Enable	RW		Remote GPO3 control: 1: Enable GPO3 control from the remote Deserializer. The GPO3 pin needs to be an output, and the value is received from the remote Deserializer. 0: Disable GPO3 control from the remote Deserializer.
		1	GPO3 Direction	RW		Local GPO3 direction: 1: Input. 0: Output.
		0	GPO3 Enable	RW		GPO3 enable: 1: Enable GPO3 operation. 0: TRI-STATE.
0x0E	GPO1 and GPO0 Configuration	7	GPO0 Output Value	RW	0x35	Local GPO0 Output Value. This value is output on the GPO0 pin when GPO0 is enabled, the local GPO0 direction is set to output, and remote GPO0 control is disabled.
		6	GPO0 Remote Enable	RW		Remote GPO0 control: 1: Enable GPO0 control from the remote Deserializer. The GPO0 pin needs to be an output, and the value is received from the remote Deserializer. 0: Disable GPO0 control from the remote Deserializer.
		5	GPO0 Direction	RW		Local GPO0 direction: 1: Input. 0: Output.
		4	GPO0 Enable	RW		GPO0 enable: 1: Enable GPO0 operation. 0: TRI-STATE.
		3	GPO1 Output Value	RW		Local GPO1 Output Value. This value is output on the GPO1 pin when GPO1 is enabled, the local GPO1 direction is set to output, and remote GPO1 control is disabled.
		2	GPO1 Remote Enable	RW		Remote GPO1 control: 1: Enable GPO1 control from the remote Deserializer. The GPO1 pin needs to be an output, and the value is received from the remote Deserializer. 0: Disable GPO1 control from the remote Deserializer.
		1	GPO1 Direction	RW		Local GPO1 direction: 1: Input. 0: Output.
		0	GPO1 Enable	RW		GPO1 enable: 1: Enable GPO1 operation. 0: TRI-STATE.

Addr (Hex)	Name	Bits	Field	R/W	Default (Hex)	Description
0x0F	I²C Master Config	7:5	RSVD		0x00	Reserved.
		4:3	SDA Output Delay	RW		SDA output delay. This field configures the output delay on the SDA output. Setting this value will increase the output delay in units of 50ns. Nominal output delay values for SCL to SDA are: 00: 350 ns 01: 400 ns 10: 450 ns 11: 500 ns
		2	Local Write Disable	RW		Disable remote writes to local registers. Setting this bit to 1 will prevent remote writes to local device registers from across the control channel. This prevents writes to the Serializer registers from an I²C Master attached to the Deserializer. Setting this bit does not affect remote access to I²C slaves at the Serializer.
		1	I²C Bus Timer Speed Up	RW		Speed up I²C bus Watchdog Timer. 1: Watchdog Timer expires after approximately 50 microseconds. 0: Watchdog Timer expires after approximately 1 second.
		0	I²C Bus Timer Disable	RW		The I²C Watchdog Timer may be used to detect when the I²C bus is free or hung up following an invalid termination of a transaction. If SDA is high and no signaling occurs for approximately 1 second, the I²C bus is assumed to be free. If SDA is low and no signaling occurs, the device will attempt to clear the bus by driving 9 clocks on SCL. 1. Disable the I²C bus Watchdog Timer. 0: Enable the I²C bus Watchdog Timer.
0x10	I²C Control	7	RSVD		0x17	Reserved.
		6:4	I²C SDA Hold Time	RW		Internal SDA hold time. This field configures the amount of internal hold time provided for the SDA input relative to the SCL input. Units are 50ns.
		3:0	I²C Filter Depth	RW		I²C glitch filter depth. This field configures the maximum width of glitch pulses on the SCL and SDA inputs that will be rejected. Units are 10 ns.
0x11	SCL High Time	7:0	SCL High Time	RW	0x82	I²C Master SCL high time. This field configures the high pulse width of the SCL output when the Serializer is the Master on the local I²C bus. Units are 50 ns for the nominal oscillator clock frequency. The default value is set to satisfy a minimum (4µs + 1µs of rise time for cases where rise time is very fast) SCL high time with the internal oscillator clock running at 26 MHz rather than the nominal 20MHz.
0x12	SCL Low Time	7:0	SCL Low Time	RW	0x82	I²C Master SCL low time. This field configures the low pulse width of the SCL output when the Serializer is the Master on the local I²C bus. This value is also used as the SDA setup time by the I²C slave for providing data prior to releasing SCL during accesses over the Bidirectional Control Channel. Units are 50 ns for the nominal oscillator clock frequency. The default value is set to satisfy a minimum (4.7µs + 0.3µs of fall time for cases where fall time is very fast) SCL low time with the internal oscillator clock running at 26 MHz rather than the nominal 20MHz.
0x13	General Purpose Control	7:0	GPCR[7:0]	RW	0x00	Scratch register. Used to write and read 8 bits.
0x14	BIST Control	7:3	RSVD		0x00	Reserved.
		2:1	Clock Source	RW		Allows the choosing of different internal oscillator clock frequencies for forward channel frame. The internal oscillator clock frequency is used when SCK is idle or missing. See Table 1 for these settings.
		0	RSVD	RW		Reserved.

Addr (Hex)	Name	Bits	Field	R/W	Default (Hex)	Description
0x1E	BCC Watchdog Control	7:1	BCC Watchdog Timer	RW	0xFE	The BCC Watchdog Timer allows termination of a control channel transaction if it fails to complete within a programmed amount of time. This field sets the Bidirectional Control Channel Watchdog timeout value in units of 2ms. This field should not be set to 0.
		0	BCC Watchdog Timer Disable	RW		Bidirectional Control Channel Watchdog Timer enable. 1: Disables BCC Watchdog Timer operation. 0: Enables BCC Watchdog Timer operation.
0x2A	CRC Errors	7:0	BIST Mode CRC Errors Count	R	0x00	Number of CRC errors in the back channel when in BIST mode.

FUNCTIONAL DESCRIPTION

The DS90UA101-Q1/DS90UA102-Q1 chipset is intended to link digital audio sources with remote audio converters and DSPs. The chipset can operate from a reference clock of 10 MHz to 50 MHz. The DS90UA101-Q1 device serializes up to 8 audio inputs and 4 general purpose inputs, along with a bidirectional control channel, into a single high-speed differential pair or single-ended coaxial cable. The high-speed serial bit stream contains an embedded clock and DC-balanced information to enhance signal quality and support AC coupling. The DS90UA102-Q1 device receives the single serial data stream and converts it back to digital audio outputs, control channel data, and general purpose outputs (GPOs). The DS90UA101-Q1/DS90UA102-Q1 chipset can accept up to 8 audio data inputs, bit clock (BCK), word clock (LRCK), and an input reference clock (SCK) ranging from 10 MHz to 50 MHz.

The control channel function of the chipset provides bidirectional communication between the two ends of the link, such as a digital signal processor (DSP) on one end and an audio digital-analog converter (DAC) on the other. The integrated Bidirectional Control Channel transfers data bidirectionally over the same differential pair used for audio data interface. This interface offers advantages over other chipsets by eliminating the need for additional wires for programming and control. The Bidirectional Control Channel bus is controlled via an I^2C port, available on both the Serializer and Deserializer.

Transmission Media

The DS90UA101-Q1/DS90UA102-Q1 chipset is intended to be used in a point-to-point data link through a shielded twisted pair (STP) or coaxial (coax) cable. The Serializer and Deserializer provide internal termination to minimize impedance discontinuities. The interconnect (cable and connectors) should have a differential impedance of 100Ω, or a single-ended impedance of 50Ω. The maximum length of cable that can be used is dependent on the quality of the cable (gauge, impedance), connector, board (discontinuities, power plane), and the electrical environment (e.g power stability, ground noise, input clock jitter, SCK frequency, etc). The resulting signal quality at the receiving end of the transmission media may be assessed by monitoring the differential eye opening of the serial data stream. This can be done by measuring the output of the CMLOUTP/N pins. These pins should each be terminated with a 0.1 µF capacitor in series with a 50Ω resistor to GND. Figure 13 illustrates the minimum eye width and eye height that is necessary for bit error free operation.

Operation with Audio System Clock as Reference Clock

The DS90UA101-Q1/DS90UA102-Q1 chipset is operated using the audio system clock (SCK) from the digital audio source. The audio data, LRCK, and BCK inputs are clocked into the Serializer using SCK. Up to 4 GPI inputs are also sampled and transported along with the digital audio inputs. Figure 14 shows the operation of the Serializer and Deserializer with the reference clock.

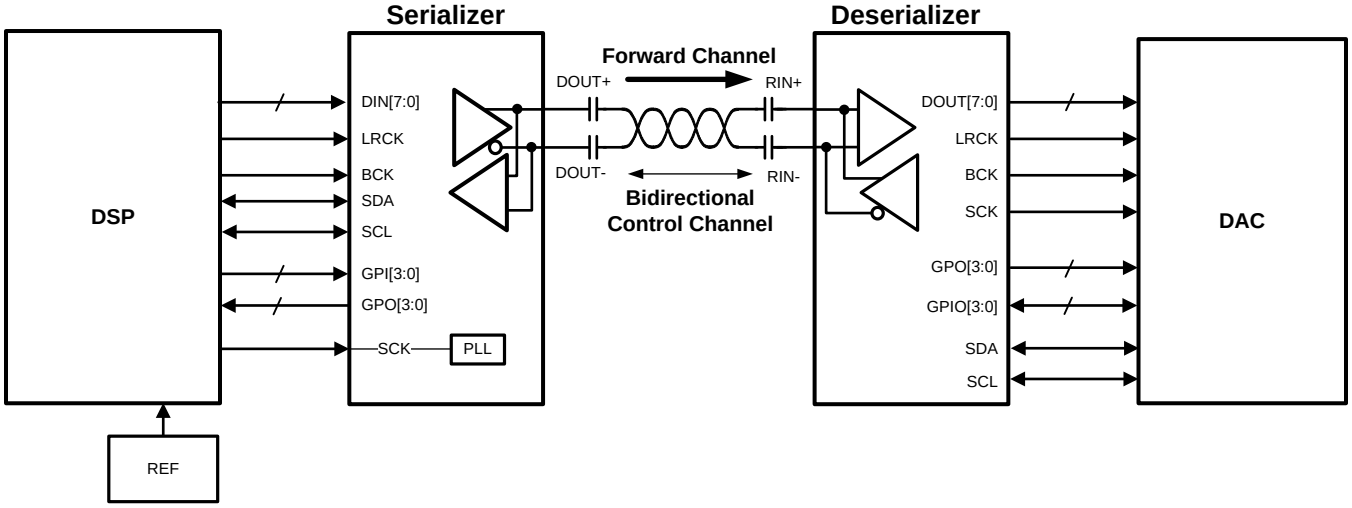


Figure 14. Operation with SCK Reference

The Serializer switches over to an internal reference clock when SCK is idle or missing. This frequency is selectable via the device control registers, as shown below (Table 1).

Table 1. Internal Oscillator Frequencies for Forward Channel Frame during Normal Operation

DS90UA101-Q1 Reg 0x14 [2:1]	Frequency (MHz)
00	~25
01	~50
10	~25
11	~12.5

SET Pin on Serializer

The SET pin on the Serializer sets the internal configuration of the part for audio sources with SCK in the range of 10 MHz to 50MHz. It requires a 10 kΩ pull-up resistor to 1.8V, and a 100 kΩ pull-down resistor to GND. The recommended resistor tolerance is 1% (Figure 15).

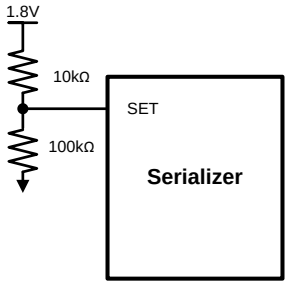


Figure 15. SET Pin configuration on DS90UA101-Q1

Line Rate Calculations for the DS90UA101-Q1/DS90UA102-Q1

The following formula is used to calculate the line rate for the DS90UA101-Q1/DS90UA102-Q1 chipset:

- Line rate = f_{SCK} * 28

Serial Frame Format

For example, for maximum line rate, f_{SCK} = 50 MHz, line rate = 50 * 28 = 1.4 Gbps.

The high-speed forward channel is composed of 28 bits of data containing digital audio data, sync signals, I^2C and parity bits. This data payload is optimized for signal transmission over an AC-coupled link. Data is randomized, balanced and scrambled. The Bidirectional Control Channel data is transferred over the single serial link along with the high-speed forward data. This architecture provides a full duplex, low-speed control path across the serial link together with the high speed forward channel.

Serial Audio Formats

There are several de-facto industry standards or formats that define the required alignments and signal polarities between the left/right clock (LRCK), bit clock (BCK), and the serial audio data. Hence, this section is dedicated to discussing various serial audio formats.

I^2S Format

An I^2S bus uses three signal lines for data transfer – a frame or word clock (LRCK), a bit clock (BCK), and a single or multiple data lines. The device which generates the appropriate BCK and LRCK signals on the bus is called Master, whereas other devices which accept BCK and LRCK as inputs are all slaves.

Bit Clock (BCK)

The bit clock pulses once for each discrete bit of data on the data lines. The bit clock frequency must be greater than or equal to the product of the sample rate, the number of bits per sample and the number of channels (which is 2 in normal stereo operation).

Word Select (LRCK)

The word select line indicates the channel being transmitted:

- LRCK = 0; channel 1 (left);
- LRCK = 1; channel 2 (right).

The LRCK line changes one clock period before the MSB is transmitted (Figure 16). This allows the slave transmitter to derive synchronous timing of the serial data that will be set up for transmission. Furthermore, it enables the receiver to store the previous word and clear the input for the next word.

Serial Data (DATA)

Serial data is transmitted in two's complement with the MSB first (as shown in Figure 16). The MSB is transmitted first because the transmitter and receiver may have different word lengths.

If the receiver is sent more bits than its word length, the bits after the LSB are ignored. On the other hand, if the receiver is sent fewer bits than its word length, the missing bits are set to zero internally. And so, the MSB has a fixed position, whereas the position of the LSB depends on the word length.

Serial data sent by the transmitter may be synchronized with either the trailing (HIGH-to-LOW) or the leading (LOW-to-HIGH) edge of the clock signal. However, the serial data must be latched into the receiver on the leading edge of the serial clock signal, and so there are some restrictions when transmitting data that is synchronized with the leading edge.

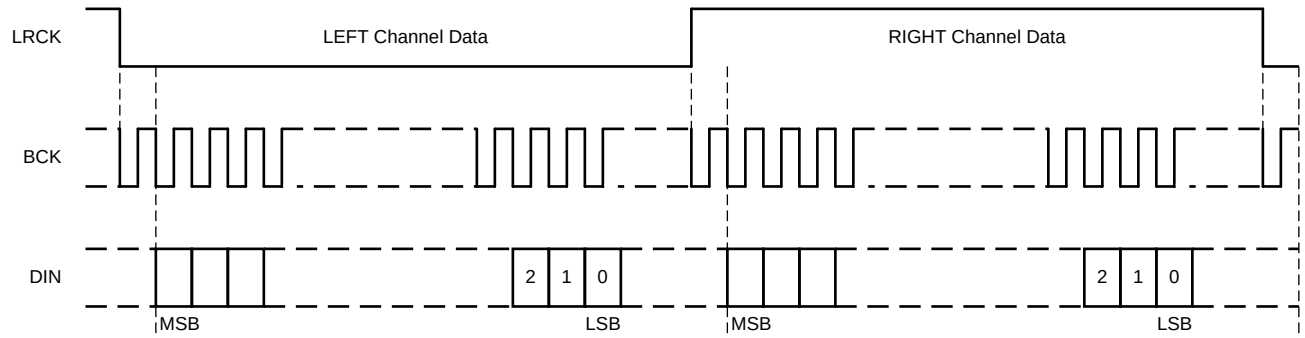


Figure 16. Stereo I²S Format

Left Justified Format

In this format, MSB of the word appears in synchronization with the LRCK edges. Unlike in I²S mode, there is no lag between Data and LRCK. Left channel data word begins at falling edge of LRCK and right channel data word begins on rising edge of the LRCK signal. Hence, as can be seen from below waveforms (Figure 17), data appears to be left justified.

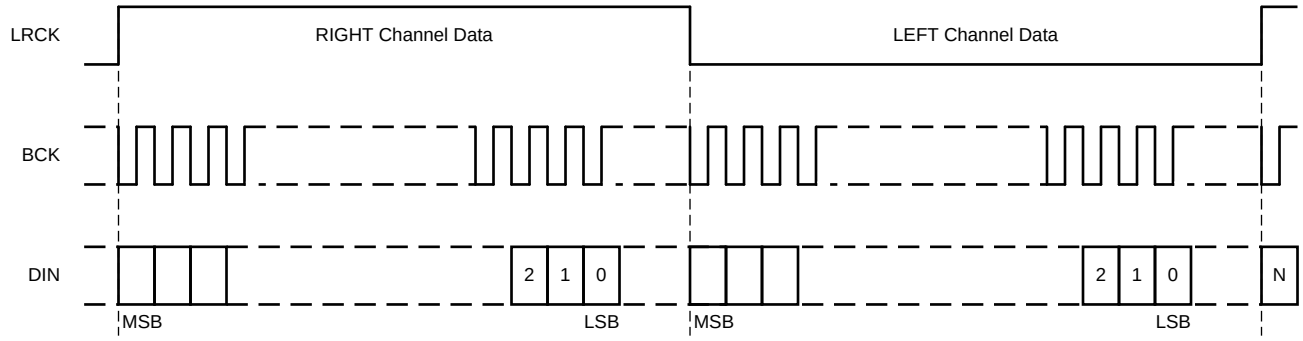


Figure 17. Left-Justified Format

Right Justified Format

In this format, LSB of the word appears just before the LRCK edges. Left channel data word may begin at any point depending upon the word length, but LSB of this data word must appear just before the rising edge of the LRCK signal. Similarly, LSB of the right channel data word must appear just before falling edge of the LRCK signal. Hence, as can be seen from below waveforms (Figure 18), data appears to be right justified.

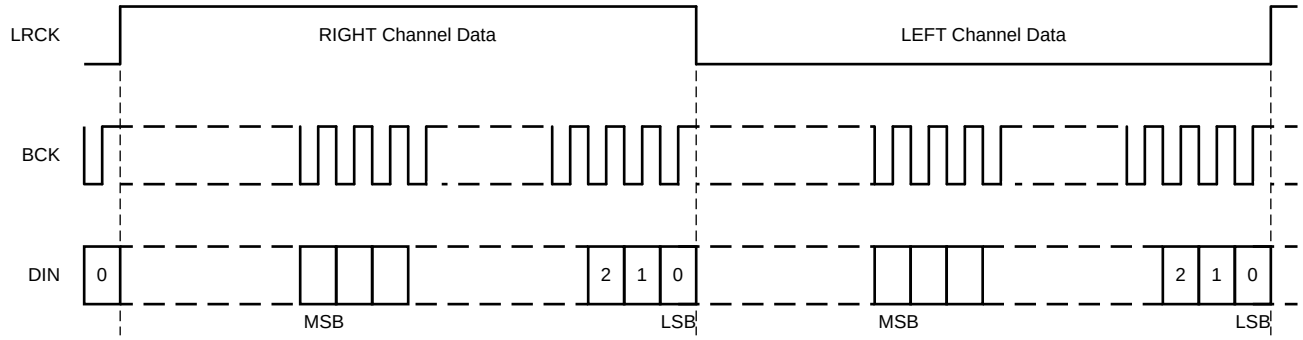


Figure 18. Right-Justified Format

TDM Format

There are no well defined rules for TDM format and it can be implemented in large number of ways depending upon the word length, bit clock, number of channels to be multiplexed, etc. For example, let's assume that word clock signal (LRCK) period = 256 * bit clock (BCK) time period. In this case, we can multiplex 4 channels with maximum word length of 64 bits each, or 8 channels with maximum word length of 32 bits each. Figure 19 illustrates the multiplexing of 8 channels with 24 bit word length, in a format similar to I^2S.

Pulse width of LRCK can be used to define a clock period for BCK or to define a slot period, i.e., the period for which individual channel can be active on the shared data line.

If the number of audio channels is more than 8, DS90UA101-Q1/DS90UA102-Q1 can easily support multiplexed data with additional devices to multiplex and de-multiplex the data. The number of channels multiplexed on each data line must be selected as a power of 2, for example, 2/ 4/ 8.

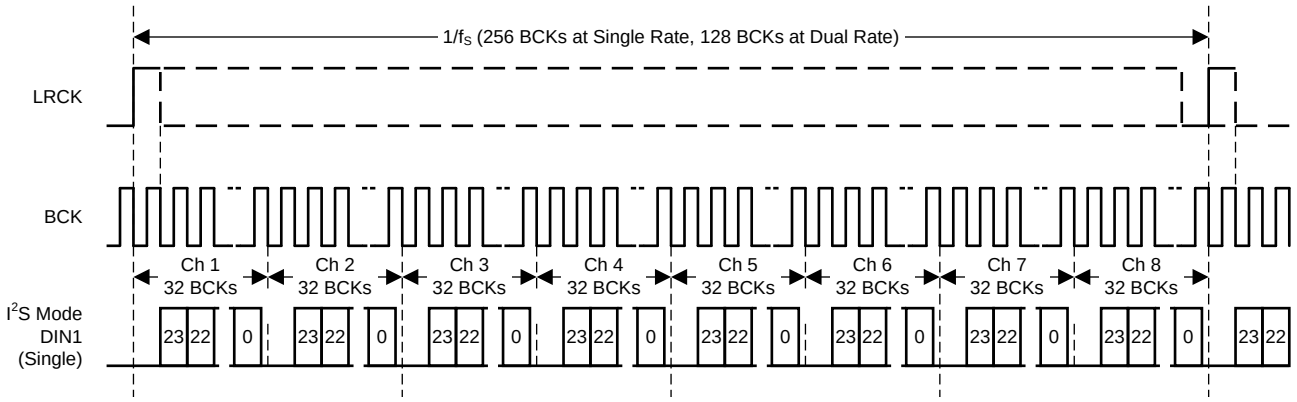


Figure 19. TDM Format

Error Detection

The chipset provides error detection operations for validating data integrity in long distance transmission and reception. The data error detection function offers users flexibility and usability of performing bit-by-bit data transmission error checking. The error detection operating modes support data validation of the following signals:

- Bidirectional Control Channel data across the serial link
- Parallel audio/sync data across the serial link

The chipset provides 1 parity bit on the forward channel and 4 CRC bits on the back channel for error detection purposes. The DS90UA101-Q1/DS90UA102-Q1 chipset checks the forward and back channel serial links for errors and stores the number of detected errors in two 8-bit registers in the Serializer and the Deserializer, respectively.

To check parity errors on the forward channel, monitor registers 0x1A and 0x1B on the Deserializer. If there is a loss of LOCK, then the counters on registers 0x1A and 0x1B are reset. Whenever there is a parity error on the forward channel, the PASS pin will go low momentarily.

To check CRC errors on the back-channel, monitor registers 0x0A and 0x0B on the Serializer.

Bidirectional Control Bus and I²C

The I²C compatible interface allows programming of the Serializer, Deserializer, or an external remote device through the Bidirectional Control Channel. For example, an audio module connected to the Deserializer can communicate with the ADC connected to the Serializer using the Bidirectional Control Channel. Register programming transactions to/from the chipset are employed through the clock (SCL) and data (SDA) lines. These two signals have open drain I/Os and both lines must be pulled-up to V_{DDIO} by an external resistor. Pull-up resistors or current sources are required on the SCL and SDA busses to pull them high when they are not being driven low. A logic LOW is transmitted by driving the output low. Logic HIGH is transmitted by releasing the output and allowing it to be pulled-up externally. The appropriate pull-up resistor values will depend upon the total bus capacitance and operating speed. The DS90UA101-Q1/DS90UA102-Q1 I²C bus data rate supports up to 400 kbps according to I²C fast mode specifications. Figure 20, Figure 21, Figure 22, Figure 23 show I²C waveforms of read/write bytes, basic operation, and start/stop conditions.

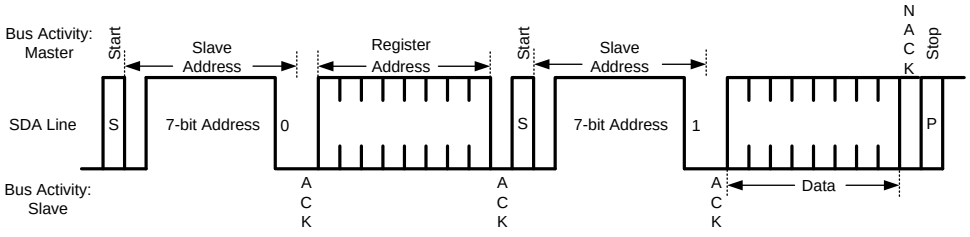


Figure 20. Read Byte

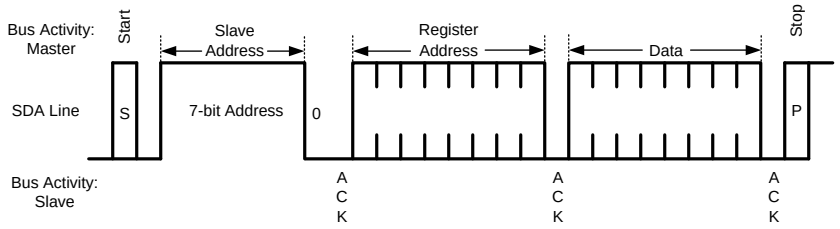


Figure 21. Write Byte

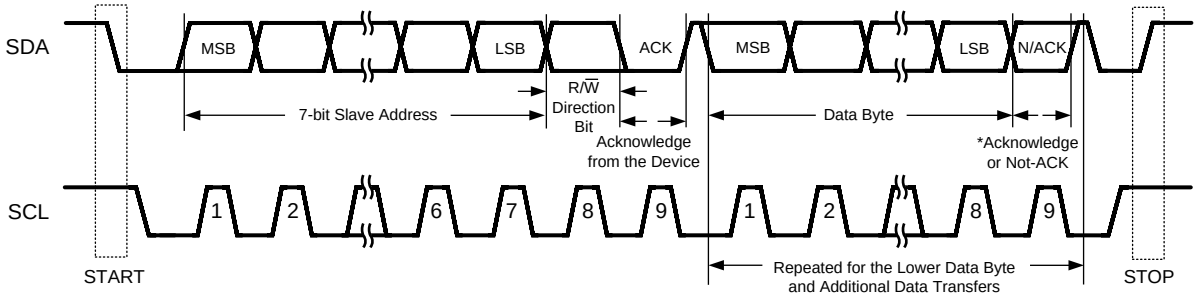


Figure 22. Basic Operation

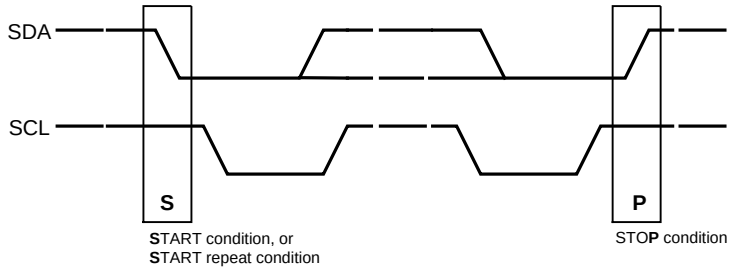


Figure 23. Start and Stop Conditions

IDx Address Decoder on the Serializer

The IDx pin (Figure 24) on the Serializer is used to decode and set the I^2C address of the Serializer. There are 6 possible I^2C addresses that can be set on the Serializer. The pin must be pulled to V_{DD} (1.8V, not V_{DDIO}) with a 10 kΩ resistor and a pull down resistor R_{ID}) of the recommended value to set the I^2C address of the Serializer (Table 2). The recommended maximum resistor tolerance is 1%.

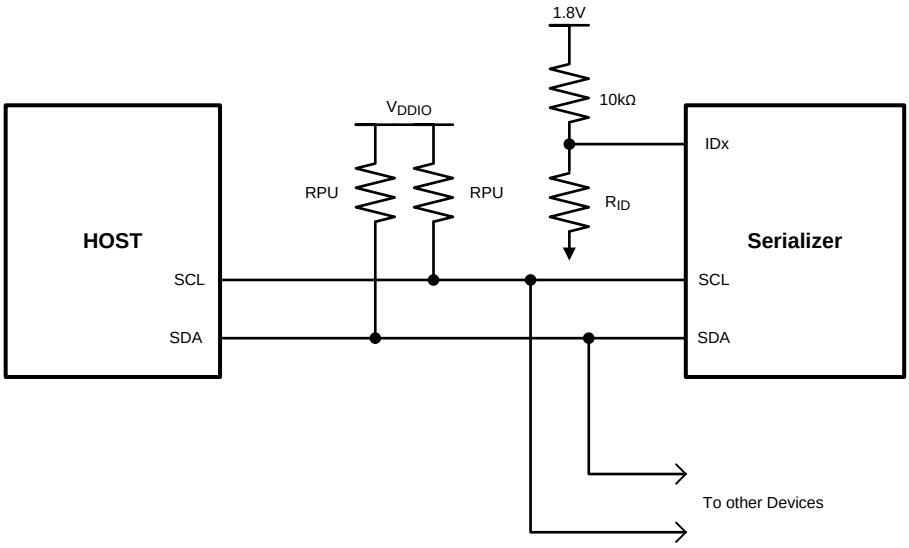


Figure 24. IDx Address Select

Table 2. IDx Recommended Resistor Values

IDx Resistor Value		
Resistor R_{ID} (kΩ) (1% Tolerance)	**7-Bit Address**	**8-Bit Address (0 appended)**
0	0x58	0xB0
2	0x59	0xB2
4.7	0x5A	0xB4
8.2	0x5B	0xB6
14	0x5C	0xB8
100	0x5D	0xBA

Note: The I^2C address of the Serializer can also be set using 0x00[7:1] once 0x00[0] is set to 1.

I^2C Pass-Through

I^2C pass-through is the feature that provides a way to access remote devices at the other end of the serial interface. For example, when the I^2C Master is connected to the Deserializer and I^2C pass-through is enabled on the Deserializer, any I^2C traffic targeted for the remote Serializer or remote slave will be allowed to pass through the Deserializer to reach those respective devices.

See Figure 25 for an example of this function:

- If Master (DSP) transmits an I^2C transaction for SER A, then DES A with I^2C pass-through enabled will transfer that I^2C command to SER A. Responses from SER A will travel from SER A --> DES A --> DSP.
- If Master transmits an I^2C transaction for address 0xA0, then DES A with I^2C pass-through enabled will transfer that I^2C command to SER A, which will then transfer it to remote slave Device A. Responses from Device A will travel from Device A --> SER A --> DES A --> DSP.
- As for DES B with I^2C pass-through disabled, any I^2C commands for SER B or Device B will NOT be passed on the I^2C bus to SER B/Device B.

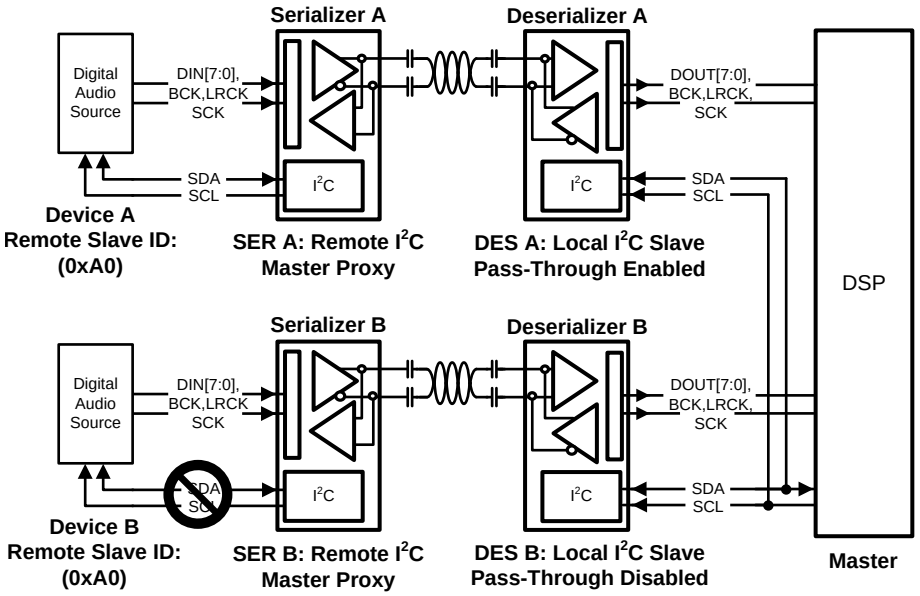


Figure 25. I²C Pass-Through

To setup I²C pass-through on the Serializer, set 0x03[2] = 1 and configure registers 0x06, 0x07, 0x08, and 0x09 as needed (Deserializer I²C ID, Deserializer Alias ID, remote slave I²C ID, remote slave Alias ID, respectively). Refer to Multiple Device Addressing for information about Alias IDs and refer to DS90UA101-Q1 REGISTER INFORMATION for information to set these registers. To communicate with the remote Deserializer from the Serializer side, registers 0x06 and 0x07 must be configured (register 0x06 is auto-loaded by default if there is LOCK). To communicate with the remote slave connected to the remote Deserializer, configure registers 0x08 and 0x09.

To setup I²C pass-through on the Deserializer, set 0x03[3] = 1 and configure registers 0x06 - 0x17 as needed. To communicate with the remote Serializer from the Deserializer side, registers 0x06 and 0x07 must be configured (register 0x06 is auto-loaded by default if there is LOCK). To communicate with one or more remote slaves connected to the remote Serializer, configure 0x08 - 0x17 accordingly.

Multiple Device Addressing

Some applications require multiple devices with the same fixed address to be accessed on the same I²C bus. The DS90UA101-Q1/DS90UA102-Q1 provides slave ID aliasing to generate different target slave addresses when connecting two or more identical devices remotely. Instead of addressing their actual I²C addresses, each remote device can be addressed through a unique alias ID by programming the Slave Alias ID register on the Serializer/Deserializer. By addressing the Slave Alias IDs, I²C slaves with identical, fixed addresses can now be addressed independently. On the DS90UA101-Q1, up to 1 Slave Alias ID index is supported. On the DS90UA102-Q1, up to 8 Slave Alias IDs can be supported. The Audio Module/DSP (I²C Master) must keep track of the alias list in order to properly address the correct device.

Refer to Figure 26 for an example of this function:

- There is a local I²C bus between Audio Module, DES A, and DES B. Audio Module is the I²C Master, and DES A and DES B are I²C slaves.
- The I²C protocol is bridged from DES A to SER A and from DES B to SER B. SER A is the master of its own local I²C bus, and Source A and its µC/EEPROM are slaves on this bus. SER B is also the master of its local I²C bus, and Source B and its µC/EEPROM are the slaves.
- Audio Module can now address remote slaves connected to SER A and SER B independently.
- Case 1: If Audio Module transmits to I²C slave 0xA0, DES A (address 0xC0) will forward the transaction to SER A, which then forwards it to remote slave Source A. Responses from Source A will travel from Source A --> SER A --> DES A --> Audio Module.
- Case 2: If Audio Module transmits to slave address 0xA4, DES B (address 0xC2) will recognize that 0xA4 is mapped to 0xA0 and will transmit the command to SER B, which then forwards it to remote slave Source B.

Responses from Source B will travel from Source B --> SER B --> DES B --> Audio Module.

- Case 3: If Audio Module sends command to address 0xA6, DES B (address 0xC2) will forward the transaction to SER B, which then forwards it to Source B's µC/EEPROM. Responses from Source B's µC/EEPROM will travel from Source B's µC/EEPROM --> SER B --> DES B --> Audio Module.

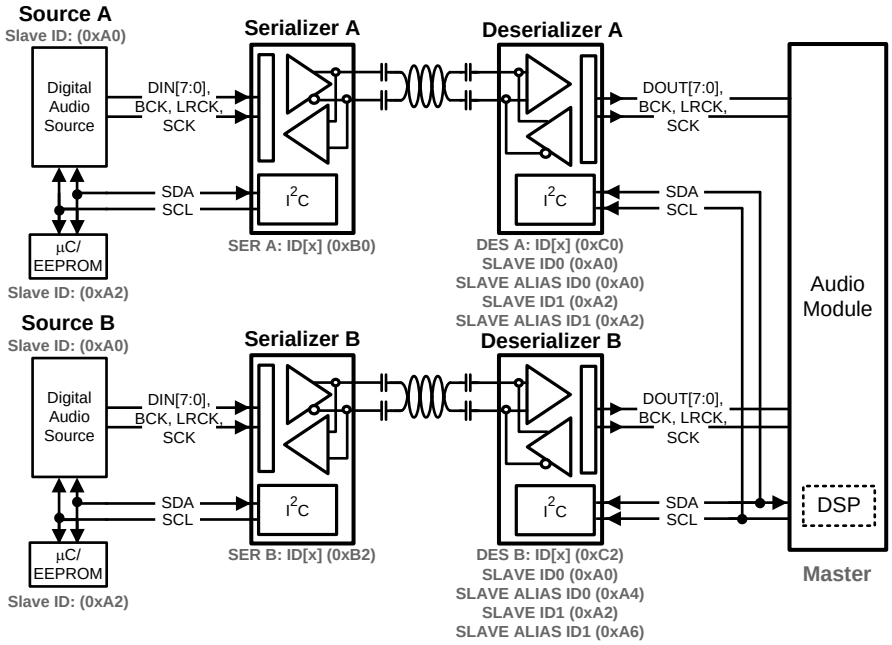


Figure 26. Multiple Device Addressing

NOTE

The alias ID must be set in order to communicate with any remote device. For example:

- When there is only one SER/DES pair and no remote slaves: if I^2C Master on the DES side wants to communicate with the remote SER, I^2C pass-through must be enabled on the DES and the SER Alias ID must also be set before the I^2C Master can communicate with the remote SER (the SER ID is automatically configured by default if there is LOCK).
- When there is only one SER/DES pair and one remote slave connected to the SER: if I^2C Master on the DES side (with pass-through enabled) wants to communicate with the remote slave, the Slave ID and Slave Alias ID must be set before the I^2C Master can communicate with the remote slave, even if there is only one remote slave.

Slave Clock Stretching

To communicate and synchronize with remote devices on the I^2C bus through the Bidirectional Control Channel, the chipset utilizes bus clock stretching (holding the SCL line low) during data transmission. On the 9th clock of every I^2C transfer (before the ACK signal), the local I^2C slave pulls the SCL line low until a response is received from the remote I^2C bus located on the other end of the serial interface. The slave device will not control the clock and only stretches it until the remote peripheral has responded. The I^2C Master must support slave clock stretching in order to communicate with remote devices.

General Purpose Inputs, Outputs (GPIs, GPOs, GPIOs) Descriptions

There are 4 dedicated general purpose inputs (GPIs) on the DS90UA101-Q1 and 4 dedicated general purpose outputs (GPOs) on the DS90UA102-Q1. Inputs to the GPI pins on the Serializer are fed to the GPO outputs on the Deserializer. The maximum GPI data rate is defined by the SCK source (up to 50 Mbps).

In addition, there are also 4 GPOs on the DS90UA101-Q1 and 4 GPIOs on the DS90UA102-Q1. The GPOs on the Serializer can be configured as outputs for the input signals that are fed into the Deserializer GPIOs. The GPIO maximum data rate is up to 66 kbps when configured for communication between Deserializer GPIO to Serializer GPO. Both the GPOs on the Serializer and GPIOs on the Deserializer can also behave as outputs whose values are set from local registers.

LVCMOS V_{DDIO} Option

1.8V/3.3V Serializer inputs are user configurable to provide compatibility with 1.8V and 3.3V system interfaces.

Power Up Requirements and PDB Pin

The Serializer is active when the PDB pin is driven HIGH. Driving the PDB pin LOW powers down the device and clears all control register configurations to default values. The PDB pin must be held low until the power supplies (V_{DDn} and V_{DDIO}) have settled to the recommended operating voltage. This can be done by driving PDB externally, or an RC network can be connected to the PDB pin to ensure PDB arrives after all the power supplies have stabilized.

Powerdown

The PDB pin's function on the Serializer is to ENABLE or powerdown the device. This pin can be controlled by the system and can be used to disable the SER to save power. If PDB = HIGH, the SER will lock to the valid input SCK and transmit data to the DES by sending a serial stream at 28 times the SCK frequency. If SCK is idle or missing, the SER will output a serial stream based on its internal oscillator frequency (Table 1). When PDB = LOW, the high-speed driver outputs are static HIGH.

SCK Clock Edge Select (TRFB)

The TRFB selects which edge of the input clock is used to latch input data. If TRFB register is 1, data is latched on the rising edge of the SCK. If TRFB register is 0, data is latched on the falling edge of the SCK.

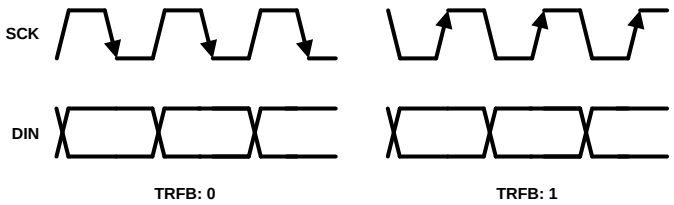


Figure 27. Programmable SCK Strobe Select

Built In Self Test (BIST)

An optional at-speed built in self test (BIST) feature supports the testing of the high speed serial link and low-speed back channel. This is useful in the prototype stage, equipment production, and in-system test and also for system diagnostics.

BIST Configuration and Status

The DS90UA101-Q1/DS90UA102-Q1 chipset can be programmed into BIST mode using either pins or registers. By default BIST configuration is controlled through pins on the DS90UA102-Q1. BIST can also be configured via registers using BIST Control Register 0x24 on the DS90UA102-Q1. Pin based configuration is defined as follows:

- BISTEN (on DS90UA102-Q1) = HIGH: Enable the BIST mode, BISTEN = LOW: Disable the BIST mode.
- GPIO3 and GPIO2 of DS90UA102-Q1: Defines the BIST clock source (SCK vs. various internal oscillator frequencies). See Table 3 below.

Table 3. BIST Pin Configuration on DS90UA102-Q1 Deserializer(1)

DS90UA102-Q1 Deserializer GPIO[3:2]	Oscillator Source	BIST Frequency (MHz)
00	External	SCK
01	Internal	~25
10	Internal	~50
11	Internal	~12.5

(1) Note: These pin settings will only be active when 0x24[3] = 1 and BIST is on.

The BIST mode provides various options for the clock source. Either external pins (GPIO3 and GPIO2 of DES) or register 0x24 on DES can be used to configure the BIST to use SCK or various internal oscillator frequencies as the clock source. Refer to Table 4 below for BIST register settings.

Table 4. BIST Register Configuration on DS90UA102-Q1 Deserializer(1)

DS90UA102-Q1 Deserializer 0x24[2:1]	Oscillator Source	BIST Frequency (MHz)
00	External	SCK
01	Internal	~50
10	Internal	~25
11	Internal	~12.5

(1) Note: These register settings will only be active when 0x24[3] = 0 and BIST is on.

The BIST status can be monitored real-time on the PASS pin. For every frame with error(s), the PASS pin toggles low momentarily. If two consecutive frames have errors, PASS will toggle twice to allow counting of frames with errors. Once the BIST is done, the PASS pin reflects the pass/fail status momentarily (pass = no errors, fail = one or more errors). The BIST result can also be read through I^2C for the number of frames that errored. The status register retains results until it is reset by a new BIST session or a device reset. For all practical purposes, the BIST status can be monitored from the BIST Error Count register 0x25 on the DS90UA102-Q1 Deserializer.

Sample BIST Sequence (Refer to Figure 28)

Step 1: BIST mode is enabled via the BISTEN pin on the DS90UA102-Q1 Deserializer, or through the Deserializer control registers. The clock source is selected through the GPIO3 and GPIO2 pins as shown in Table 3.

Step 2: The DS90UA101-Q1 Serializer BIST start command is activated through the back channel.

Step 3: The BIST pattern is generated and sent through the serial interface to the Deserializer. Once the Serializer and Deserializer are in the BIST mode and the Deserializer acquires LOCK, the PASS pin of the Deserializer goes high and BIST starts checking the data stream. If an error in the payload is detected the PASS pin will switch low momentarily. During the BIST test, the PASS output can be monitored and counted to determine the payload error rate.

Step 4: To stop the BIST mode, the Deserializer BISTEN pin is set low and the Deserializer stops checking the data. The final test result is not maintained on the PASS pin. To check the number of BIST errors, check the BIST Error Count register, 0x25 on the Deserializer. The link returns to normal operation after the Deserializer BISTEN pin is low.

Figure 29 below shows the waveform diagram of a typical BIST test for two cases. Case 1 is error free, and Case 2 shows one with multiple errors. In most cases, it is difficult to generate errors due to the robustness of the link (differential data transmission, adaptive equalization, etc.), thus they may be introduced by greatly extending the cable length, increasing the frequency, or by reducing signal condition enhancements (Rx equalization).

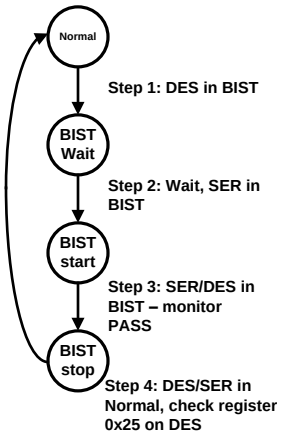


Figure 28. BIST System Flow Diagram

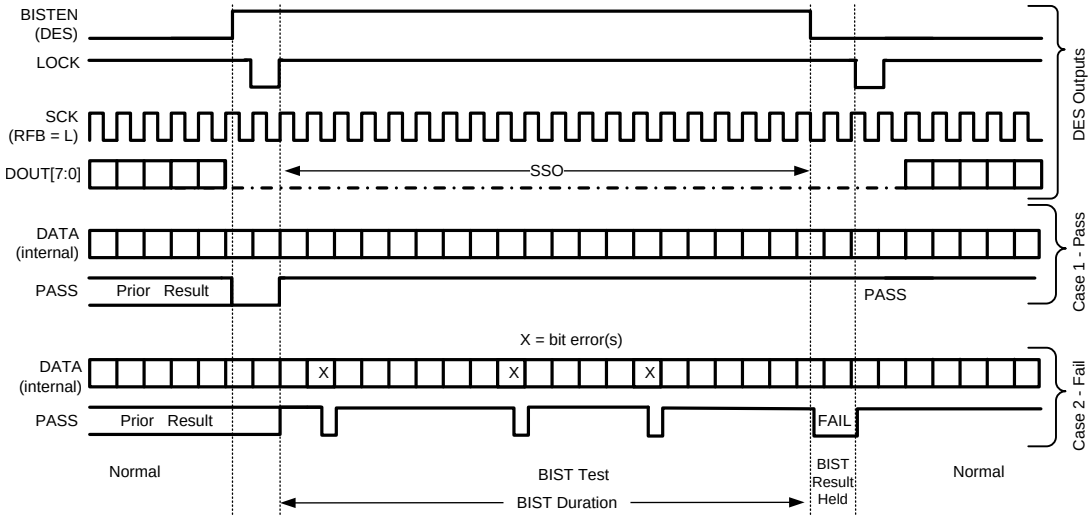


Figure 29. BIST Timing Diagram

APPLICATIONS INFORMATION

AC Coupling

The SER/DES supports only AC-coupled interconnects through an integrated DC-balanced coding scheme. External AC coupling capacitors must be placed in series with the serial interface signal path as illustrated in Figure 30 or Figure 31. Applications utilizing STP cable require a 0.1 µF coupling capacitor on both outputs (DOUT+, DOUT-). Applications utilizing single-ended 50Ω coaxial cable require a 0.1 µF capacitor on the true serial interface output (DOUT+). The unused data pin (DOUT-) requires a 0.047 µF capacitor coupled to a 50Ω resistor to GND.

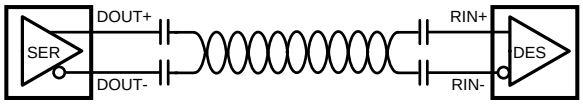


Figure 30. AC-Coupled Connection (STP)

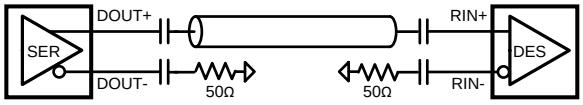


Figure 31. AC-Coupled Connection (Coaxial)

For high-speed serial transmissions, the smallest available package should be used for the AC coupling capacitor. This will help minimize degradation of signal quality due to package parasitics.

Typical Application Connection

Figure 32 and Figure 33 show typical application connections of the DS90UA101-Q1 Serializer. The serial interface outputs must have external 0.1 µF coupling capacitors connected to the high-speed interconnect. The Serializer has internal termination.

Bypass capacitors are placed near the power supply pins. Ferrite beads should also be used for effective noise suppression. The digital audio electrical interface is LVCMOS format. The V_{DDIO} pin may be connected to 3.3V or 1.8V. Device I^2C address select is configured via the IDx pin.

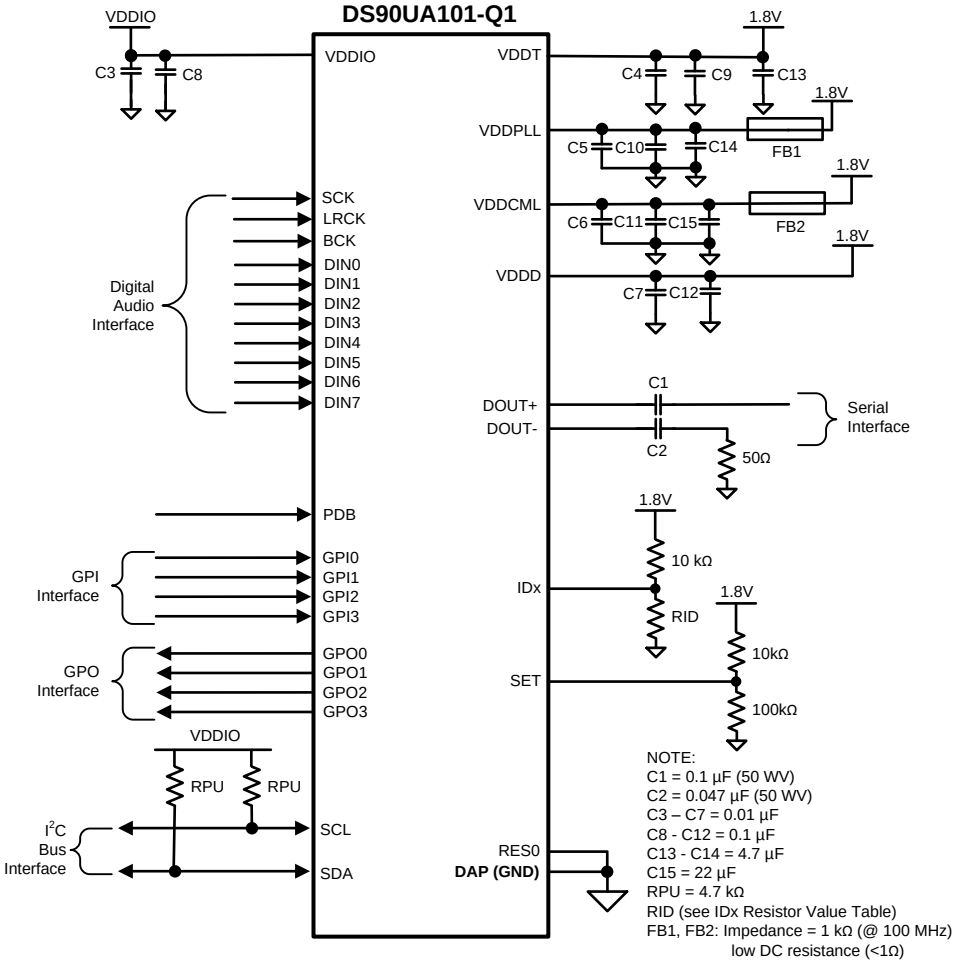


Figure 32. DS90UA101-Q1 Typical Connection Diagram (Coaxial Interconnect)

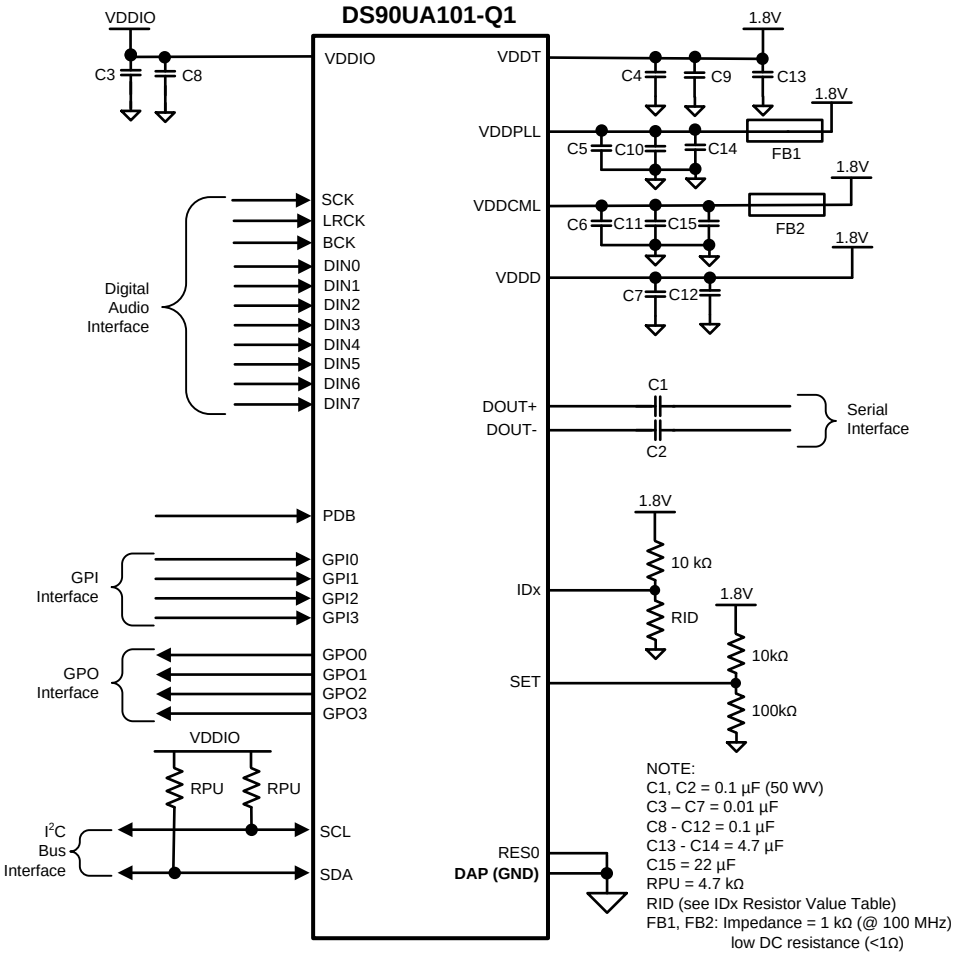


Figure 33. DS90UA101-Q1 Typical Connection Diagram (STP Interconnect)

PCB Layout and Power System Considerations

Circuit board layout and stack-up for the Ser/Des devices should be designed to provide low-noise power feed to the device. Good layout practice will also separate high frequency or high-level inputs and outputs to minimize unwanted stray noise pickup, feedback and interference. Power system performance may be greatly improved by using thin dielectrics (2 to 4 mils) for power / ground sandwiches. This arrangement provides plane capacitance for the PCB power system with low-inductance parasitics, which has proven especially effective at high frequencies, and makes the value and placement of external bypass capacitors less critical. External bypass capacitors should include both RF ceramic and tantalum electrolytic types. RF capacitors may use values in the range of 0.01 µF to 0.1 µF. Tantalum capacitors may be in the 2.2 µF to 10 µF range. Voltage rating of the tantalum capacitors should be at least 5X the power supply voltage being used.

Surface mount capacitors are recommended due to their smaller parasitics. When using multiple capacitors per supply pin, locate the smaller value closer to the pin. A large bulk capacitor is recommend at the point of power entry. This is typically in the 50 µF to 100 µF range and will smooth low frequency switching noise. It is recommended to connect power and ground pins directly to the power and ground planes with bypass capacitors connected to the plane with via on both ends of the capacitor. Connecting power or ground pins to an external bypass capacitor will increase the inductance of the path.

A small body size X7R chip capacitor, such as 0603, is recommended for external bypass. Its small body size reduces the parasitic inductance of the capacitor. The user must pay attention to the resonance frequency of these external bypass capacitors, usually in the range of 20-30 MHz. To provide effective bypassing, multiple capacitors are often used to achieve low impedance between the supply rails over the frequency of interest. At high frequency, it is also a common practice to use two vias from power and ground pins to the planes, reducing the impedance at high frequency.

Some devices provide separate power for different portions of the circuit. This is done to isolate switching noise effects between different sections of the circuit. Separate planes on the PCB are typically not required. Pin Description tables typically provide guidance on which circuit blocks are connected to which power pin pairs. In some cases, an external filter many be used to provide clean power to sensitive circuits such as PLLs.

Use at least a four-layer board with a power and ground plane. Locate LVCMOS signals away from the differential lines to prevent coupling from the LVCMOS lines to the differential lines. Closely-coupled differential lines of 100Ω are typically recommended for differential interconnect. The closely coupled lines help to ensure that coupled noise will appear as common-mode and thus is rejected by the receivers. The tightly coupled lines will also radiate less.

Information on the LLP style package is provided in TI Application Note 1187.

Interconnect Guidelines

See AN-1108 and AN-905 for full details.

- Use 100Ω coupled differential pairs
- Use the S/2S/3S rule in spacings
  - – S = space between the pair
  - – 2S = space between pairs
  - – 3S = space to LVCMOS signal
- Minimize the number of Vias
- Use differential connectors when operating above 500 Mbps line speed
- Maintain balance of the traces
- Minimize skew within the pair

Additional general guidance can be found in the LVDS Owner's Manual - available in PDF format from the Texas Instrument web site at: www.ti.com/lvds.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS90UA101TRTVJQ1	ACTIVE	WQFN	RTV	32	2500	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 105	UA101Q	Samples
DS90UA101TRTVRQ1	ACTIVE	WQFN	RTV	32	1000	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 105	UA101Q	Samples
DS90UA101TRTVTQ1	ACTIVE	WQFN	RTV	32	250	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 105	UA101Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

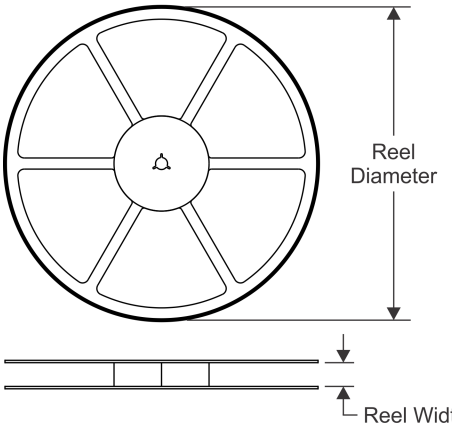
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

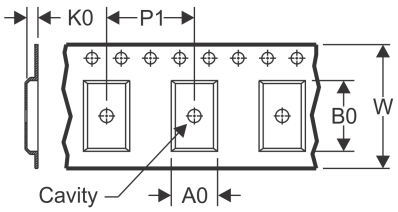
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

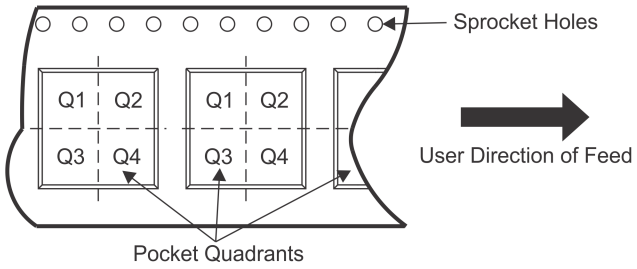


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

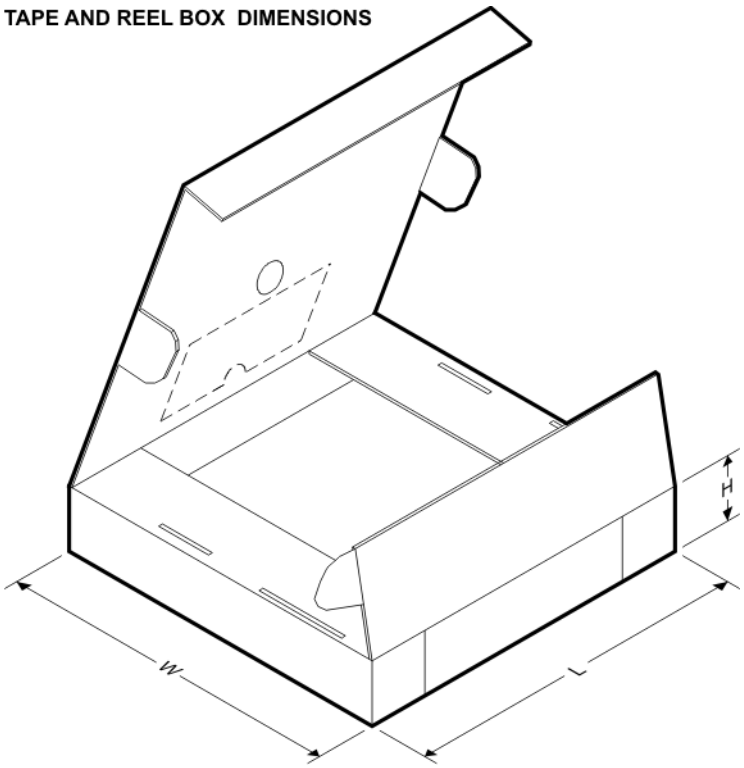
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS90UA101TRTVJQ1	WQFN	RTV	32	2500	330.0	12.4	5.3	5.3	1.3	8.0	12.0	Q1
DS90UA101TRTVRQ1	WQFN	RTV	32	1000	178.0	12.4	5.3	5.3	1.3	8.0	12.0	Q1
DS90UA101TRTVTQ1	WQFN	RTV	32	250	178.0	12.4	5.3	5.3	1.3	8.0	12.0	Q1

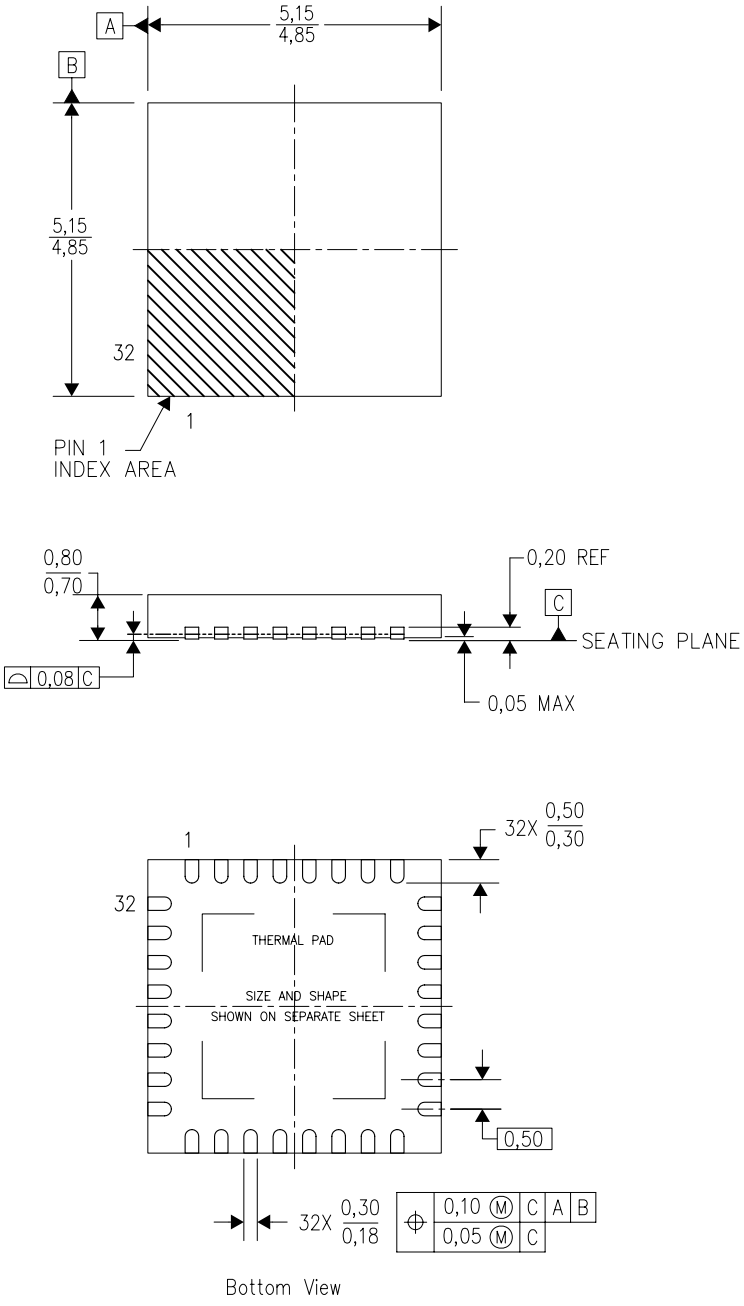
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS90UA101TRTVJQ1	WQFN	RTV	32	2500	367.0	367.0	35.0
DS90UA101TRTVRQ1	WQFN	RTV	32	1000	210.0	185.0	35.0
DS90UA101TRTVTQ1	WQFN	RTV	32	250	210.0	185.0	35.0

RTV (S–PWQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD



4206245/C 10/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–Leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale (https:www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265