QUICK START GUIDE FOR DEMONSTRATION CIRCUIT 1335A-A

HIGH POWER, HIGH EFFICIENCY POE PD INTERFACE WITH INTEGRATED SWITCHING REGULATOR

LTC4269IDKD-1

DESCRIPTION

Demonstration circuit 1335A-A is a high-power supply featuring the LTC®4269IDKD-1. This board acts as an IEEE 802.3at compliant, high power Power-over-Ethernet (PoE), Powered Device (PD) and connects at the RJ45 to a compatible high power Power Sourcing Equipment (PSE) device, such as the DC1366.

The LTC4269IDKD-1 provides IEEE802.3at standard (PoE+) PD interfacing and power supply control. When the PD is fully powered, the PD interface switches power over from the PSE to the switcher through an internal, low resistance, high power MOSFET. The highly integrated LTC4269IDKD-1 controls a high-power, small-sized power supply that utilizes a highly-efficient isolated flyback topology with synchronous rectification. The DC1335A-A supplies a 3.3V output at up to 7A.

DC1335A-A also demonstrates the use of an auxiliary 48V wall adapter. When present, the auxiliary supply becomes the dominant supply over PoE to provide power.

Design files for this circuit board are available. Call the LTC factory.

Table 1. Performance Summary (T_A = 25°C)

PARAMETER	CONDITION	VALUE
Port Voltage (V_{PORT})	At Ethernet port	37V – 57V
Auxiliary Voltage (V_{AUX})	From Aux- to Aux+ terminals	44V – 57V
Output Voltage (V_{OUT}) Initial Set-point	V_{PORT} = 37V to 57V, I_{OUT} = 0A to 5A	3.33V ± 1%
Maximum Output Current	V_{PORT} = 42V	6.6A
Typical Output Voltage Ripple	V_{IN} = 50V, I_{OUT} = 6.6A	40mV_{P-P} (typ)
Output Regulation	Over Entire Input Voltage and Output Current Range	±0.5% (typ)
Load Transient Response	Peak to Peak Deviation with Load Step of 2.5A to 5A	±450mV (typ)
	Settling Time (within 1% of V_{OUT})	< 100us (typ)
Switching Frequency		250kHz (typ)
Efficiency	V_{PORT} = 50V, I_{OUT} = 6.5A, not incl. diode bridge	89% (typ)

OPERATING PRINCIPLES

A compatible high power PSE board, such as the DC1366, is connected to the DC1335A-A at the RJ45 connector J1 (see the schematic). As required by IEEE802.3at, a diode bridge is used across the data pairs and signal pairs. Schottky diodes (D2-9) are used at the input to improve efficiency over standard diode bridges. The LTC4269IDKD-1 provides an IEEE802.3at standard PoE 25k signature resistance and is set for a power class 4. When the PD is powered and voltage is above the PoE “On Voltage”, the

LTC4269IDKD-1 switches the port voltage over to the power supply controller through its internal MOSFET which lies between the V_{PORTN} and V_{NEG} pins. This voltage charges C18/19 through a trickle charge resistor, R9 to power the bias pin, V_{CC}, of the power supply controller. Once the bias power gets to its $V_{CC(ON)}$ threshold, the IC begins a controlled soft-start of the output. As the output voltage rises, bias power is taken over by the bias supply made up of T1's bias winding and D11.

When the soft-start period is over, the output voltage is regulated by observing the pulses across the bias winding during the flyback time. The Primary Gate drive (PG) and Synchronous Gate (SG) drive is then Pulse Width Modulated (PWM) in order to keep the output voltage constant. The synchronous gate drive signal is transmitted to the secondary via the small signal transformer, T2. The output of T2 then drives a discrete gate drive buffer, R22 and Q6/7 in order to achieve fast gate transition times, hence a higher efficiency.

The two-stage input filter, C5, L2, and C6 and output filter, C1/3, L1, and C10 are the reasons that this PoE flyback supply has exceptionally low differential mode conducted emissions.

QUICK START PROCEDURE

Demonstration circuit 1335A-A is easy to set up to evaluate the performance of the LTC4269IDKD-1 in a PoE+ PD application. Refer to Figure 1 for proper equipment setup and follow the procedure below:

NOTE: When measuring the input or output voltage ripple, care must be taken to avoid a long ground lead on the oscilloscope probe. Measure the output (or input) voltage ripple by touching the probe tip and probe ground directly across the +VOUT and –VOUT (or VPORT_P and VPORT_N) terminals. See Figure 2 for proper scope probe technique.

1. Place test equipment (voltmeter, ammeter, and electronic load) across output.

2. Input supplies:

a. Connect a PoE+ capable PSE with a CAT-5 cable to the RJ45 connector, J1. See Figure 1.
b. Or, connect a 37V to 57V capable power supply ("Power Supply" in Figure 1) across VPORT_P and VPORT_N.
c. If evaluating the auxiliary power supply ("Auxiliary Supply" in Figure 1) capability, connect a 44V to 57V capable power supply across AUX+ to AUX-.

3. Check for the proper output voltage of 3.33V.

4. Once the proper output voltage is confirmed, adjust the load within the operating range and observe the output voltage regulation, ripple voltage, efficiency and other parameters.

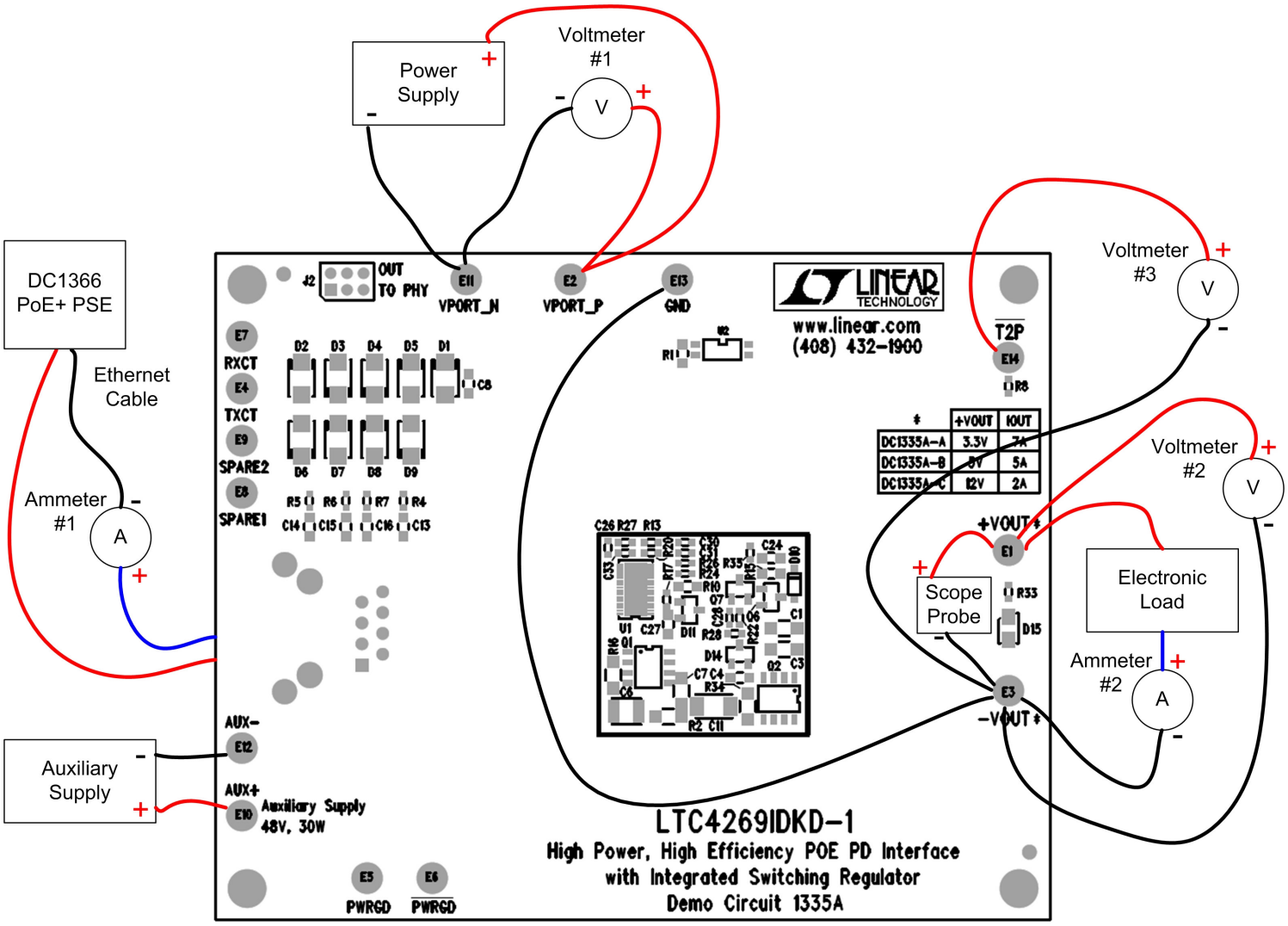


Figure 1. Proper Measurement Equipment Setup

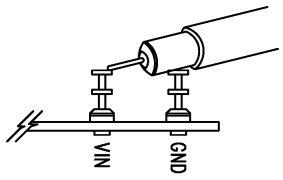


Figure 2. Measuring Input or Output Ripple

MEASURED DATA

Figures 3 through 9 are measured data for a typical DC1335A-A.

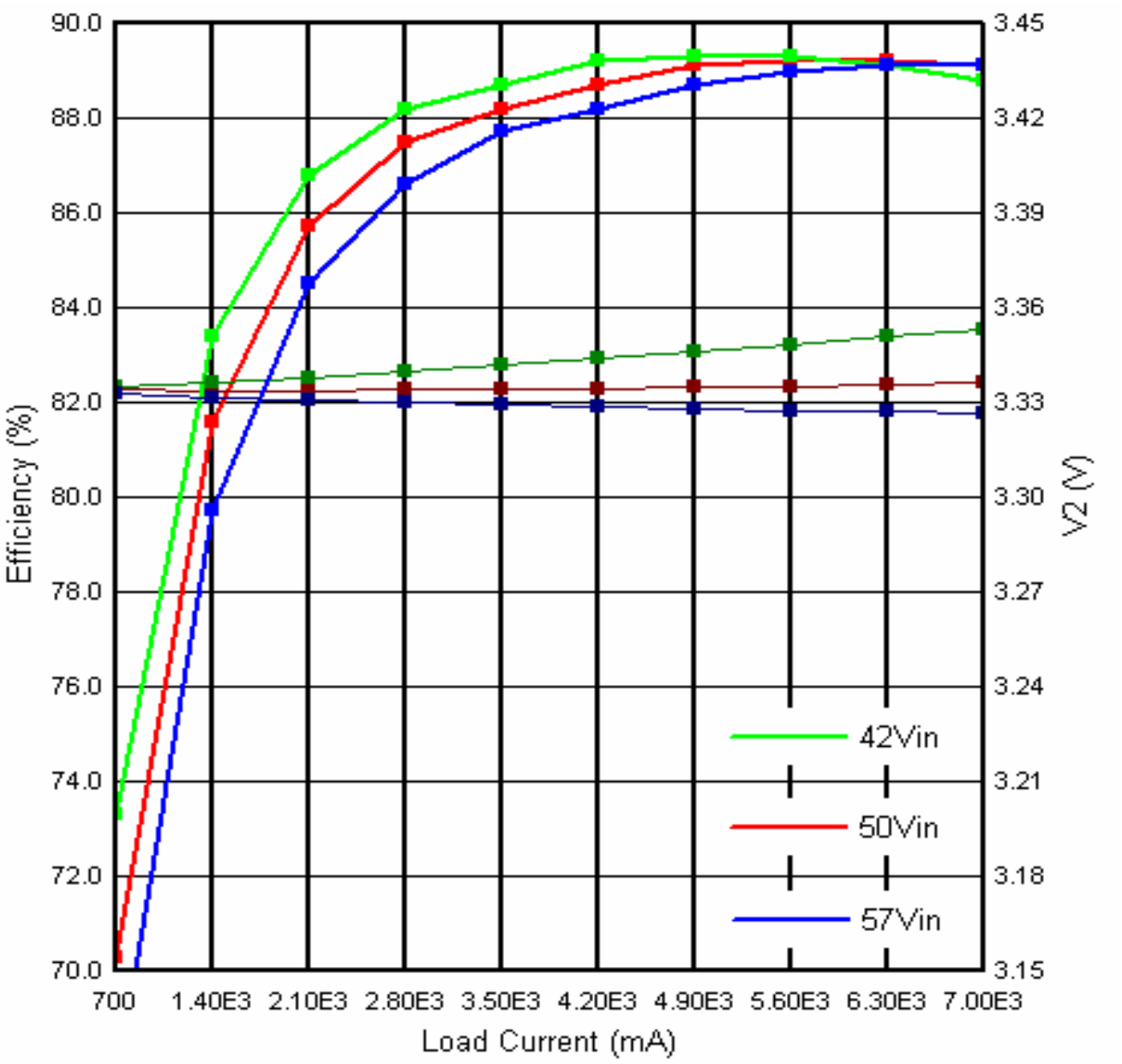


Figure 3. Efficiency (not including Diode Bridge) and Output Voltage (V2) Regulation

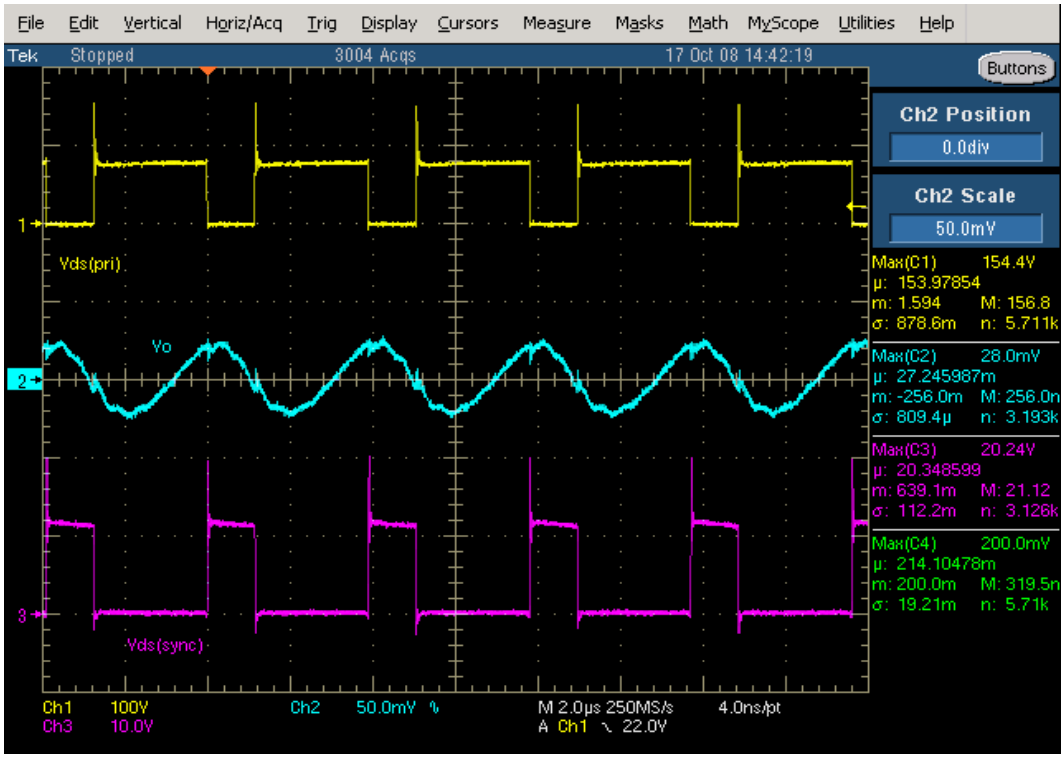


Figure 4. Output Ripple (57Vport, 7A)

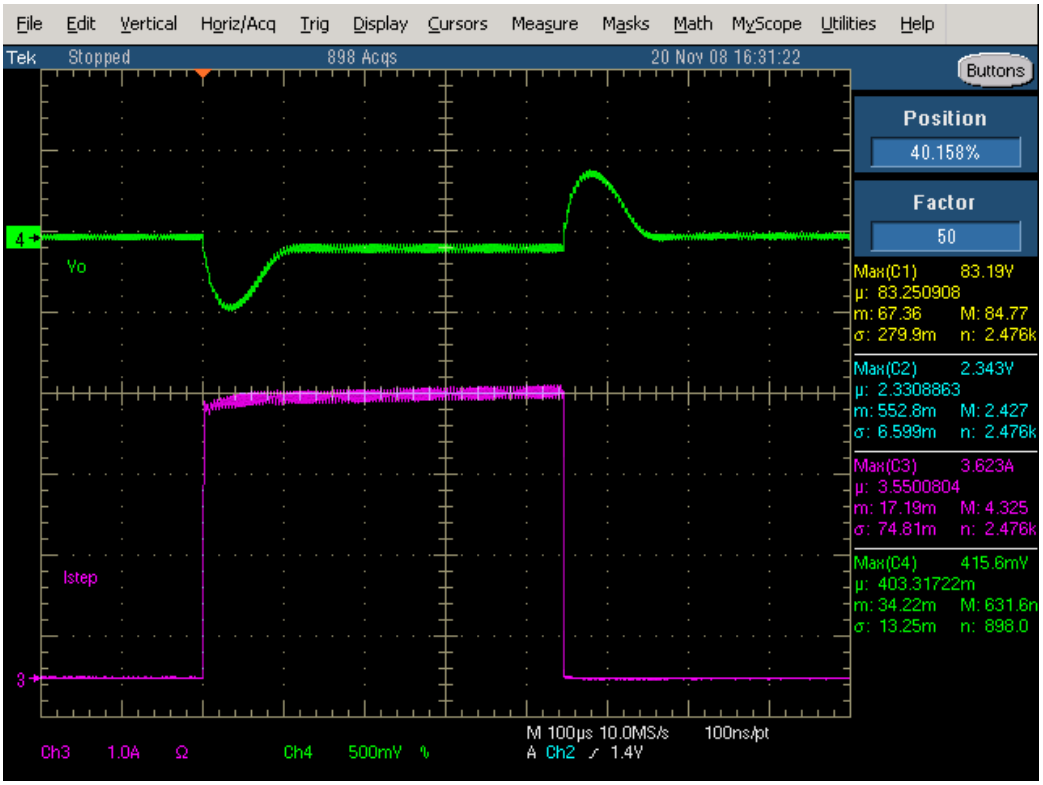


Figure 5. Load Transient Response (50Vport, 3.5A to 7A to 3.5A)

Figure 6. Temp Data (37Vport, 5A, Top)

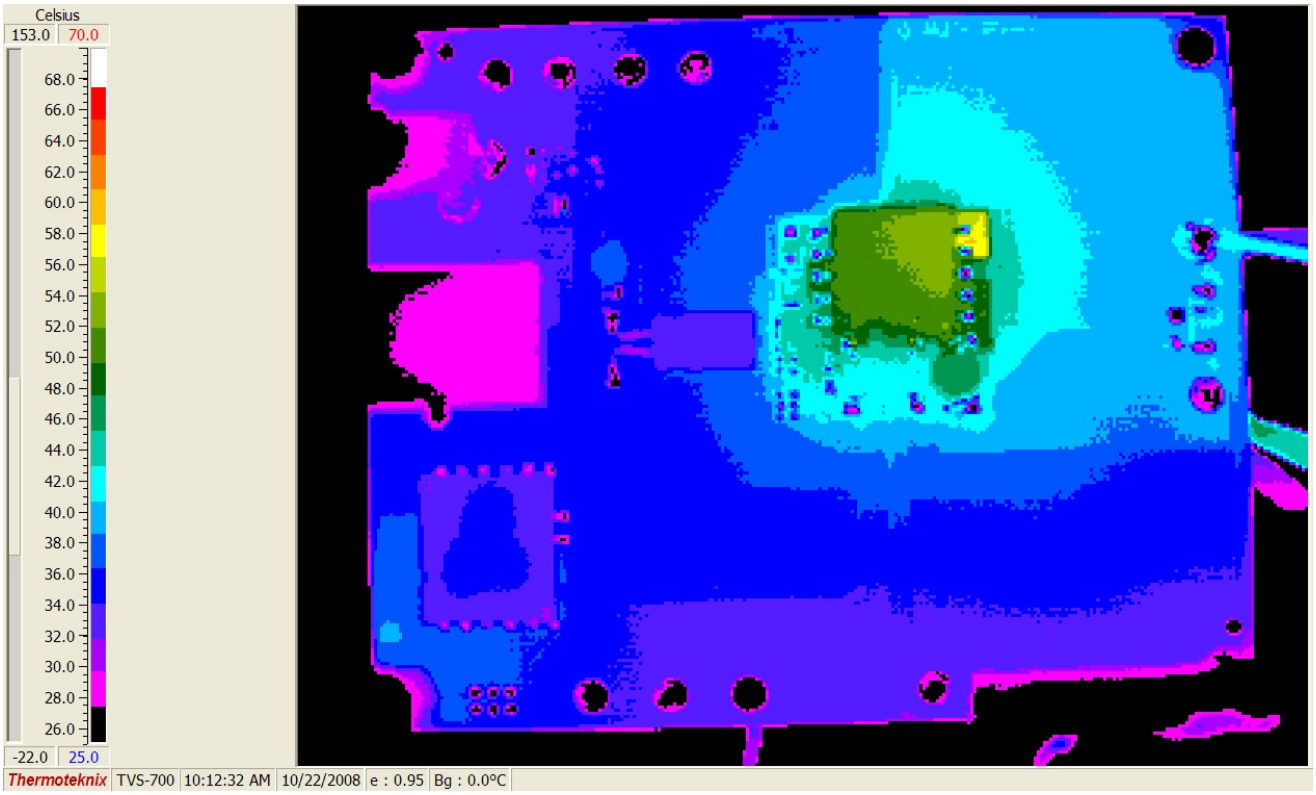


Figure 7. Temp Data (37Vport, 5A, Bottom)

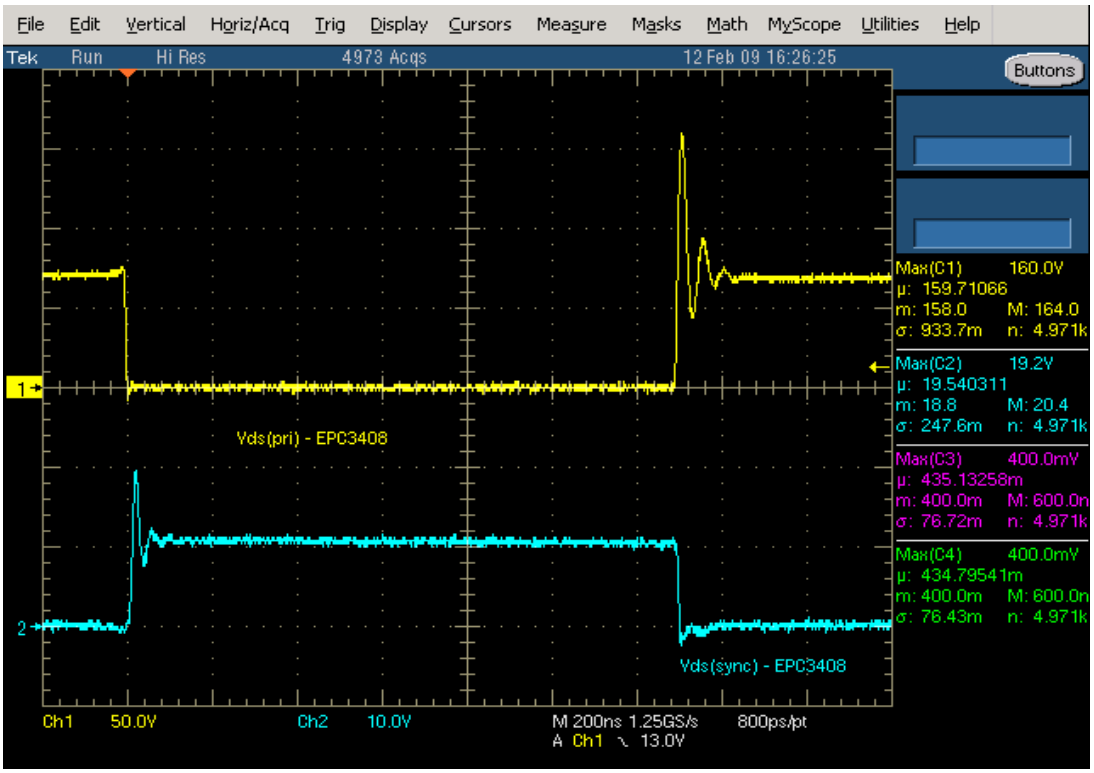


Figure 8. Stresses (50Vport, 7A, T1=EPC3408G-LF)

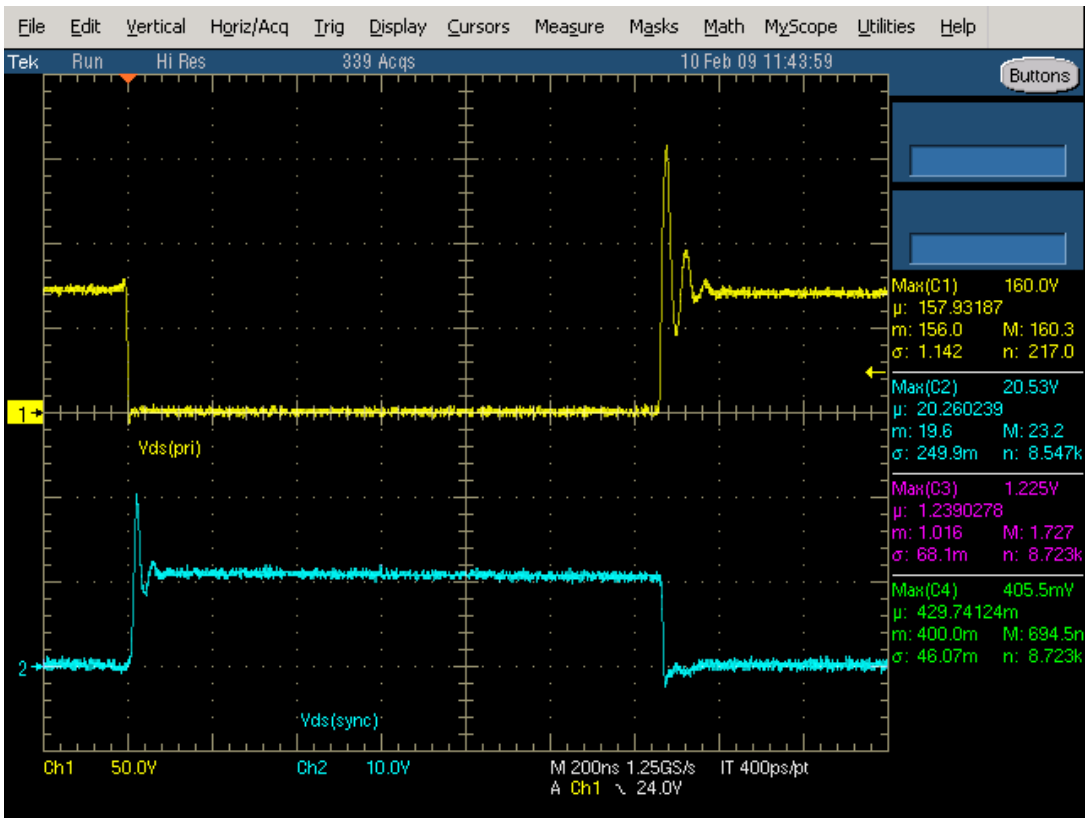
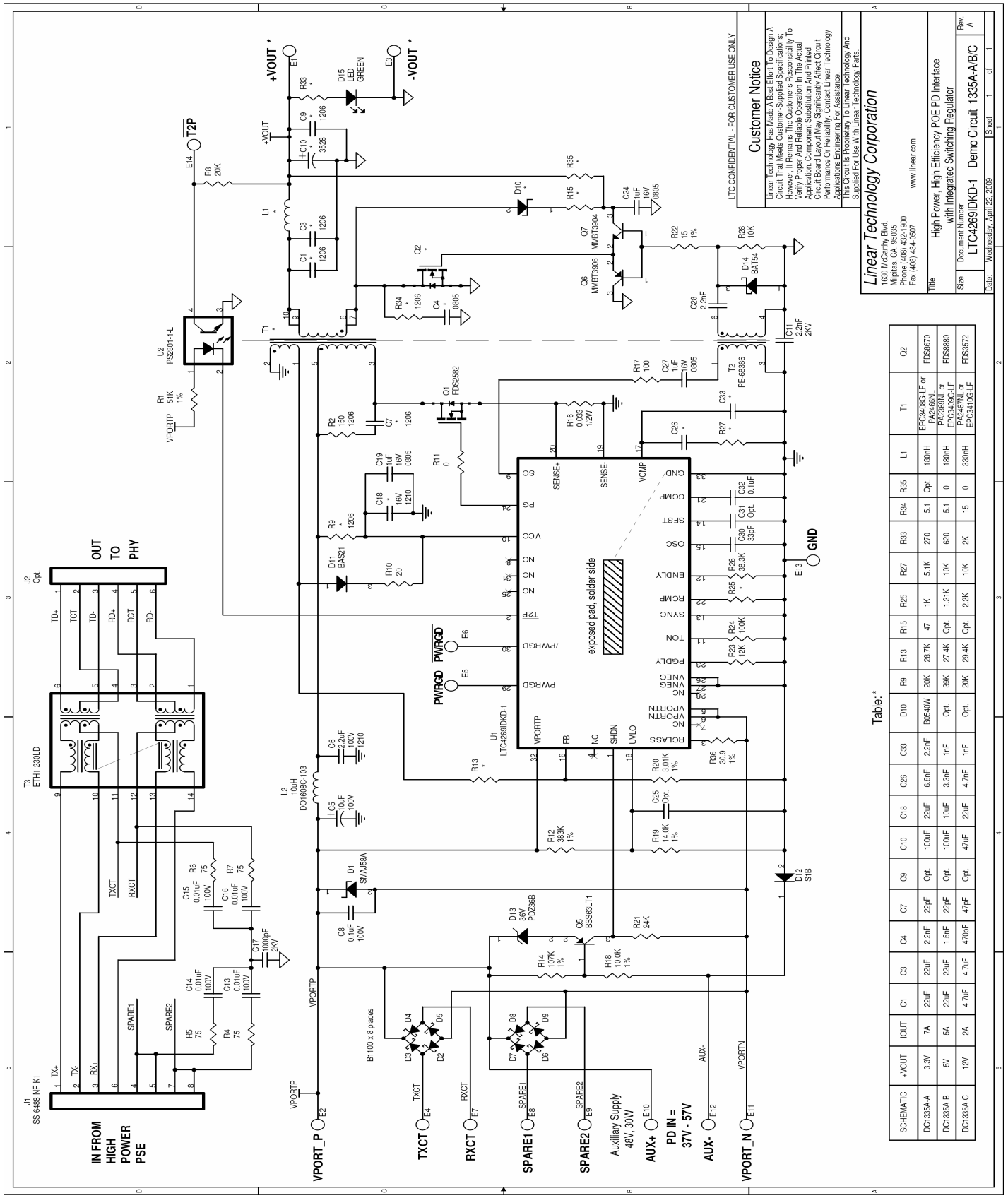


Figure 9. Stresses (50Vport, 7A, T1=PA2466NL)



SCHEMATIC	+VOUT	IOUT	C1	C3	C4	C7	C9	C10	C18	C26	C33	D10	R9	R13	R15	R25	R27	R33	R34	R35	L1	T1	Q2
DC1335A-A	3.3V	7A	22uF	22uF	2.2nF	22pF	Opt.	100uF	22uF	6.8nF	2.2nF	B0540W	20K	28.7K	47	1K	5.1K	270	5.1	Opt.	180nH	EPC3408G-LF or PA2466NL	FDS8670
DC1335A-B	5V	5A	22uF	22uF	1.5nF	22pF	Opt.	100uF	10uF	3.3nF	1nF	Opt.	39K	27.4K	Opt.	1.21K	10K	620	5.1	0	180nH	PA2369NL or EPC3409G-LF	FDS8880
DC1335A-C	12V	2A	4.7uF	4.7uF	470pF	47pF	Opt.	47uF	22uF	4.7nF	1nF	Opt.	20K	29.4K	Opt.	2.2K	10K	2K	15	0	330nH	PA2467NL or EPC3410G-LF	FDS3572

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