



50V N-Channel Enhancement Mode MOSFET - ESD Protected

Voltage 50 V Current 350mA

Features

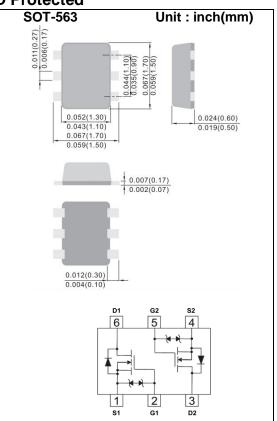
- RDS(ON), VGS@10V, ID@500mA<1.6Ω
- RDS(ON), VGS@4.5V, ID@200mA<2.5Ω
- RDS(ON), VGS@2.5V, ID@100mA<4.5Ω
- Advanced Trench Process Technology
- Specially Designed for Battery Operated Systems, Solid-State Relays Drivers: Relay, Displays, Memories, etc.
- ESD Protected 2KV HBM
- Lead free in compliance with EU RoHS 2011/65/EU directive.
- Green molding compound as per IEC61249 Std. (Halogen Free)

Mechanical Data

Case: SOT-563 Package

• Terminals : Solderable per MIL-STD-750, Method 2026

Approx. Weight: 0.00009 ounces, 0.0026 grams



Maximum Ratings and Thermal Characteristics (T_A=25 °C unless otherwise noted)

PARAMETER		SYMBOL	LIMIT	UNITS
Drain-Source Voltage		V _{DS}	50	V
Gate-Source Voltage		V_{GS}	<u>+</u> 20	V
Continuous Drain Current		I _D	350	mA
Pulsed Drain Current		I _{DM}	1200	mA
Power Dissipation	T _A =25°C	P _D	223	mW
	Derate above 25°C		1.8	mW/°C
Operating Junction and Storage Temperature Range		T_{J}, T_{STG}	-55~150	°C
Typical Thermal resistance - Junction to Ambient (Note 3)		$R_{ heta JA}$	560	°C/W





Electrical Characteristics (T_A=25 °C unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
Static						
Drain-Source Breakdown Voltage	BV_{DSS}	V _{GS} =0V,I _D =250uA	50	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}$, $I_{D}=250uA$	0.8	1.0	1.5	V
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} =10V,I _D =500mA	-	0.96	1.6	Ω
		V _{GS} =4.5V,I _D =200mA	-	1.25	2.5	
		V _{GS} =2.5V,I _D =100mA	-	2.73	4.5	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} =50V, V_{GS} =0V	-	0.01	1	uA
Gate-Source Leakage Current	I_{GSS}	V _{GS} = <u>+</u> 20V,V _{DS} =0V	-	<u>+</u> 3.0	<u>+</u> 10	uA
Dynamic						
Total Gate Charge	Q_g	V _{DS} =25V, I _D =250mA, V _{GS} =4.5V ^(Note 1,2)	-	0.63	1	nC
Gate-Source Charge	Q_gs		-	0.2	-	
Gate-Drain Charge	Q_gd		-	0.23	-	
Input Capacitance	Ciss	V _{DS} =25V, V _{GS} =0V, f=1.0MHZ	-	25	50	pF
Output Capacitance	Coss		-	9.5	20	
Reverse Transfer Capacitance	Crss	I=1.UIVIAZ	-	2.1	5	
Switching						
Turn-On Delay Time	td _(on)	\/ O5\/ 500 ·· A	-	2.2	5	ns
Turn-On Rise Time	tr	$\begin{array}{c} V_{DD}{=}25V,\ I_{D}{=}500mA,\\ V_{GS}{=}10V,\\ R_{G}{=}6\Omega \end{array}$	-	19.2	38	
Turn-Off Delay Time	td _(off)		-	6.2	12	
Turn-Off Fall Time	tf		-	23	50	
Drain-Source Diode						
Maximum Continuous Drain-Source Diode Forward Current	I _S		-	-	500	mA
Diode Forward Voltage	V _{SD}	I _S =500mA, V _{GS} =0V	-	0.86	1.5	V

NOTES:

- 1. Pulse width<a>300us, Duty cycle<a>2%
- 2. Essentially independent of operating temperature typical characteristics.
- 3. R_{BUA} is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. mounted on a 1 inch square pad of copper





TYPICAL CHARACTERISTIC CURVES

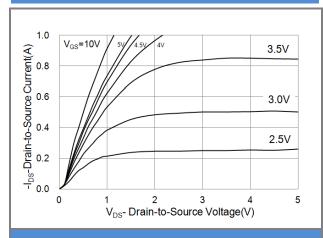


Fig.1 On-Region Characteristics

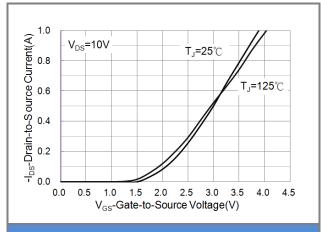


Fig.2 Transfer Characteristics

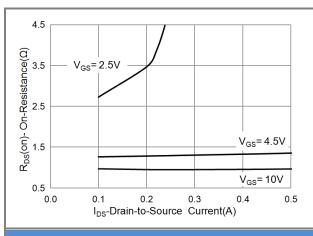


Fig.3 On-Resistance vs. Drain Current

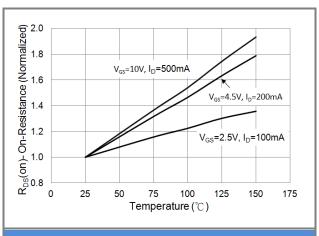


Fig.4 On-Resistance vs. Junction temperature

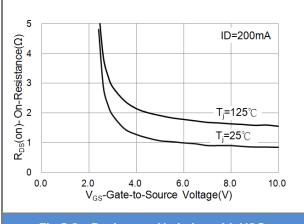


Fig.5 On-Resistance Variation with VGS.

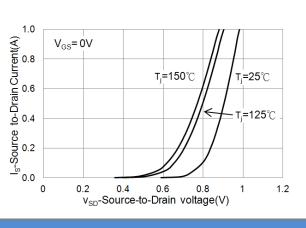


Fig.6 Body Dlode CharacterIsIcs





TYPICAL CHARACTERISTIC CURVES

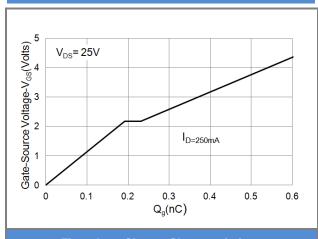


Fig.7 Gate-Charge Characteristics

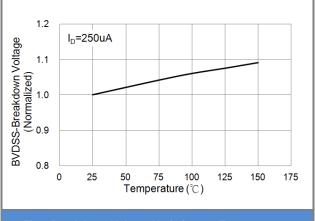


Fig.8 Breakdown Voltage Variation vs. Temperature

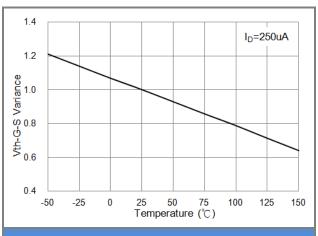


Fig.9 Threshold Voltage Variation with Temperature.

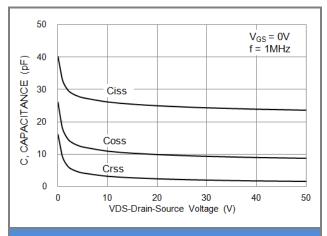


Fig.10 Capacitance vs. Drain-Source Voltage.

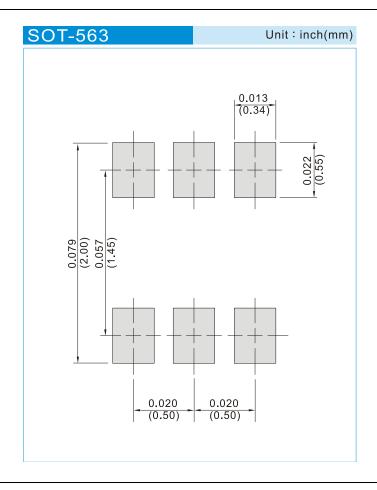




PART NO PACKING CODE VERSION

Part No Packing Code	Package Type	Packing type	Marking	Version
PJX138K_R1_00001	SOT-563	4K pcs / 7" reel	8KB	Halogen free
PJX138K_R2_00001	SOT-563	10K pcs / 13" reel	8KB	Halogen free
PJX138K_R1_00002	SOT-563	8K pcs / 7" reel	8KB	Halogen free
PJX138K_R2_00002	SOT-563	20K pcs / 13" reel	8KB	Halogen free

MOUNTING PAD LAYOUT







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