

FP1012V

High frequency, high current power inductors



Product features

- Vertical design utilizes less board space
- High current carrying capacity
- Operating frequency up to 3 MHz
- Inductance range from 70 nH to 470 nH
- Current range 22 A to 190 A
- 10.0 mm x 6.0 mm footprint surface mount package in 12 mm height
- Moisture sensitivity level (MSL): 1
- Ferrite core material
- Weight: 3.1 grams typical

Applications

- Multi-phase and Vcore regulators
- Voltage regulator modules (VRMs) and high power density VRMs
 - Server and desktop
 - Central processing unit (CPU)
 - Graphics processing unit (GPU)
 - Application specific integrated circuit (ASIC)
- Data networking and storage systems
- Graphics cards and battery power systems
- Point-of-Load modules

Environmental compliance and general specifications

- Storage temperature range (component): -40 °C to +125 °C
- Operating temperature range: -40 °C to +125 °C (ambient plus self-temperature rise)
- Solder reflow temperature: J-STD-020 (latest revision) compliant



Product specifications

Part number ⁸	OCL ¹ (nH) ±10%	FLL ² (nH) minimum	I _{avg} ³ (A)	I _{pk} ¹ (A)	I _{pk} ² (A)	I _{pk} ³ (A)	DCR (mΩ) @ +20 °C ±10%	K-factor ⁷
V2 version								
FP1012V2-R070-R	70	50	84	130+	130+	130+	0.125	305
FP1012V2-R080-R	80	57	84	130+	130+	125	0.125	305
FP1012V2-R090-R	90	64	84	130+	117	110	0.125	305
FP1012V2-R100-R	100	72	84	125	105	100	0.125	305
FP1012V2-R120-R	120	86	84	105	88	81	0.125	305
FP1012V2-R150-R	150	108	84	83	70	66	0.125	305
FP1012V2-R330-R	330	231	84	36	28	26	0.125	305
FP1012V2-R470-R	470 (±15%)	329	84	22	19	18	0.125	305
V3 version								
FP1012V3-R070-R	70	50	84	190	172	160	0.125	305
FP1012V3-R080-R	80	57	84	170	146	132	0.125	305
FP1012V3-R090-R	90	64	84	150	128	121	0.125	305
FP1012V3-R100-R	100	72	84	138	115	110	0.125	305
FP1012V3-R120-R	120	86	84	116	96	89	0.125	305
FP1012V3-R150-R	150	108	84	91	77	72	0.125	305
FP1012V3-R240-R	240	168	84	56	48	45	0.125	305
FP1012V3-R330-R	330	231	84	40	32	30	0.125	305

1. Open circuit inductance (OCL) test parameters: 100 kHz, 0.1 Vrms, 0.0 Adc, +25 °C

2. Full load inductance (FLL) test parameters: 100 kHz, 0.1 Vrms, I_{avg}¹, +25 °C

3. I_{avg}³: DC current for an approximate temperature rise of 40 °C without core loss. Derating is necessary for AC currents. PCB layout, trace thickness and width, air-flow, and proximity of other heat generating components will affect the temperature rise. It is recommended that the temperature of the part not exceed +125 °C under worst case operating conditions verified in the end application.

4. I_{pk}¹: Peak current for approximately 20% rolloff @ +25 °C

5. I_{pk}²: Peak current for approximately 20% rolloff @ +100 °C

6. I_{pk}³: Peak current for approximately 20% rolloff @ +125 °C

7. K-factor: Used to determine Bp-p for core loss (see graph). Bp-p = K * L * ΔI * 10⁻³. Bp-p:(Gauss), K: (K-factor from table), L: (Inductance in nH), ΔI (Peak to peak ripple current in Amps).

8. Part number definition: FP1012Vx-Rxxx-R

FP1012 = Product code and size

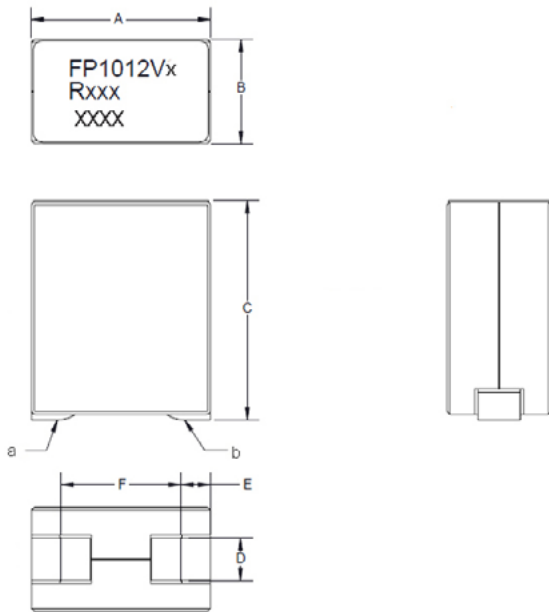
Vx= Version indicator

Rxxx=Inductance value in μH, R=decimal point

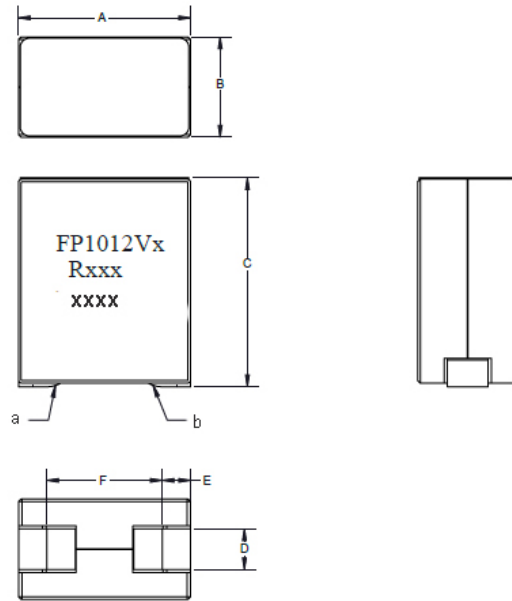
-R suffix = RoHS compliant

Dimensions-mm

FP1012V2

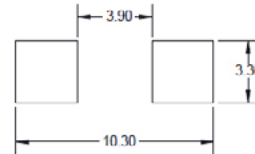


FP1012V3

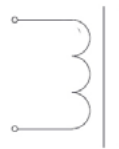


Dimension	FP1012V2/V3
A	10 maximum
B	6.0 maximum
C	12 maximum
D	2.3 nominal
E	1.6 reference
F	6.5 reference

Recommended pad layout FP1012V2/V3



Schematic FP1012V2/V3

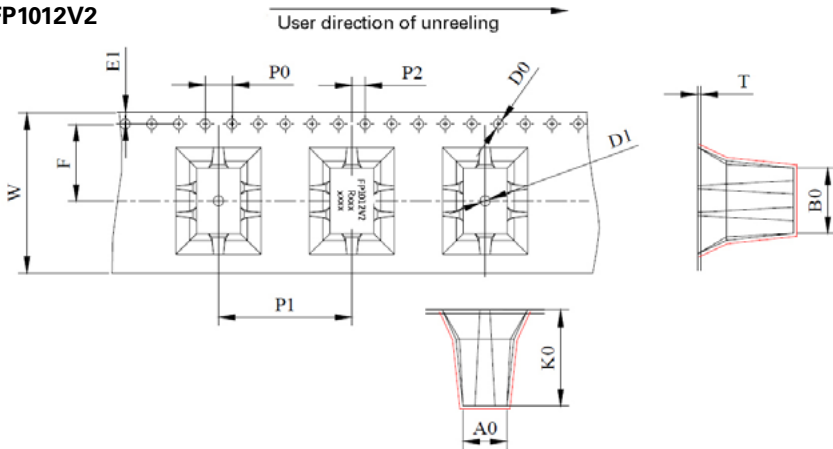


Part marking: FP1012=Product code and size, Vx=Version indicator, Rxxx= inductance value in uH, R=decimal point, xxxx= lot code
Tolerances are ± 0.15 millimeters unless stated otherwise
All soldering surfaces to be coplanar within 0.1 millimeters
Pad layout tolerances are ± 0.1 millimeters unless stated otherwise
DCR is measured from point "a" to point "b"
Traces or vias underneath the inductor is not recommended

Packaging information- mm

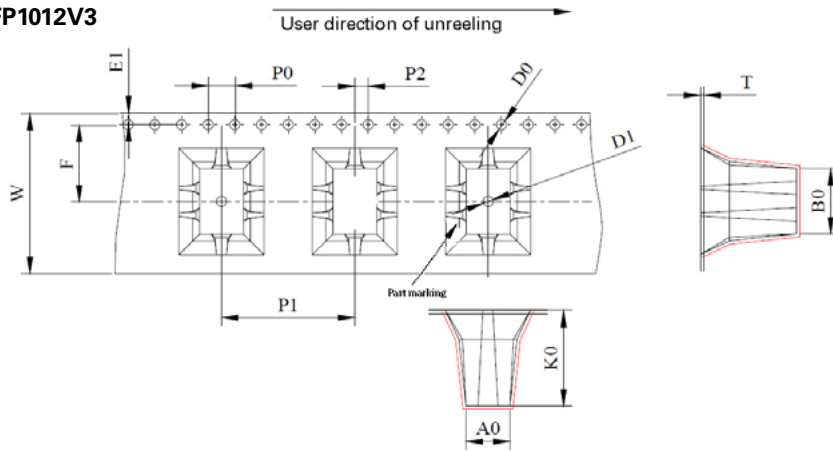
Supplied in tape and reel packaging, 250 parts per 13" diameter reel (EIA-481 compliant)

FP1012V2



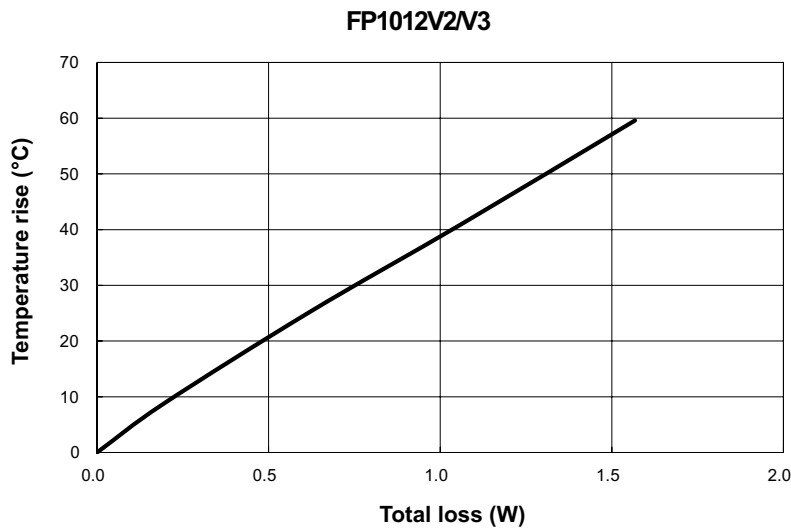
W ±0.3	24.00
F ±0.1	11.50
E1 ±0.10	1.75
P0 ±0.10	4.00
P1 ±0.10	20.00
P2 ±0.1	2.00
D0 +0.10/-0	1.50
D1 +0.10/-0	1.50
A0	6.2 ±0.10
B0	10.2 ±0.10
K0	12.2 ±0.10
T ±0.05	0.5

FP1012V3

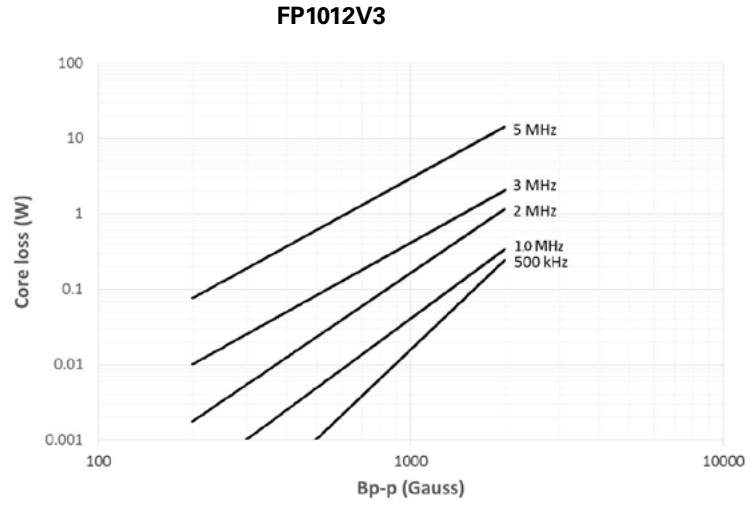
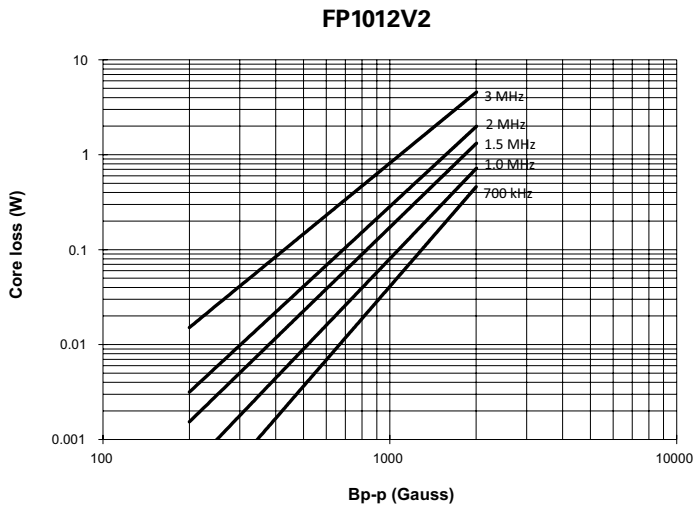


W ±0.3	24.00
F ±0.1	11.50
E1 ±0.10	1.75
P0 ±0.10	4.00
P1 ±0.10	20.00
P2 ±0.1	2.00
D0 +0.10/-0	1.50
D1 +0.10/-0	1.50
A0	6.2 ±0.10
B0	10.2 ±0.10
K0	12.2 ±0.10
T ±0.05	0.5

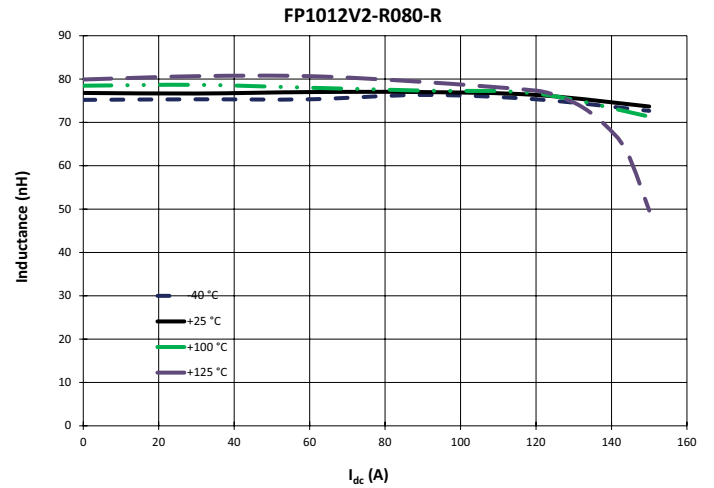
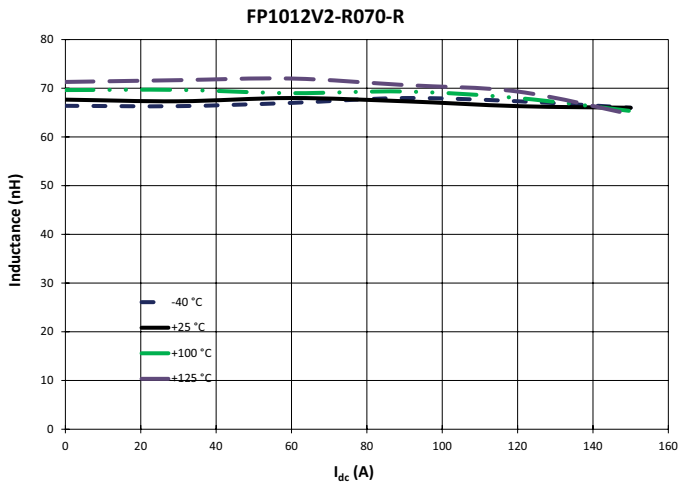
Temperature rise vs. total loss



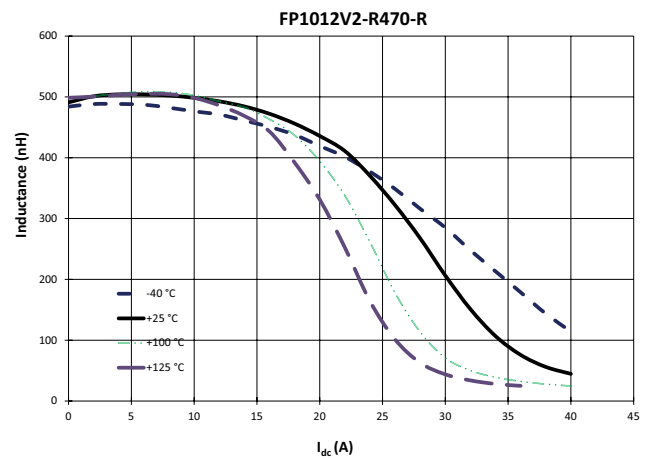
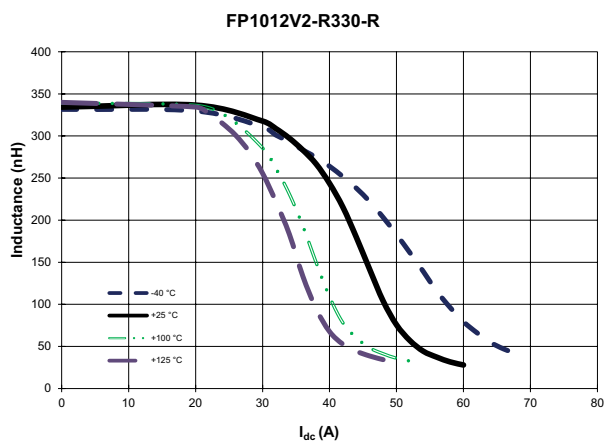
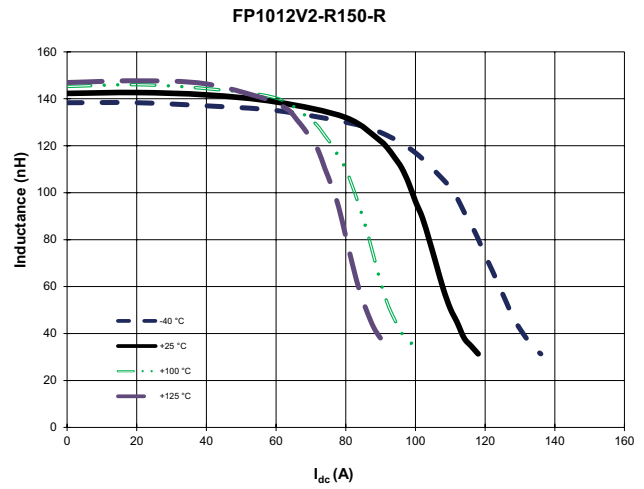
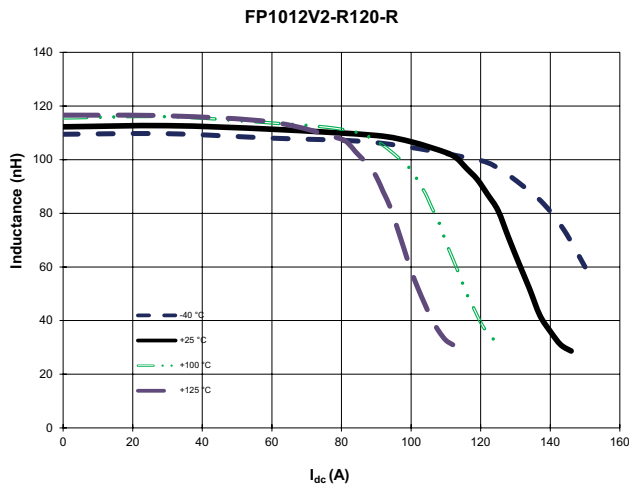
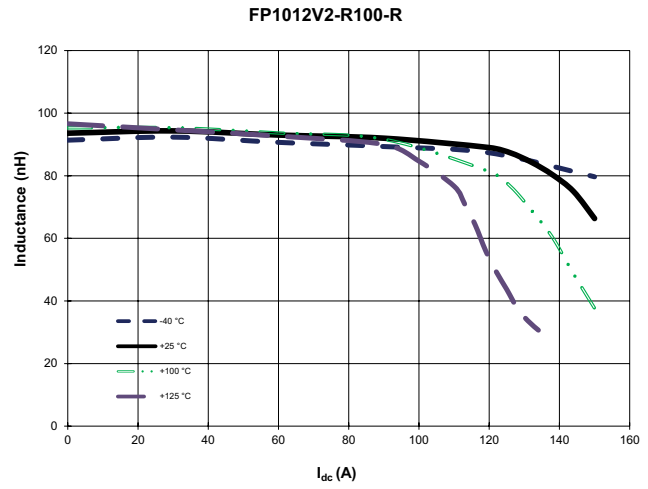
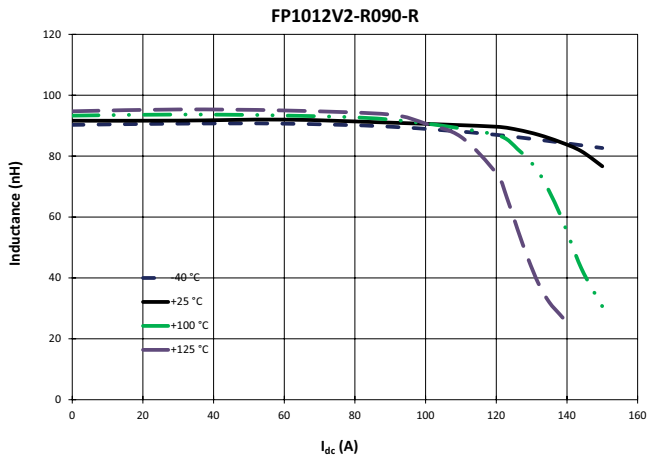
Core loss vs Bp-p



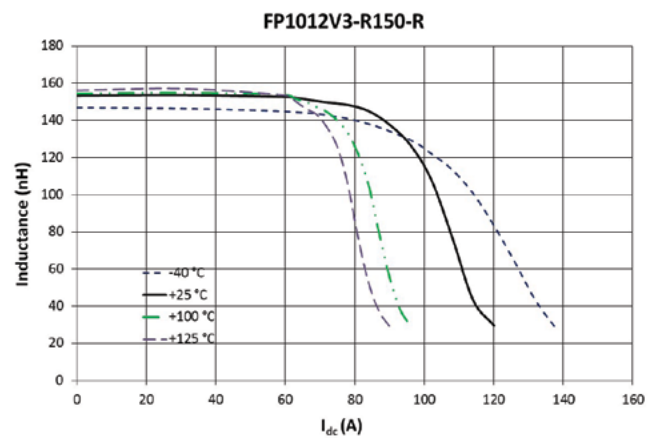
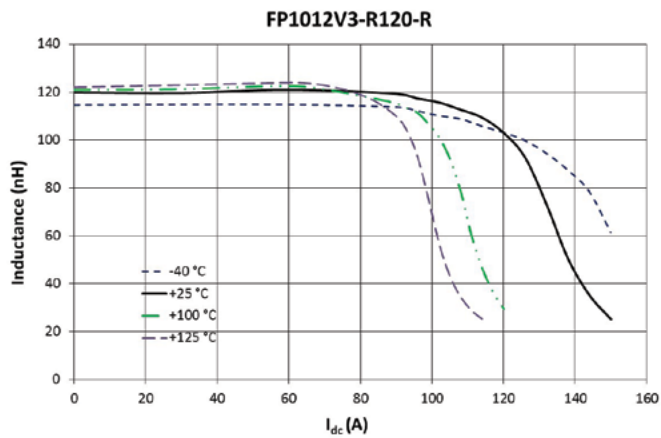
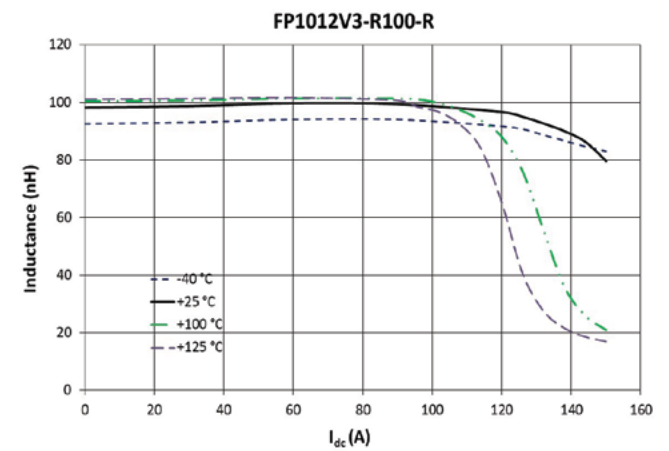
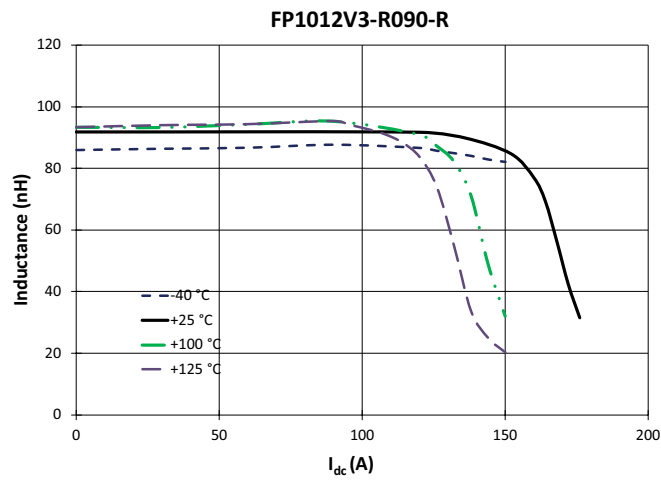
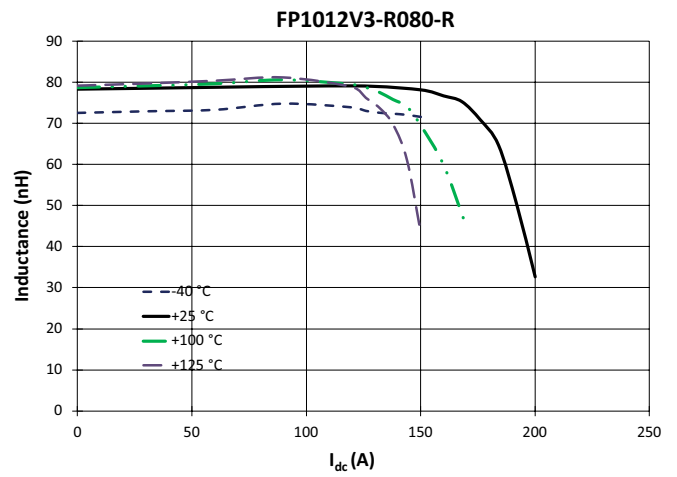
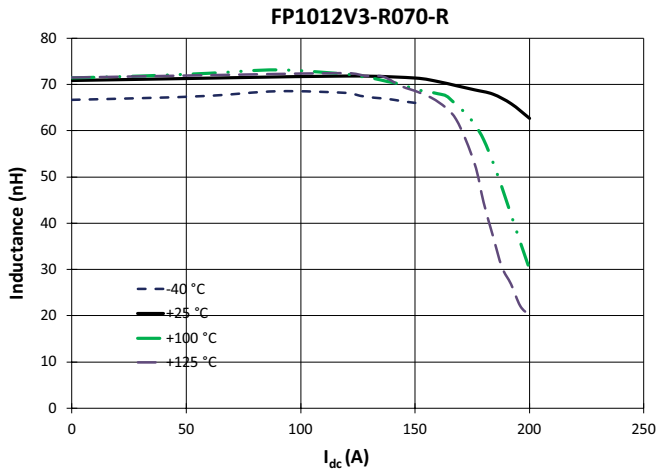
Inductance characteristics



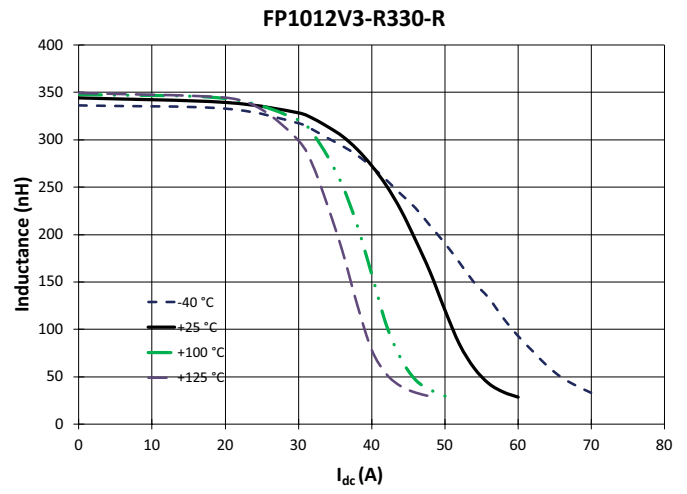
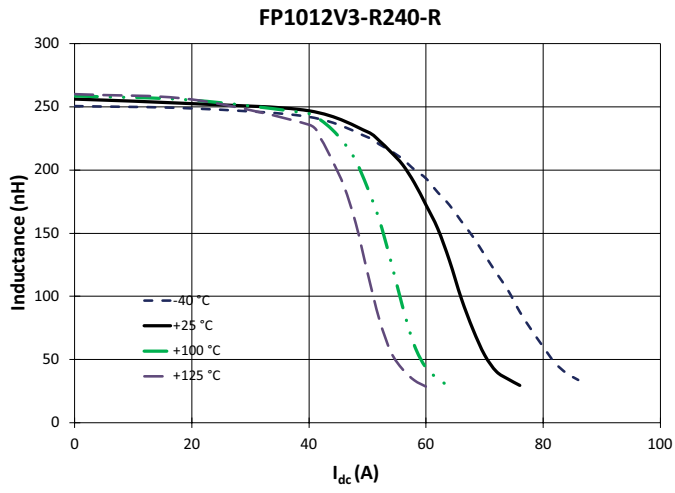
Inductance characteristics



Inductance characteristics



Inductance characteristics



Solder reflow profile

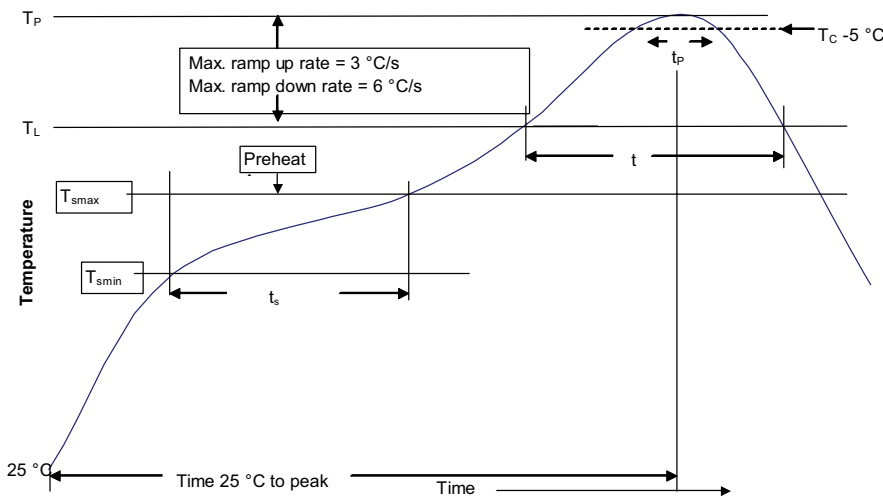


Table 1 - Standard SnPb solder (T_C)

Package thickness	Volume mm ³ <350	Volume mm ³ ≥350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2 - Lead (Pb) free solder (T_C)

Package thickness	Volume mm ³ <350	Volume mm ³ 350 - 2000	Volume mm ³ >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 – 2.5 mm	260 °C	250 °C	245 °C
>2.5 mm	250 °C	245 °C	245 °C

Reference J-STD-020

Profile feature	Standard SnPb solder	Lead (Pb) free solder
Preheat and soak		
• Temperature min. (T_{smin})	100 °C	150 °C
• Temperature max. (T_{smax})	150 °C	200 °C
• Time (T_{smin} to T_{smax}) (t_s)	60-120 seconds	60-120 seconds
Ramp up rate T_L to T_p	3 °C/ second max.	3 °C/ second max.
Liquidous temperature (T_L)	183 °C	217 °C
Time (t_L) maintained above T_L	60-150 seconds	60-150 seconds
Peak package body temperature (T_p)*	Table 1	Table 2
Time (t_p)* within 5 °C of the specified classification temperature (T_C)	20 seconds*	30 seconds*
Ramp-down rate (T_p to T_L)	6 °C/ second max.	6 °C/ second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

* Tolerance for peak profile temperature (T_p) is defined as a supplier minimum and a user maximum.

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