

# ACPL-4800

## High CMR Intelligent Power Module and Gate Drive Interface Optocoupler



### Data Sheet



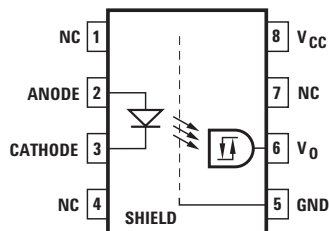
Lead (Pb) Free  
RoHS 6 fully compliant

RoHS 6 fully compliant options available;  
-xxxE denotes a lead-free product

#### Description

The ACPL-4800 fast speed optocoupler contains a GaAsP LED and photo detector with built-in Schmitt trigger to provide logic-compatible waveforms, eliminating the need for additional wave shaping. The totem pole output eliminates the need for a pull up resistor and allows for direct drive Intelligent Power Module or gate drive.

#### Functional Diagram

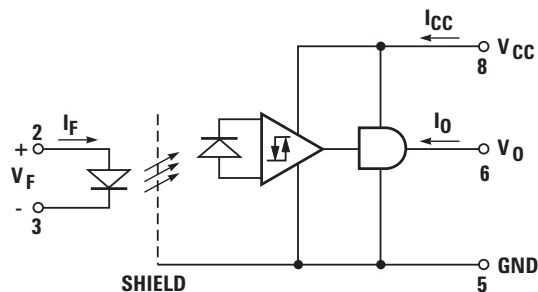


TRUTH TABLE  
(POSITIVE LOGIC)

LED	V <sub>O</sub>
ON	HIGH
OFF	LOW

Note: The connection of a 0.1  $\mu$ F bypass capacitor between pins 5 & 8 is recommended.

#### Schematic



#### Features

- Performance Specified for Fast IPM Applications over Industrial Temperature Range: -40°C to 100°C
- Wide Operating V<sub>CC</sub> Range: 4.5 to 20 Volts
- Typical Propagation Delays 150 ns
- Maximum Pulse Width Distortion PWD = 250 ns
- Propagation Delay Difference Min. -100 ns, Max. 250 ns
- 30 kV/ $\mu$ s Minimum Common Mode Transient Immunity at V<sub>CM</sub> = 1000 V
- Hysteresis
- Totem Pole Output (No Pull-up Resistor Required)
- Safety Approval:  
UL 1577, 3750 V<sub>rms</sub> / 1 minute  
CSA File CA88324, Notice #5  
IEC/EN/DIN EN 60747-5-2, V<sub>IORM</sub> = 630 V<sub>peak</sub>

#### Applications

- IPM Interface Isolation
- Isolated IGBT/MOSFET Gate Drive
- AC and Brushless DC Servo Motor Drives
- Low Power Inverters
- General Digital Isolation

**CAUTION:** It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and /or degradation which may be induced by ESD.

## Ordering Information

ACPL-4800 is UL Recognized with 3750 Vrms for 1 minute per UL1577 and is approved under CSA Component Acceptance Notice #5, File CA 88324.

Part number	Option		Surface Mount	Gull Wing	Tape & Reel	IEC/EN/DIN EN 60747-5-2	Quantity	
	RoHS Compliant	Package						
ACPL-4800	-000E	300mil DIP-8					50 per tube	
	-300E		X	X			50 per tube	
	-500E		X	X	X		1000 per reel	
	-060E						X	50 per tube
	-360E		X	X			X	50 per tube
	-560E		X	X	X		X	1000 per reel

To order, choose a part number from the part number column and combine with the desired option from the option column to form an order entry.

Example 1:

ACPL-4800-560E to order product of 300mil DIP Gull Wing Surface Mount package in Tape and Reel packaging with IEC/EN/DIN EN 60747-5-2 Safety Approval in RoHS compliant.

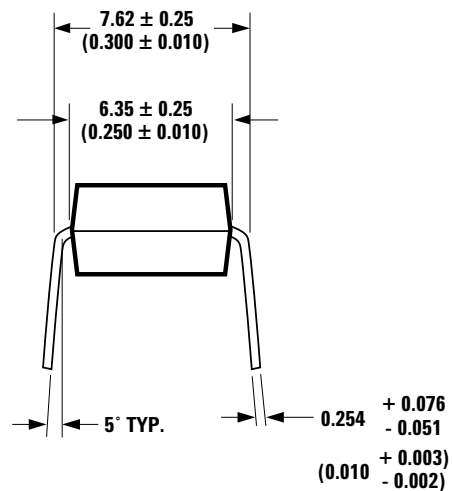
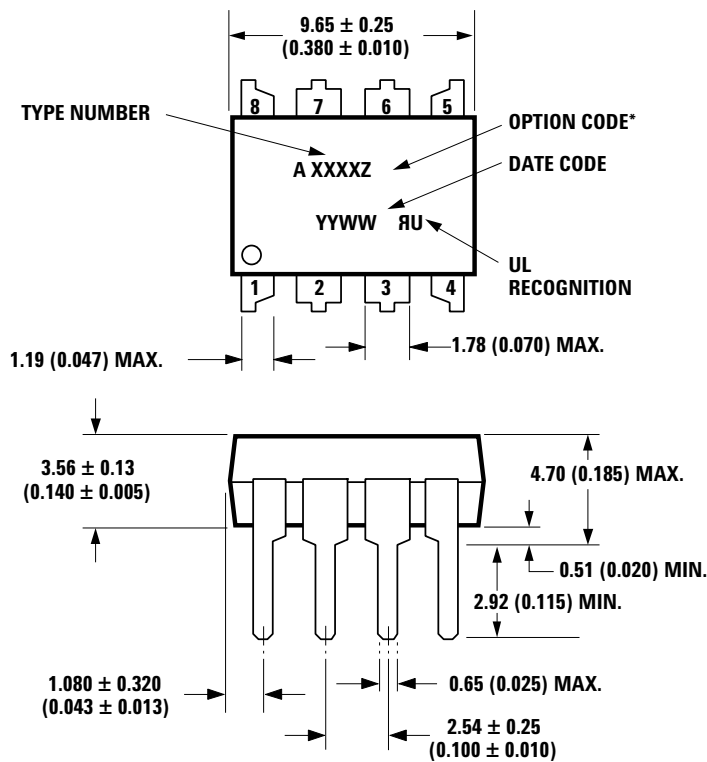
Example 2:

ACPL-4800-000E to order product of 300mil DIP package in tube packaging and RoHS compliant.

Option datasheets are available. Contact your Avago sales representative or authorized distributor for information.

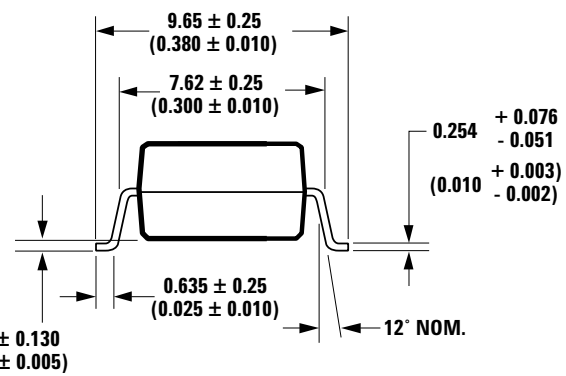
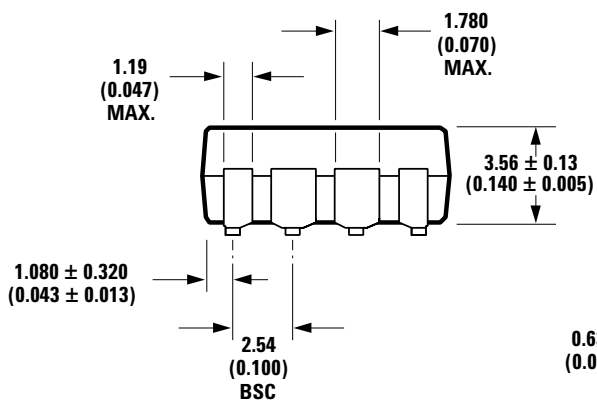
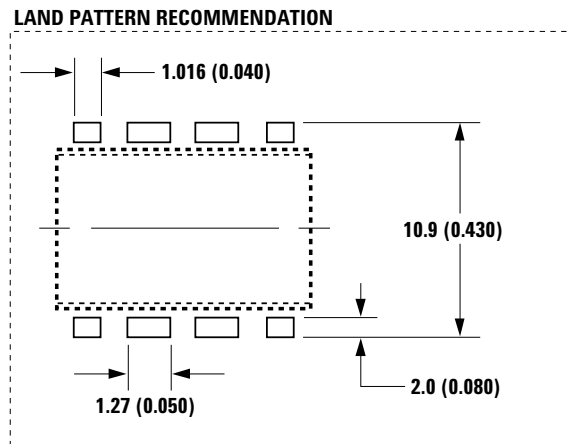
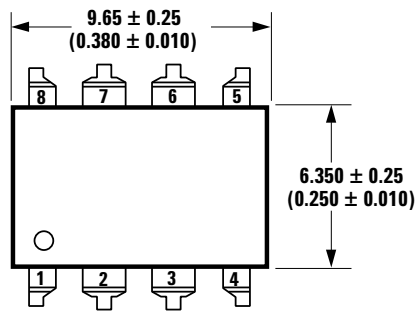
## Package Outline Drawings

### DIP-8 Package



DIMENSIONS IN MILLIMETERS AND (INCHES).  
 \* MARKING CODE LETTER FOR OPTION NUMBERS  
 "V" = OPTION 060  
 OPTION NUMBERS 300 AND 500 NOT MARKED.

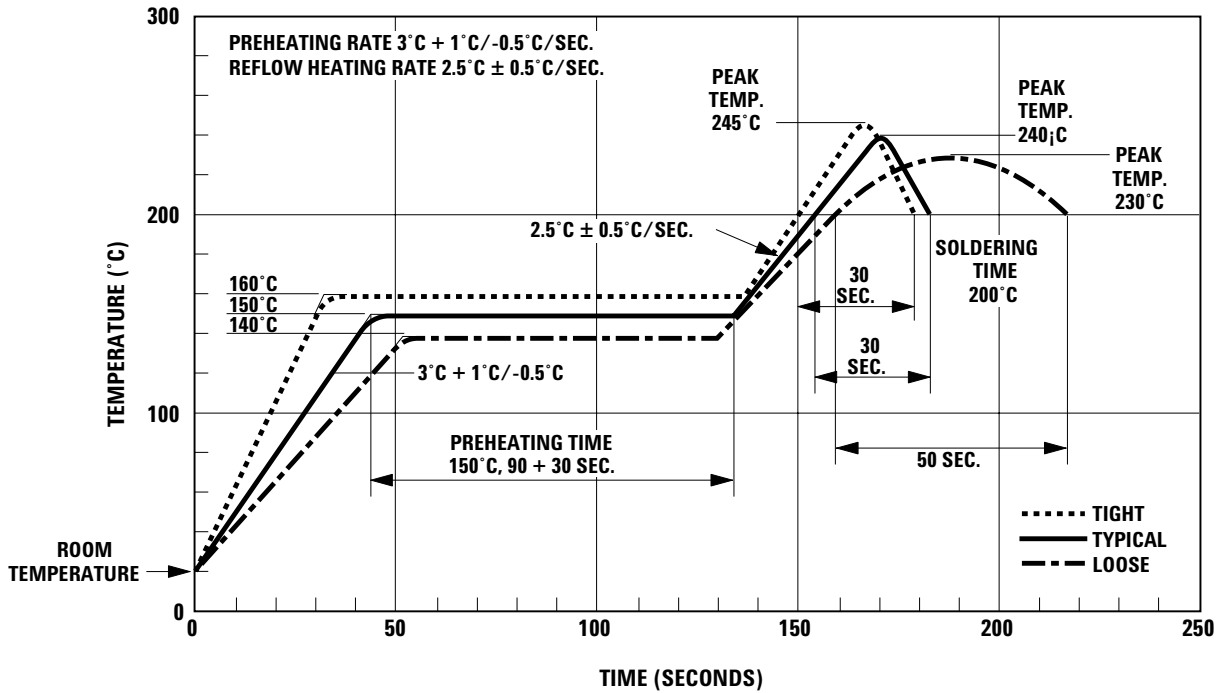
# DIP-8 Package with Gull Wing Surface Mount Option 300



DIMENSIONS IN MILLIMETERS (INCHES).  
LEAD COPLANARITY =  $0.10$  mm ( $0.004$  INCHES).

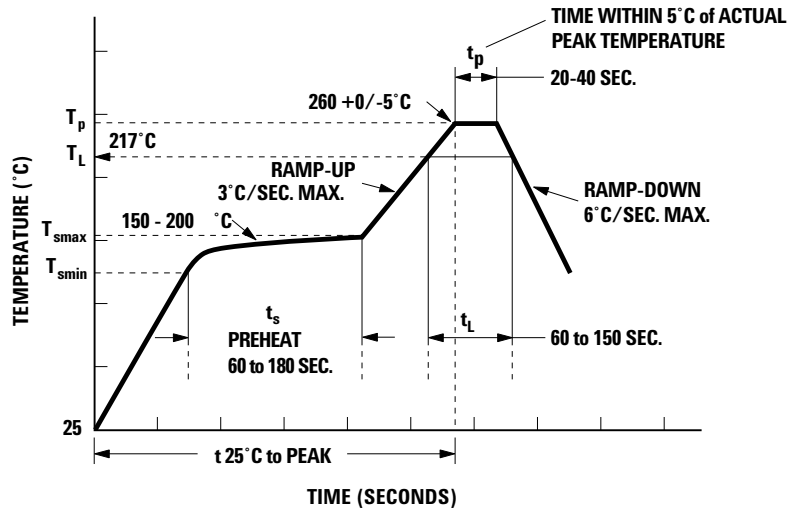
NOTE: FLOATING LEAD PROTRUSION IS  $0.25$  mm (10 mils) MAX.

### Solder Reflow Temperature Profile (Gull Wing Surface Mount Option 300 Parts)



Note: Non-halide flux should be used

### Recommended Pb-Free IR Profile



NOTES:  
 THE TIME FROM 25 C to PEAK TEMPERATURE = 8 MINUTES MAX.  
 $T_{smax} = 200^{\circ}\text{C}$ ,  $T_{smin} = 150^{\circ}\text{C}$

Note: Non-halide flux should be used

## Insulation and Safety Related Specifications

Parameter	Symbol	8-Pin DIP	Unit	Conditions
Minimum External Air Gap(External Clearance)	L(101)	7.1	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (External Creepage)	L(102)	7.4	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.08		Through insulation distance, conductor to conductor, usually the direct distance between the photo emitter and photo detector inside the optocoupler cavity.
Minimum Internal Tracking (Internal Creepage)		NA	mm	Measured from input terminals to output terminals, along internal cavity.
Tracking Resistance (Comparative Tracking Index)	CTI	200	mm	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

Option 300 - surface mount classification is Class A in accordance with CECC 00802.

## IEC/EN/DIN EN 60747-5-2 Insulation Characteristics (Option 060)

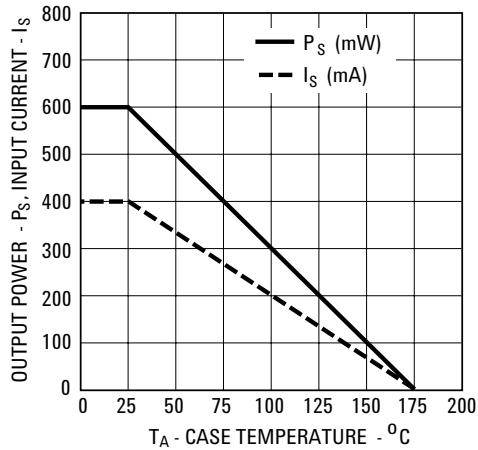
Description	Symbol	Characteristic	Unit
Installation classification per DIN VDE 0110/1.89, Table 1			
for rated mains voltage $\leq 300 V_{rms}$		I-IV	
for rated mains voltage $\leq 450 V_{rms}$		I-III	
Climatic Classification		55/85/21	
Pollution Degree (DIN VDE 0110/1.89)		2	
Maximum Working Insulation Voltage	$V_{IORM}$	630	$V_{peak}$
Input to Output Test Voltage, Method b* $V_{IORM} \times 1.875 = V_{PR}$ , 100% Production Test with $t_m = 1$ sec, Partial discharge $< 5$ pC	$V_{PR}$	1181	$V_{peak}$
Input to Output Test Voltage, Method a* $V_{IORM} \times 1.5 = V_{PR}$ , Type and Sample Test, $t_m = 60$ sec, Partial discharge $< 5$ pC	$V_{PR}$	945	$V_{peak}$
Highest Allowable Over-voltage(Transient Over-voltage $t_{ini} = 10$ sec)	$V_{IOTM}$	6000	$V_{peak}$
Safety-limiting values - maximum values allowed in the event of a failure.			
Case Temperature	$T_S$	175	$^{\circ}C$
Input Current	$I_{S, INPUT}$	230	mA
Output Power (refer to Thermal Derating Curve)	$P_{S, OUT-PUT}$	600	mW
Insulation Resistance at $T_S$ , $V_{IO} = 500$ V	$R_S$	$> 10^9$	$\Omega$

\* Refer to the optocoupler section of the Isolation and Control Components Designer's Catalog, under Product Safety Regulations section, (IEC/EN/DIN EN 60747-5-2) for a detailed description of Method a and Method b partial discharge test profiles.

Note:

Isolation characteristics are guaranteed only within the safety maximum ratings which must be ensured by protective circuits in application.

## Thermal Derating Curve



## Absolute Maximum Rating

Parameter	Symbol	Min.	Max.	Units	Note
Storage Temperature	$T_S$	-55	125	$^{\circ}\text{C}$	
Operating Temperature	$T_A$	-40	100	$^{\circ}\text{C}$	
Average Forward Input Current	$I_{F(AVG)}$		10	mA	
Peak Transient Input Current ( $\leq 1 \mu\text{s}$ Pulse Width, 300 pps) ( $\leq 200 \mu\text{s}$ Pulse Width, < 1% Duty Cycle)	$I_{F(TRAN)}$		1.0 40	A mA	
Reverse Input Voltage	$V_R$		5	V	
Average Output Current	$I_O$		25	mA	
Supply Voltage	$V_{CC}$	0	25	V	
Output Voltage	$V_O$	-0.5	25	V	
Total Package Power Dissipation	$P_T$		210	mW	1
Lead Solder Temperature (Through Hole Parts Only)		260 $^{\circ}\text{C}$ for 10 sec., 1.6 mm below seating plane			
Solder Reflow Temperature Profile (Surface Mount Parts Only)		See Package Outline Drawings section			

## Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Power Supply Voltage	$V_{CC}$	4.5	20	V
Forward Input Current (ON)	$I_{F(ON)}$	6	10	mA
Forward Input Voltage (OFF)	$V_{F(OFF)}$	-	0.8	V
Operating Temperature	$T_A$	-40	100	$^{\circ}\text{C}$

## Electrical Specification

$-40^{\circ}\text{C} \leq T_A \leq 100^{\circ}\text{C}$ ,  $4.5\text{V} \leq V_{CC} \leq 20\text{V}$ ,  $6\text{mA} \leq I_{F(\text{ON})} \leq 10\text{mA}$ ,  $0\text{V} \leq V_{F(\text{OFF})} \leq 0.8\text{V}$ , unless otherwise specified.

All Typicals at  $T_A = 25^{\circ}\text{C}$ .

Parameter	Sym.	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Logic Low Output Voltage	$V_{OL}$			0.5	V	$I_{OL} = 6.4\text{mA}$	1, 3	
Logic High Output Voltage	$V_{OH}$	2.4	$V_{CC} - 1.1\text{V}$		V	$I_{OH} = -2.6\text{mA}$ $I_{OH} = -0.4\text{mA}$	2, 3, 7	
Output Leakage Current ( $V_{OUT} = V_{CC} + 0.5\text{V}$ )	$I_{OHH}$			100 500	$\mu\text{A}$	$V_{CC} = 5\text{V}$ $V_{CC} = 20\text{V}$	$I_F = 10\text{mA}$	
Logic Low Supply Current	$I_{CCL}$		1.9 2.0	3.0 3.0	mA	$V_{CC} = 5.5\text{V}$ $V_{CC} = 20\text{V}$	$V_F = 0\text{V}$ $I_O = \text{Open}$	
Logic High Supply Current	$I_{CCH}$		1.5 1.6	2.5 2.5	mA	$V_{CC} = 5.5\text{V}$ $V_{CC} = 20\text{V}$	$I_F = 10\text{mA}$ $I_O = \text{Open}$	
Logic Low Short Circuit Output Current	$I_{OSL}$	25 50			mA	$V_O = V_{CC} = 5.5\text{V}$ $V_O = V_{CC} = 20\text{V}$	$V_F = 0\text{V}$	2
Logic High Short Circuit Output Current	$I_{OSH}$			-25 -50	mA	$V_{CC} = 5.5\text{V}$ $V_{CC} = 20\text{V}$	$I_F = 6\text{mA}$ $V_O = \text{GND}$	2
Input Forward Voltage	$V_F$		1.5	1.7 1.85	V	$T_A = 25\text{C}$	$I_F = 6\text{mA}$	4
Input Reverse Breakdown Voltage	$BV_R$	5			V	$I_R = 10\ \mu\text{A}$		
Input Diode Temperature Coefficient	$\Delta V_F$ $\Delta T_A$		-1.7		mV/ $^{\circ}\text{C}$	$I_F = 6\text{mA}$		
Input Capacitance	$C_{IN}$		60		pF	$f = 1\text{MHz}$ , $V_F = 0\text{V}$		3

## Switching Specifications (AC)

$-40^{\circ}\text{C} \leq T_A \leq 100^{\circ}\text{C}$ ,  $4.5\text{V} \leq V_{\text{CC}} \leq 20\text{V}$ ,  $6\text{mA} \leq I_{\text{F(ON)}} \leq 10\text{mA}$ ,  $0\text{V} \leq V_{\text{F(OFF)}} \leq 0.8\text{V}$ .

All Typicals at  $T_A = 25^{\circ}\text{C}$ ,  $I_{\text{F(ON)}} = 6\text{mA}$  unless otherwise specified.

Parameter	Sym.	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Propagation Delay Time to Logic Low Output Level	$t_{\text{PHL}}$		150	350	ns	With Peaking Capacitor	5,6	5
Propagation Delay Time to Logic High Output Level	$t_{\text{PLH}}$		110	350	ns	With Peaking Capacitor	5,6	5
Pulse Width Distortion	PWD			250	ns	$ t_{\text{PHL}} - t_{\text{PLH}} $		8
Propagation Delay Difference Between Any 2 Parts	PDD	-100		250	ns			10
Output Rise Time (10-90%)	$t_r$		16		ns		5,8	
Output Fall Time (90-10%)	$t_f$		20		ns		5,8	
Logic High Common Mode Transient Immunity	$ C_{\text{MH}} $	-30000			V/ $\mu\text{s}$	$ V_{\text{CM}}  = 1000\text{V}$ , $I_{\text{F}} = 6.0\text{mA}$ , $V_{\text{CC}} = 5\text{V}$ , $T_A = 25^{\circ}\text{C}$	9	6
Logic Low Common Mode Transient Immunity	$ C_{\text{ML}} $	30000			V/ $\mu\text{s}$	$ V_{\text{CM}}  = 1000\text{V}$ , $V_{\text{F}} = 0\text{V}$ , $V_{\text{CC}} = 5\text{V}$ , $T_A = 25^{\circ}\text{C}$	9	6

## Package Characteristics

Parameter	Sym.	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Input-Output Momentary Withstand Voltage*	$V_{\text{ISO}}$	3750			$V_{\text{rms}}$	$\text{RH} < 50\%$ , $t = 1\text{min}$ , $T_A = 25^{\circ}\text{C}$		4,7
Input-Output Resistance	$R_{\text{I-O}}$		$10^{12}$		$\Omega$	$V_{\text{I-O}} = 500\text{Vdc}$		4
Input-Output Capacitance	$C_{\text{I-O}}$		0.6		pF	$f = 1\text{MHz}$ , $V_{\text{I-O}} = 0\text{Vdc}$		4

\* The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating refer to the IEC/EN/DIN EN 60747-5-2 Insulation Characteristics Table (if applicable), your equipment level safety specification or Avago Application Note 1074 entitled "Optocoupler Input-Output Endurance Voltage," publication number 5963-2203E.

### Notes:

- Derate total package power dissipation,  $P_T$ , linearly above  $70^{\circ}\text{C}$  free-air temperature at a rate of  $4.5\text{mW}/^{\circ}\text{C}$ .
- Duration of output short circuit time should not exceed 10 ms.
- Input capacitance is measured between pin 2 and pin 3.
- Device considered a two-terminal device: pins 1, 2, 3, and 4 shorted together and pins 5, 6, 7, and 8 shorted together.
- The  $t_{\text{PLH}}$  propagation delay is measured from the 50% point on the leading edge of the input pulse to the 1.3 V point on the leading edge of the output pulse. The  $t_{\text{PHL}}$  propagation delay is measured from the 50% point on the trailing edge of the input pulse to the 1.3 V point on the trailing edge of the output pulse.
- $C_{\text{MH}}$  is the maximum slew rate of the common mode voltage that can be sustained with the output voltage in the logic high state,  $V_O > 2.0\text{V}$ .  $C_{\text{ML}}$  is the maximum slew rate of the common mode voltage that can be sustained with the output voltage in the logic low state,  $V_O < 0.8\text{V}$ .
- In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage  $\geq 4500\text{V rms}$  for one second (leakage detection current limit,  $\text{II-O} \leq 5\mu\text{A}$ ). This test is performed before the 100% production test for partial discharge (Method b) shown in the IEC/EN/DIN EN 60747-5-2 Insulation Characteristics Table, if applicable.
- Pulse Width Distortion (PWD) is defined as  $|t_{\text{PHL}} - t_{\text{PLH}}|$  for any given device.
- Use of a  $0.1\mu\text{F}$  bypass capacitor connected between pins 5 and 8 is recommended.
- The difference between  $t_{\text{PLH}}$  and  $t_{\text{PHL}}$  between any two devices under the same test condition.



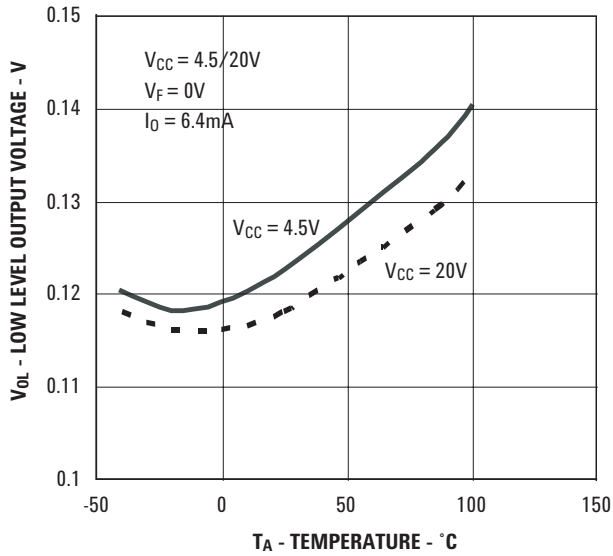


Figure 1. Typical Logic Low Output Voltage vs. Temperature

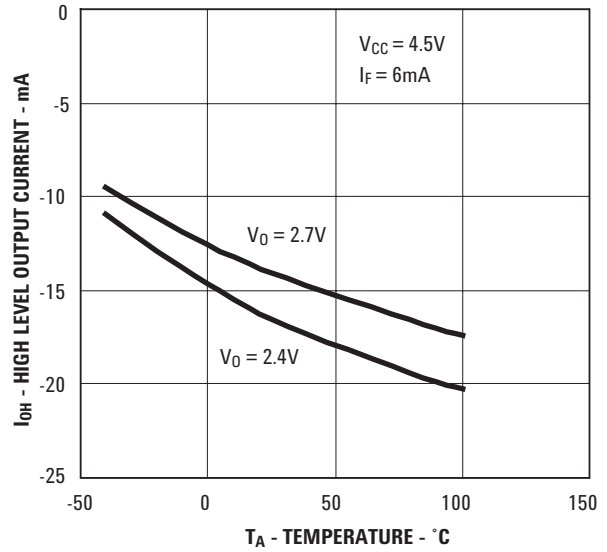


Figure 2. Typical Logic High Output Current vs. Temperature

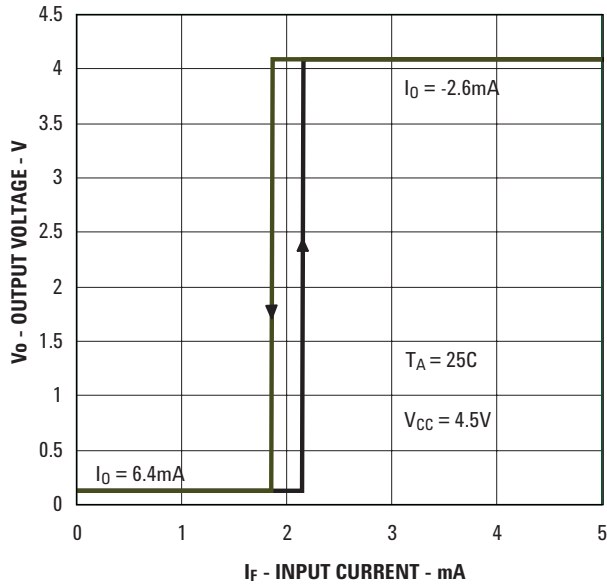


Figure 3. Typical Output Voltage vs. Forward Input Current

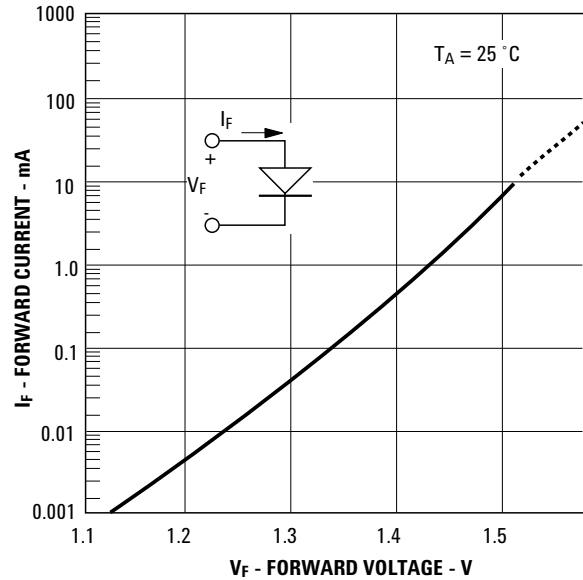


Figure 4. Typical Input Diode Forward Characteristic

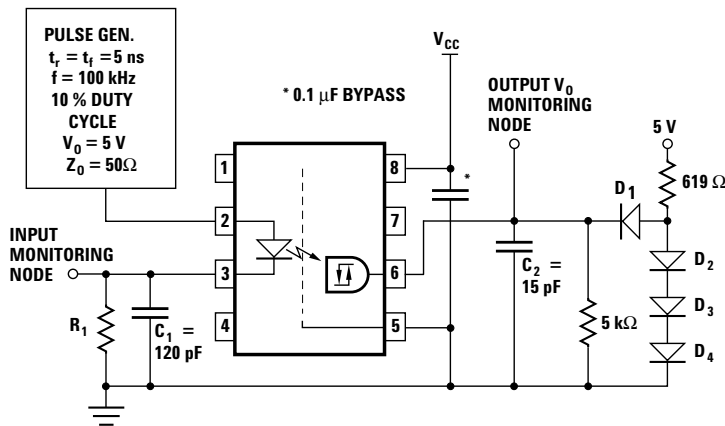
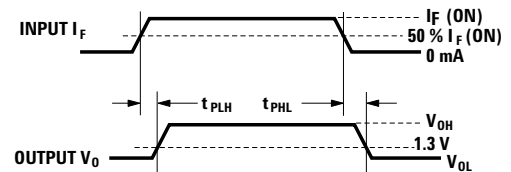


Figure 5. Test Circuit for  $t_{PLH}$ ,  $t_{PHL}$ ,  $t_r$ ,  $t_f$

THE PROBE AND JIG CAPACITANCES ARE INCLUDED IN C1 AND C2.

$R_1$	1.10 k $\Omega$	681 $\Omega$	330 $\Omega$
$I_F$ (ON)	3 mA	5 mA	10 mA

ALL DIODES ARE 1N916 OR 1N3064.



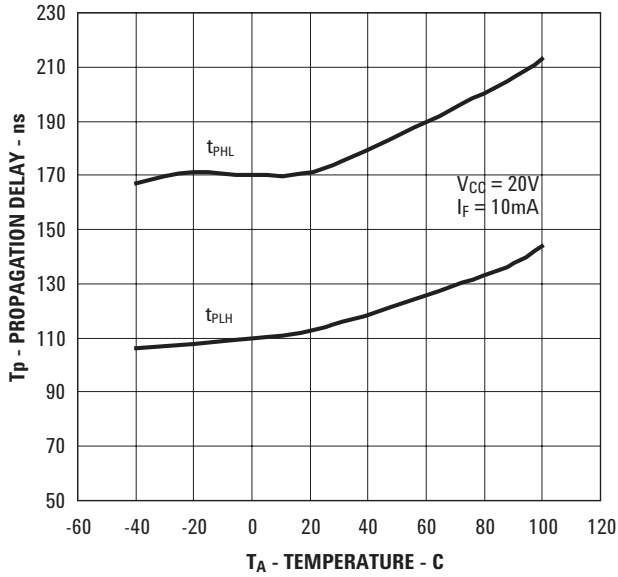


Figure 6. Typical Propagation Delays vs. Temperature.

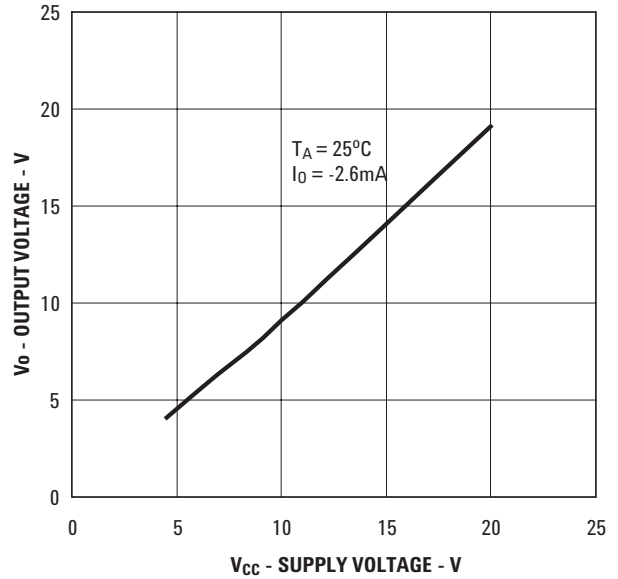


Figure 7. Typical Logic High Output Voltage vs. Supply Voltage

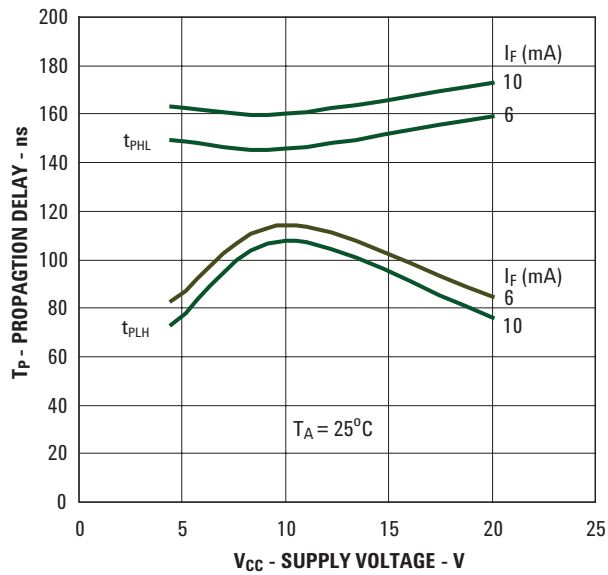


Figure 8. Typical Propagation Delay vs. Supply Voltage

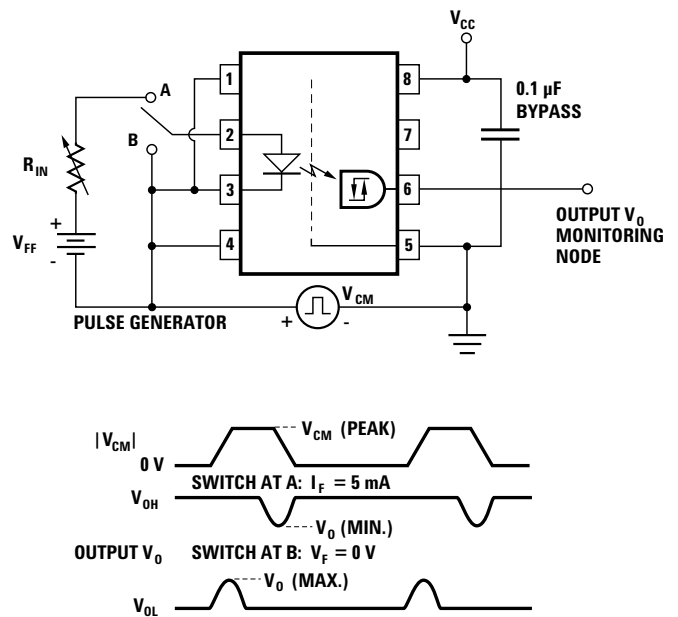


Figure 9. Test Circuit for Common Mode Transient Immunity and Typical Waveforms

For product information and a complete list of distributors, please go to our web site: [www.avagotech.com](http://www.avagotech.com)

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