SNx5HVD308xE Low-Power RS-485 Transceivers

1 Features

- Meets or exceeds the requirements of the TIA/EIA-485A standard
- Low quiescent power
  - 0.3-mA Active mode
  - 1-nA Shutdown Mode
- 1/8 Unit load up to 256 nodes on a bus
- Bus-Pin ESD protection up to 15 kV
- Industry-standard SN75176 footprint
- Failsafe receiver (bus open, bus shorted, bus idle)
- Glitch-free power-up and power-down bus inputs and outputs

2 Applications

- Energy meter networks
- Motor control
- Power inverters
- Industrial automation
- Building automation networks
- Battery-powered applications
- Telecommunications equipment

3 Description

The SNx5HVD308xE are half-duplex transceivers designed for RS-485 data bus networks. Powered by a 5-V supply, they are fully compliant with TIA/EIA-485A standard. With controlled transition times, these devices are suitable for transmitting data over long twisted-pair cables. The SN65HVD3082E and SN75HVD3082E are optimized for signaling rates up to 200 kbps. The SN65HVD3085E is suitable for data transmission up to 1 Mbps, whereas the SN65HVD3088E is suitable for applications that require signaling rates up to 20 Mbps.

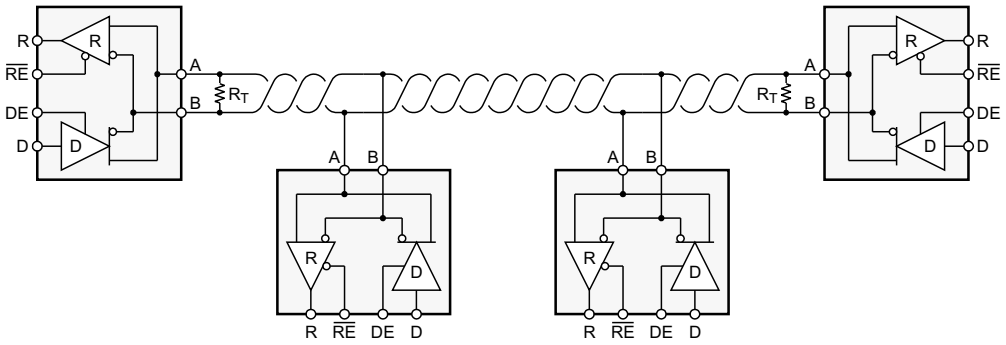
These devices are designed to operate with very low supply current, typically 0.3 mA, exclusive of the load. When in the inactive-shutdown mode, the supply current drops to a few nanoamps, which makes these devices ideal for power-sensitive applications.

The wide common-mode range and high ESD protection levels of these devices makes them suitable for demanding applications such as energy meter networks, electrical inverters, status and command signals across telecom racks, cabled chassis interconnects, and industrial automation networks where noise tolerance is essential. These devices match the industry-standard footprint of the SN75176 device. Power-on-reset circuits keep the outputs in a high-impedance state until the supply voltage has stabilized. A thermal-shutdown function protects the device from damage due to system fault conditions. The SN75HVD3082E is characterized for operation from 0°C to 70°C and SN65HVD308xE are characterized for operation from –40°C to 85°C air temperature. The D package version of the SN65HVD3082E has been characterized for operation from –40°C to 105°C.

Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
SN65HVD3082E SN65HVD3088E	SOIC (D) (8)	4.90 mm × 3.91 mm
	VSSOP (DGK) (8)	3.00 mm × 3.00 mm
	PDIP (P) (8)	9.81 mm × 6.35 mm
SN75HVD3082E SN65HVD3085E	SOIC (D) (8)	4.90 mm × 3.91 mm
	VSSOP (DGK) (8)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Schematic

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision K (July 2021) to Revision L (November 2021)	Page
• Deleted *Feature*: Available in a small MSOP-8 package	1
• Deleted Available in a Small MSOP-8 Package from the title	1
• Changed the ψ_{JT} D package value from 78.8 to 8.8 in the Thermal Information	5

Changes from Revision J (October 2017) to Revision K (July 2021)	Page
• Changed the *Thermal Information* section	5

Changes from Revision I (September 2016) to Revision J (October 2017)	Page
• Changed 3.3 V to 5 V on the V_{CC} pin in Figure 9-4	19

Changes from Revision H (August 2015) to Revision I (September 2016)	Page
• Added text to the *Section 3,* "The D package version of the SN65HVD3082E has been characterized for operation from -40°C to 105°C."	1
• Changed the Operating free-air temperature for SN65HVD3082E (D package) From: MAX = 85°C To: 105°C in *Section 6.3*	5

Changes from Revision G (May 2009) to Revision H (August 2015)	Page
• Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1
• Deleted *Dissipation Ratings* table	1
• Added storage temperature T_{stg} to *Absolute Maximum Ratings* table	4

- Deleted *Package Thermal Information* table 6

Changes from Revision F (March 2009) to Revision G (May 2009) **Page**

- Added Graph - *Driver Rise and Fall Time vs Temperature* 9
- Added IDLE Bus to the *Function* Table..... 15
- Added *Receiver Failsafe* section..... 19

5 Pin Configuration and Functions

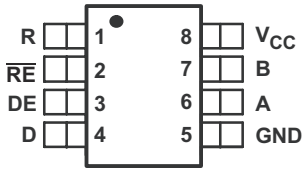


Figure 5-1. D (SOIC), P (PDIP), and DGK (VSSOP) Packages, 8-Pin, Top View

Table 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
A	6	Bus input/output	Driver output or receiver input (complementary to B)
B	7	Bus input/output	Driver output or receiver input (complementary to A)
D	4	Digital input	Driver data input
DE	3	Digital input	Driver enable, active high
GND	5	Reference potential	Local device ground
R	1	Digital output	Receive data output
$\overline{RE}$	2	Digital input	Receiver enable, active low
V_{CC}	8	Supply	4.5-V to 5.5-V supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range unless otherwise noted(1) (2)

	MIN	MAX	UNIT
Supply voltage, V_{CC}	–0.5	7	V
Voltage at A or B	–9	14	V
Voltage at any logic pin	–0.3	V_{CC} + 0.3	V
Receiver output current	–24	24	mA
Voltage input, transient pulse, A and B, through 100 Ω (see Figure 7-13)	–50	50	V
Junction Temperature, T_J		170	°C
Storage temperature, T_{stg}		150	°C

(1) Operation outside the *Absolute Maximum Ratingss* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime
(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	Bus pins and GND	±15000	V
			All pins	±4000	
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)		±1000	
		Electrical Fast Transient/Burst, A, B, and GND(3)		±4000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.
(3) Tested in accordance with IEC 61000-4-4.

6.3 Recommended Operating Conditions

over operating free-air temperature range unless otherwise noted(1)

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.5		5.5	V
Voltage at any bus terminal (separately or common mode) , V_I		–7		12	V
High-level input voltage (D, DE, or $\overline{RE}$ inputs), V_{IH}		2		V_{CC}	V
Low-level input voltage (D, DE, or $\overline{RE}$ inputs), V_{IL}		0		0.8	V
Differential input voltage, V_{ID}		–12		12	V
Output current, I_O	Driver	–60		60	mA
	Receiver	–8		8	
Differential load resistance, R_L		54	60		Ω
Signaling rate, $1/t_{UI}$	SN65HVD3082E, SN75HVD3082E			0.2	Mbps
	SN65HVD3085E			1	
	SN65HVD3088E			20	
Operating free-air temperature, T_A	SN65HVD3082E (D package)	–40		105	°C
	SN65HVD3082E (DGK and P packages), SN65HVD3085E, SN65HVD3088E	–40		85	
	SN75HVD3082E	0		70	
Junction temperature, T_J		–40		130	°C

(1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet.

6.4 Thermal Information

THERMAL METRIC(1)		SN65HVD3085E, SN65HVD3088E		SN65HVD3088E	UNIT
		D (SOIC)	DGK (VSSOP)	P (PDIP)	
		8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	130	180	70	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	80	66	80	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	55	110	40	°C/W
ψ_{JT}	Junction-to-top characterization parameter	7.9	4.6	17.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	47	73.1	28.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Thermal Information

THERMAL METRIC(1)		SN65HVD3082E, SN75HVD3082E		SN65HVD3082E	UNIT
		D (SOIC)	DGK (VSSOP)	P (PDIP)	
		8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	114.4	142.2	88.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	55.1	35.8	65.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	61.6	75.6	69.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	8.8	0.8	35.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	60.8	74.8	64.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.6 Electrical Characteristics: Driver

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
$\|V_{OD}\|$	Differential output voltage	I_O = 0, No Load	3	4.3		V
		R_L = 54 Ω (see Figure 7-1)	1.5	2.3		
		R_L = 100 Ω	2			
		V_{TEST} = –7 V to 12 V (see Figure 7-2)	1.5			
$\Delta\|V_{OD}\|$	Change in magnitude of differential output voltage	See Figure 7-1 and Figure 7-2	–0.2	0	0.2	V
$V_{OC(SS)}$	Steady-state common-mode output voltage	See Figure 7-3	1	2.6	3	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage		–0.1	0	0.1	
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage	See Figure 7-3		500		mV
I_{OZ}	High-impedance output current	See receiver input currents in Electrical Characteristics: Receiver				
I_I	Input current	D, DE	–100		100	μA
I_{OS}	Short-circuit output current	−7 V ≤ V_O ≤ 12 V (see Figure 7-7)	–250		250	mA

(1) All typical values are at 25°C and with a 5-V supply.

6.7 Electrical Characteristics: Receiver

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
V_{IT+}	Positive-going differential input threshold voltage	I_O = –8 mA		–85	–10	mV
$V_{IT–}$	Negative-going differential input threshold voltage	I_O = 8 mA	–200	–115		mV
V_{hys}	Hysteresis voltage (V_{IT+} – $V_{IT–}$)			30		mV
V_{OH}	High-level output voltage	V_{ID} = 200 mV, I_{OH} = –8 mA (see Figure 7-8)	4	4.6		V
V_{OL}	Low-level output voltage	V_{ID} = –200 mV, I_O = 8 mA (see Figure 7-8)		0.15	0.4	V
I_{OZ}	High-impedance-state output current	V_O = 0 or V_{CC}, $\overline{RE}$ = V_{CC}	–1		1	μA
I_I	Bus input current	V_{IH} = 12 V, V_{CC} = 5 V		0.04	0.1	mA
		V_{IH} = 12 V, V_{CC} = 0 V		0.06	0.125	
		V_{IH} = –7 V, V_{CC} = 5 V	–0.1	–0.04		
		V_{IH} = –7 V, V_{CC} = 0 V	–0.05	–0.03		
I_{IH}	High-level input current, ($\overline{RE}$)	V_{IH} = 2 V	–60	–30		μA
I_{IL}	Low-level input current, ($\overline{RE}$)	V_{IL} = 0.8 V	–60	–30		μA
C_{diff}	Differential input capacitance	V_I = 0.4 sin (4E6πt) + 0.5 V, DE at 0 V		7		pF

(1) All typical values are at 25°C and with a 5-V supply.

6.8 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
I_{CC}	Driver and receiver enabled	D at V_{CC} or open, DE at V_{CC}, $\overline{RE}$ at 0 V, No load			425	900	µA
	Driver enabled, receiver disabled	D at V_{CC} or open, DE at V_{CC}, $\overline{RE}$ at V_{CC}, No load			330	600	µA
	Receiver enabled, driver disabled	D at V_{CC} or open, DE at 0 V, $\overline{RE}$ at 0 V, No load			300	600	µA
	Driver and receiver disabled	D at V_{CC} or open, DE at 0 V, $\overline{RE}$ at V_{CC}			0.001	2	µA
$P_{(AVG)}$	Average power dissipation	Input to D is a 50% duty cycle square wave at max specified signal rate R_L = 54 Ω V_{CC} = 5.5 V, T_J = 130°C	ALL HVD3082E			203	mW
			ALL HVD3085E			205	
			ALL HVD3088E			276	

(1) All typical values are at 25°C and with a 5-V supply.

6.9 Switching Characteristics: Driver

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH} t_{PHL}	Propagation delay time, low-to-high-level output Propagation delay time, high-to-low-level output	R_L = 54 Ω, C_L = 50 pF (see Figure 7-4)	HVD3082E		700	1300	ns
			HVD3085E		150	500	
			HVD3088E		12	20	
t_r t_f	Differential output signal rise time Differential output signal fall time	R_L = 54 Ω, C_L = 50 pF (see Figure 7-4)	HVD3082E	500	900	1500	ns
			HVD3085E		200	300	
			HVD3088E		7	15	
$t_{sk(p)}$	Pulse skew ($\lvert t_{PHL} - t_{PLH} \rvert$)	R_L = 54 Ω, C_L = 50 pF (see Figure 7-4)	HVD3082E		20	200	ns
			HVD3085E		5	50	
			HVD3088E		1.4	2	
t_{PZH} t_{PZL}	Propagation delay time, high-impedance-to-high-level output Propagation delay time, high-impedance-to-low-level output	R_L = 110 Ω, $\overline{RE}$ at 0 V (see Figure 7-5 and Figure 7-6)	HVD3082E		2500	7000	ns
			HVD3085E		1000	2500	
			HVD3088E		13	30	
t_{PHZ} t_{PLZ}	Propagation delay time, high-level-to-high-impedance output Propagation delay time, low-level-to-high-impedance output	R_L = 110 Ω, $\overline{RE}$ at 0 V (see Figure 7-5 and Figure 7-6)	HVD3082E		80	200	ns
			HVD3085E		60	100	
			HVD3088E		12	30	
$t_{PZH(SHDN)}$ $t_{PZL(SHDN)}$	Propagation delay time, shutdown-to-high-level output Propagation delay time, shutdown-to-low-level output	R_L = 110 Ω, $\overline{RE}$ at V_{CC} (see Figure 7-5)	HVD3082E		3500	7000	ns
			HVD3085E		2500	4500	
			HVD3088E		1600	2600	

6.10 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15 pF (see Figure 7-9)	HVD3082E HVD3085E		75	200	ns
			HVD3086E			100	
t_{PHL}	Propagation delay time, high-to-low-level output		HVD3082E HVD3085E		79	200	ns
			HVD3088E			100	
$t_{sk(p)}$	Pulse skew ($\lvert t_{PHL} - t_{PLH} \rvert$)		HVD3082E HVD3085E		4	30	ns
			HVD3088E			10	
t_r	Output signal rise time	V_{ID} = –1.5 V to 1.5 V, C_L = 15 pF (see Figure 7-9)			1.5	3	ns
t_f	Output signal fall time				1.8	3	
t_{PZH}	Output enable time to high level	C_L = 15 pF, DE at 3 V (see Figure 7-10 and Figure 7-11)	HVD3082E HVD3085E		5	50	ns
			HVD3088E			30	
t_{PZL}	Output enable time to low level		HVD3082E HVD3085E		10	50	ns
			HVD3088E			30	
t_{PHZ}	Output enable time from high level		HVD3082E HVD3085E		5	50	ns
			HVD3088E			30	
t_{PLZ}	Output disable time from low level		HVD3082E HVD3085E		8	50	ns
			HVD3088E			30	
$t_{PZH(SHDN)}$	Propagation delay time, shutdown-to-high-level output	C_L = 15 pF, DE at 0 V, (see Figure 7-12)			1600	3500	ns
$t_{PZL(SHDN)}$	Propagation delay time, shutdown-to-low-level output				1700	3500	

6.11 Typical Characteristics

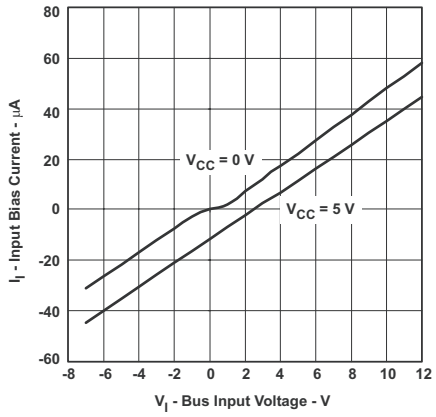


Figure 6-1. Bus Input Current versus Bus Input Voltage

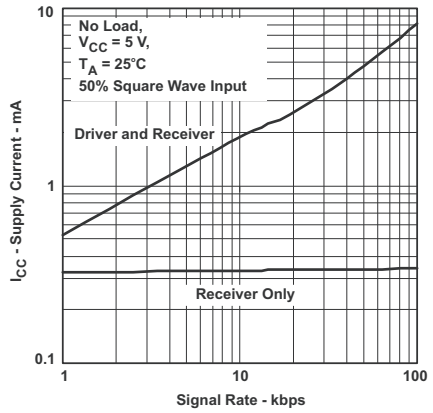


Figure 6-2. SN65HVD3082E RMS Supply Current versus Signaling Rate

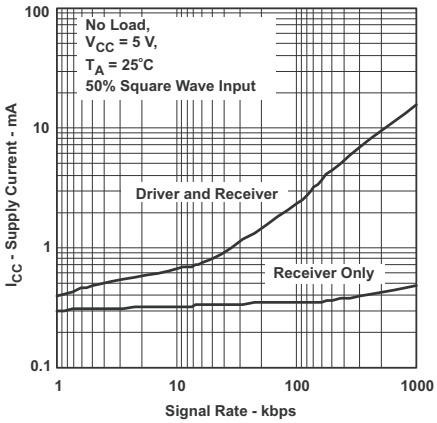


Figure 6-3. SN65HVD3085E RMS Supply Current versus Signaling Rate

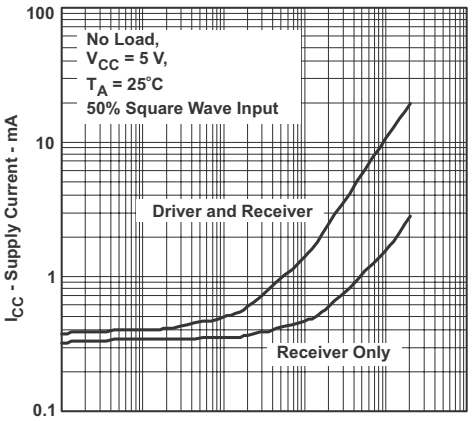


Figure 6-4. SN65HVD3088E RMS Supply Current versus Signal Rate

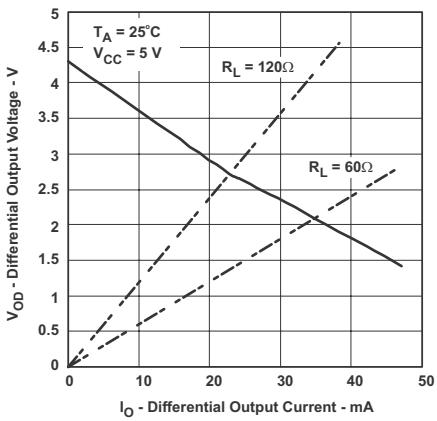


Figure 6-5. Driver Differential Output Voltage versus Driver Output Current

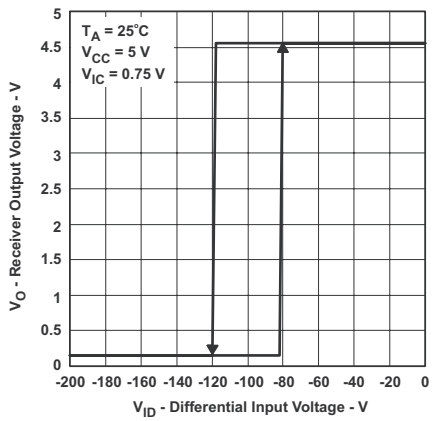


Figure 6-6. Receiver Output Voltage versus Differential Input Voltage

6.11 Typical Characteristics (continued)

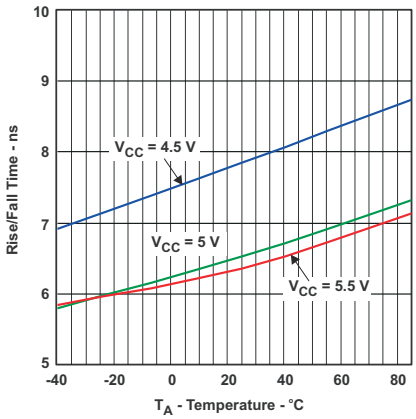


Figure 6-7. SN65HVD3088E Driver Rise and Fall Time versus Temperature

7 Parameter Measurement Information

Test load capacitance includes probe and jig capacitance (unless otherwise specified). Signal generator characteristics: rise and fall time < 6 ns, pulse rate 100 kHz, 50% duty cycle. Z_O = 50 Ω (unless otherwise specified).

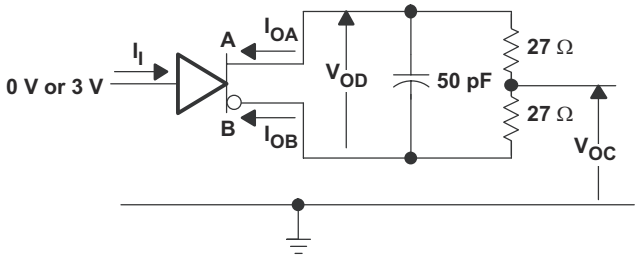


Figure 7-1. Driver Test Circuit, V_{OD} and V_{OC} Without Common-Mode Loading

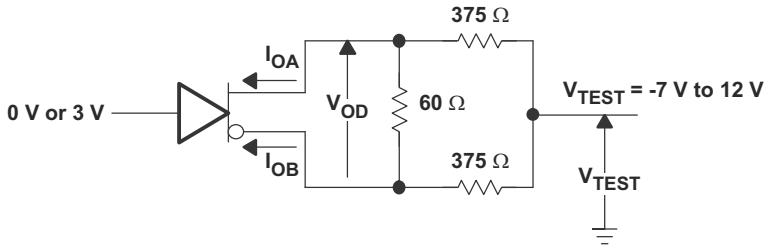


Figure 7-2. Driver Test Circuit, V_{OD} With Common-Mode Loading

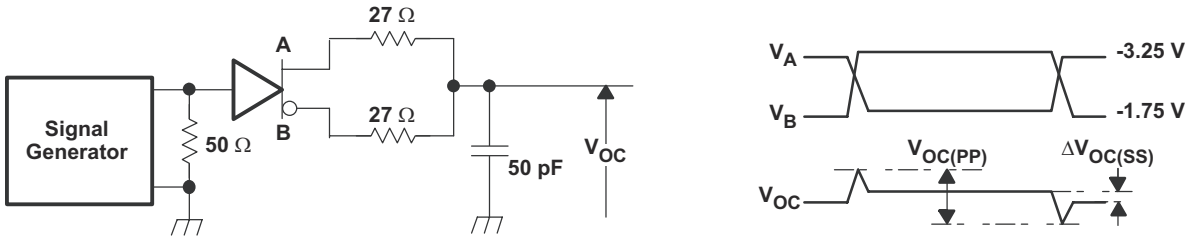


Figure 7-3. Driver V_{OC} Test Circuit and Waveforms

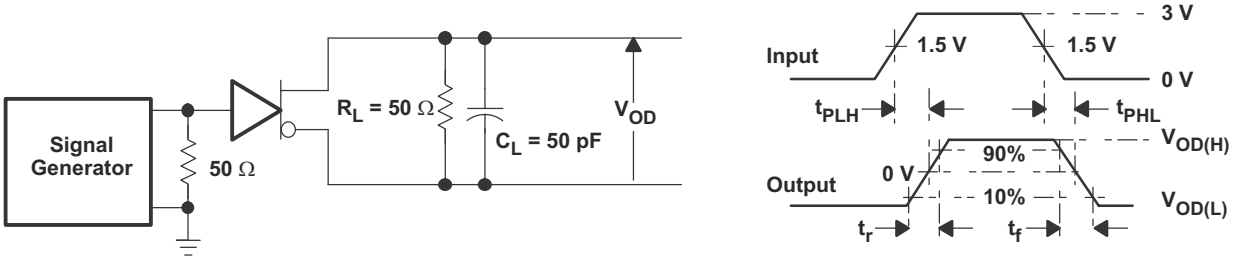


Figure 7-4. Driver Switching Test Circuit and Waveforms

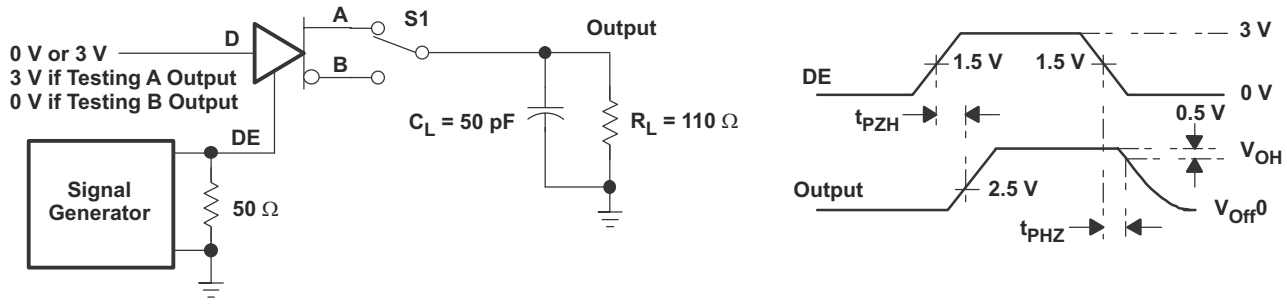


Figure 7-5. Driver Enable and Disable Test Circuit and Waveforms, High Output

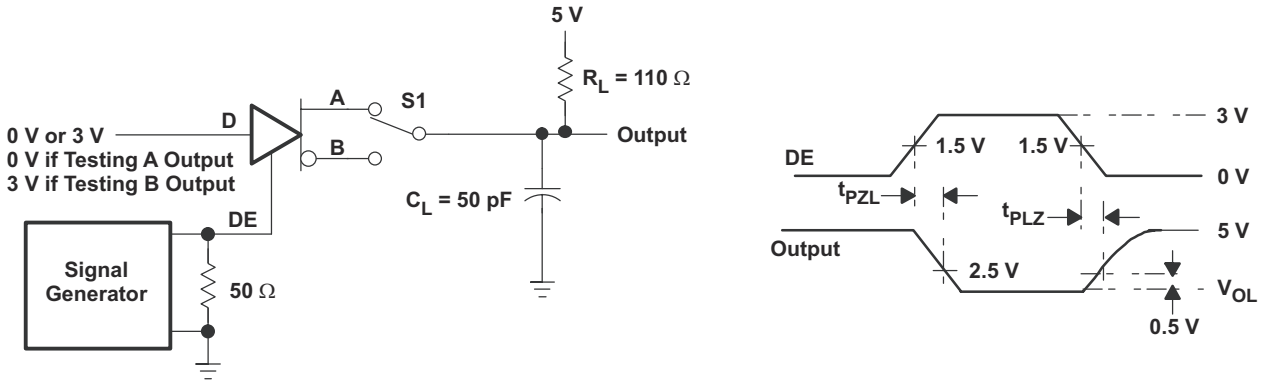


Figure 7-6. Driver Enable and Disable Test Circuit and Waveforms, Low Output

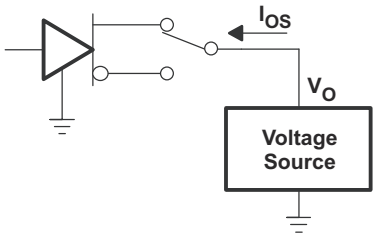


Figure 7-7. Driver Short-Circuit

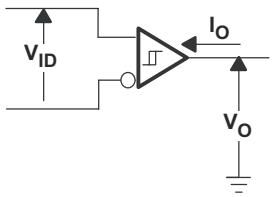


Figure 7-8. Receiver Switching Test Circuit and Waveforms

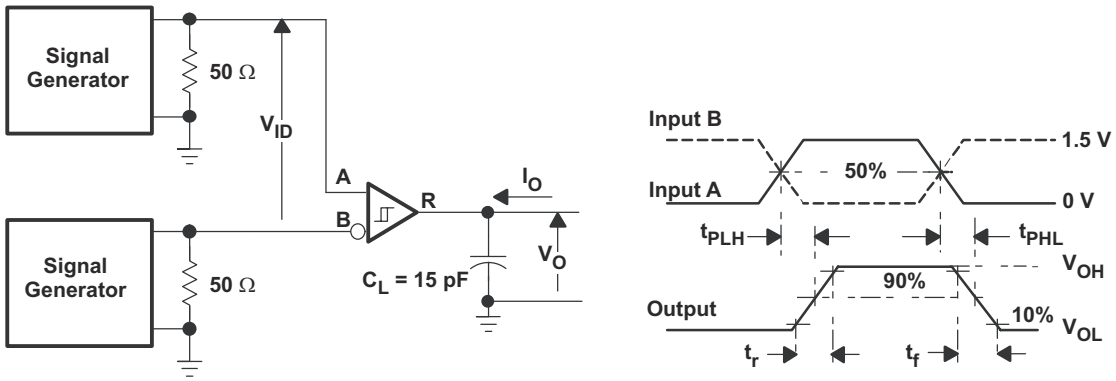


Figure 7-9. Receiver Switching Test Circuit and Waveforms

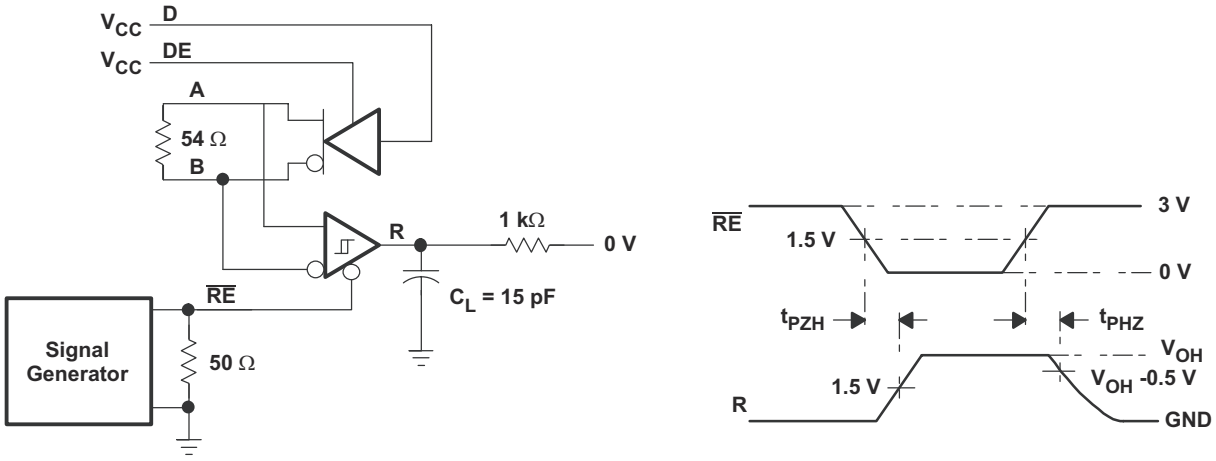


Figure 7-10. Receiver Enable and Disable Test Circuit and Waveforms, Data Output High

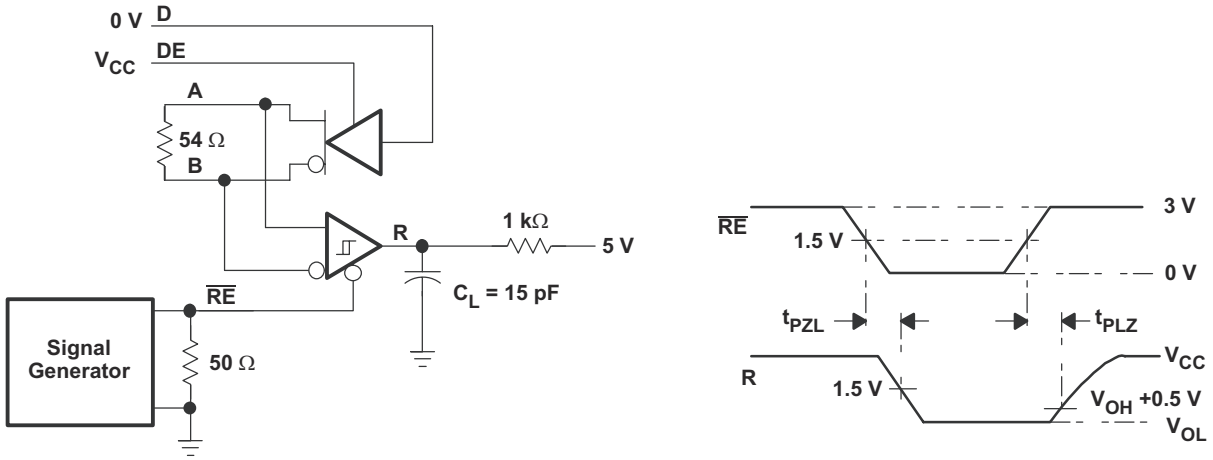


Figure 7-11. Receiver Enable and Disable Test Circuit and Waveforms, Data Output Low

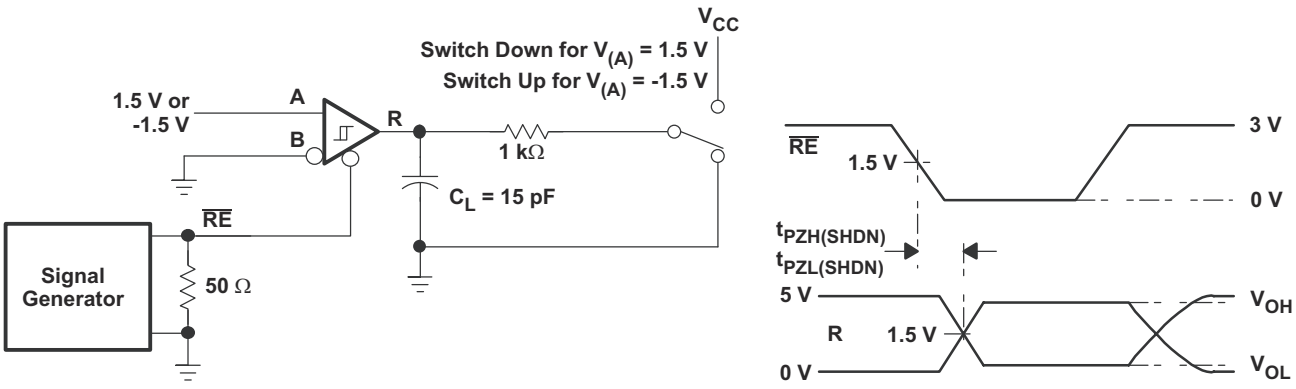


Figure 7-12. Receiver Enable From Shutdown Test Circuit and Waveforms

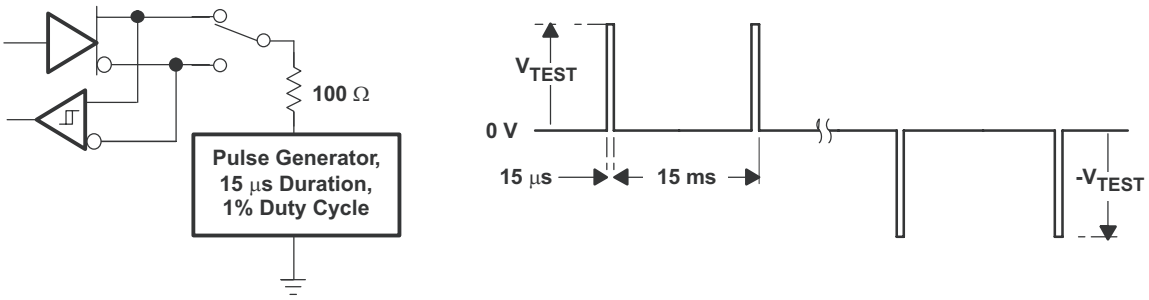


Figure 7-13. Test Circuit and Waveforms, Transient Overvoltage Test

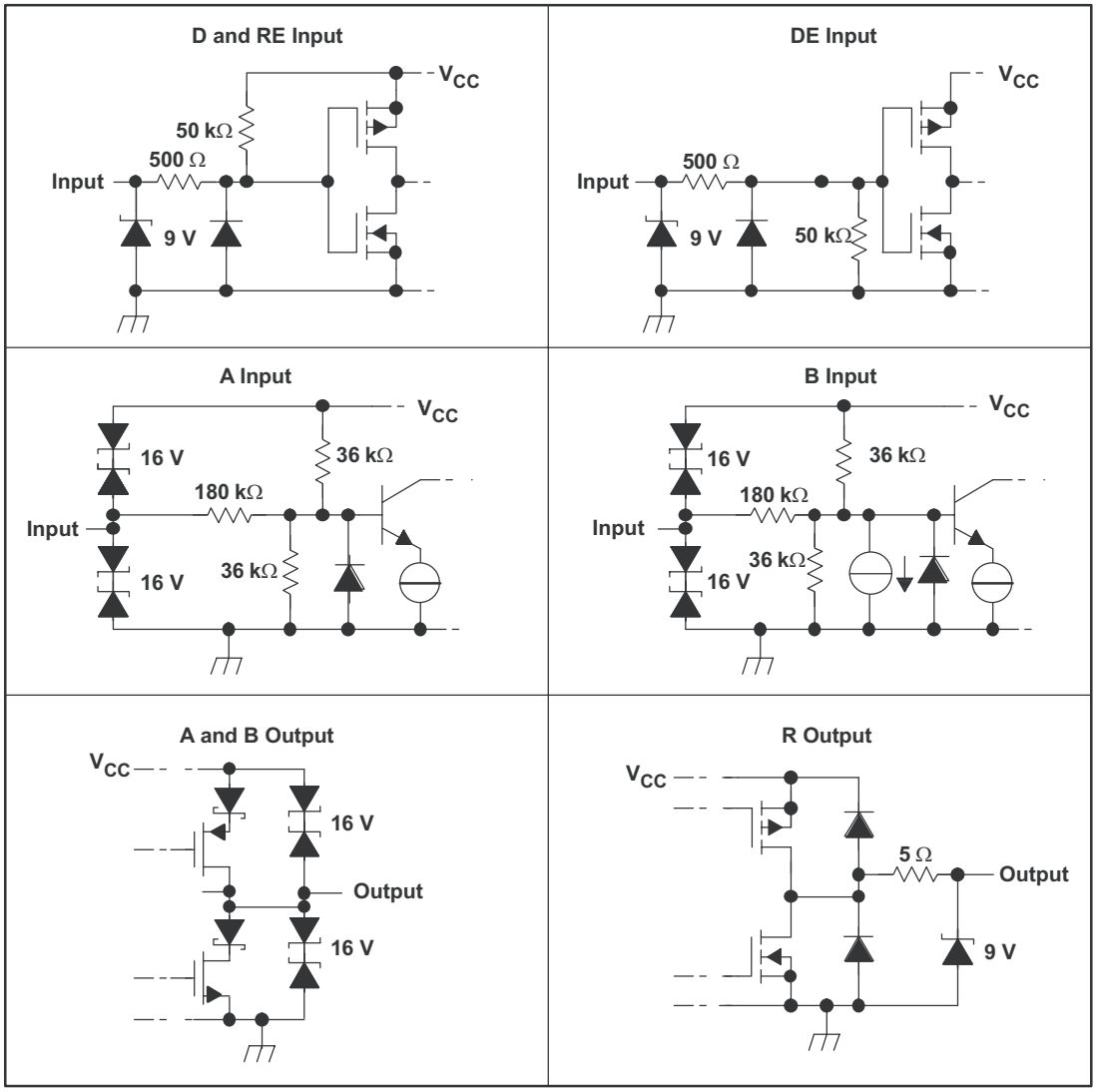


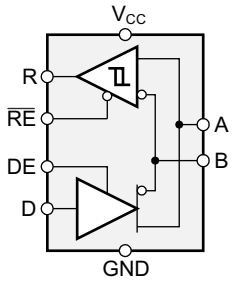
Figure 7-14. Equivalent Input and Output Schematic Diagrams

8 Detailed Description

8.1 Overview

The SNx5HVD308xE family of half-duplex RS-485 transceivers is suitable for data transmission at rates up to 200 kbps (for SN65HVD3082E and SN75HVD3082E), 1 Mbps (for SN65HVD3085E), or 20 Mbps (for SN65HVD3088E) over controlled-impedance transmission media (such as twisted-pair cabling). Up to 256 units of SNx5HVD308xE may share a common RS-485 bus due to the family's low bus input currents. The devices also feature a high degree of ESD protection and typical standby current consumption of 1 nA.

8.2 Functional Block Diagram



8.3 Feature Description

The SNx5HVD308xE provides internal biasing of the receiver input thresholds for open-circuit, bus-idle, or short-circuit failsafe conditions. It features a typical hysteresis of 30 mV in order to improve noise immunity. Internal ESD protection circuits protect the transceiver bus terminals against ±15-kV Human Body Model (HBM) electrostatic discharges.

The devices protect themselves against damage due to overtemperature conditions through use a of a thermal shutdown feature. Thermal shutdown is entered at 165°C (nominal) and causes the device to enter a low-power state with high-impedance outputs.

8.4 Device Functional Modes

When the driver enable pin, DE, is logic high, the differential outputs A and B follow the logic states at data input D. A logic high at D causes A to turn high and B to turn low. In this case the differential output voltage defined as $V_{OD} = V_A – V_B$ is positive. When D is low, the output states reverse, B turns high, A becomes low, and V_{OD} is negative.

When DE is low, both outputs turn high-impedance. In this condition the logic state at D is irrelevant. The DE pin has an internal pull-down resistor to ground, thus when left open the driver is disabled (high-impedance) by default. The D pin has an internal pull-up resistor to V_{CC}, thus, when left open while the driver is enabled, output A turns high and B turns low.

Table 8-1. Driver Function Table

INPUT	ENABLE(1)	OUTPUTS(1)		FUNCTION
D	DE	A	B	
H	H	H	L	Actively drive bus High
L	H	L	H	Actively drive bus Low
X	L	Z	Z	Driver disabled
X	OPEN	Z	Z	Driver disabled by default
OPEN	H	H	L	Actively drive bus High by default

(1) H = high level, L = low level, Z = high impedance, X = irrelevant

When the receiver enable pin, $\overline{RE}$, is logic low, the receiver is enabled. When the differential input voltage defined as $V_{ID} = V_A – V_B$ is positive and higher than the positive input threshold, V_{IT+}, the receiver output, R, turns high. When V_{ID} is negative and lower than the negative input threshold, $V_{IT–}$, the receiver output, R, turns low. If V_{ID} is between V_{IT+} and $V_{IT–}$ the output is indeterminate.

When $\overline{RE}$ is logic high or left open, the receiver output is high-impedance and the magnitude and polarity of V_{ID} are irrelevant. Internal biasing of the receiver inputs causes the output to go failsafe-high when the transceiver is disconnected from the bus (open-circuit), the bus lines are shorted (short-circuit), or the bus is not actively driven (idle bus).

Table 8-2. Receiver Function Table

DIFFERENTIAL INPUT	ENABLE (1)	OUTPUT(1)	FUNCTION
$V_{ID} = V_A - V_B$	$\overline{RE}$	R	
$V_{IT+} < V_{ID}$	L	H	Receive valid bus High
$V_{IT-} < V_{ID} < V_{IT+}$	L	?	Indeterminate bus state
$V_{ID} < V_{IT-}$	L	L	Receive valid bus Low
X	H	Z	Receiver disabled
X	OPEN	Z	Receiver disabled by default
Open-circuit bus	L	H	Fail-safe high output
Short-circuit bus	L	H	Fail-safe high output
Idle (terminated) bus	L	H	Fail-safe high output

(1) H = high level, L = low level, Z = high impedance, X = irrelevant, ? = indeterminate

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The SNx5HVD308xE devices are half-duplex RS-485 transceivers commonly used for asynchronous data transmissions. The driver and receiver enable pins allow for the configuration of different operating modes.

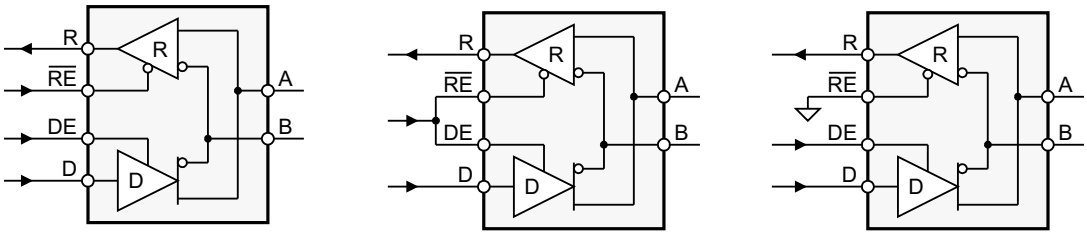


Figure 9-1. Half-Duplex Transceiver Configurations

Using independent enable lines provides the most flexible control as it allows for the driver and the receiver to be turned on and off individually. While this configuration requires two control lines, it allows for selective listening into the bus traffic whether the driver is transmitting data or not.

Combining the enable signals simplifies the interface to the controller by forming a single direction-control signal. In this configuration, the transceiver operates as a driver when the direction-control line is high and as a receiver when the direction-control line is low.

Additionally, only one line is required when connecting the receiver-enable input to ground and controlling only the driver-enable input. In this configuration, a node not only receives the data from the bus, but also the data it sends and can verify that the correct data have been transmitted.

9.2 Typical Application

An RS-485 bus consists of multiple transceivers connecting in parallel to a bus cable. To eliminate line reflections, each cable end is terminated with a termination resistor, R_T, whose value matches the characteristic impedance, Z_0, of the cable. This method, known as parallel termination, allows for higher data rates over longer cable length.

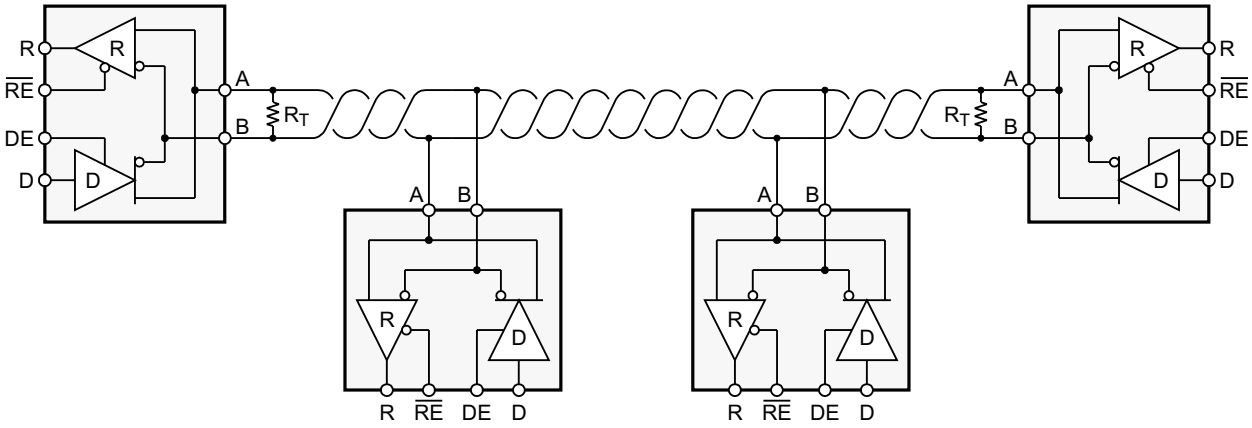


Figure 9-2. Typical Application Circuit

9.2.1 Design Requirements

RS-485 is a robust electrical standard suitable for long-distance networking that may be used in a wide range of applications with varying requirements, such as distance, data rate, and number of nodes.

9.2.1.1 Data Rate and Bus Length

There is an inverse relationship between data rate and bus length, meaning the higher the data rate, the shorter the cable length; and conversely, the lower the data rate, the longer the cable may be without introducing data errors. While most RS-485 systems use data rates between 10 kbps and 100 kbps, some applications require data rates up to 250 kbps at distances of 4,000 feet and longer. Longer distances are possible by allowing for small signal jitter of up to 5 or 10%.

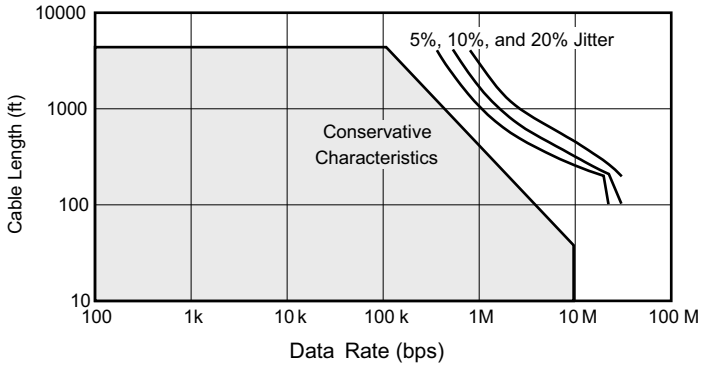


Figure 9-3. Cable Length vs Data Rate Characteristic

9.2.1.2 Stub Length

When connecting a node to the bus, the distance between the transceiver inputs and the cable trunk, known as the stub, must be as short as possible. Stubs present a non-terminated piece of bus line which can introduce reflections as the length of the stub increases. As a general guideline, the electrical length, or round-trip delay, of a stub must be less than one-tenth of the rise time of the driver, thus giving a maximum physical stub length as shown in Equation 1.

$$L_{stub} \leq 0.1 \times t_r \times v \times c \quad (1)$$

where:

- t_r is the 10/90 rise time of the driver
- c is the speed of light (3×10^8 m/s)
- v is the signal velocity of the cable or trace as a factor of c

9.2.1.3 Bus Loading

The RS-485 standard specifies that a compliant driver must be able to driver 32 unit loads (UL), where 1 unit load represents a load impedance of approximately 12 kΩ. Because the SNx5HVD308xE is a 1/8 UL transceiver, it is possible to connect up to 256 receivers to the bus.

9.2.1.4 Receiver Failsafe

The differential receiver is failsafe to invalid bus states caused by:

- open bus conditions such as a disconnected connector,
- shorted bus conditions such as cable damage shorting the twisted-pair together, or
- idle bus conditions that occur when no driver on the bus is actively driving

In any of these cases, the differential receiver outputs a failsafe logic High state, so that the output of the receiver is not indeterminate.

Receiver failsafe is accomplished by offsetting the receiver thresholds so that the *input indeterminate* range does not include zero volts differential. To comply with the RS-422 and RS-485 standards, the receiver output must output a High when the differential input V_{ID} is more positive than +200 mV, and must output a Low when the V_{ID} is more negative than –200 mV. The receiver parameters which determine the failsafe performance are V_{IT+} and $V_{IT–}$ and V_{HYS}. As seen in the table, differential signals more negative than –200 mV will always cause a Low receiver output. Similarly, differential signals more positive than +200 mV will always cause a High receiver output.

When the differential input signal is close to zero, it will still be above the V_{IT+} threshold, and the receiver output is High. Only when the differential input is more negative than $V_{IT–}$ will the receiver output transition to a Low state. So, the noise immunity of the receiver inputs during a bus fault condition includes the receiver hysteresis value V_{HYS} (the separation between V_{IT+} and $V_{IT–}$) as well as the value of V_{IT+}.

9.2.2 Detailed Design Procedure

In order to protect bus nodes against high-energy transients, the implementation of external transient protection devices is necessary.

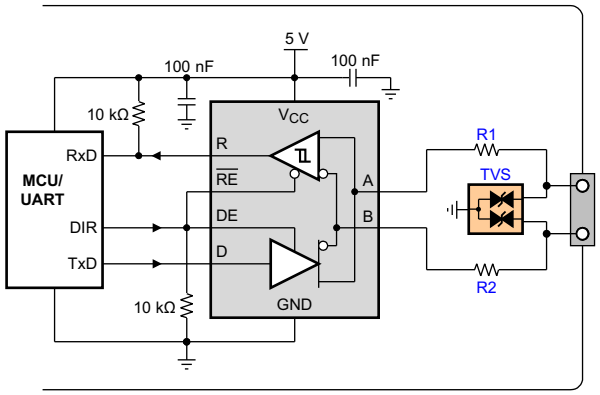


Figure 9-4. Transient Protection Against ESD, EFT, and Surge Transients

Figure 9-4 suggests a protection circuit against 10-kV ESD (IEC 61000-4-2), 4-kV EFT (IEC 61000-4-4), and 1-kV surge (IEC 61000-4-5) transients. Table 9-1 shows the associated Bill of Materials.

Table 9-1. Bill of Materials

DEVICE	FUNCTION	ORDER NUMBER	MANUFACTURER
XCVR	RS-485 Transceiver	SNx5HVD308xE	TI
R1, R2	10-Ω, Pulse-Proof Thick-Film Resistor	CRCW060310RJNEAHP	Vishay
TVS	Bidirectional 400-W Transient Suppressor	CDSOT23-SM712	Bourns

9.2.2.1 Power Usage in an RS-485 Transceiver

Power consumption is a concern in many applications. Power supply current is delivered to the bus load as well as to the transceiver circuitry. For a typical RS-485 bus configuration, the load that an active driver must drive consists of all of the receiving nodes, plus the termination resistors at each end of the bus.

The load presented by the receiving nodes depends on the input impedance of the receiver. The TIA/EIA-485A standard defines a unit load as allowing up to 1 mA. With up to 32 unit loads allowed on the bus, the total current supplied to all receivers can be as high as 32 mA. The HVD308xE is rated as a 1/8 unit load device. As shown in Figure 6-1, the bus input current is less than 0.125 mA, allowing up to 256 nodes on a single bus.

The current in the termination resistors depends on the differential bus voltage. The standard requires active drivers to produce at least 1.5 V of differential signal. For a bus terminated with one standard 120-Ω resistor at each end, this sums to 25 mA differential output current whenever the bus is active. Typically the HVD308xE can drive more than 25-mA to a 60-Ω load, resulting in a differential output voltage higher than the minimum required by the standard (see Figure 6-3).

Overall, the total load current can be 60 mA to a loaded RS-485 bus. This is in addition to the current required by the transceiver itself; the HVD308xE circuitry requires only about 0.4 mA with both driver and receiver enabled, and only 0.3 mA with either the driver enabled or with the receiver enabled. In low-power shutdown mode, neither the driver nor receiver is active, and the supply current is low.

Supply current increases with signaling rate primarily due to the totem pole outputs of the driver (see Figure 6-2). When these outputs change state, there is a moment when both the high-side and low-side output transistors are conducting and this creates a short spike in the supply current. As the frequency of state changes increases, more power is used.

9.2.2.2 Low-Power Shutdown Mode

When both the driver and receiver are disabled (DE low and $\overline{RE}$ high) the device is in shutdown mode. If the enable inputs are in this state for less than 60 ns, the device does not enter shutdown mode. This guards against inadvertently entering shutdown mode during driver or receiver enabling. Only when the enable inputs are held in this state for 300 ns or more, the device is assured to be in shutdown mode. In this low-power shutdown mode, most internal circuitry is powered down, and the supply current is typically 1 nA. When either the driver or the receiver is re-enabled, the internal circuitry becomes active.

If only the driver is re-enabled (DE transitions to high) the driver outputs are driven according to the D input after the enable times given by $t_{PZH(SHDN)}$ and $t_{PZL(SHDN)}$ in the driver switching characteristics. If the D input is open when the driver is enabled, the driver outputs defaults to A high and B low, in accordance with the driver failsafe feature.

If only the receiver is re-enabled (RE transitions to low) the receiver output is driven according to the state of the bus inputs (A and B) after the enable times given by $t_{PZH(SHDN)}$ and $t_{PZL(SHDN)}$ in the receiver switching characteristics. If there is no valid state on the bus the receiver responds as described in the failsafe operation section.

If both the receiver and driver are re-enabled simultaneously, the receiver output is driven according to the state of the bus inputs (A and B) and the driver output is driven according to the D input.

Note

The state of the active driver affects the inputs to the receiver. Therefore, the receiver outputs are valid as soon as the driver outputs are valid.

10 Power Supply Recommendations

To ensure reliable operation at all data rates and supply voltages, each supply must be decoupled with a 100-nF ceramic capacitor located as close to the supply pins as possible. This helps to reduce supply voltage ripple present on the outputs of switched-mode power supplies and also helps to compensate for the resistance and inductance of the PCB power planes.

11 Layout

11.1 Layout Guidelines

Robust and reliable bus node design often requires the use of external transient protection devices in order to protect against EFT and surge transients that may occur in industrial environments. Because these transients have a wide frequency bandwidth (from approximately 3 MHz to 3 GHz), high-frequency layout techniques must be applied during PCB design.

- Place the protection circuitry close to the bus connector to prevent noise transients from entering the board.
- Use V_{CC} and ground planes to provide low-inductance.

Note

High-frequency currents follow the path of least inductance and not the path of least impedance.

- Design the protection components into the direction of the signal path. Do not force the transients currents to divert from the signal path to reach the protection device.
- Apply 100-nF to 220-nF bypass capacitors as close as possible to the V_{CC} pins of transceiver, UART, and controller ICs on the board.
- Use at least two vias for V_{CC} and ground connections of bypass capacitors and protection devices to minimize effective via-inductance.
- Use 1-kΩ to 10-kΩ pullup or pulldown resistors for enable lines to limit noise currents in these lines during transient events.
- Insert series pulse-proof resistors into the A and B bus lines if the TVS clamping voltage is higher than the specified maximum voltage of the transceiver bus pins. These resistors limit the residual clamping current into the transceiver and prevent it from latching up.
- While pure TVS protection is sufficient for surge transients up to 1 kV, higher transients require metal-oxide varistors (MOVs) which reduce the transients to a few hundred volts of clamping voltage, and transient blocking units (TBUs) that limit transient current to 200 mA.

11.2 Layout Example

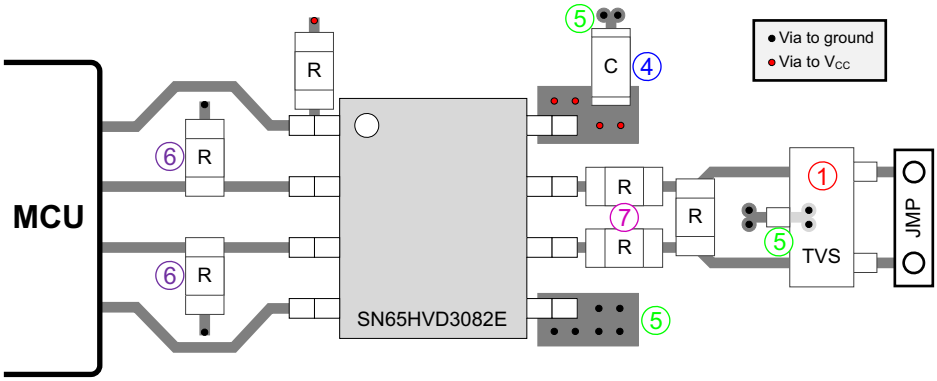


Figure 11-1. Layout Example

11.3 Thermal Considerations for IC Packages

θ_{JA} (Junction-to-Ambient Thermal Resistance) is defined as the difference in junction temperature to ambient temperature divided by the operating power.

θ_{JA} is **not** a constant and is a strong function of:

- the PCB design (50% variation)
- altitude (20% variation)
- device power (5% variation)

θ_{JA} can be used to compare the thermal performance of packages if the specific test conditions are defined and used. Standardized testing includes specification of PCB construction, test chamber volume, sensor locations, and the thermal characteristics of holding fixtures. θ_{JA} is often misused when it is used to calculate junction temperatures for other installations.

TI uses two test PCBs as defined by JEDEC specifications. The low-k board gives average in-use condition thermal performance and consists of a single trace layer 25-mm long and 2-oz thick copper. The high-k board gives best case in-use condition and consists of two 1-oz buried power planes with a single trace layer 25-mm long with 2-oz thick copper. A 4% to 50% difference in θ_{JA} can be measured between these two test cards.

θ_{JC} (Junction-to-Case Thermal Resistance) is defined as difference in junction temperature to case divided by the operating power. It is measured by putting the mounted package up against a copper block cold plate to force heat to flow from die, through the mold compound into the copper block.

θ_{JC} is a useful thermal characteristic when a heatsink is applied to package. It is NOT a useful characteristic to predict junction temperature as it provides pessimistic numbers if the case temperature is measured in a non-standard system and junction temperatures are backed out. It can be used with θ_{JB} in 1-dimensional thermal simulation of a package system.

θ_{JB} (Junction-to-Board Thermal Resistance) is defined to be the difference in the junction temperature and the PCB temperature at the center of the package (closest to the die) when the PCB is clamped in a cold-plate structure. θ_{JB} is only defined for the high-k test card.

θ_{JB} provides an overall thermal resistance between the die and the PCB. It includes a bit of the PCB thermal resistance (especially for BGAs with thermal balls) and can be used for simple 1-dimensional network analysis of package system (see Figure 11-2).

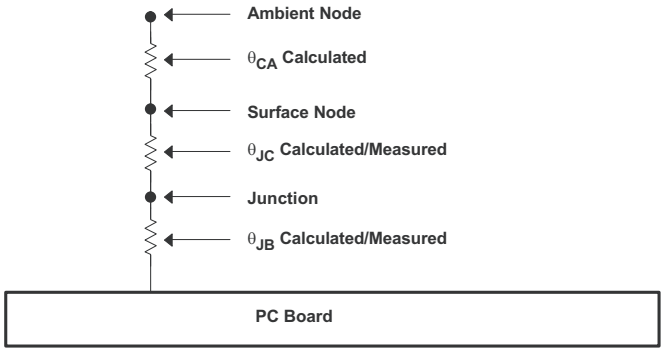


Figure 11-2. Thermal Resistance

12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

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12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 12-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN65HVD3082E	Click here	Click here	Click here	Click here	Click here
SN75HVD3082E	Click here	Click here	Click here	Click here	Click here
SN65HVD3085E	Click here	Click here	Click here	Click here	Click here
SN65HVD3088E	Click here	Click here	Click here	Click here	Click here

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.
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12.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.7 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65HVD3082ED	NRND	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VP3082	
SN65HVD3082EDG4	NRND	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VP3082	
SN65HVD3082EDGK	NRND	VSSOP	DGK	8	80	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	NWN	
SN65HVD3082EDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU | SN | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	NWN	Samples
SN65HVD3082EDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VP3082	Samples
SN65HVD3082EDRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VP3082	Samples
SN65HVD3082EP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	65HVD3082	Samples
SN65HVD3082EPE4	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	65HVD3082	Samples
SN65HVD3085ED	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VP3085	Samples
SN65HVD3085EDG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VP3085	Samples
SN65HVD3085EDGK	ACTIVE	VSSOP	DGK	8	80	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	NWK	Samples
SN65HVD3085EDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	NWK	Samples
SN65HVD3085EDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VP3085	Samples
SN65HVD3088ED	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VP3088	Samples
SN65HVD3088EDG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VP3088	Samples
SN65HVD3088EDGK	ACTIVE	VSSOP	DGK	8	80	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	NWH	Samples
SN65HVD3088EDGKG4	ACTIVE	VSSOP	DGK	8	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	NWH	Samples
SN65HVD3088EDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	NWH	Samples
SN65HVD3088EDGKRG4	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	NWH	Samples
SN65HVD3088EDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VP3088	Samples
SN65HVD3088EDRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VP3088	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN75HVD3082ED	NRND	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	VN3082	
SN75HVD3082EDG4	NRND	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	VN3082	
SN75HVD3082EDGK	NRND	VSSOP	DGK	8	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	NWM	
SN75HVD3082EDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	Call TI | SN | NIPDAU	Level-1-260C-UNLIM	0 to 70	NWM	Samples
SN75HVD3082EDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	VN3082	Samples
SN75HVD3082EDRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	VN3082	Samples
SN75HVD3082EP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	75HVD3082	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

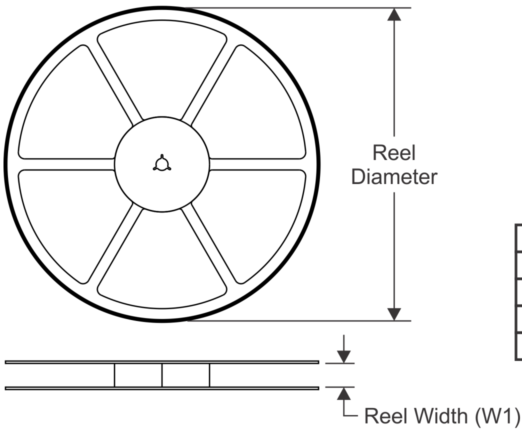
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

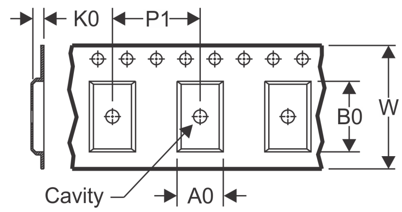
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

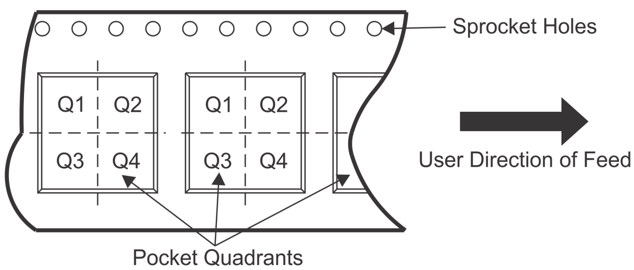


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

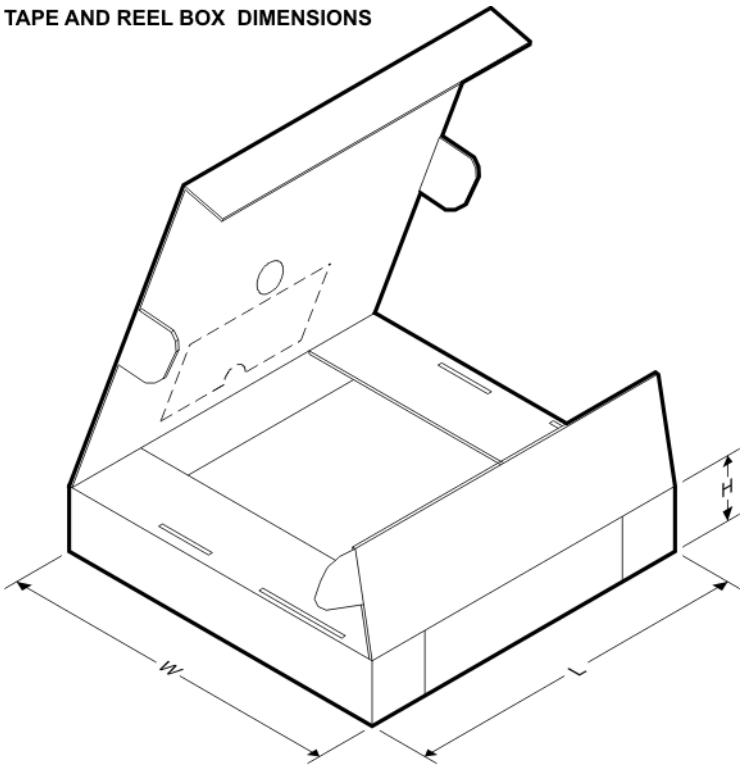
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65HVD3082EDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
SN65HVD3082EDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
SN65HVD3082EDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65HVD3082EDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65HVD3082EDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65HVD3082EDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65HVD3085EDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
SN65HVD3085EDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65HVD3088EDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN75HVD3082EDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
SN75HVD3082EDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN75HVD3082EDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

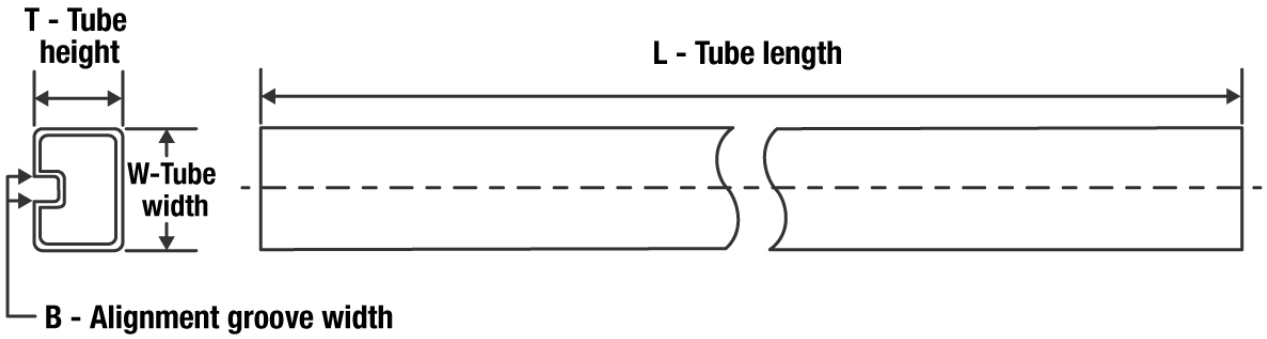
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

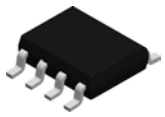
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65HVD3082EDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
SN65HVD3082EDGKR	VSSOP	DGK	8	2500	350.0	350.0	43.0
SN65HVD3082EDR	SOIC	D	8	2500	340.5	338.1	20.6
SN65HVD3082EDR	SOIC	D	8	2500	340.5	336.1	25.0
SN65HVD3082EDR	SOIC	D	8	2500	367.0	367.0	35.0
SN65HVD3082EDR	SOIC	D	8	2500	853.0	449.0	35.0
SN65HVD3085EDGKR	VSSOP	DGK	8	2500	364.0	364.0	27.0
SN65HVD3085EDR	SOIC	D	8	2500	340.5	336.1	25.0
SN65HVD3088EDR	SOIC	D	8	2500	340.5	336.1	25.0
SN75HVD3082EDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
SN75HVD3082EDR	SOIC	D	8	2500	367.0	367.0	35.0
SN75HVD3082EDR	SOIC	D	8	2500	340.5	336.1	25.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN65HVD3082ED	D	SOIC	8	75	507	8	3940	4.32
SN65HVD3082EDG4	D	SOIC	8	75	507	8	3940	4.32
SN65HVD3082EDGK	DGK	VSSOP	8	80	331.47	6.55	3000	2.88
SN65HVD3082EP	P	PDIP	8	50	506	13.97	11230	4.32
SN65HVD3082EPE4	P	PDIP	8	50	506	13.97	11230	4.32
SN65HVD3085ED	D	SOIC	8	75	507	8	3940	4.32
SN65HVD3085EDG4	D	SOIC	8	75	507	8	3940	4.32
SN65HVD3085EDGK	DGK	VSSOP	8	80	274	6.55	500	2.88
SN65HVD3085EDGK	DGK	VSSOP	8	80	331.47	6.55	3000	2.88
SN65HVD3088ED	D	SOIC	8	75	507	8	3940	4.32
SN65HVD3088EDG4	D	SOIC	8	75	507	8	3940	4.32
SN65HVD3088EDGK	DGK	VSSOP	8	80	331.47	6.55	3000	2.88
SN65HVD3088EDGK	DGK	VSSOP	8	80	330	6.55	500	2.88
SN65HVD3088EDGKG4	DGK	VSSOP	8	80	331.47	6.55	3000	2.88
SN65HVD3088EDGKG4	DGK	VSSOP	8	80	330	6.55	500	2.88
SN75HVD3082ED	D	SOIC	8	75	507	8	3940	4.32
SN75HVD3082EDG4	D	SOIC	8	75	507	8	3940	4.32
SN75HVD3082EDGK	DGK	VSSOP	8	80	331.47	6.55	3000	2.88
SN75HVD3082EP	P	PDIP	8	50	506	13.97	11230	4.32

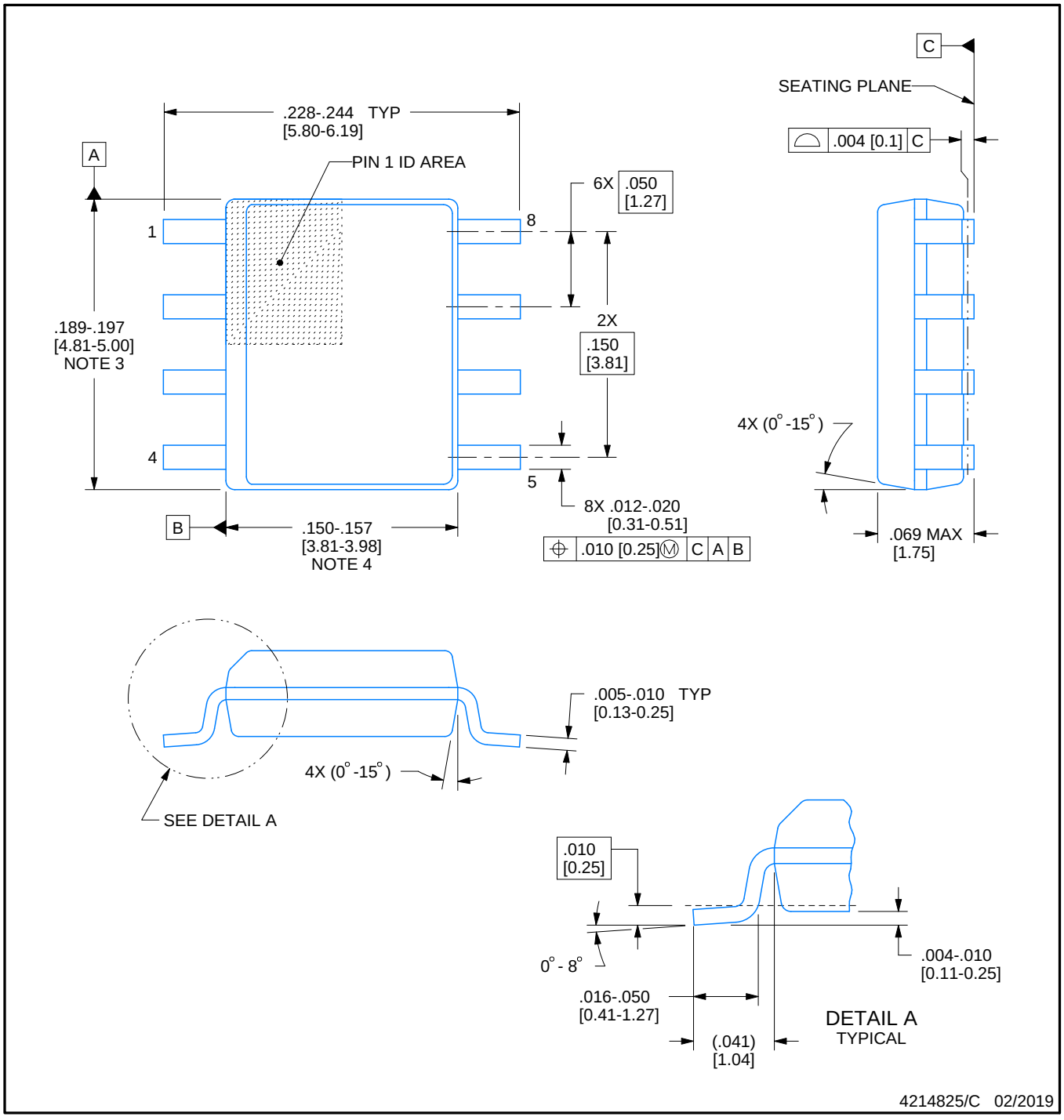


PACKAGE OUTLINE

D0008A

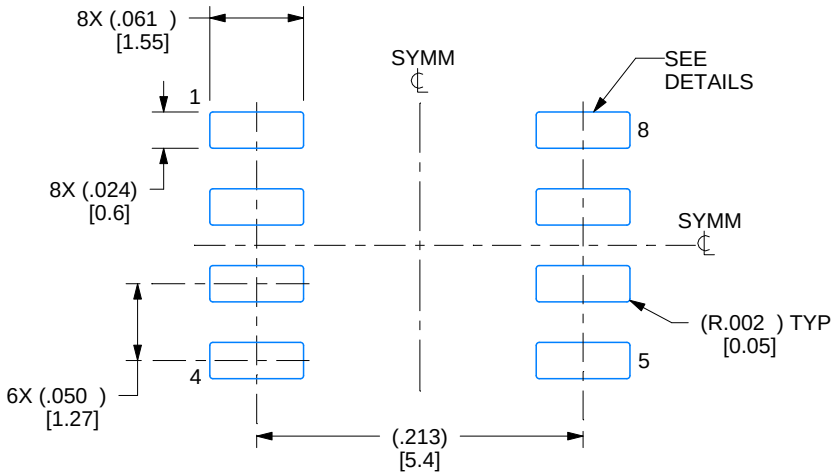
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

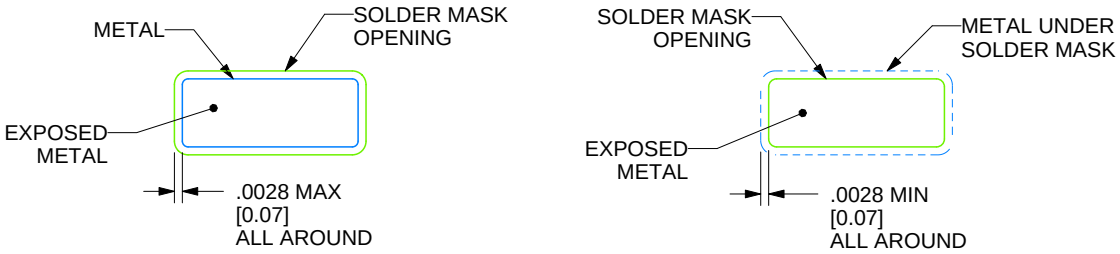


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

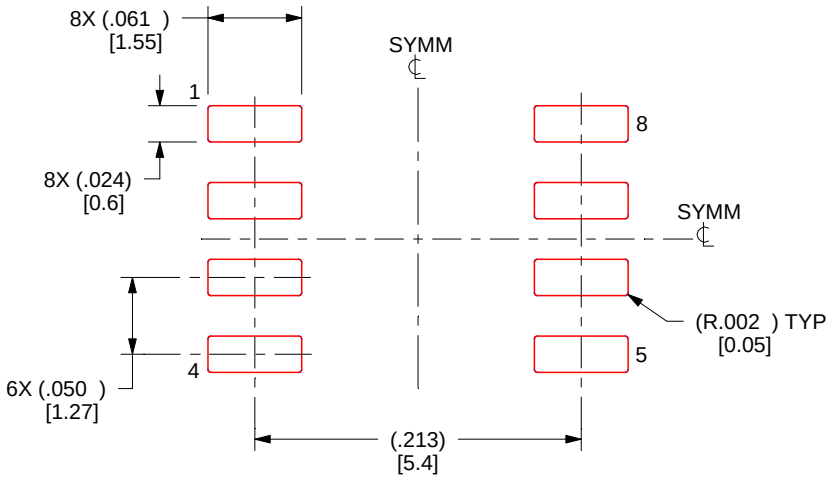
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



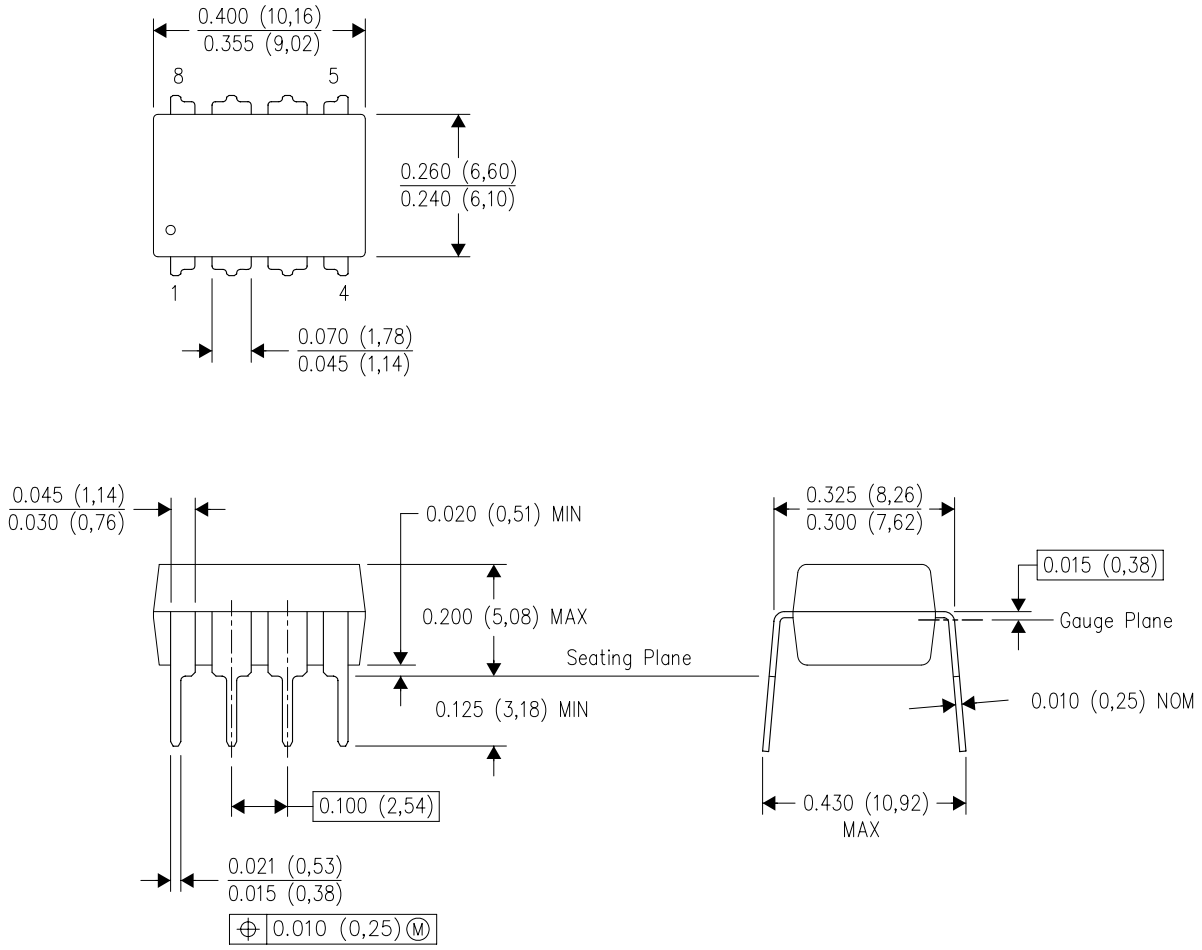
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

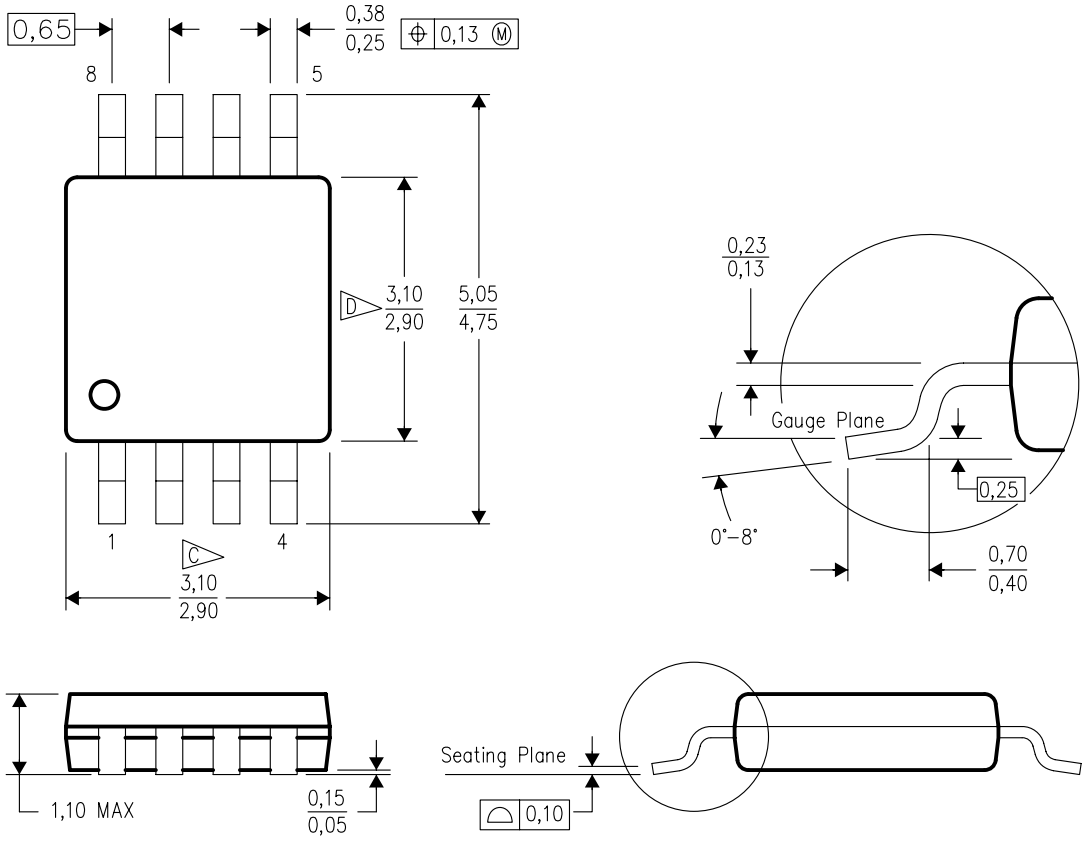
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

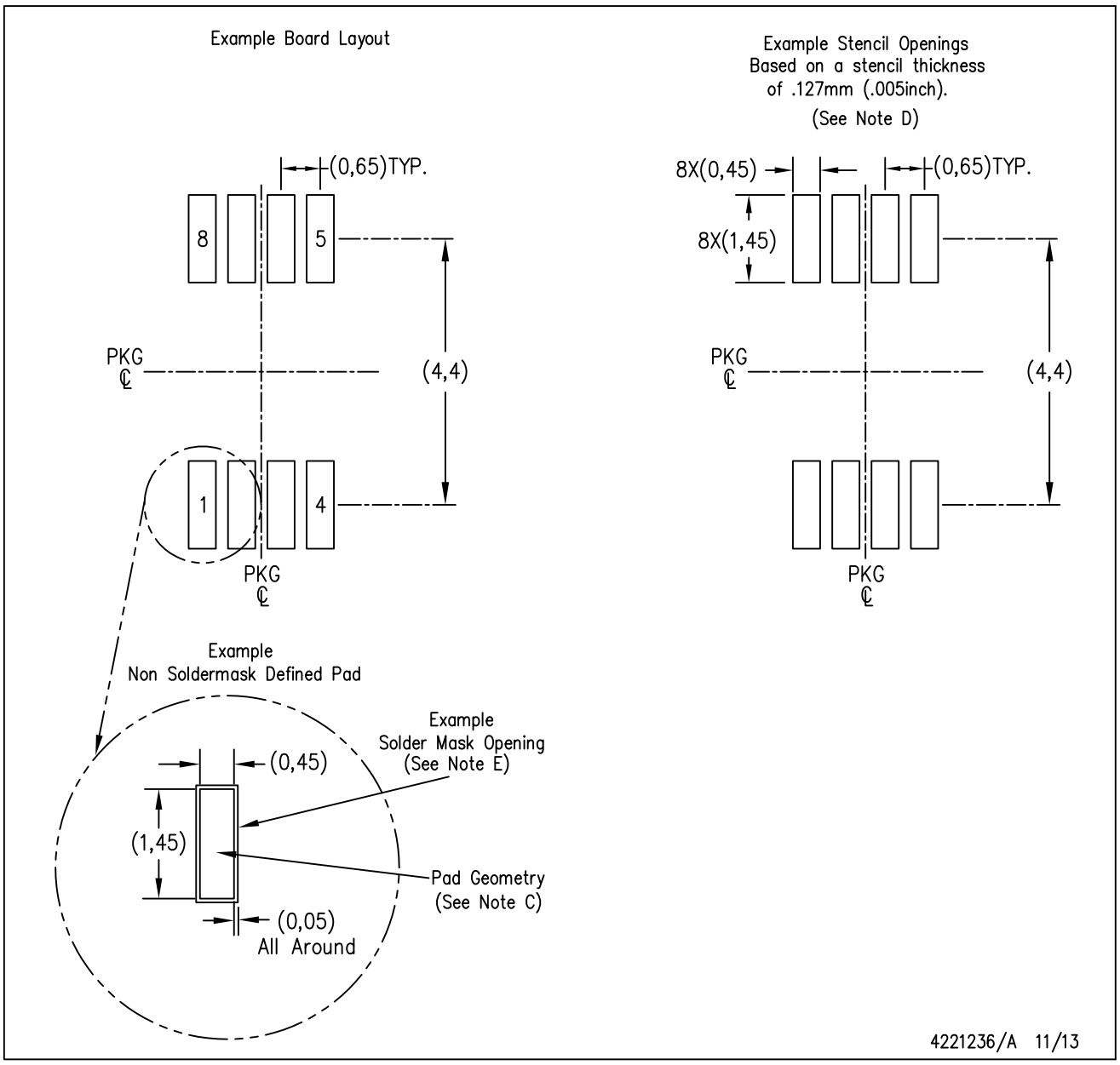
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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