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Advanced Power MOSFET

IRFM120A

FEATURES

IEEE802.3af Compatible

- Avalanche Rugged Technology
- □ Rugged Gate Oxide Technology
- Lower Input Capacitance
- ☐ Improved Gate Charge
- ☐ Extended Safe Operating Area
- \Box Lower Leakage Current : 10 μ A (Max.) @ $V_{DS} = 100V$
- \square Lower $R_{DS(ON)}$: 0.155 Ω (Typ.)

 $BV_{DSS} = 100 V$

 $R_{DS(on)} = 0.2 \Omega$

 $I_D = 2.3 A$





1. Gate 2. Drain 3. Source

Absolute Maximum Ratings

Symbol	Characteristic	Value	Units	
V_{DSS}	Drain-to-Source Voltage	100	V	
I _D	Continuous Drain Current (T _A =25℃)	2.3	A	
	Continuous Drain Current (T _A =70 °C)	1.84		
I _{DM}	Drain Current-Pulsed ①	18	Α	
V_{GS}	Gate-to-Source Voltage	±20	V	
E _{AS}	Single Pulsed Avalanche Energy ②	123	mJ	
I _{AR}	Avalanche Current ①	2.3	Α	
E _{AR}	Repetitive Avalanche Energy ①	0.24	mJ	
dv/dt	Peak Diode Recovery dv/dt 3	6.5	V/ns	
P _D	Total Power Dissipation (T _A =25°C) *	2.4	W	
' D	Linear Derating Factor *	0.019	W/℃	
T_J , T_STG	Operating Junction and		°C	
	Storage Temperature Range	- 55 to +150		
T_L	Maximum Lead Temp. for Soldering	000		
	Purposes, 1/8" from case for 5-seconds	300		

Thermal Resistance

Symbol	Characteristic	Тур.	Max.	Units
$R_{\theta JA}$	Junction-to-Ambient *		52	сw

^{*} When mounted on the minimum pad size recommended (PCB Mount).

Electrical Characteristics (T_A =25 $^{\circ}$ C unless otherwise specified)

Symbol	Characteristic	Min.	Тур.	Max.	Units	Test Condition
BV_{DSS}	Drain-Source Breakdown Voltage	100			V	$V_{GS}=0V,I_{D}=250\mu A$
Δ BV/ Δ T $_{ m J}$	Breakdown Voltage Temp. Coeff.		0.12	-	V/°C	I _D =250μA See Fig 7
$V_{GS(th)}$	Gate Threshold Voltage	2.0	ŀ	4.0	V	$V_{DS} = 5V, I_{D} = 250 \mu A$
	Gate-Source Leakage, Forward			100	nA	V _{GS} =20V
I _{GSS}	Gate-Source Leakage, Reverse			-100	IIA	V _{GS} =-20V
	Drain-to-Source Leakage Current			1	μA	V _{DS} =30V 6
I _{DSS}				10		V _{DS} =100V
				100		V _{DS} =80V,T _A =125 ℃
R _{DS(on)}	Static Drain-Source		0.2			V 40VI 44EA
	On-State Resistance			0.2	$V_{GS} = 10V, I_{D} = 1.15A$ (4)	
g _{fs}	Forward Transconductance		3.12		S	V _{DS} =40V,I _D =1.15A
C _{iss}	Input Capacitance		370	480		\/ _0\/\/ _25\/f_1MUz
C _{oss}	Output Capacitance		95	110	pF	V _{GS} =0V,V _{DS} =25V,f =1MHz See Fig 5
C _{rss}	Reverse Transfer Capacitance		38	45		
t _{d(on)}	Turn-On Delay Time		14	40		\/ _50\/ _0.2\
t _r	Rise Time		14	40	20	$V_{DD} = 50V, I_D = 9.2A,$
$t_{d(off)}$	Turn-Off Delay Time		36	90	ns	$R_G=18\Omega$
t _f	Fall Time		28	70		See Fig 13 4 5
Q_{q}	Total Gate Charge		16	22		V _{DS} =80V,V _{GS} =10V,
Q_{gs}	Gate-Source Charge		2.7		nC	I _D =9.2A
Q_{gd}	Gate-Drain("Miller") Charge		7.8			See Fig 6 & Fig 12 4 5

Source-Drain Diode Ratings and Characteristics

Symbol	Characteristic	Min.	Тур.	Max.	Units	Test Condition
I _S	Continuous Source Current			2.3	^	Integral reverse pn-diode
I _{SM}	Pulsed-Source Current ①			18	А	in the MOSFET
V _{SD}	Diode Forward Voltage 4			1.5	V	T _J =25 °C,I _S =2.3A,V _{GS} =0V
t _{rr}	Reverse Recovery Time		98		ns	T _J =25℃,I _F =9.2A
Q _{rr}	Reverse Recovery Charge		0.34		μC	di _F /dt=100A/µs 4

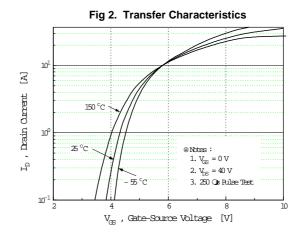
Notes;

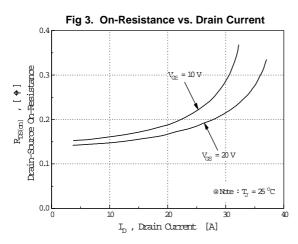
- ① Repetitive Rating : Pulse Width Limited by Maximum Junction Temperature
- @ L=35mH, I_{AS}=2.3A, V_DD=25V, R_G=27 $\!\Omega$, Starting T_J=25 $\!^{\circ}\!\!$ C
- $\ \, \ \,$ 3 $\ \, I_{SD}{\le}9.2A,\,di/dt{\le}300A/\mu s,\,V_{DD}{\le}BV_{DSS}\,,\,Starting\,T_{J}{=}25\,^{\circ}\!C$
- 4 Pulse Test : Pulse Width = $250\mu s$, Duty Cycle $\leq 2\%$
- 5 Essentially Independent of Operating Temperature
- 6 Adjusted for Cisco

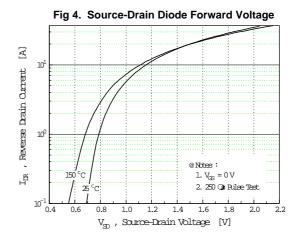
Fig 1. Output Characteristics

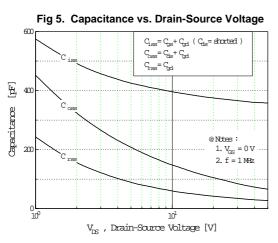
Top: V_{GS}
10V
10V
80V
70V
60V
55V
50V
Bottom: 45V

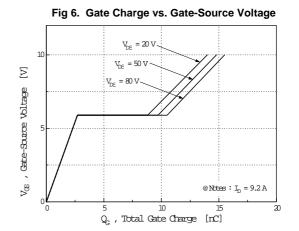
10 Nttes:
1. 250 (S Rulse Test
2. T_A = 25 °C
10 V_{DS} , Drain-Source Voltage [V]

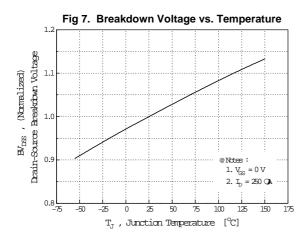












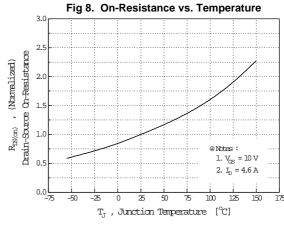
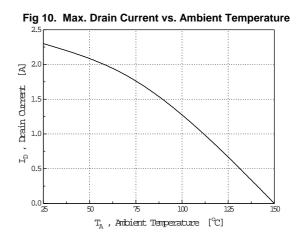


Fig 9. Max. Safe Operating Area 102 Operation in This Area is Limited by R DS(on A 10 (s 10 $I_{\rm D}$, Diain Current 10 10 1. $\mathrm{T_A}$ = 25 $^{\circ}\mathrm{C}$ 2. $T_J = 150$ °C 3. Single Pulse 10 10 10 V_{DS} , Drain-Source Voltage [V]



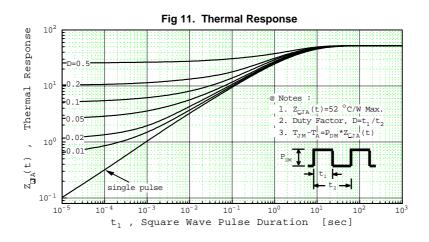


Fig 12. Gate Charge Test Circuit & Waveform

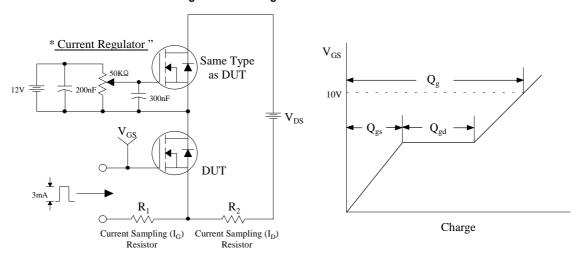


Fig 13. Resistive Switching Test Circuit & Waveforms

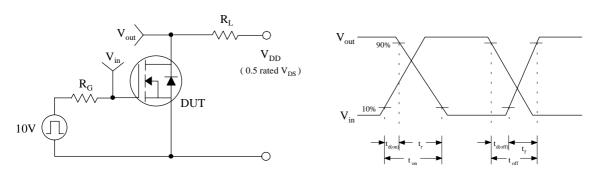
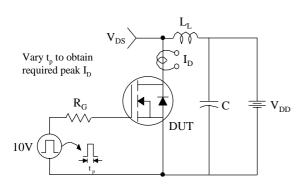


Fig 14. Unclamped Inductive Switching Test Circuit & Waveforms



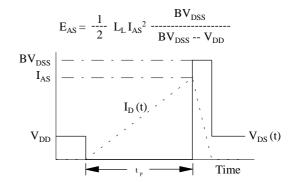
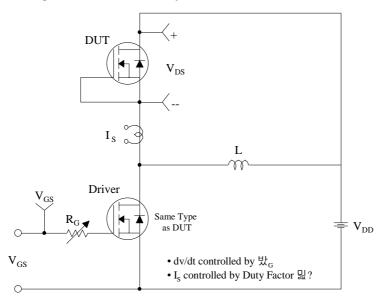
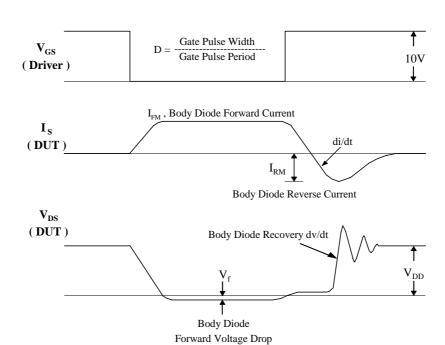


Fig 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms





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