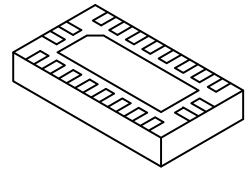
Dual-Supply, 8-Bit Signal Translator with Configurable Voltage Supplies and Signals Levels, 3-State Outputs and Auto Direction Sensing

FXMA108



WQFN−20
CASE 510CD

MARKING DIAGRAM

\$Y&Z&2&K FXMA108

\$Y	= **onsemi** logo
&Z	= Assembly Plant Code
&2	= 2−Digit Date Code
&K	= 2−Digits Lot Run Traceability Code
FXMA108	= Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 14 of this data sheet.

Description

The FXMA108 is a configurable dual−voltage supply translator designed for both uni−directional and bidirectional voltage translation between two logic levels. The device allows translation between voltages as high as 5.5 V to as low as 1.65 V. The A port tracks the V_{CCA} level and the B port tracks the V_{CCB} level. This allows for bi−directional voltage translation over a variety of voltage levels: 1.8 V, 2.5 V, 3.3 V, and 5.0 V.

The device remains in 3−state until both V_{CC}s reach active levels, allowing either V_{CC} to be powered−up first. Internal power−down control circuits place the device in 3−state if either V_{CC} is removed.

The /OE input, when high, disables both the A and B Side by placing them in a 3−state condition. The /OE input is supplied by V_{CCA}.

The FXMA108 supports bi−directional translation without the need for a direction control pin. The two sides of the device have auto−direction−sense capability. Either port may sense an input signal and transfer it as an output signal to the other port.

Features

- Bi−Directional Interface between Two Levels from 1.65 V to 5.5 V
- Fully Configurable: Inputs and Outputs Track V_{CC}
- Non−Preferential Power−Up; Either V_{CC} May Be Powered−Up First
- Outputs Remain in 3−State Until Active V_{CC} Level is Reached
- Outputs Switch to 3−State if Either V_{CC} is at GND
- Power−Off Protection
- Bus Hold On Data Inputs Eliminates the Need for Pull−Up Resistors
- Control Input (/OE) is Referenced to V_{CCA} Voltage
- Packaged in 20−Terminal WQFN
- Direction Control Not Needed
- 80 Mbps Throughput when Translating between 2.5 V and 5.0 V
- ESD Protection Exceeds:
  - 8 kV Human Body Model (B Port I/O to GND) (JESD22−A114 & Mil Std 883e 3015.7)
  - 5 kV Human Body Model (A Port I/O to GND) (JESD22−A114 & Mil Std 883e 3015.7)
  - 2 kV Charged Device Model (ESD STM 5.3) (JESD22−C101)

Applications

- Cell Phones, PDA, Digital Camera, Portable GPS, and Storage

FUNCTIONAL DIAGRAM

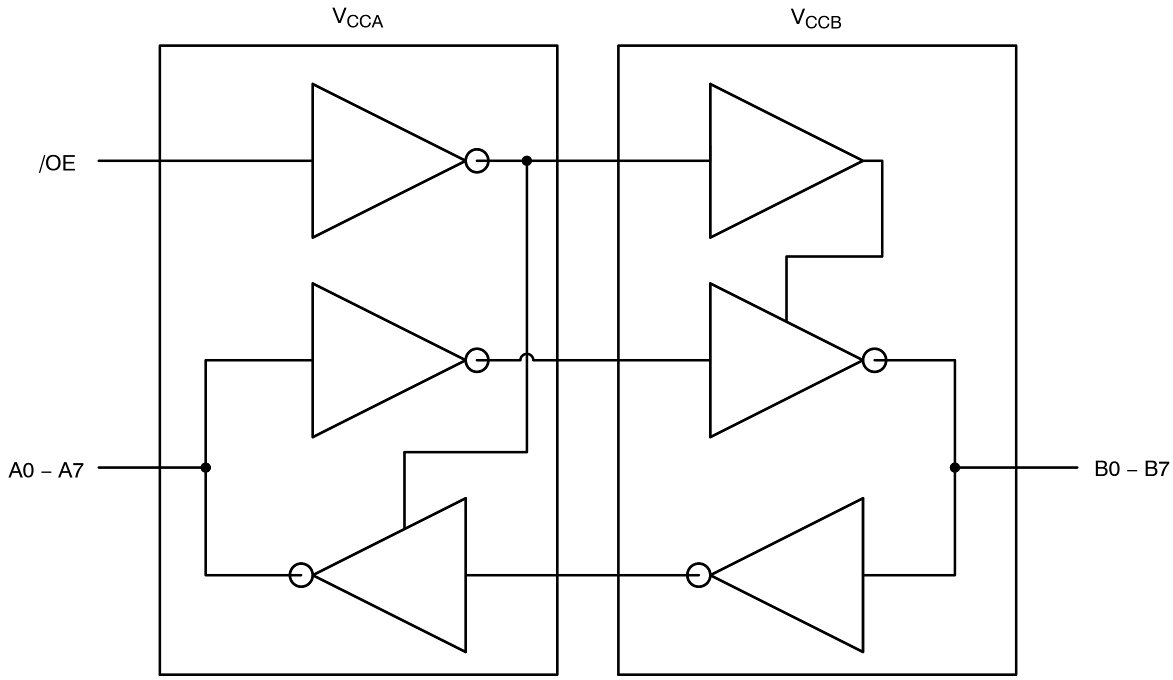


Figure 1. Block Diagram

FUNCTIONAL TABLE

Control	Outputs
/OE	
LOW Logic Level	Normal Operation
HIGH Logic Levl	3–State

PIN CONFIGURATION

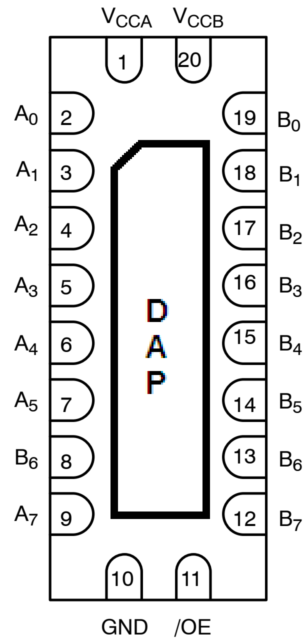


Figure 2. Pin Configuration (Top Through View)

PIN DEFINITIONS

Pin No.	Symbol	Description
1	V_{CCA}	A−Side Power Supply
2	A0	A−Side Inputs or 3−State Outputs
3	A1	A−Side Inputs or 3−State Outputs
4	A2	A−Side Inputs or 3−State Outputs
5	A3	A−Side Inputs or 3−State Outputs
6	A4	A−Side Inputs or 3−State Outputs
7	A5	A−Side Inputs or 3−State Outputs
8	A6	A−Side Inputs or 3−State Outputs
9	A7	A−Side Inputs or 3−State Outputs
10	GND	Ground
11	/OE	Output Enable Input
12	B7	B−Side Inputs or 3−State Outputs
13	B6	B−Side Inputs or 3−State Outputs
14	B5	B−Side Inputs or 3−State Outputs
15	B4	B−Side Inputs or 3−State Outputs
16	B3	B−Side Inputs or 3−State Outputs
17	B2	B−Side Inputs or 3−State Outputs
18	B1	B−Side Inputs or 3−State Outputs
19	B0	B−Side Inputs or 3−State Outputs
20	V_{CCB}	B−Side Power Supply
DAP	NC	No Connect

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Condition	Min	Max	Unit
V_{CC}	Supply Voltage		V_{CCA}	−0.5	7.0	V
			V_{CCB}	−0.5	7.0	
V_{IN}	DC Input Voltage		I/O Side A and B	−0.5	7.0	V
			Control Input (/OE)	−0.5	7.0	
V_O	Output Voltage		Output 3−State	−0.5	7.0	V
			Output Active (A_n) (Note 1)	−0.5	V_{CCA} + 0.5	
			Output Active (B_n) (Note 1)	−0.5	V_{CCB} + 0.5	
I_{IK}	DC Input Diode Current		V_{IN} < 0 V		−50	mA
I_{OK}	DC Output Diode Current		V_O < 0 V		−50	mA
			V_O > V_{CC}		+50	
I_{OH}/I_{OL}	DC Output Source/Sink Current			−50	+50	mA
I_{CC}	DC V_{CC} or Ground Current (Per Supply Pin)				±100	mA
T_{STG}	Storage Temperature Range			−65	+150	°C
ESD	Electrostatic Discharge Capability	Human Body Model, JESD22−A114, and Mil Std 883e 3015.7	B Port I/O to GND		8000	V
		Human Body Model, JESD22−A114 and Mil Std 883e 3015.7	A Port I/O to GND		5000	
		Charged Device Model, JESD22−C101 per ESD STM 5.3			2000	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. I_O absolute maximum ratings must be observed.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Conditions	Typ	Max	Unit
V_{CC}	Power Supply	Operating V_{CCA} or V_{CCB}	1.65	5.50	V
V_{IN}	Input Voltage	Side A and B	0	5.5	V
		Control Input (/OE)	0	V_{CCA}	V
T_A	Operating Temperature, Free Air		−40	+85	°C
dt/dV	Input Edge Rate	$V_{CCA/B}$ = 1.65 V to 5.5 V		10	ns/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

2. All unused inputs and input/outputs must be held at V_{CCI} or GND. V_{CCI} is the V_{CC} associated with the input side.

Power−Up/Power−Down Sequence

onsemi translators offer an advantage in that either V_{CC} may be powered up first. This benefit derives from the chip design. When either V_{CC} is at 0 V, outputs are in a high−impedance state. The control input (/OE) is designed to track the V_{CCA} supply. A pull−up resistor tying /OE to V_{CCA} should be used to ensure that bus contention, excessive currents, or oscillations do not occur during power−up or power−down. The size of the pull−up resistor is based upon the current−sinking capability of the device driving the /OE pin.

The recommended power−up sequence is:

1. Apply power to the first V_{CC}.
2. Apply power to the second V_{CC}.
3. Drive the /OE input LOW to enable the device.

The recommended power−down sequence is:

1. Drive /OE input HIGH to disable the device.
2. Remove power from either V_{CC}.
3. Remove power from the other V_{CC}.

Pull−Up/Pull−Down Resistors

Do not use pull−up or pull−down resistors. This device has bus−hold circuits: pull−up or pull−down resistors are not recommended because they interfere with the output state. The current through these resistors may exceed the hold drive, $I_{I(HOLD)}$ and/or $I_{I(OD)}$ bus−hold currents. The bus−hold feature eliminates the need for extra resistors.

DC ELECTRICAL CHARACTERISTICS (T_A = −40°C to +85°C)

Symbol	Parameter	Conditions	V_{CCA} (V)	V_{CCB} (V)	Min	Max	Unit
V_{IHA}	High Level Input Voltage	Data Inputs An Control Pin /OE	1.65 – 5.50	1.65–5.50	0.65 x V_{CCA}		V
V_{IHB}		Data Inputs Bn	1.65 – 5.50	1.65–5.50	0.65 x V_{CCA}		
V_{ILA}	Low Level Input Voltage	Data Inputs An Control Pin /OE	1.65 – 5.50	1.65–5.50		0.35 x V_{CCA}	V
V_{ILB}		Data Inputs Bn	1.65 – 5.50	1.65–5.50		0.35 x V_{CCA}	
V_{OHA}	High Level Output Voltage (Note 3)	I_{OH} = 20 μA	1.65 – 5.50	1.65–5.50	V_{CCA} – 0.4		V
V_{OHB}		I_{OH} = 20 μA	1.65 – 5.50	1.65–5.50	V_{CCB} – 0.4		
V_{OLA}	Low Level Output Voltage (Note 3)	I_{OL} = 20 μA	1.65 – 5.50	1.65–5.50		0.4	V
V_{OLB}		I_{OL} = 20 μA	1.65 – 5.50	1.65–5.50		0.4	
$I_{I(HOLD)}$	Bushold Input Minimum Drive Current	V_{IN} = 1.60 V	4.5	4.5	140		μA
		V_{IN} = 2.90 V	4.5	4.5	–140		
		V_{IN} = 1.05 V	3.0	3.0	75		
		V_{IN} = 1.95 V	3.0	3.0	–75		
		V_{IN} = 0.80 V	2.3	2.3	45		
		V_{IN} = 1.50 V	2.3	2.3	–45		
		V_{IN} = 0.57 V	1.65	1.65	25		
		V_{IN} = 1.07 V	1.65	1.65	–25		
$I_{I(ODH)}$	Bushold Input Overdrive High Current (Note 4)	Data Inputs An, Bn	5.5	5.5	750		μA
			3.6	3.6	450		
			2.7	2.7	300		
			1.95	1.95	200		
$I_{I(ODL)}$	Bushold Input Overdrive Low Current (Note 5)	Data Inputs An, Bn	5.5	5.5	–750		μA
			3.6	3.6	–450		
			2.7	2.7	–300		
			1.95	1.95	–200		
I_I	Input Leakage Current	Control Inputs /OE V_{IN} = V_{CCA} or GND	1.65 – 5.50	5.5		±1	μA
I_{OFF}	Power Off Leakage Current	An, V_O = 0 V to 5.5 V	0	5.5		±2	μA
		Bn, V_O = 0 V to 5.5 V	5.5	0		±2	
I_{OZ}	3–State Output Leakage	An, Bn V_O = 0 V or 5.5 V, /OE V_{IH}	5.5	5.5		±5	μA
		An, V_O = 0 V or 5.5 V, /OE = GND	5.5	0		±5	
		Bn, V_O = 0 V or 5.5 V, /OE = GND	0	5.5		±5	
$I_{CCA/B}$	Quiescent Supply Current (Notes 6, 7)	V_{IN} = V_{CCI} or GND, I_O = 0 /OE = GND	1.65 – 5.50	1.65 – 5.50		10	μA
I_{CCZ}		V_{IN} = V_{CCI} or GND, I_O = 0 /OE = V_{IH}	1.65 – 5.50	1.65 – 5.50		10	
I_{CCA}	Quiescent Supply Current (Notes 6, 7)	V_{IN} = V_{CCB} or GND, I_O = 0 B–to–A Direction /OE = GND	0	1.65 – 5.50		–10	μA
		V_{IN} = V_{CCA} or GND, I_O = 0 A–to–B	1.65 – 5.50	0		10	

DC ELECTRICAL CHARACTERISTICS (T_A = −40°C to +85°C) (continued)

Symbol	Parameter	Conditions	V_{CCA} (V)	V_{CCB} (V)	Min	Max	Unit
I_{CCB}	Quiescent Supply Current	$V_{IN} = V_{CCA}$ or GND, $I_O = 0$ A−to−B Direction /OE = GND	1.65 – 5.50	0		−10	µA
		$V_{IN} = V_{CCB}$ or GND, $I_O = 0$ B−to−A	0	1.65 – 5.50		10	

3. This is the output voltage for static conditions.
4. An external driver must source at least the specified current to switch LOW−to−HIGH.
5. An external driver must source at least the specified current to switch HIGH−to−LOW.
6. V_{CCI} is the V_{CC} associated with the input side.
7. Reflects current per supply, V_{CCA} or V_{CCB}.

DYNAMIC OUTPUT ELECTRICAL CHARACTERISTICS
A PORT (An) (Output Load: C_L = 15 pF, $R_L \geq 1$ MΩ.) (Note 8)

		T_A = −40°C to +85°C				
		V_{CCA} = 4.5 V to 5.5 V	V_{CCA} = 3.0 V to 3.6 V	V_{CCA} = 2.3 V to 2.7 V	V_{CCA} = 1.65 V to 1.95 V	
Symbol	**Parameter**	**Max**	**Max**	**Max**	**Max**	**Unit**
t_{rise}	Output Rise Time A Side (Note 9)	2.5	3.0	3.5	4.0	ns
t_{fall}	Output Fall Time A Side (Note 10)	2.5	3.0	3.5	4.0	ns

DYNAMIC OUTPUT ELECTRICAL CHARACTERISTICS
B PORT (Bn) (Output Load: C_L = 15 pF, $R_L \geq 1$ MΩ.) (Note 8)

		T_A = −40°C to +85°C				
		V_{CCB} = 4.5 V to 5.5 V	V_{CCB} = 3.0 V to 3.6 V	V_{CCB} = 2.3 V to 2.7 V	V_{CCB} = 1.65 V to 1.95 V	
Symbol	**Parameter**	**Max**	**Max**	**Max**	**Max**	**Unit**
t_{rise}	Output Rise Time B Side (Note 9)	3.5	3.5	3.5	4.0	ns
t_{fall}	Output Fall Time B Side (Note 10)	3.5	3.5	3.5	4.0	ns

8. Dynamic output characteristics are guaranteed, but not tested in production.
9. *See Figure 8*.
10. *See Figure 9*.

AC CHARACTERISTICS (V_{CCA} = 4.5 V to 5.5 V, Output Load) (*See Table 2*)

Symbol	Parameter	T_A = −40°C to +85°C								Unit
		V_{CCB} = 4.5 V to 5.5 V		V_{CCB} = 3.0 V to 3.6 V		V_{CCB} = 2.3 V to 2.7 V		V_{CCB} = 1.65 V to 1.95 V		
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{PLH}, t_{PHL}	A−to−B Side	1.5	5.0	1.75	6.0	2.0	6.5	2.6	10.5	ns
	B−to−A Side	1.5	5.0	1.75	6.0	2.0	6.5	2.6	10.5	
t_{PZL}, t_{PZH}	/OE−to−A, /OE−to−B		1.7		1.7		1.7		1.7	μs
t_{skew}	A Port, B Side (Note 11)		0.5		0.5		0.5		0.5	ns

11. Skew is the variation of propagation delay between output signals and applies only to output signals on the same Side (An or Bn) and switching with the same polarity (LOW−to−HIGH or HIGH−to−LOW). Skew is guaranteed, but not tested in production *(see Figure 11).*

AC CHARACTERISTICS (V_{CCA} = 3.0 V to 3.6 V, Output Load) (*See Table 2*)

Symbol	Parameter	T_A = −40°C to +85°C								Unit
		V_{CCB} = 4.5 V to 5.5 V		V_{CCB} = 3.0 V to 3.6 V		V_{CCB} = 2.3 V to 2.7 V		V_{CCB} = 1.65 V to 1.95 V		
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{PLH}, t_{PHL}	A−to−B Side	2.0	5.5	2.2	6.5	2.4	7.5	2.6	11.0	ns
	B−to−A Side	2.0	5.5	2.2	6.5	2.4	7.5	2.6	11.0	
t_{PZL}, t_{PZH}	/OE−to−A, /OE−to−B		1.7		1.7		1.7		1.7	μs
t_{skew}	A Port, B Side (Note 12)		0.7		0.7		0.7		0.7	ns

12. Skew is the variation of propagation delay between output signals and applies only to output signals on the same Side (An or Bn) and switching with the same polarity (LOW−to−HIGH or HIGH−to−LOW). Skew is guaranteed, but not tested in production *(see Figure 11).*

AC CHARACTERISTICS (V_{CCA} = 2.3 V to 2.7 V, Output Load) (*See Table 2*)

Symbol	Parameter	T_A = −40°C to +85°C								Unit
		V_{CCB} = 4.5 V to 5.5 V		V_{CCB} = 3.0 V to 3.6 V		V_{CCB} = 2.3 V to 2.7 V		V_{CCB} = 1.65 V to 1.95 V		
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{PLH}, t_{PHL}	A−to−B Side	2.0	6.5	2.2	7.7	2.4	8.5	2.6	11.0	ns
	B−to−A Side	2.0	7.0	2.2	7.5	2.4	8.5	2.6	12.0	
t_{PZL}, t_{PZH}	/OE−to−A, /OE−to−B		1.7		1.7		1.7		1.7	μs
t_{skew}	A Port, B Side (Note 13)		0.7		0.7		0.7		0.7	ns

13. Skew is the variation of propagation delay between output signals and applies only to output signals on the same Side (An or Bn) and switching with the same polarity (LOW−to−HIGH or HIGH−to−LOW). Skew is guaranteed but not tested in production *(see Figure 11).*

AC CHARACTERISTICS (V_{CCA} = 1.65 V to 1.95 V, Output Load) (*See Table 2*)

Symbol	Parameter	T_A = −40°C to +85°C								Unit
		V_{CCB} = 4.5 V to 5.5 V		V_{CCB} = 3.0 V to 3.6 V		V_{CCB} = 2.3 V to 2.7 V		V_{CCB} = 1.65 V to 1.95 V		
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{PLH}, t_{PHL}	A−to−B Side	2.0	10.0	2.2	11.0	2.4	12.0	2.6	14.0	ns
	B−to−A Side	2.0	10.0	2.2	10.5	2.4	11.0	2.6	14.0	
t_{PZL}, t_{PZH}	/OE−to−A, /OE−to−B		1.7		1.7		1.7		1.7	μs
t_{skew}	A Port, B Side (Note 14)		1.2		1.2		1.2		1.2	ns

14. Skew is the variation of propagation delay between output signals and applies only to output signals on the same Side (An or Bn) and switching with the same polarity (LOW−to−HIGH or HIGH−to−LOW). Skew is guaranteed, but not tested in production *(see Figure 11).*

MAXIMUM DATA RATE (*For output load, see Table 2.*) (Notes 15, 16)

V_{CCA}	Direction	T_A = −40°C to +85°C V_{CCB} = 4.5 V to 5.5 V Min	V_{CCB} = 3.0 V to 3.6 V Min	V_{CCB} = 2.3 V to 2.7 V Min	V_{CCB} = 1.65 V to 1.95 V Min	Unit
V_{CCA} = 4.5 V to 5.5 V	A–to–B	100	100	80	60	Mbps
	B–to–A	100	100	80	80	
V_{CCA} = 3.0 V to 3.6 V	A–to–B	100	100	80	60	
	B–to–A	100	100	80	80	
V_{CCA} = 2.3 V to 2.7 V	A–to–B	80	80	60	40	
	B–to–A	80	80	60	60	
V_{CCA} = 1.65 V to 1.95 V	A–to–B	80	80	60	40	
	B–to–A	80	80	40	40	

15. Maximum data rate is guaranteed, but not tested in production.
16. Maximum data rate is specified in megabits per second with all outputs switching, *(see Figure 10).* It is equivalent to two times the F−toggle frequency, specified in megahertz. For example, 100 Mbps is equivalent to 50 MHz.

CAPACITANCE (T_A = ±25°C)

Symbol	Parameter		Conditions	Typical	Unit
C_{IN}	Input Capacitance, Control Pin /(OE)		V_{CCA} = V_{CCB} = GND	3	pF
$C_{I/O}$	Input / Output Capacitance	An	V_{CCA} = V_{CCB} = 5.0 V, /OE = V_{CCA}	4	pF
		Bn		5	
C_{PD}	Power Dissipation Capacitance		V_{CCA} = V_{CCB} = 5.0 V, V_{IN} = 0 V or V_{CC}, f = 10 MHz	28	pF

I/O ARCHITECTURE BENEFIT

The FXMA108 I/O architecture benefits the end user, beyond level translation, in the following three ways:

Auto Direction without an external direction pin.

Drive Capacitive Loads. Automatically shifts to a higher current drive mode only during "Dynamic Mode" or HL / LH transitions.

Lower Power Consumption. Automatically shifts to low−power mode during "Static Mode" (no transitions), lowering power consumption.

The FXMA108 does not require a direction pin. Instead, the I/O architecture detects input transitions on both side and automatically transfers the data to the corresponding output. For example, for a given channel, if both A and B side are at a static LOW, the direction has been established as A →B, and a LH transition occurs on the B port; the FXMA108 internal I/O architecture automatically changes direction from A → B to B → A.

During HL / LH transitions, or "Dynamic Mode," a strong (typically 30 mA) output driver drives the output channel in parallel with a weak (typically 100 μA) output driver. After a typical delay of approximately 10 ns – 50 ns, the strong driver is turned off, leaving the weak driver enabled for holding the logic state of the channel. This weak driver is called the "bus hold." "Static Mode" is when only the bus hold drives the channel. The bus hold can be over ridden (typically 500 μA) in the event of a direction change. The strong driver allows the FXMA108 to quickly charge and discharge capacitive transmission lines during dynamic mode. Static mode conserves power, where I_{CC} is typically < 5 μA.

Bus Hold Minimum Drive Current

Specifies the minimum amount of current the bus hold driver can source/sink. The bus hold minimum drive current (I_{HOLD}) is V_{CC} dependent and guaranteed in the DC Electrical tables. The intent is to maintain a valid output state in a static mode, but that can be overridden when an input data transition occurs.

Bus Hold Input Overdrive Drive Current

Specifies the minimum amount of current required (by an external device) to overdrive the bus hold in the event of a direction change. The bus hold overdrive (I_{ODH}, I_{ODL}) is V_{CC} dependent and guaranteed in the DC Electrical tables.

Dynamic Output Current

The strength of the output driver during LH / HL transitions is captured in Figure 3 (I_{OLH}, I_{OHD}). The plot depicts the FXMA108 typical dynamic output current with a lumped capacitance of 4 pF.

Because the strong output driver is turned on only during LH / HL transitions, the actual drive current is difficult to measure directly. Approximate the drive current with the following formula:

$$I_{OHD} \approx \left(C_{I/O}\right) \times \frac{\Delta V_{OUT}}{\Delta t} = \left(C_{I/O}\right) \times \frac{0.6 \times V_{CCO}}{t_{RISE}} \quad \text{(eq. 1)}$$

where $C_{I/O}$ = the typical lumped capacitance and V_{CCO} is the supply voltage of the output driver.

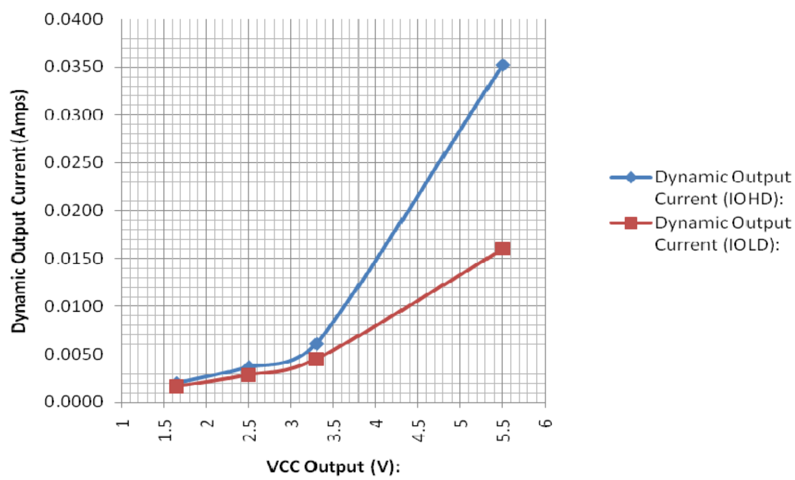


Figure 3. Typical Dynamic Output Current

AC TESTS AND WAVEFORMS

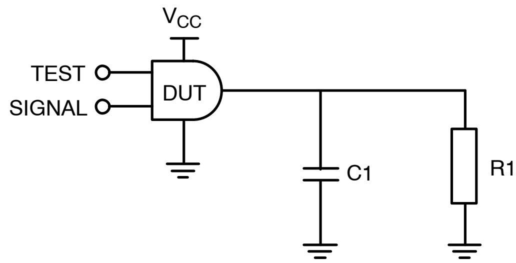


Figure 4. AC Test Circuit

Table 1. TEST CIRCUIT PARAMETERS

Test	Input Signal	Output Enable Control
t_{PLH}, t_{PHL}	Data Pulses	0 V
t_{PZL}	0 V	HIGH−to−LOW Switch
t_{PZH}	V_{CCI}	HIGH−to−LOW Switch

Table 2. AC LOAD TABLE

V_{CCO}	C1	R1
1.8 V ± 0.15 V	15 pF	1 MΩ
2.5 V ± 0.2 V	15 pF	1 MΩ
3.3 V ± 0.3 V	15 pF	1 MΩ
5.0 V ± 0.5 V	15 pF	1 MΩ

AC TESTS AND WAVEFORMS (continued)

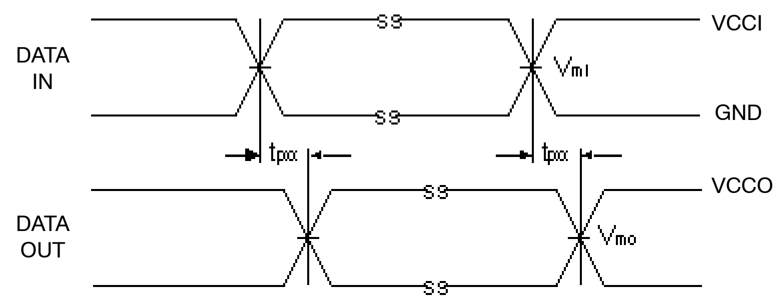


Figure 5. Waveform for Inverting and Non−Inverting Functions

NOTES:
17. Input $t_R = t_F$ = 2.0 ns, 10% to 90%.
18. Input $t_R = t_F$ = 2.5 ns, 10% to 90%, at V_{IN} = 3.0 V to 5.5 V only.

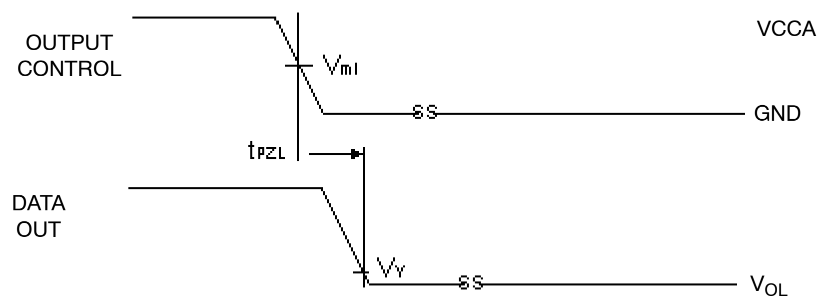


Figure 6. 3−State Output Low Enable Time for Low Voltage Logic

NOTES:
19. Input $t_R = t_F$ = 2.0 ns, 10% to 90%.
20. Input $t_R = t_F$ = 2.5 ns, 10% to 90%, at V_{IN} = 3.0 V to 5.5 V only.

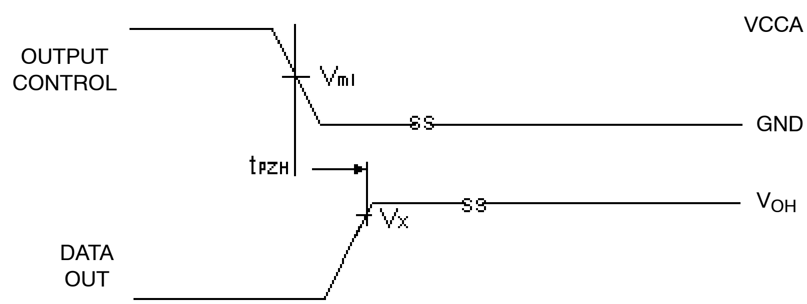


Figure 7. 3−State Output High Enable Time for Low Voltage Logic

NOTES:
21. Input $t_R = t_F$ = 2.0 ns, 10% to 90%.
22. Input $t_R = t_F$ = 2.5 ns, 10% to 90%, at V_{IN} = 3.0 V to 5.5 V only.

AC TESTS AND WAVEFORMS (continued)

Symbol	V_{CC}
V_{MI} (Note 23)	$V_{CCI}/2$
V_{MO}	$V_{CCO}/2$
V_X	0.9 x V_{CCO}
V_Y	0.1 x V_{CCO}

23. $V_{CCI} = V_{CCA}$ for control pin /OE or $V_{MI} = (V_{CCA}/2)$.

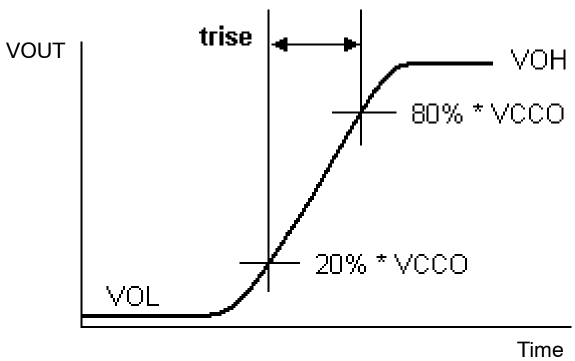


Figure 8. Active Output Rise Time

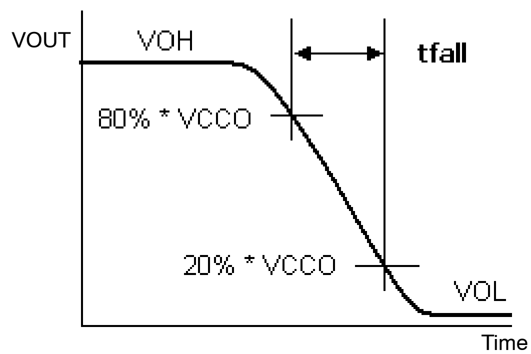
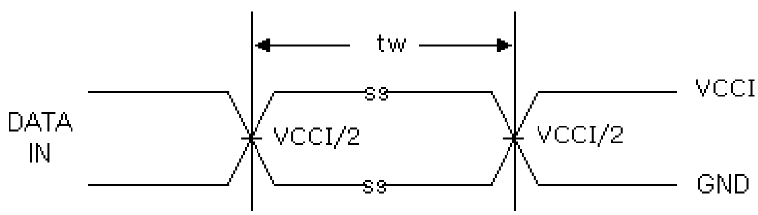
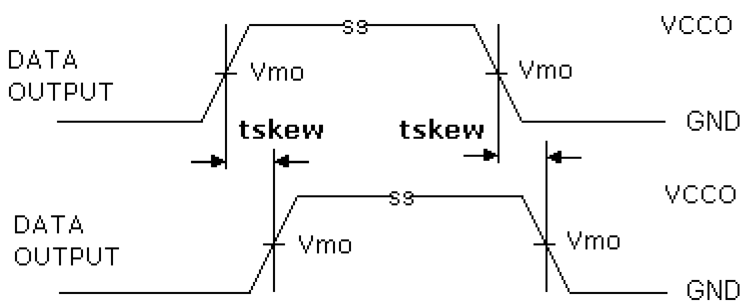


Figure 9. Active Output Fall Time



Max data rate, f = 1 / tw

Figure 10. Maximum Data Rate



tskew = (tpHLmax – tpHLmin) or (tpLHmax – tpLHmin)

Figure 11. Output Skew Time

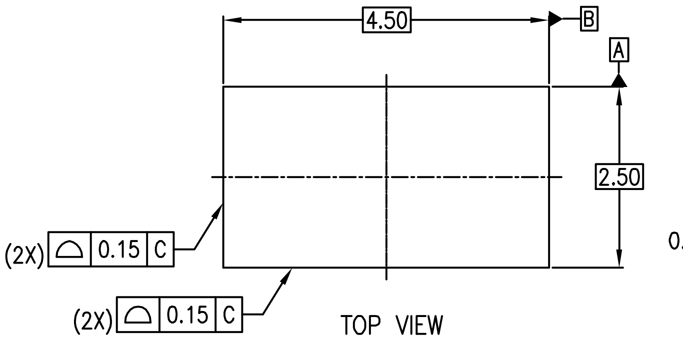
ORDERING INFORMATION

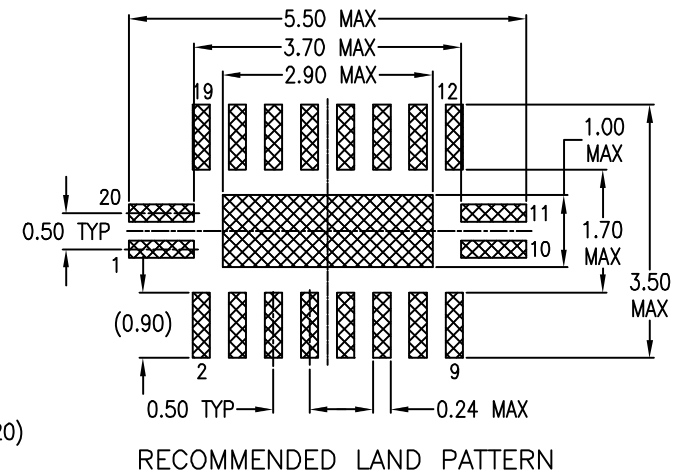
Part Number	Operating Temperature Range	Package	Shipping†
FXMA108BQX	−40 to 85°C	WQFN20 4.5 x 2.5, 0.5P (Pb−Free)	3000 / Tape & Reel

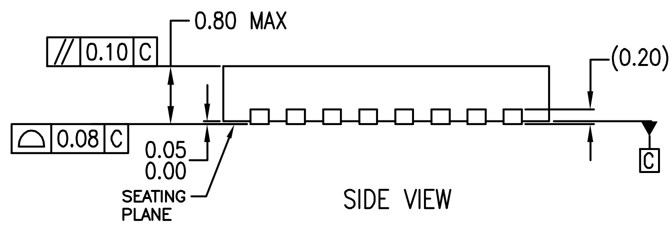
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

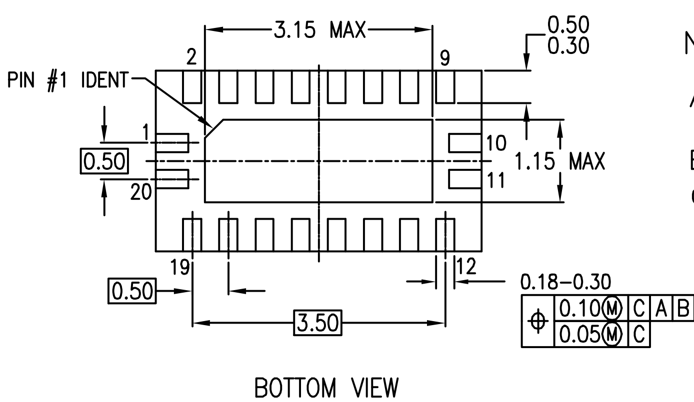
WQFN20 4.5x2.5, 0.5P
CASE 510CD
ISSUE O

DATE 31 AUG 2016









NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO–241, VARIATION AC
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994

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