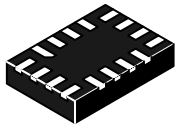
Type-C CC with High Speed Digital (HSD) Port Protection Switch

FUSB252



UQFN16 1.8 x 2.6, 0.4P
CASE 523BF

Description

The FUSB252 is an integrated port protection switch for USB Type−C® applications. This product will protect HSD+/− and CCx pins when stressed with voltages up to 20 V. Over−Voltage Protection (OVP) at 5.8 V typical will protect the system for Electrical Overstress (EOS) damage. With a fully integrated USB 2.0 switch for HSD+/−, this product can be easily integrated into existing solutions. The HSD switches can pass USB 2.0 signals with bandwidth 1 GHz to maintain signal integrity and eye compliance.

The CC switches have very low RON of 0.3 Ω to minimize signal attenuation. The FUSB252 also provides Dead Battery support per the Type−C specification Additional features include Under−Voltage Lockout (UVLO) and thermal shutdown.

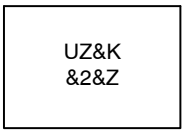
Features

- Fully Type−C Port Protection
- Supports USB Type−C Specification 1.2
- V_{CC} 0 V − 5.5 V
- 20 V DC Protection on V_{CC}
- 16 V DC Protection on HSD Port
- V_{DD} Operating Range, 2.7 V − 5.5 V
- Current Capability: 1 A
- CC R_{ON}: 0.3 Ω Typical
- HSD R_{ON}: 5 Ω Typical
- Wide −3 db Bandwidth: 1 GHz
- Low Power Operation: I_{CC} = 9 μA Typical
- Dead Battery Support (UFP Support when No Power Applied)
- CC Over−Voltage Protection: Typical = 5.6 V
- This is a Pb−Free Device

Applications

- Smartphones
- Tablets
- Laptops

MARKING DIAGRAM



UZ	= Device Code
&K	= 2−Digit Lot Run Traceability Code
&2	= 2−Digit Date Code
&Z	= Assembly Location

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

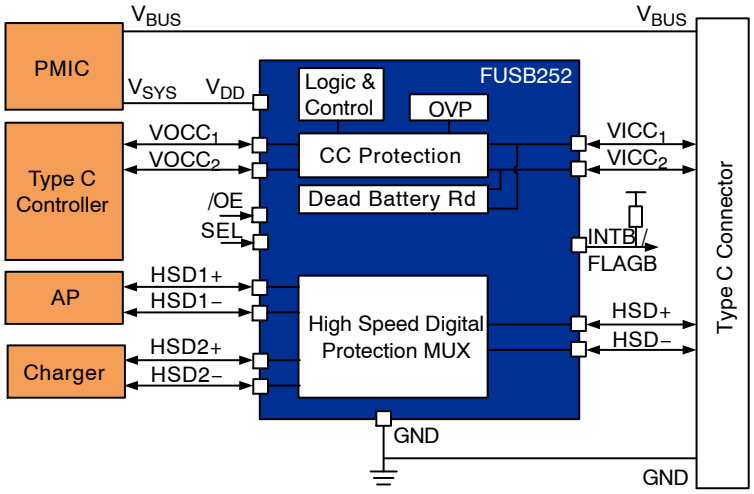


Figure 1. Typical Application

ORDERING INFORMATION

Part Number	Operating Temperature Range	Package	Top Mark	Shipping†
FUSB252UMX	−40 to 85°C	16−Lead Ultrathin Molded Leadless Package (UMLP) 1.8 x 2.6 mm	UZ	5000 / Tape and Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

BLOCK DIAGRAM

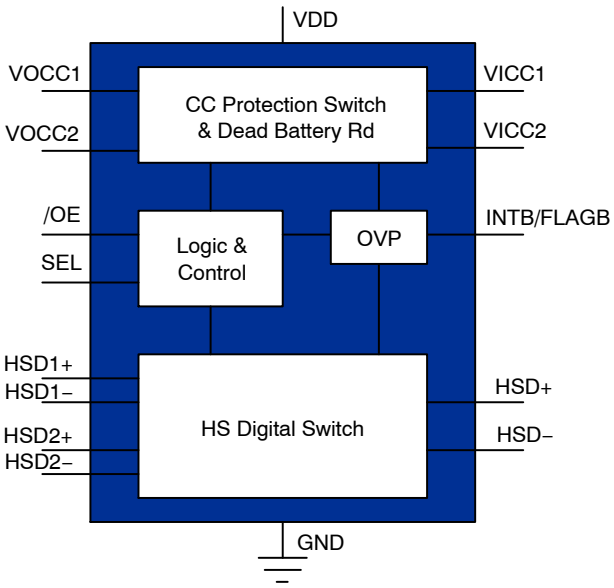


Figure 2. Block Diagram

REFERENCE SCHEMATIC

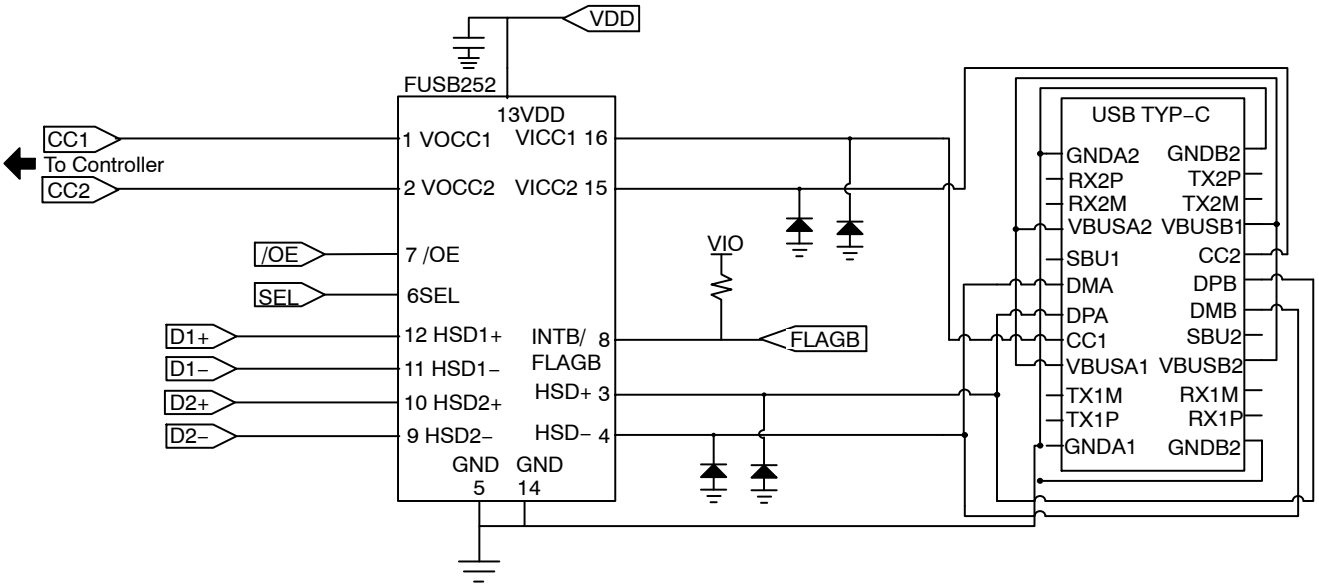


Figure 3. Reference Schematic

PIN CONFIGURATIONS

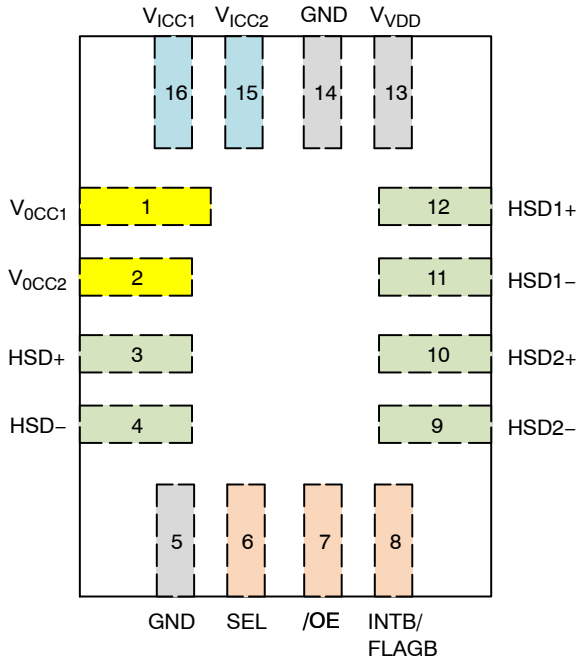


Figure 4. Pin Assignment (Top Through View)

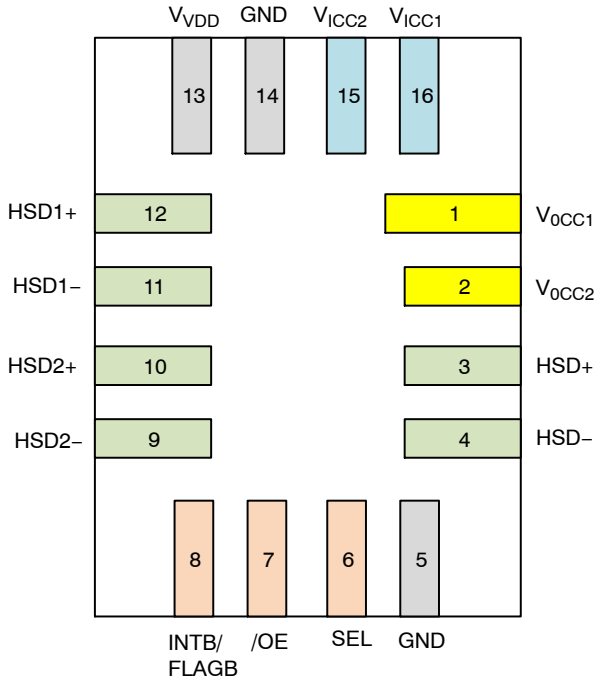


Figure 5. Pin Assignment (Bottom View)

PIN DESCRIPTION

Bump	Name	Type	Description
POWER INTERFACE			
13	VDD	Power	Power
5, 14	GND	Ground	Ground
USB TYPE−C CONNECTOR INTERFACE INPUT			
15, 16	VICC1, 2	Input	Type C CC Interface OVP protection input, Connect to connector
USB TYPE−C CONNECTOR INTERFACE OUTPUT			
1, 2	VOCC1, 2	Output	Type C CC Interface output. Connect to controller
USB HIGH SPEED DATA INTERFACE			
3	HSD+	I/O	Common High Speed Digital / USB Data Bus
4	HSD−	I/O	Common High Speed Digital / USB Data Bus
12	HSD1+	I/O	Multiplexed Source Input 1
11	HSD1−	I/O	Multiplexed Source Input 1
10	HSD2+	I/O	Multiplexed Source Input 2
9	HSD2−	I/O	Multiplexed Source Input 2
SIGNAL INTERFACE			
7	/OE	I/O	Switch Enable
6	SEL	I/O	Switch Select
8	INTB/FLAGB	Output	OVP Interrupt Flag

Table 1. CC SWITCH TRUTH TABLE CONFIGURATION

V_{DD}	V_{ICC} Voltage	CC Switch Configuration
0 V – UVLO (Not Valid)	0 V – 5.8 V	OFF Dead Battery Rd Inserted
	5.8 V to 20 V	OFF Dead Battery Rd Inserted
2.7 V – 5.5 V (Valid)	0 V – 5.8 V	On
	5.8 V to 20 V	OFF (OVP)

Table 2. CC SWITCH TRUTH TABLE CONFIGURATION

/OE	SEL	VDD	HSD+ / HSD–	CC
1	0	Not Valid	X (Open/High–Z)	Dead Battery
0	0	Not Valid	X (Open/High–Z)	Dead Battery
1	X	Valid	X (Open/High–Z)	On
0	0	Valid	HSD1+ / HSD1–	On
0	1	Valid	HSD2+ / HSD2–	On

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter			Min	Max	Unit
V_{VDD}	Supply Voltage from V_{DD}			−0.5	12.0	V
V_{VICC}	V_{ICCx}, to GND			−0.5	24	V
V_{SW}	$V_{HSD±}$, to GND			−5	16	V
V_{OCC}, V_{SW}	V_{OCCx} $V_{HSDx±}$ to GND			−0.5	6	V
$V_{CONTROL}$	DC Input Voltage (S, /OE)			−0.5	V_{VDD}	V
I_{CCSW}	DC CC Switch Current				1.25	A
I_{USBSW}	DC Output Current				100	mA
I_{IK}	DC Input Diode Current			−50		mA
$T_{STORAGE}$	Storage Temperature Range			−65	+150	°C
T_J	Maximum Junction Temperature				+150	°C
T_L	Lead Temperature (Soldering, 10 seconds)				+260	°C
ESD	IEC 61000−4−2 System ESD	Connector Pins (V_{VDD}, V_{ICCx}, $V_{HSD±}$)	Air Gap	15		kV
			Contact	8		
	IEC 61000−4−5 Surge ESD	V_{ICCx} to GND		−24	24	V
		$V_{HSD±}$ to GND		−16	16	V
	Human Body Model, JEDEC JESD22−A114	Power to GND		4		kV
		External Pins to GND ($V_{HSD±}$, V_{ICCx})				
		System Side Pin ($V_{HSDx±}$, V_{OCCx}, S, /OE, FLAGB)		2		
	Charged Device Model, JEDEC LESD22−C101	All Pins		1		

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
V_{VDD}	Supply Voltage	2.7	4.2	5.5	V
V_{ICC}	Type C Input Voltage	0		5.5	V
V_{OCC}	Type C Output Voltage	0		5.5	V
I_{CCSW}	Maximum CC Switch Current			1	A
V_{CNTRL}	Control Input Voltage (SEL, /OE)	−0.5		V_{VDD}	V
V_{SW}	HSD/USB Switch I/O Voltage	−0.5		4.5	V
T_A	Operating Temperature	−40		+85	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

DC CHARACTERISTICS (Unless otherwise specified: Recommended T_A and T_J temperature ranges. All typical values are at T_A = 25°C and V_{DD} = 4.2 V unless otherwise specified.)

Symbol	Characteristic	V_{DD} (V)	Conditions	T_A = −40°C to +85°C, T_J = −40°C to +125°C			Unit
				Min	Typ	Max	
BASIC OPERATION DEVICE							
I_{CC}	Quiescent Supply Current	2.7 to 5.5	/OE = L, I_{OUT} = 0		9		μA
			/OE = H, I_{OUT} = 0		9		
I_{OFF}	Power−Off Leakage Current	0			3		μA
BASIC OPERATION CC SWITCH							
$I_{SD(DB)}$	Dead Battery Supply Current	0 to UVLO	Dead Battery State Supply Current		15		μA
R_{ON}	CC Path On Resistance	2.7 to 5.5	I_{OUT} = 200 mA		350	480	mΩ
V_{OV_TRIP}	Input OVP Lockout	2.7 to 5.5	V_{ICC} Rising		5.65	6.20	V
			V_{ICC} Falling		5.3		
V_{OV_HYS}	Input OVP Hysteresis	2.7 to 5.5			0.35		V
V_{UVLO}	Under−Voltage Lockout	2.7 to 5.5	V_{DD} Rising		2.55	2.70	V
			V_{DD} Falling		2.5		
TSD	Thermal Shutdown (Note 1)		Shutdown Threshold		150		°C
			Return from Shutdown		130		
			Hysteresis		20		
Rd	Dead Battery Pull−Down Resistance	0 to UVLO	Dead Battery Resistance	4.08	5.10	6.12	kΩ
			Voltage on Pin	0.25		2.6	V
BASIC OPERATION HSD SWITCH							
V_{OV_TRIP}	Input OVP Lockout	2.7 to 5.5	$V_{HSD\pm}$ Rising		4.4	5.0	V
			$V_{HSD\pm}$ Falling		4.1		
V_{OV_HYS}	Input OVP Hysteresis	2.7 to 5.5			0.3		V
V_{UV_TRIP}	Input Under−Voltage Lockout	2.7 to 5.5			−1.2		V
V_{IH}	Input Voltage High	2.7 to 5.5		1.3			V
V_{IL}	Input Voltage Low	2.7 to 5.5				0.5	V
I_{IN}	Control Input Leakage	2.7 to 5.5	V_{SW} = 0 to V_{DD}		0.1		μA
I_{OZ}	Off State Leakage	4.2	0 ≤ HSDn ≤ 3.6 V		2		μA
		4.2	0 ≤ HSD1$n_{\pm}$, HSD2$n_{\pm}$ ≤ 3.6 V		100		nA
R_{ON}	HS Switch On Resistance	4.2	V_{SW} = 0.4 V, I_{ON} = −8 mA		5		Ω
ΔR_{ON}	HS Delta R_{ON}	4.2	V_{SW} = 0.4 V, I_{ON} = −8 mA		0.1		Ω

1. Guaranteed by characterization, not production tested.

AC CHARACTERISTICS (Unless otherwise specified: Recommended T_A and T_J temperature ranges. All typical values are at T_A = 25°C and V_{DD} = 3.8 V unless otherwise specified.)

Symbol	Characteristic	V_{DD} (V)	Conditions	T_A = −40°C to +85°C, T_J = −40°C to +125°C			Unit
				Min	Typ	Max	
CC SWITCH TIMING PARAMETER							
t_{OVP}	Response Time (Note 2)	2.7 to 5.5	I_{OUT} = 0.2 A, C_L = 200 pF, V_{ICCx} 5 V to 6 V		0.5	1.0	μs
t_{ON}	Turn−On Time		V_{DD} Rising 2 V to 3 V		25		ms
T_{MBB}	Make−Before−Break	2.7 to 5.5	V_{DD} Rising 2 V to 3 V		600		ns
CC SWITCH CAPACITANCE							
C_{ON}	Switch Path On Capacitance (Note 2)	2.7 to 5.5			100		pF
CC SWITCH BANDWIDTH							
BW	PD Traffic Bandwidth (Note 2)	2.7 to 5.5	R_L = 50 Ω, C_L = 200 pF		25		MHz
HSD SWITCH TIMING PARAMETER							
t_{OVP}	Response Time (Note 2)	2.7 to 5.5	I_{OUT} = 0.2 A, $V_{D\pm}$ 4 V to 5V		0.5	1.0	μs
t_{ON}	Turn−On Time, /OE to Output (Note 2)	2.7 to 5.5	R_L = 50 Ω, C_L = 5 pF, V_{SW} = 0.8 V		25		ms
t_{OFF}	Turn−Off Time, /OE to Output (Note 2)	2.7 to 5.5	R_L = 50 Ω, C_L = 5 pF, V_{SW} = 0.8 V		100	400	ns
t_{PD}	Propagation Delay (Note 2)	2.7 to 5.5	R_L = 50 Ω, C_L = 5 pF		0.25		ns
T_{BBM}	Break−Before−Make (Note 2)	2.7 to 5.5	R_L = 50 Ω, C_L = 5 pF, V_{SWx} = 0.8 V SEL = H ↔ L		100		μs
O_{IRR}	Off Isolation	2.7 to 5.5	R_L = 50 Ω, f = 240 MHz		−25		dB
Xtalk	Non−Adjacent Channel Crosstalk	2.7 to 5.5	R_L = 50 Ω, f = 240 MHz		−40		dB
HSD SWITCH CAPACITANCE							
C_{IN}	Control Pin Input Capacitance (Note 2)	0			1.5		pF
C_{ON}	HSD+ / HSD− On Capacitance (Note 2)	2.7 to 5.5	/OE = L, f = 240 MHz		4		pF
C_{OFF}	HSD1x / HSD2x Off Capacitance (Note 2)	2.7 to 5.5	/OE = H		2.5		pF
USB SWITCH BANDWIDTH							
BW	−3 db Bandwidth (Note 2)	2.7 to 5.5	R_L = 50 Ω, C_L = 0 pF		1400		MHz
		2.7 to 5.5	R_L = 50 Ω, C_L = 5 pF		560		
USB HIGH−SPEED−RELATED							
$t_{SK(P)}$	Skew of Opposite Transitions of the Same Output (Note 2)		R_L = 50 Ω, C_L = 5 pF		25		ps
t_J	Total Jitter (Note 2)		R_L = 50 Ω, C_L = 5 pF, t_R = t_F = 500 ps (10−90%) at 480 Mbps (PRBS = 2^{15} − 1)		200		ps

2. Guaranteed by characterization, not production tested.

OPERATION AND APPLICATION DESCRIPTION

Out of Spec Surge/Spike Voltage due to Hot Plug

The FUSB252 protects end systems against 20 V DC on the CC pin, in cases where the FUSB252 is tested to mimic a hot plug event, a fully charged cable connected to a power supply set to 20 V is used to zap the VICC pins of the device. In these cases, the inductance of the cable causes voltage spikes that are higher than the absolute maximum ratings of the of the VICC pins. These voltages can cause damage to the VOCC pins. This scenario does not occur in normal usage. The Type−C specification prevents the plug from having 20 V on VBUS from a PD source prior to a PD contract being completed. When the 20 V potential is on VBUS and shorted to the CC pin, it causes a detach and the voltage spikes are less likely to occur. The following reference circuit is required when the application calls for additional protection to protect against such event as hot plug.

Application Specific Schematic

- Place a 5 V to 6 V rated Zener TVS diode such as (CZRF52C5V6 or CD1005−Z5V1) on the VOCC pin, and a 5 Ω resistor to device ground to prevent the FUSB252 from being damaged during these tests. With this additional protection if is also important to select the right external VICC IEC TVS for the best overall performance.
- Without the additional protection the device by itself can withstand up to 9 V under the same hot plug condition.

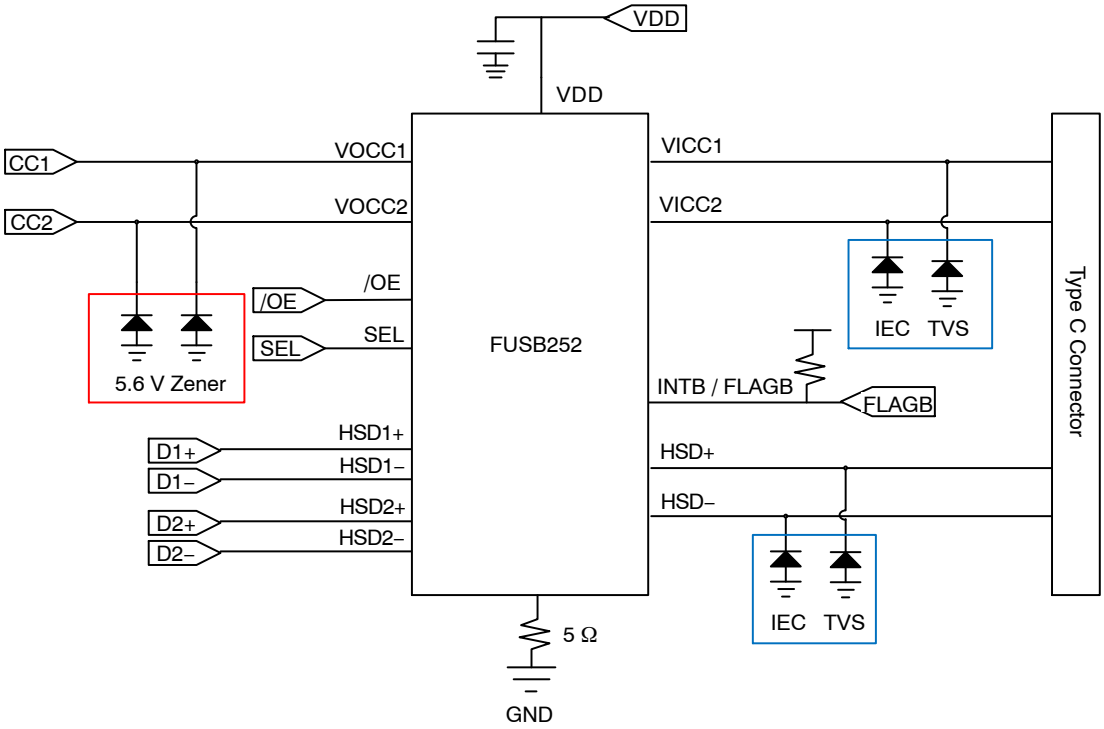


Figure 6. Reference Schematic

Over−Voltage Protection

When over−voltage event is detected, device will activate OVP to shutdown the switch within t_{OVP}, as well as signal the FLAGB to indicate there is OV event to the system.

Fault Reporting

Upon the detection of an over−voltage event, the INTB/FLAGB signals the fault by activating LOW.

Type−C Solution Reference

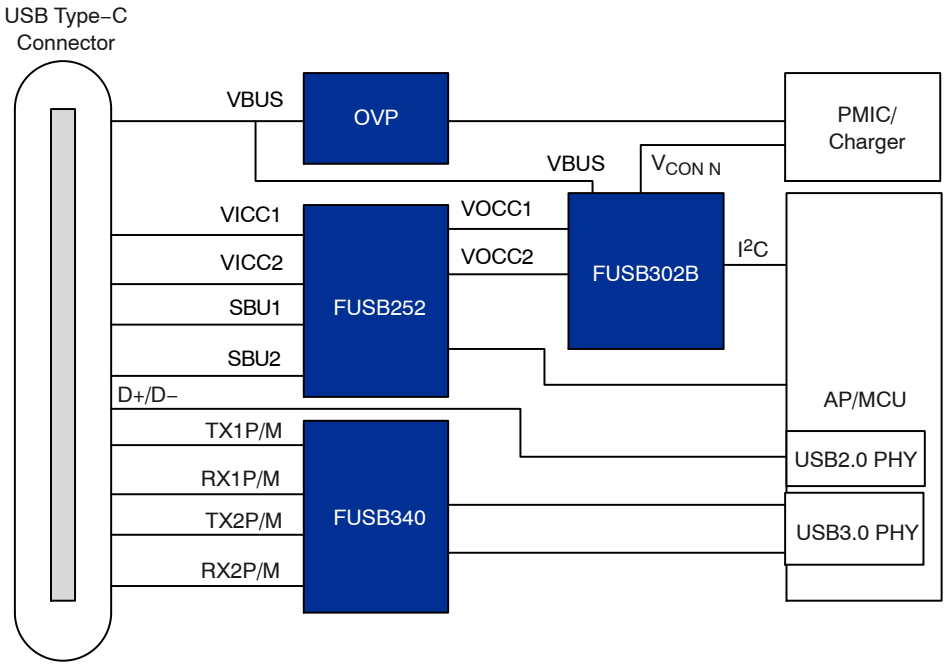


Figure 7. Example of Type−C Solution Reference (SBU)

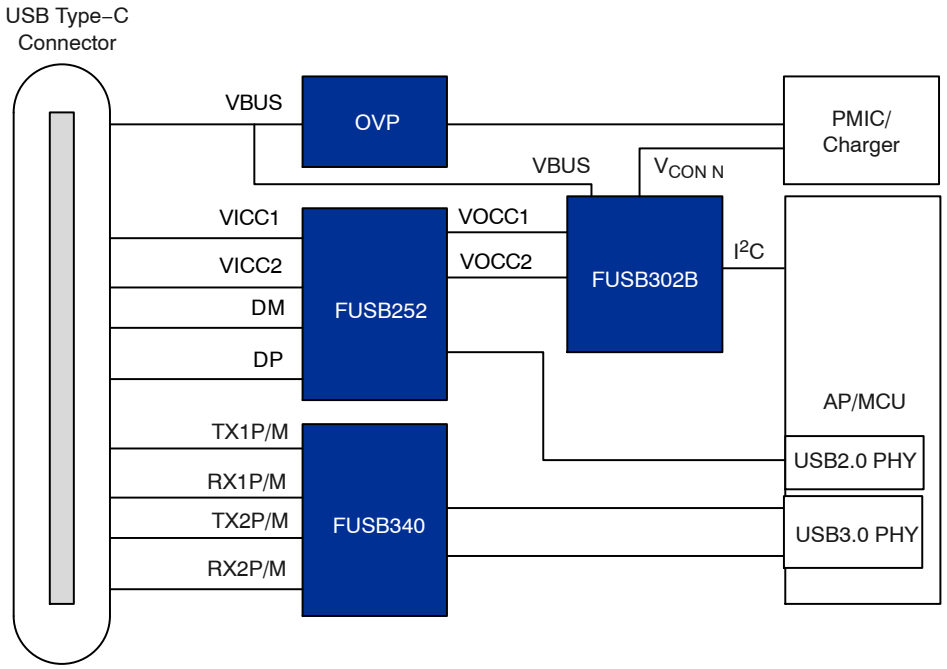


Figure 8. Example of Type−C Solution Reference (USB)

TEST DIAGRAMS

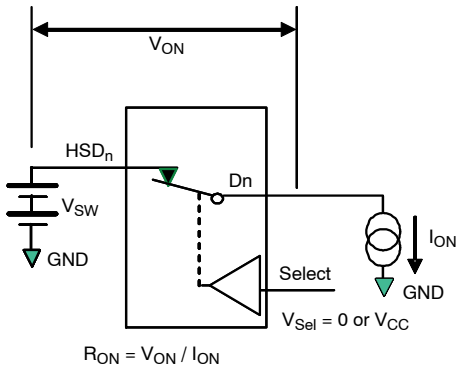
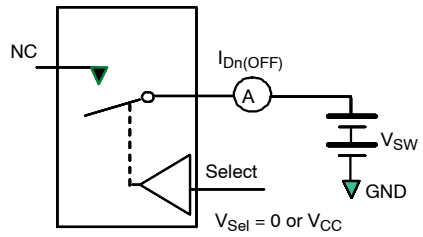
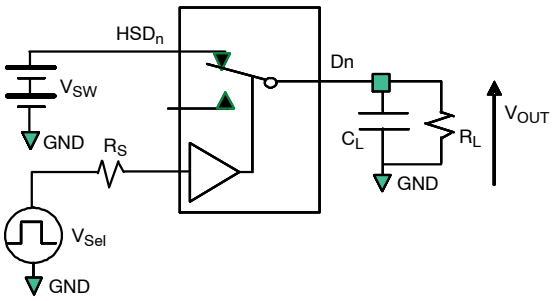


Figure 9. On Resistance



NOTE: Each switch port is tested separately.

Figure 10. Off Leakage



NOTE: R_L , R_S, and C_L are functions of the application environment (see AC Tables for specific values) C_L includes test fixture and stray capacitance.

Figure 11. AC Test Circuit Load

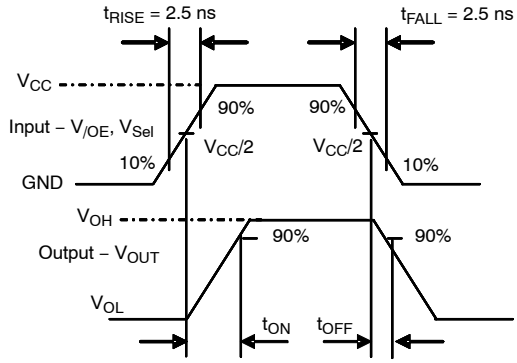


Figure 12. Turn−On / Turn−Off Waveforms

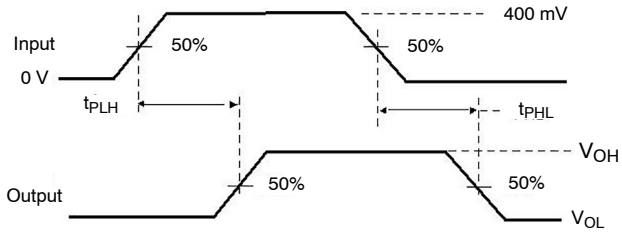


Figure 13. Propagation Delay ($t_R t_F$ − 500 ps)

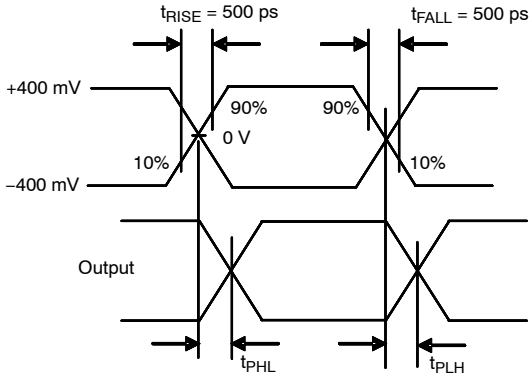
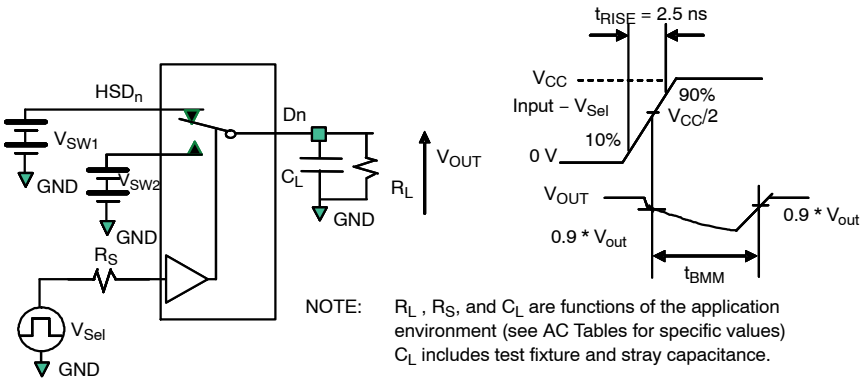


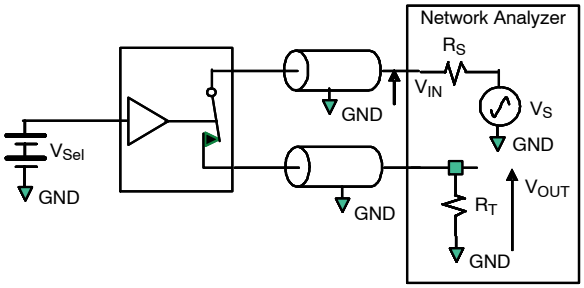
Figure 14. Intra−Pair Skew Test $t_{SK(P)}$

TEST DIAGRAMS (continued)



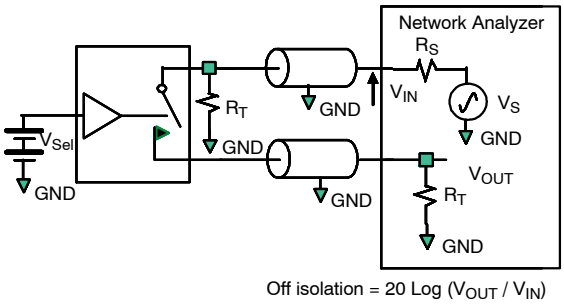
NOTE: R_L , R_S, and C_L are functions of the application environment (see AC Tables for specific values)
C_L includes test fixture and stray capacitance.

Figure 15. Break−Before−Make Interval Timing



NOTE: R_S and R_T, are functions of the application environment (see AC Tables for specific values)

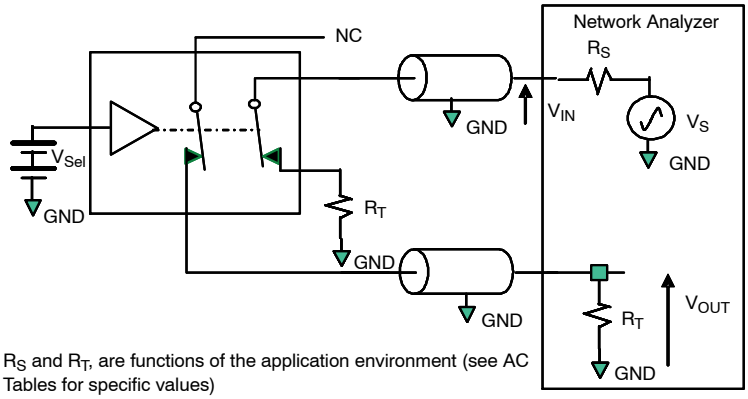
Figure 16. Bandwidth



Off isolation = 20 Log (V_{OUT} / V_{IN})

NOTE: R_S and R_T, are functions of the application environment (see AC Tables for specific values)

Figure 17. Channel Off Isolation



NOTE: R_S and R_T, are functions of the application environment (see AC Tables for specific values)

Crosstalk = 20 Log (V_{OUT} / V_{IN})

Figure 18. Non−Adjacent Channel−to−Channel Crosstalk

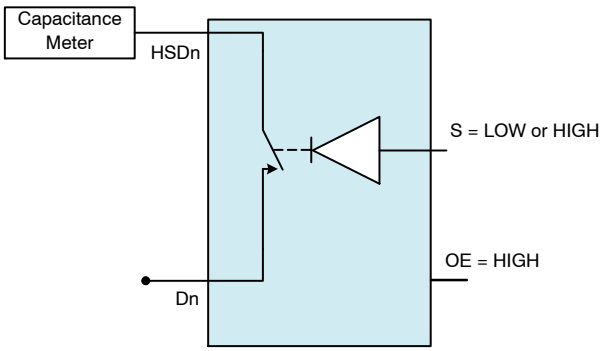


Figure 19. Channel Off Capacitance

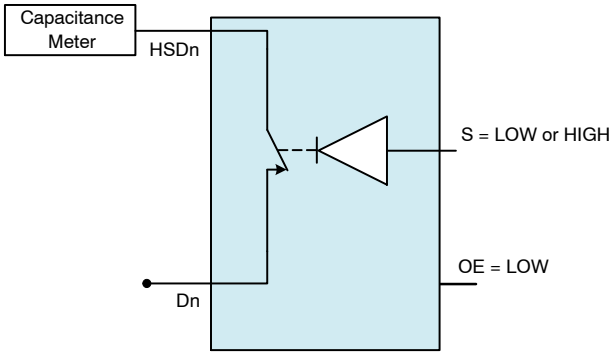
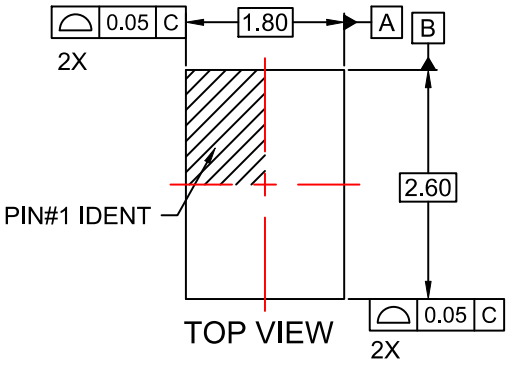


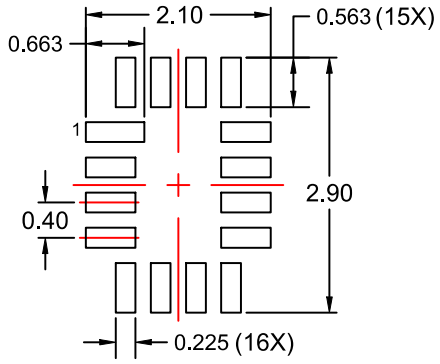
Figure 20. Channel On Capacitance

UQFN16 1.8x2.6, 0.4P
CASE 523BF
ISSUE O

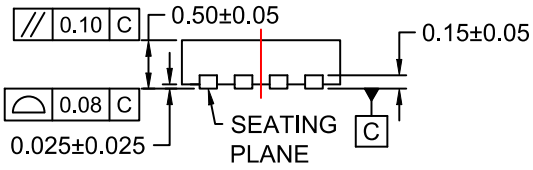
DATE 31 OCT 2016



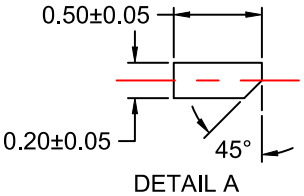
TOP VIEW



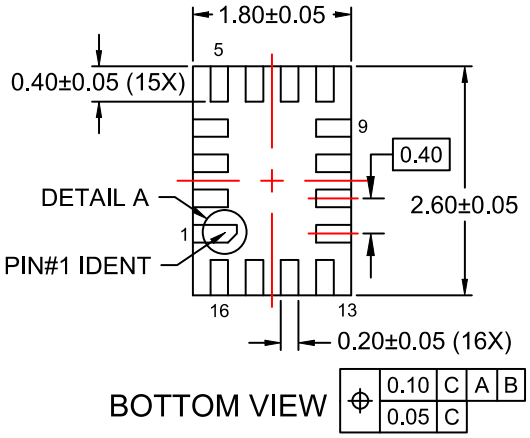
RECOMMENDED
LAND PATTERN



SIDE VIEW

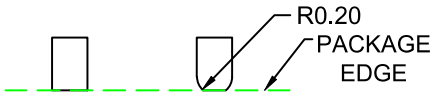


DETAIL A
SCALE : 2X



BOTTOM VIEW

LEAD SHAPE AT PACKAGE EDGE



LEAD
OPTION 1
SCALE : 2X

LEAD
OPTION 2
SCALE : 2X

NOTES:

A. PACKAGE DOES NOT FULLY CONFORM TO JEDEC STANDARD.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.

D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.

E. TERMINAL SHAPE MAY VARY ACCORDING TO PACKAGE SUPPLIER, SEE TERMINAL SHAPE VARIANTS.

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